



The DUNE Far Detector Interim Design Report
Volume 2: Single-Phase Module
Deep Underground Neutrino Experiment (DUNE)

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DUNE
DEEP UNDERGROUND
NEUTRINO EXPERIMENT

FERMILAB-DESIGN-2018-02

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Chapter 1

Design Motivation and Overview

1.1 Introduction to the DUNE Single-Phase Far Detector Design

The DUNE single-phase (SP) LArTPC detector module will be the culmination of several decades of LArTPC technology development, and once operational, it will open new windows of opportunity in the study of neutrinos. DUNE's rich physics program, with discovery potential for charge-parity symmetry violation (CPV) in the neutrino sector, and capability to make significant observations of nucleon decay and astrophysical events, is enabled by the exquisite resolution of the LArTPC detector technique.

Experience with design, construction, operation, and data analysis with numerous single-phase LArTPC experiments and prototypes has informed the approach to realizing the massive DUNE SP modules. Each far detector module will feature the largest LArTPCs ever constructed, at approximately 10 kt active volume each. Aside from the challenges inherent in such a large undertaking, DUNE presents the added complication of construction and operation in a location that is 1.5 km (one mile) underground with limited access.

The design of the DUNE SP module presented in this document reflects an approach to achieving the science goals of the experiment, and addresses the challenges of constructing and operating a massive detector in a deep underground environment.

1.2 Single-Phase LArTPC Operational Principle

The precision tracking and calorimetry offered by the single-phase LArTPC technology provides excellent capabilities for identifying interactions of interest while mitigating sources of background. The operational principle of a single-phase LArTPC is summarized here for reference.

Charged particles traversing the active volume of the LArTPC ionize the medium, while also producing scintillation light. The ionization drifts along an E field that is present throughout the volume, towards a series of anode layers. Each anode layer is composed of finely spaced wires arranged at characteristic angles, and appropriate biasing of these wires allows the ionization to drift through the successive layers before terminating on a wire in the collection layer. The individual wires in the anode layers can be instrumented with low-noise electronics that record the current in the wire as a function of time. The argon scintillation light, which at 127 nm wavelength is deep in the UV spectrum, can be recorded by photon detectors (PDs) that shift the wavelength closer to the visible spectrum and subsequently record the time and pulse characteristics of the incident light.

The performance of the LArTPC hinges on several key factors. First, the purity of the LAr must be extremely high in order to allow ionization to drift over several meters towards the anode planes. The levels of electronegative contaminants (e.g., oxygen, water), must be reduced and maintained to parts per trillion (ppt) levels in order to achieve minimum charge attenuation over the longest drift lengths in the LArTPC. Second, the electronic readout of the LArTPC requires very low noise levels so that the signal of drifting ionization is clearly discernible over the baseline of the electronics. Third, a uniform E field must be established over the detector volume, requiring a robust and stable high voltage system. Finally, the sheer size of the SP module means that once it is filled with LAr, all components within the cryostat are inaccessible for decades. All internal devices must have long operating lifetimes at LAr temperatures.

1.3 Motivation of Single-Phase LArTPC Design at DUNE

The DUNE Single-Phase far detector (FD) design builds on several decades of experience in designing, constructing, and operating LArTPCs. It implements unique design features to maximize the capability of the experiment, as well as new features motivated by the unprecedented scale of the FD modules and the deep underground location where construction will occur.

Among the features driven by the underground location of the experiment, all detector components are sized to fit within the constraints of the SURF shafts and access pathways.

A drift time of several milliseconds is typical for ionization to arrive at the anode wires after drifting several meters. This lengthy duration of time, as well as aspects of the DUNE physics program looking for rare and low-energy processes, makes the deep underground location essential for the SP module. The ~ 1.5 km overburden of earth greatly reduces the rate of cosmic rays reaching the active volume of the detector module, greatly enhancing the ability to search for rare and low-energy signatures without the influence of cosmic-induced backgrounds.

1.4 Overview of the Single-Phase Design

The DUNE SP module features a 10 kt active mass LArTPC, with all associated cryogenic, electronic readout, computing, and safety systems. The SP module is designed to maximize the active volume within the confines of the membrane cryostat while minimizing dead regions. The detector elements have been modularized such that their production can proceed in parallel with the construction of the DUNE caverns and cryostats, and sized so that they conform to the access restrictions for transport underground. Table 1.1 summarizes some of the high-level parameters of the SP module.

Table 1.1: SP module parameters

Parameter	Value	Note
Cryostat LAr mass	17.5 kt	
Active LAr mass	10 kt	
Active Height	12 m	
Active Length	58 m	
Maximum Drift	3.53 m	
Number of anode plane assembly (APA) channels	384,000	
Number of photon detection system (PDS) channels	6000	

The cryostat is constructed such that its long axis is aligned with the beam arriving from Fermilab. The TPC inside the cryostat is composed of two rows of cathode plane assemblies (CPAs) oriented along the long axis of the cryostat, flanked on either side by rows of anode plane assemblies. A field cage (FC) completely surrounds the four open sides of the four drift regions to ensure that the E field within is uniform and unaffected by the presence of the cryostat walls and other nearby conductive structures. Integrated within each APA are elements of the PDS as well as electronics to process the APA signals. Around the periphery of the TPC various instrumentation for monitoring the cryogenic environment is present. Outside of the cryostat, additional electronic readout and data acquisition equipment is present to transfer information from the detector module. Figure 1.1 illustrates the basic arrangement of the TPC elements within the SP module.

1.5 Detector Systems

Table 1.2 lists the principal detection systems of the SP module along with the primary purpose of each system. In this section, the primary detector systems are introduced briefly. The subsequent chapters of this document provide extensive descriptions of each of these systems.

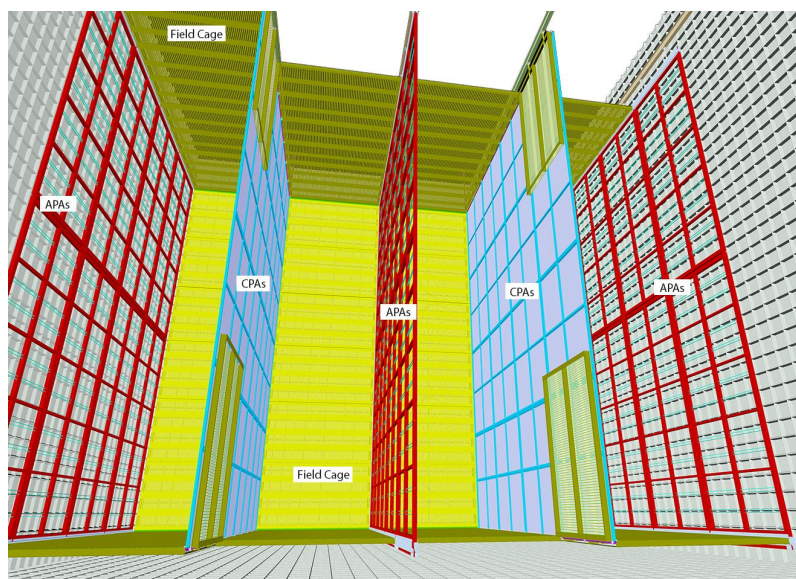


Figure 1.1: A diagram showing the arrangement of the main TPC elements in the SP module. Two rows of cathode plane assemblies are interleaved with three rows of anode plane assemblies. The FC structure (only partially depicted to enable visibility of other elements) surrounds the outer area of the APA and CPA rows. Elements of the PDS are integrated within the APA structure.

Table 1.2: SP module systems.

System	Name	Purpose
APA	anode plane assemblies	ionization signal development
HV	high voltage	establish uniform drift field
CE	cold electronics	process APA signals
PD	photon detection	light collection and triggering
DAQ	data acquisition	record and handle digital data
CISC	cryogenics instrumentation and slow controls	maintain and monitor LAr volume

1.5.1 Anode Plane Assemblies

The APA system, described in full detail in Chapter 2, is used to capture the signals created by ionization drifting in the TPC volume. Each APA features a metal frame, on each side of which there are three instrumented and two uninstrumented anode layers. The design of the anode layers is arranged to provide three complementary views of the ionization present in the TPC that can be combined to form 3D representations of the distribution of the charge.

Among the novel features of the SP LArTPC is the presence of wrapped anode wires that follow a helical trajectory around the height of the APA. This design choice was made to minimize the need to tile electronic readout around the perimeter of the APA, which would lead to dead space between neighboring anode plane assemblies. This choice also was driven by reconstruction performance, with the angle of the wrap chosen such that a given induction plane wire does not intersect a given collection plane wire more than once, which greatly reduces pathologies in pattern recognition.

1.5.2 TPC Electronics

The electronics system, described in full detail in Chapter 3, is responsible for manipulating the signals present on the APA wires and ultimately transferring them out of the cryostat and on to the data acquisition (DAQ) system. Several stages of signal processing occur within the cryostat, including front-end (FE) amplification and pulse shaping, analog-to-digital conversion, and control and communication functions.

1.5.3 CPA, Field Cage and High Voltage

The high voltage (HV) system, described in full detail in Chapter 4, creates the uniform electric field in the TPC volume that causes ionization to drift towards the anode plane assemblies. The HV system contains both the cathode plane assemblies, which are operated at a voltage of -180 kV, as well as the FC elements which progressively step the CPA voltage down in magnitude.

A novel feature of the HV system is the use of resistive panels for the cathode plane assemblies, which serves to control the flow of stored energy in this system in the event of an unexpected electrical discharge. This feature provides protection to the SP module elements and guards against damage that would negatively impact detector performance.

1.5.4 Photon Detection

The PDS, described in full detail in Chapter 5, is used to capture scintillation light produced by interactions in the TPC. The scintillation light of argon is very deep in the ultraviolet, so the PD elements are designed to shift this wavelength closer to the visible spectrum where the SP module

has high efficiency. The PDS light detectors are geometrically arranged as approximately 15 cm wide vertical strips mounted in the anode plane assemblies, with ten strips per APA. The light collection implementation continues to be optimized. Electronic signals are generated via silicon photomultipliers (SiPMs) immersed in the LAr and passed on to readout modules outside the cryostat.

1.5.5 Data Acquisition

The DAQ system is described in full detail in Chapter 6. DUNE physics requires that the DAQ system record APA and PDS signals with high efficiency both from relatively high-energy (>100 MeV) single interactions from beam and atmospheric neutrinos, interactions from proton decay (that are localized in both space and time), and from multiple low-energy (<100 MeV) interactions distributed throughout the detector over tens of seconds from supernova neutrino bursts (SNBs).

1.5.6 Cryogenic Instrumentation and Slow Controls

The cryogenic instrumentation and slow controls (CISC) system, described in full detail in Chapter 7. This system provides comprehensive monitoring for all detector module components as well as for the LAr quality and behavior. Beyond passive monitoring, CISC also provides a control system for some of the detector components.

1.6 Technical Coordination

Chapter 8 provides an overview of detector integration and installation functions. These include project support, integration, infrastructure, the DUNE integration and test facility (ITF), and installation.

Chapter 2

Anode Plane Assemblies

2.1 Anode Plane Assembly (APA) Overview

Anode planes (or wire planes) are the DUNE SP module elements used to sense, through both signal induction and direct collection, the ionization electrons created when charged particles traverse the LAr volume inside the SP module. To facilitate fabrication and installation underground, the anode design is modular, with anode plane assemblies (APAs) tiled together to form the readout system for a 10 kt detector module. A single APA is 6 m high by 2.3 m wide, but two of them are connected vertically, and twenty-five of these vertical stacks are linked together to define a 12 m tall by 58 m long mostly-active readout plane. As described below, the planes are active on both sides, so three such wire readout planes are interleaved with two high voltage surfaces to define four 3.6 m wide drift regions inside each SP module, as shown in the detector schematic views in Figure 2.1. Each single-phase 10 kt module, therefore, will contain 150 anode plane assemblies.

Each APA frame is covered by over 2500 sense wires laid in three planes oriented at angles to each other: a vertical collection plane, X , and two induction planes at $\pm 35.7^\circ$ to the vertical, U and V . These enable multi-dimensional reconstruction of particle tracks. An additional 960 wires that are not read out make up an outer shielding plane, G , to improve signal shapes on the U induction channels. The angled wires are wrapped around the frame from one side to the other, allowing all channels to be read out from one end of the APA only (the top or bottom), and thereby minimizing the dead regions between neighboring anode plane assemblies. Signals induced or collected on the wires are transferred through soldered connections to wire termination boards mounted at the end of the APA frame that in turn connect to front-end (FE) readout electronics sitting in the LAr. Figures 2.2 and 2.3 illustrate the layout of the wires on an APA, showing how they wrap around the frame and terminate on wire boards at the head end where readout electronics are mounted.

The anode plane assemblies represent a critical interface point between the various detector subsystems within the SP module. As already mentioned, the TPC readout electronics mount directly to the APA frames. The photon detectors (PDs) for detecting scintillation light produced in the LAr are also housed inside the frames, sandwiched between the wires on the two sides, requiring

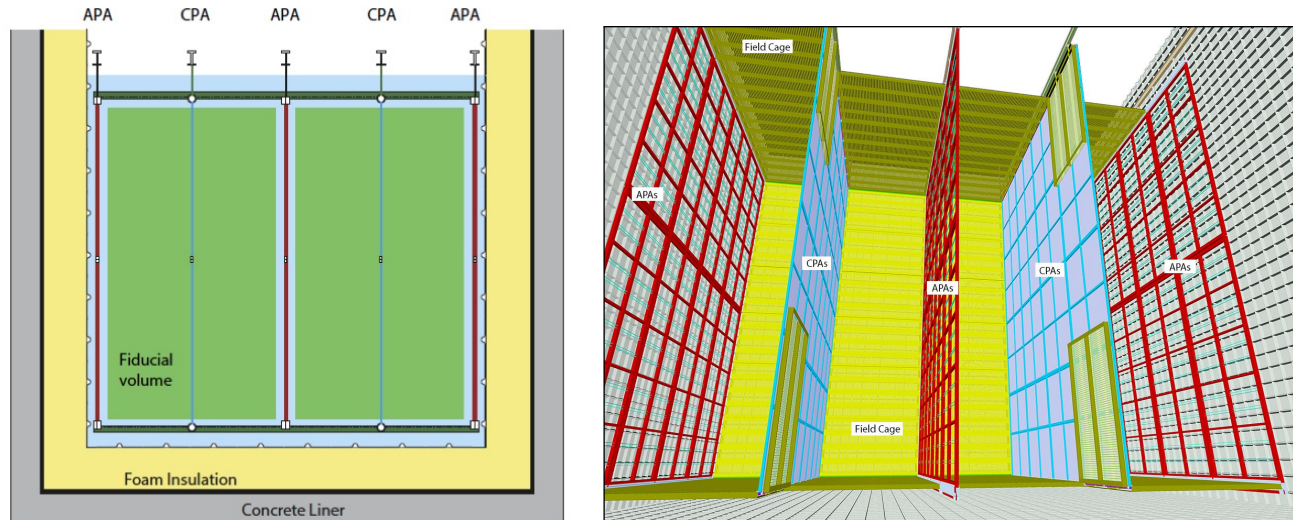


Figure 2.1: Left: End-on schematic view of the active argon volume showing the four drift regions and anode-cathode plane ordering of the TPC inside the detector. Right: View of the partially installed DUNE TPC inside the membrane cryostat. The anode plane assemblies are shown in red, cathode plane assemblies are in cyan, FC modules in yellow/green. Some of the FC modules are in their folded position against the cathode to providing aisle access during installation.

careful coordination in the frame design as well as placing a requirement on the transparency of the APA structures. In addition, the electric field cage (FC) panels connect directly to the edges of the APA frames. Finally, the anode plane assemblies must support the routing of cables for both the TPC electronics and the photon detector systems. All of these considerations have important impacts on the design, fabrication, and installation planning for the anode plane assemblies.

Full-scale anode plane assemblies have recently been produced at the Physical Sciences Laboratory (PSL) at the University of Wisconsin and at the Daresbury Laboratory in the UK for the ProtoDUNE-SP project at CERN. Figure 2.4 shows a completed APA produced at PSL just before shipment to CERN for use in ProtoDUNE-SP. This effort has greatly informed the design and production planning for the DUNE detector modules, and future ProtoDUNE-SP running is expected to provide valuable validation information for many fundamental aspects of the APA design.

The design, construction, testing, and installation of the anode plane assemblies is overseen by the APA consortium within the DUNE collaboration. Multiple APA production sites will be set up in the USA and the UK, with each nation producing approximately half of the anode plane assemblies needed for the SP modules. Factory setup is anticipated to begin in 2020, with APA fabrication for the first 10 kt far detector module running from 2021–2023.

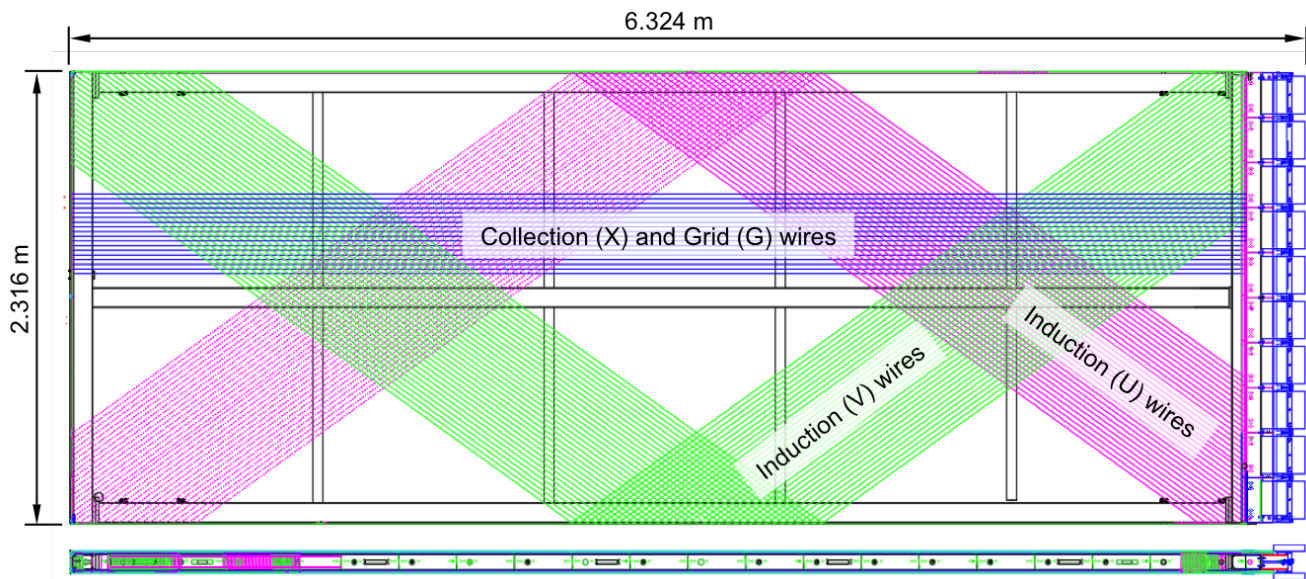


Figure 2.2: Illustration of the DUNE APA wire wrapping scheme showing small portions of the wires from the three signal planes (U , V , X). The fourth wire plane (G) above these three, and parallel to X , is present to improve the pulse shape on the U plane signals. The TPC electronics boxes, shown in blue on the right, mount directly to the frame and process signals from both the collection and induction channels. The APA is shown turned on its side in a horizontal orientation.

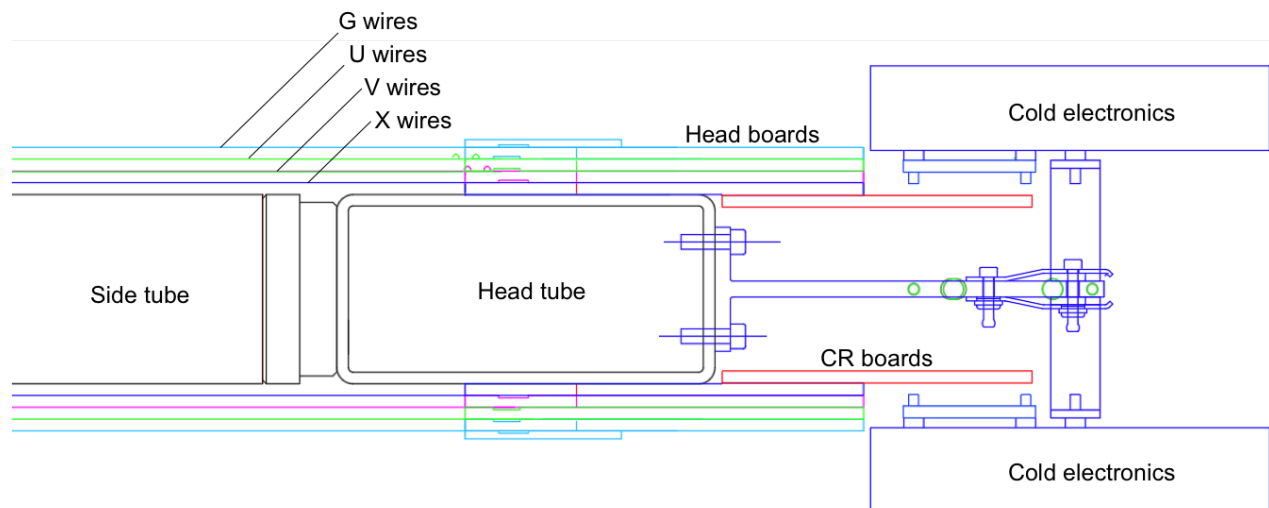


Figure 2.3: Cross section view of an APA frame near the head end showing the layers of wires (X , V , U , G inside to out) on both sides of the frame and terminating on wire boards at the head end of the frame, which connect directly to TPC readout electronics.

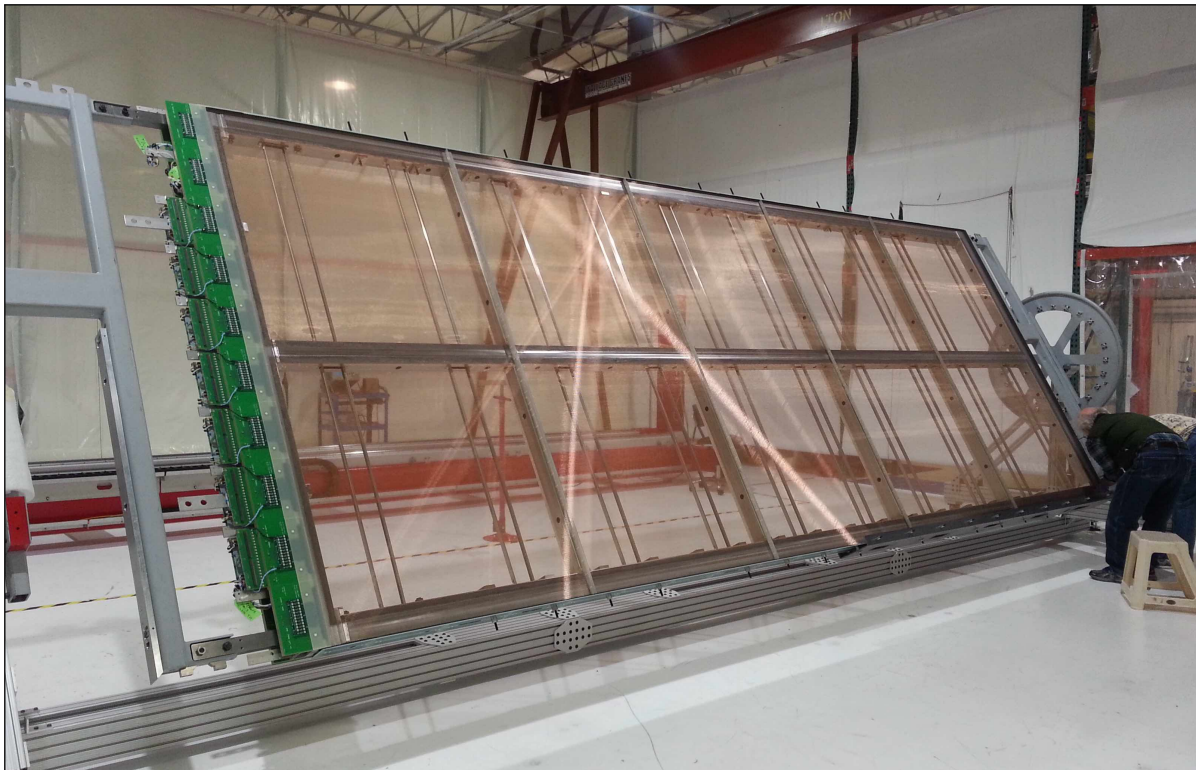


Figure 2.4: Completed ProtoDUNE-SP APA ready for shipment to CERN.

2.2 Design

The physics performance of the SP module is a function of many intertwined detector parameters including argon purity, drift distance, electric field, wire pitch, wire length, and noise levels in the readout electronics. Energy deposits from minimum ionizing particles (MIPs) originating anywhere inside the active volume of the detector should be identifiable with near 100% efficiency. This requirement sets constraints on the APA design, such as limits on the wire pitch, wire length, and choice of wire material. This section details the current APA design and discuss some areas where design enhancements are being considered based on experience from prototypes. We begin with an overview of the key fundamental parameters of the anode plane assemblies and their connection to the physics requirements of the experiment.

2.2.1 APA Overview and Key Design Parameters

Each APA is 6 m high, 2.3 m wide, and 12 cm thick. The underlying support frame is made from stainless steel hollow tube sections that are precisely machined and bolted together. A fine, conducting mesh covers the rectangular openings in the frame on both sides, to define a uniform electrical ground plane (GP) behind the wires. The four layers of sense and shielding wires at varying angles relative to each other completely cover the frame. The wires are terminated on boards that anchor them and also provide the connection to the TPC readout electronics. Starting from the outermost wire layer, there is first an uninstrumented shielding plane (vertical, G),

followed by two induction planes ($\pm 35.7^\circ$ to the vertical, U, V), and finally the collection plane (vertical, X). All wire layers span the entire height of the APA frame. The two planes of induction wires wrap in a helical fashion around the long edges and over both sides of the APA. The layout of the wire layers is illustrated above in Figures 2.2 and 2.3. Below we summarize the key design parameters and the considerations driving the main design choices for the anode plane assemblies.

- **APA size.** The size of the anode plane assemblies is chosen for fabrication purposes, compatibility with over-the-road shipping, and for eventual transport to the 4850 ft. level at SURF and installation into the membrane cryostat of a detector module. The dimensions are also chosen such that an integral number of electronic readout channels and boards fill in the full area of the APA.
- **Detector active area.** anode plane assemblies should be sensitive over most of the full area of an APA frame, with dead regions between anode plane assemblies due to frame elements, wire boards, electronics, or cabling kept to a minimum. The wrapped style shown in Figure 2.2 allows all channels to be read out at the top of the APA, eliminating the dead space between anode plane assemblies that would otherwise be created by electronics and associated cabling. In addition, in the design of the SP module, a central row of anode plane assemblies is flanked by drift-field regions on either side (see Figure 2.1), and the wrapped design allows the induction plane wires to sense drifted ionization that originates from either side of the APA. This double-sided feature is also effective for the anode plane assemblies located against the cryostat walls where there is a drift field on only one side, since the grid layer facing the wall effectively blocks any ionization generated outside the TPC from drifting in to the wires on that side of the APA.
- **Wire angles.** The X wires run vertical to provide optimal reconstruction of beam-induced particle tracks, which are predominantly forward (in the beam direction). The angle of the induction planes on the APA, $\pm 35.7^\circ$, was chosen to ensure that each induction wire only crosses a given collection wire once, reducing the ambiguities that the reconstruction must address. Simulation studies (see next item) show that this configuration performs similarly to an optimal 45° wire angle for the primary DUNE physics channels. The design angle of the induction wires, coupled with their pitch, was also chosen such that an integer multiple of electronics boards are needed to read out one APA.
- **Wire pitch.** The choice of wire pitch, 4.7 mm, combined with key parameters for other TPC systems (described in their respective sections of the technical design report (TDR)), can achieve the required performance for energy deposits by MIPs while providing good tracking resolution and good granularity for particle identification. The SP requirement that it be possible to determine the fiducial volume to 1% implies a vertex resolution of 1.5 cm along each coordinate direction. The 4.7 mm wire pitch achieves this for the y and z coordinates. The resolution on x , the drift-coordinate, will be better than in the y - z plane, due to the combination of drift-velocity and electronics sampling-rate. Finally, as already mentioned, the total number of wires on an APA should match the granularity of the electronics boards (each FE motherboard can read out 128 wires, mixed between the U, V, X planes). This determines the exact wire spacings of 4.790 mm and 4.669 mm on the collection and induction planes, respectively. To achieve the reconstruction precision required (e.g., for dE/dx reconstruction accuracy and multiple Coulomb scattering determination),

the tolerance on the wire pitch is ± 0.5 mm.

In 2017, the DUNE Far Detector Task Force, utilizing a full far detector (FD) simulation and reconstruction chain, performed many detector optimization studies to quantify the impact of design choices, including wire pitch and wire angle, on DUNE physics performance. The results indicated that a reduction in wire spacing (to 3 mm) or a change in wire angle (to 45°) would not significantly impact the performance for the main physics goals of DUNE, including ν_μ to ν_e oscillations and charge-parity symmetry violation (CPV) sensitivity. Figure 2.5 reproduces two plots from the Task Force report showing the impact of wire pitch and orientation on distinguishing electrons versus photons in the detector. This is a key low-level metric for oscillation physics since photon induced showers can fake electron showers and create neutral-current generated backgrounds in the ν_e charged-current event sample. Two important handles for reducing this contamination are the energy density at the start of the shower and the visible gap between a photon shower and the vertex of the neutrino interaction due to the non-zero photon interaction length. Figure 2.5(a) shows the reconstructed ionization energy loss density (dE/dx) in the first centimeters of electron and photon showers, illustrating the separation between the single MIP signal from electrons and the double MIP signal when photons pair-produce an e^+e^- . The final electron signal selection efficiency is shown as a function of the background rejection rate for different wire configurations in Figure 2.5(b). At a signal efficiency of 90%, for example, the background rejection can be improved by about 1% using either 3 mm spacing or 45° wire angles for the induction planes. This slight improvement in background rejection with more dense hit information or more optimal wire angles is not surprising, but the impact on high-level physics sensitivities from these changes is very small. The conclusions of the Far Detector Task Force, therefore, are that the substantial cost impacts of making such changes to the SP module design are not justified.

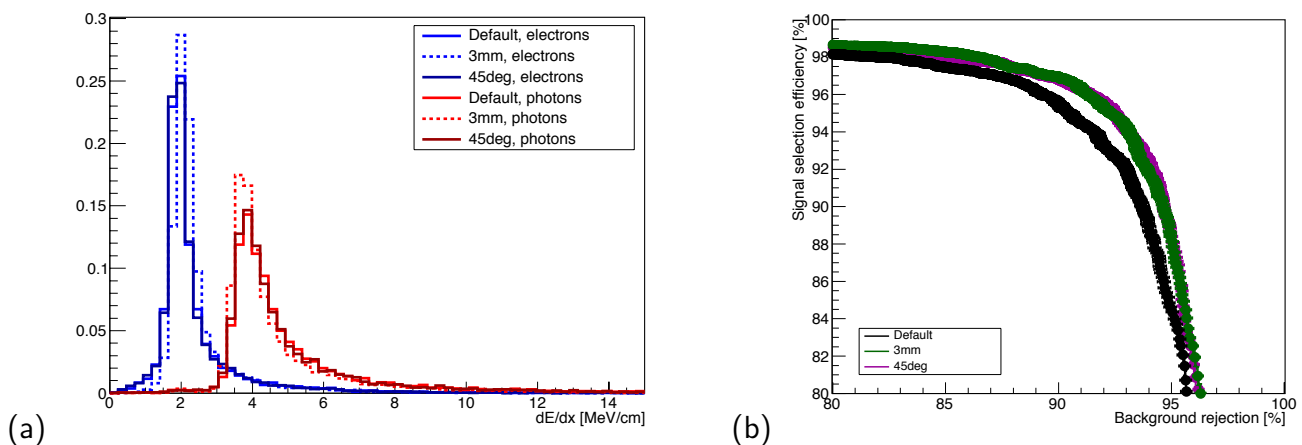


Figure 2.5: Summary of electron–photon separation performance studies from the DUNE Far Detector Task Force. (a) $e-\gamma$ separation by dE/dx for the nominal wire spacing and angle (4.7 mm/ 37.5°) compared to 3 mm spacing or 45° induction wire angles. (b) Electron signal selection efficiency versus photon (background) rejection for the different detector configurations. The 3 mm wire pitch and 45° wire angle have similar impacts, so the 45° curve is partially obscured by the 3 mm curve.

- **Wire plane transparency and signal shapes.** The ordering of the layers, from the outside in, is $G-U-V-X$, followed by the grounding mesh. The operating voltages of the

APA layers are listed in Table 2.1. Figure 2.6 shows the field simulation and expected signal shapes for the bias voltages listed in the table. When operated at these voltages, the drifting ionization follows trajectories around the grid and induction wires, ultimately terminating on a collection plane wire. The grid and induction layers are completely transparent to drifting ionization, and the collection plane is completely opaque. The grid layer is present for pulse-shaping purposes and not connected to the electronics readout; it effectively shields the first induction plane from the drifting charge and removes the long leading edge from the signals on that layer.

Anode Plane	Bias Voltage
<i>G</i> - Grid	−665 V
<i>U</i> - Induction	−370 V
<i>V</i> - Induction	0 V
<i>X</i> - Collection	820 V
Grounding Mesh	0 V

Table 2.1: Baseline bias voltages for APA wire layers.

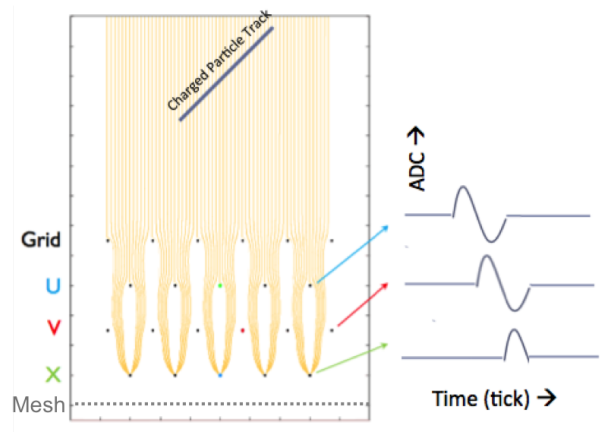


Figure 2.6: Field lines and resulting signal shapes on the APA induction and collection wires.

- Wire type and tension.** The wire selected for the anode plane assemblies is $150\ \mu\text{m}$ beryllium (1.9%) copper wire, chosen for its mechanical and electrical properties, ease of soldering, and cost. The tension on the wires, combined with intermediate support combs (described in Section 2.2.5.4) on the APA frame cross beams, ensure that the wires are held taut in place with minimal sag. Wire sag can impact the precision of reconstruction, as well as the transparency of the TPC wire planes. The tension must be low enough that when the wires are cooled, which increases their tension due to thermal contraction, they stay safely below the break load of the beryllium copper wire. To further mitigate wire slippage and its impact on detector performance, each wire in the APA is anchored twice at all end points, with both solder and epoxy. See Section 2.2.4 for more details about the wires.

Some of the principal design parameters for the DUNE anode plane assemblies are summarized in Table 2.2.

2.2.2 APA Frames

The APA frames are an assembly of rectangular hollow section (RHS) stainless steel tubes. As seen in Figure 2.7, there are three long tubes, a foot tube, a head tube, and eight cross-piece ribs that bolt together to create the 6.0 m tall by 2.3 m wide frame. All hollow sections are 3 in. deep with varying widths depending on their role, see Figure 2.7.

The head and foot tubes are bolted to the side and center pieces via abutment flanges welded to

Table 2.2: APA design parameters

Parameter	Value
Active height	5.984 m
Active width	2.300 m
Wire pitch (U, V)	4.669 mm
Wire pitch (X, G)	4.790 mm
Wire pitch tolerance	± 0.5 mm
Wire plane spacing	4.75 mm
Wire plane spacing tolerance	± 0.5 mm
Wire Angle (w.r.t. vertical) (U, V)	35.7°
Wire Angle (w.r.t. vertical) (X, G)	0°
Number of wires / APA	960 (X), 960 (G), 800 (U), 800 (V)
Number of electronic channels / APA	2560
Wire material	beryllium copper
Wire diameter	$150 \mu\text{m}$

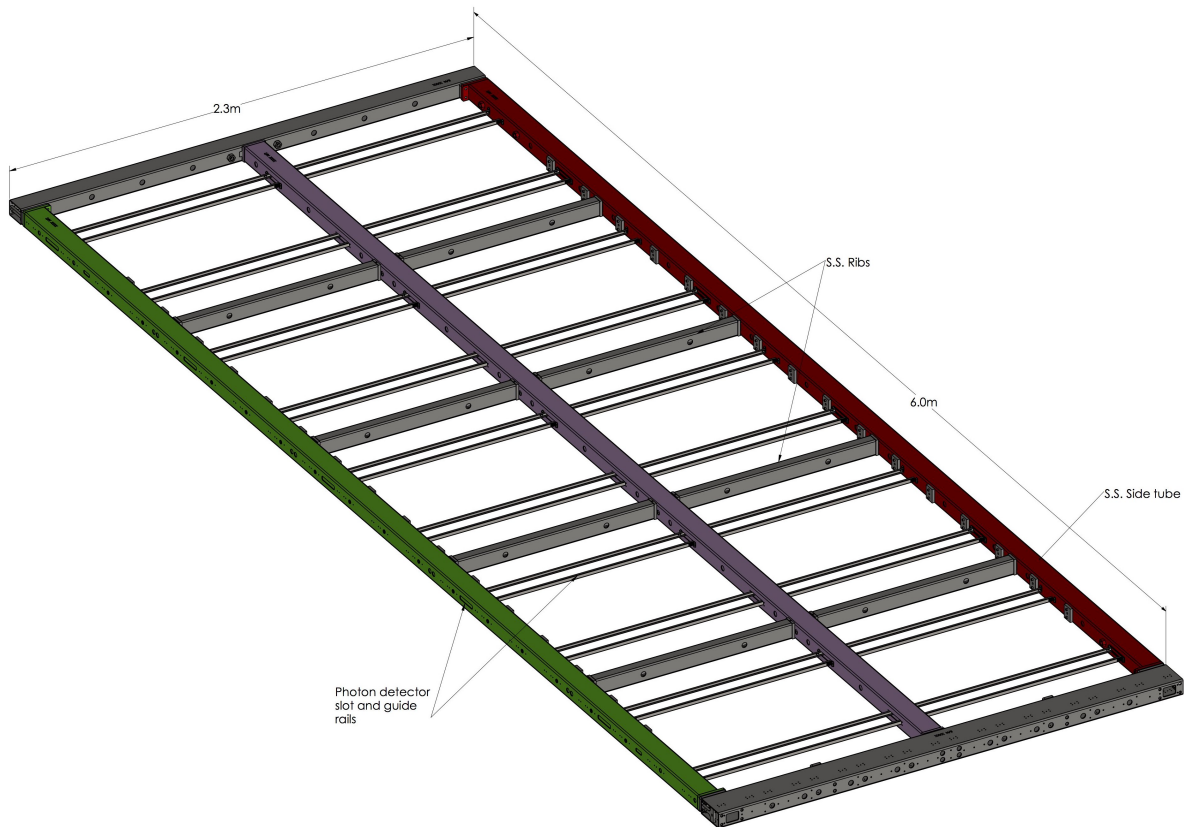


Figure 2.7: A ProtoDUNE-SP APA frame showing overall dimensions and the 13 separate stainless steel tube sections that bolt together to form a complete frame. The long tubes and foot tube are 3×4 in cross section, the head tube is 3×6 in and the ribs are 3×2 in. Also shown are the slots and guide rails used to house the light guide bar PDs in ProtoDUNE-SP.

the tubes. In production, the pieces can be individually machined and cleaned prior to assembly, which gives flexibility both in the production process and helps achieve the flatness and shape tolerances. During final assembly, shims are used to create a flat, rectangular frame of the specified dimensions. The central cross pieces are attached to the side pieces in a similar manner. Figure 2.8 shows models of the different joints.

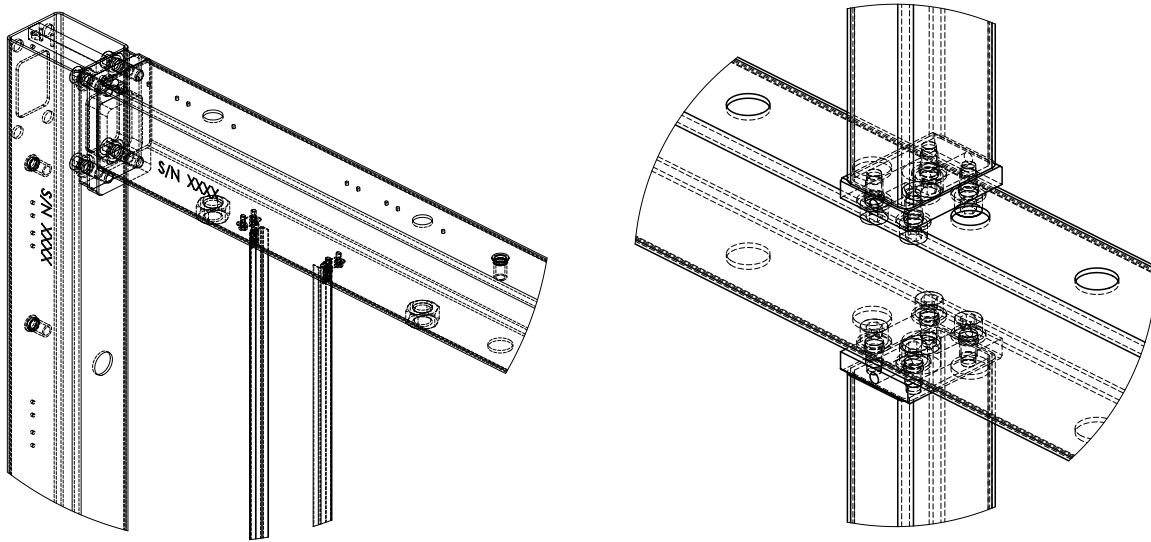


Figure 2.8: The bolted joints in the APA frame. Left: Connection between the head tube and a side tube. Right: Connections between the center tube and the rib pieces on either side. These bolted connections can be shimmed during assembly to ensure the frame meets dimensional and flatness specifications.

The APA frames also house the photon detection system (PDS). In the ProtoDUNE-SP design, rectangular slots are machined in the outer frame tubes and guide rails are used to secure a light guide bar detector, though alternative PD designs are being considered for the SP modules. (See Section 2.3 for more details on interfacing with the PDS.) Also, in a SP module, pairs of APA frames will be mechanically connected to form a 12 m tall structure, as shown in Figure 2.9, with electronics for TPC readout located at both the top and bottom of this two-frame assembly and PDs installed throughout. The APA frame design, therefore, must support the routing of cables to the top of the detector from both the bottom APA readout electronics and the PDs mounted throughout both anode plane assemblies. The dimensions of the stainless steel tube sections used in the frame are currently being revisited from that used in ProtoDUNE-SP to ensure sufficient space is available to accommodate all detector cables. See again Section 2.3 on interfaces or Chapter 5.

2.2.3 Grounding Mesh

A fine mesh screen is mounted on both sides of the frames beneath the sense wires to provide a ground plane that evenly terminates the E field and improves the uniformity of field lines around the wire planes. This mesh also shields the wires to minimize any potential signal pickup from other detectors. The mesh used is formed from a woven conducting wire (80 μm bronze) and is

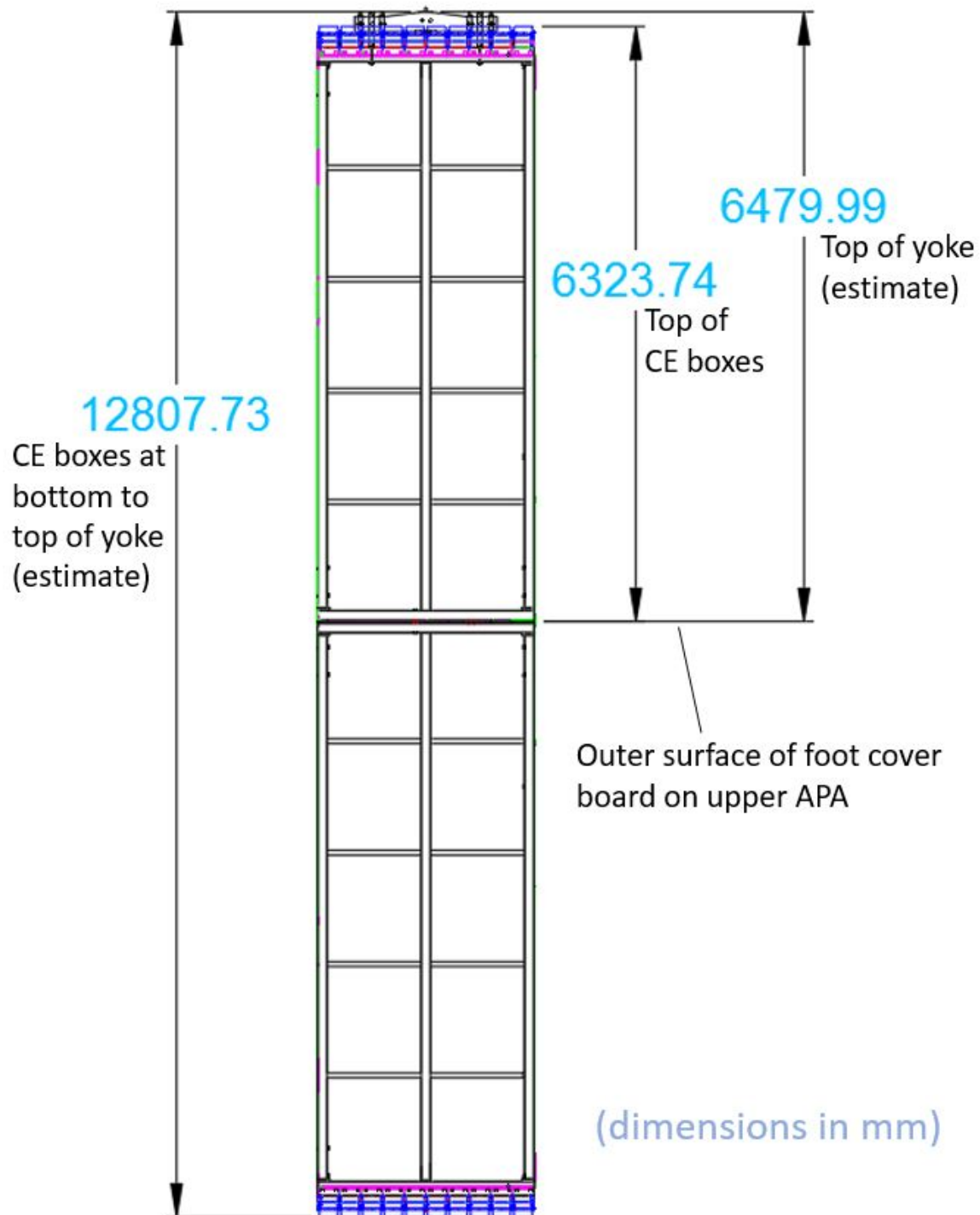


Figure 2.9: Diagram of an APA pair, with bottom APA hung from the top APA. The dimensions of the APA pair, including the accompanying CE (CE) and mechanical supports (the yoke), are indicated.

85% transparent to allow scintillation photons to pass through to the PDs mounted inside the frame.

In the ProtoDUNE-SP anode plane assemblies, the mesh was installed in four parts, along the length of the left- and right-hand halves of each side of the APA. The mesh was clamped around the perimeter of the opening and then pulled tight (by opening and closing clamps, as needed, during the process). Once the mesh was taut, a 25 mm wide strip was masked off around the opening and epoxy was applied through the mesh to attach it directly to the steel frame. Although measurements have shown that this gives good electrical contact between the mesh and the frame, a deliberate electrical connection was also made. Figure 2.10 depicts the mesh application setup for a full-size ProtoDUNE-SP APA.



Figure 2.10: Grounding mesh being clamped to the APA and taped off, ready for gluing to a ProtoDUNE-SP frame.

The mesh installation procedure described above is difficult and prone to wrinkles remaining in the mesh that can affect the E field uniformity and the transparency of the wire planes. For the DUNE mass production, a window-frame design is being considered, where mesh is pre-stretched over smaller sub-frames that can be clipped into each gap between cross beams in the full APA frame. See Section 2.4 for more information.

2.2.4 Wires

The 150 μm (0.006 in) diameter beryllium copper (CuBe) wire chosen for use in the anode plane assemblies is known for its high durability and yield strength. It is composed of 98 % copper, 1.9 % beryllium, and a negligible amount of other elements. Each APA contains a total of 23.4 km of wire.

The key properties for its use in the anode plane assemblies are low resistivity, high tensile or yield strength, and a coefficient of thermal expansion suitable for use with the APA's stainless steel frame (see Table 2.3 for a summary of properties). Tensile strength of the wire describes the wire-breaking stress. The yield strength is the stress at which the wire starts to take a permanent (inelastic) deformation, and is the important limit stress for this case. The wire purchased from Little Falls Alloys ¹ for use on ProtoDUNE-SP had tensile strength over 1380 MPa and yield strength more than 1100 MPa (19.4 N for 150 μm diameter wire). The stress while in use is around 280 MPa (5 N), leaving a comfortable margin.

The coefficient of thermal expansion (CTE) describes how a material expands or contracts with changes in temperature. The CTEs of CuBe alloy and 304 stainless steel are very similar. Integrated down to 87 K, they are 2.7 mm/m for stainless steel and 2.9 mm/m for CuBe. Since the wire contracts slightly more than the frame, for a wire starting at 5 N at room temperature, for example, the tension increases to around 5.5 N when everything reaches LAr temperature.

The change in wire tension during cool-down is also important to consider. In the worst case, the wire cools quickly to 87 K before any significant cooling of the much larger frame. In the limiting case with complete contraction of the wire and none in the frame, the tension would peak around 11.7 N, which is still well under the 20 N yield tension. In practice, however, the cooling will be done gradually to avoid this tension spike as well as other thermal shocks to the detectors.

Table 2.3: Summary of properties of the beryllium copper wire used on the anode plane assemblies.

Parameter	Value
Resistivity	7.68 $\mu\Omega\text{-cm}$ @ 20° C
Resistance	4.4 $\Omega\text{/m}$ @ 20° C
Tensile strength (from property sheets)	1436 MPa / 25.8 N for 150 μm wire
CTE of beryllium copper integrated to 87 K	2.9×10^{-3} m/m
CTE of stainless steel integrated to 87 K	2.7×10^{-3} m/m

2.2.5 Wire Boards and Anchoring Elements

To guide and secure the 3520 wires on an APA, stacks of custom FR4 circuit boards attach to the outside edges of the frame, as shown in the engineering drawings in Figure 2.11. There are 204 *wire boards* on each APA and 337 total circuit boards, where this number includes the wire

¹Little Falls Alloys™, <http://www.lfa-wire.com/>

connections between the different elements of the APA electrical circuit at the head end of the frame.

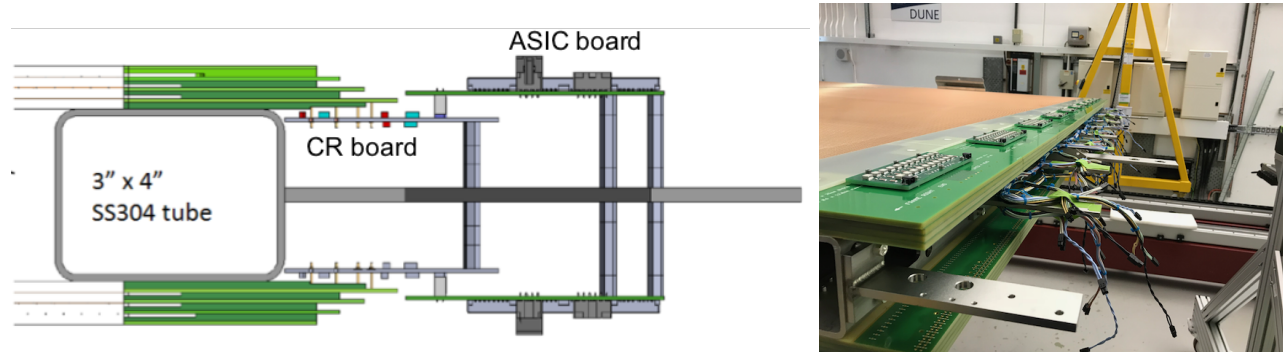


Figure 2.12: The wire board stack at the head end of an APA and the connection to the CE. The set of wire boards within a stack can be seen on both sides of the APA, with the CR board extending further to the right to provide a connection to the CE.

2.2.5.2 CR Boards

The capacitive-resistive (CR) boards carry a bias resistor and a DC-blocking capacitor for each wire in the X and U -planes. These boards are attached to the board stacks after fabrication of all wire planes. Electrical connections to the board stack are made through Mill-Max pins that plug into the wire boards. Connections from the CR boards to the CE are made through a pair of 96-pin Samtec³ connectors.

Surface-mount bias resistors on the CR boards have resistance of $50\text{ M}\Omega$ and are constructed with a thick film on a ceramic substrate. Rated for 2.0 kV operation, the resistors measure $3.0\times 6.1\text{ mm}$ ($0.12\times 0.24\text{ in}$). The selected DC-blocking capacitors have capacitance of 3.9 nF and are rated for 2.0 kV operation. Measuring $5.6\times 6.4\text{ mm}$ ($0.22\times 0.25\text{ in}$) across and 2.5 mm (0.10 in) high, the capacitors feature flexible terminals to comply with PC board expansion and contraction. They are designed to withstand 1000 thermal cycles between the extremes of the operating temperature range. Tolerance is also 5%.

In addition to the bias and DC-blocking capacitors for all X and U -plane wires, the CR boards include two R-C filters for the bias voltages. The resistors are of the same type used for wire biasing except with a resistance of $2\text{ M}\Omega$. Wire plane bias filter capacitors are 39 nF , consisting of ten 3.9 nF surface-mount capacitors connected in parallel. They are the same capacitors as those used for DC blocking.

The selected capacitors were designed by the manufacturer to withstand repeated temperature excursions over a wide range. Their mechanically compliant terminal structure accommodates CTE mismatches. The resistors employ a thick-film technology that is also tolerant of wide temperature excursions. Capacitors and resistors were qualified for ProtoDUNE-SP by subjecting samples to repeated testing at room temperature and at -190°C . Performance criteria were measured across

³Samtec™ <https://www.samtec.com/>

five thermal cycles, and no measurable changes were observed. During the production of 140 CR boards, more than 10,000 units of each component were tested at room temperature, at LAr temperature, and again at room temperature. No failures or measurable changes in performance were observed.

2.2.5.3 Side and Foot Boards

The boards along the sides and foot of the APA have notches, pins, and other location features to hold the wires in the correct position as they wrap around the edge from one side of the APA to the other.

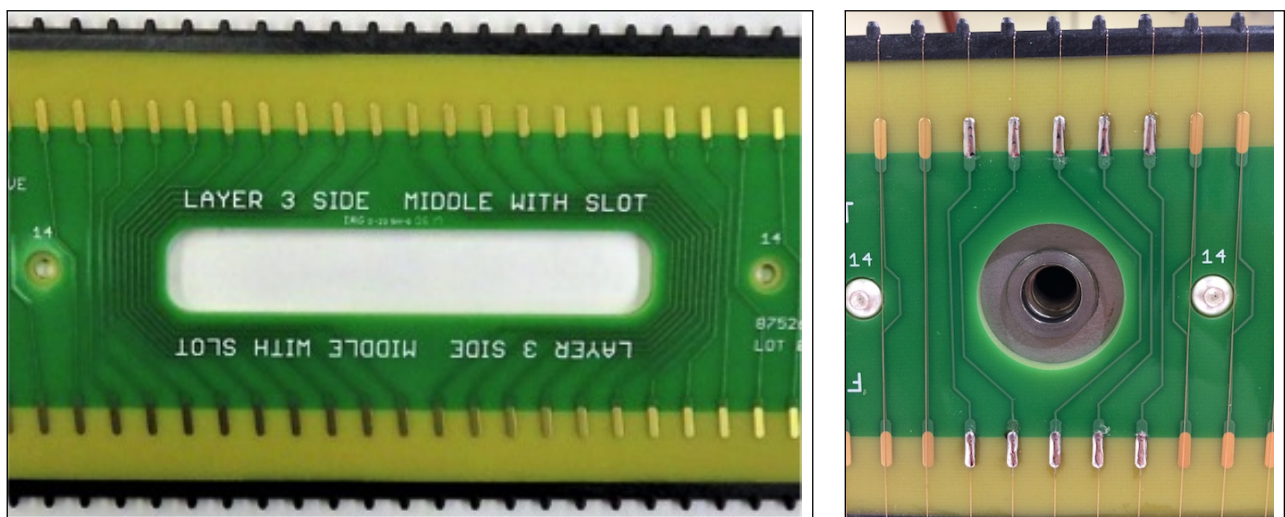


Figure 2.13: Side boards with traces that connect wires around openings. The wires are wound straight over the openings, then soldered to pads at the ends of the traces, then the wire sections between the pads are trimmed away.

A number of hole or slot features are needed in the edge boards to provide access to the underlying frame (see Figure 2.13 for examples). In order that these openings not be covered by wires, the sections of wire that would go over the openings are replaced by traces on the boards. After the wires are wrapped, the wires over the opening are soldered to pads at the ends of the traces and the section of wire between the pads is snipped out. These traces are easily and economically added to the boards by the many commercial fabricators who make circuit boards.

The placement of the angled wires are fixed by teeth that are part of an injected molded strip that is glued to the edge of the FR4 boards. The polymer used for the strips is Vectra e130i (a trade name for 30% glass filled liquid crystal polymer, or LCP). It retains its strength at cryogenic temperature and has a CTE similar enough to FR4 that differential contraction is not a problem. The wires make a partial wrap around the pin as they change direction from the face of the APA to the edge.

2.2.5.4 Support Combs

Support combs are glued at four points along each side of the APA, along the four cross beams. These combs maintain the wire and plane spacing along the length of the APA. A dedicated jig is used to install the combs and provides the alignment and the pressure to allow the glue to dry. The glue used is the Gray epoxy 2216 described below. An eight-hour cure time is required after comb installation on each side of the APA before the jig can be removed and production can continue. Figure 2.14 shows a detail of the wire support combs on a ProtoDUNE-SP APA.

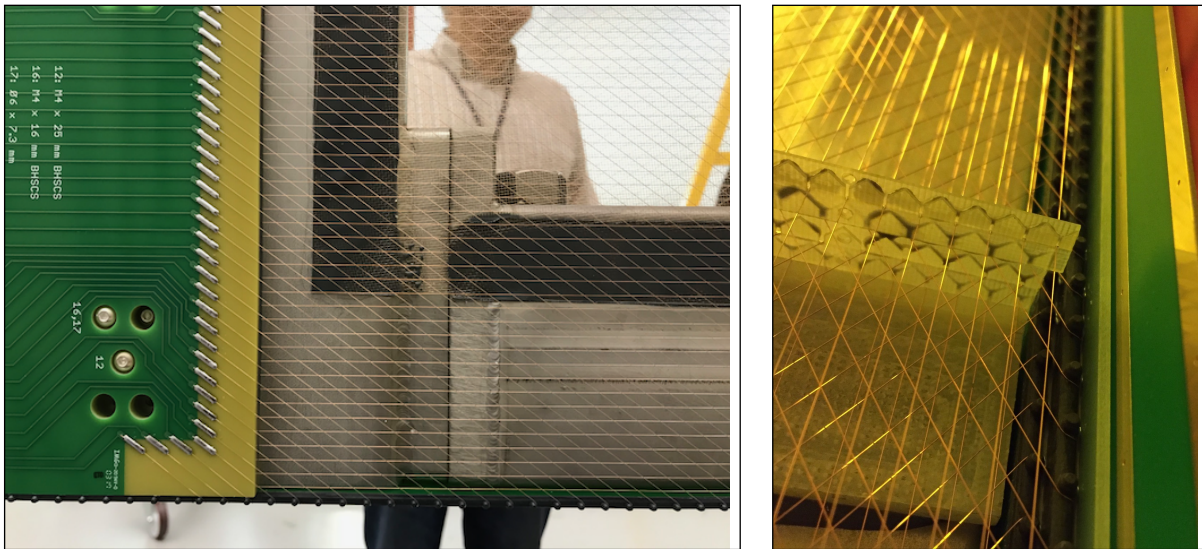


Figure 2.14: Left: APA corner where end boards meet side boards. The injection molded teeth that guide the U and V wires around the edge are visible at the bottom. Right: The wire support combs.

2.2.5.5 Solder and Epoxy

The ends of the wires are soldered to pads on the edges of the wire boards. Solder provides both an electrical connection and a physical anchor to the wire pads. A 62% tin, 36% lead, and 2% silver solder was chosen. A eutectic mix (63/37) is the best of the straight tin-lead solders but the 2% added silver gives better creep resistance.

Once a wire layer is complete, the next layer of boards is glued on, this glue providing an additional physical anchor. Gray epoxy 2216 by 3M⁴ is used for the glue. It is strong, widely used (therefore much data is available), and it retains good properties at cryogenic temperatures.

⁴3M™<https://www.3m.com/>

2.3 Interfaces

The interface between the APA consortium and other detector consortia, facilities, and working groups covers a wide range of activities. Table 2.4 summarizes the interface control documents under development. In the following, we elaborate slightly on the interfaces with the TPC readout electronics and the PDS, as well as the connections between neighboring anode plane assemblies in the SP module and cable routing. Other important interfaces are to the TPC high voltage (HV) system (the FC) and the detector support system (DSS) inside the DUNE cryostats.

Table 2.4: Summary of interface control documents being developed.

Interface Document	DUNE doc-db number
Interface to TPC electronics	6670
Interface to photon detector system	6667
Interface to drift high voltage system	6673
Interface to DAQ	6676
Interface to slow controls and cryogenics infrastructure	6679
Integration facility interface	7021
Facility interfaces (Detector Hall, Cryostat, and Cryogenics)	6967
Installation interface	6994
Calibration interface	7048
Software computing interface	7102
Physics interface	7075

2.3.1 TPC Cold Electronics

The TPC readout electronics is directly mounted to the APA immersed in LAr in order to reduce the input capacitance and thus the inherent electronics noise. With the wire-wrapped design, all 2560 wires to be read out (recall 960 are G -plane wires used for charge shielding only and so not read out) are terminated on wire boards that stack along one end (the head) of the APA frame. The 2560 channels are read out by 20 FE motherboards (128 channels per board), each of which includes eight 16-channel FE ASICs, eight 16-channel ADC ASICs, low-voltage regulators, and input signal protection circuits. A schematic view of the head end of an APA with electronics installed and a cable tray mounted above is shown in Figure 2.15.

The interface between the APA and TPC CE covers a wide range of topics, including the hardware design and production, testing, integration, installation, and commissioning. The hardware interface has two basic components, mechanical and electrical. The mechanical interface includes the support of the 20 CE boxes, with each housing a 128 channel FE motherboard. These are the gray colored, vertically oriented boxes shown in Figure 2.15.

The electrical interface covers the choice of wire-bias voltages to the four wire planes so that 100% transparency can be achieved for drifting ionization electrons, cable connection for the wire bias

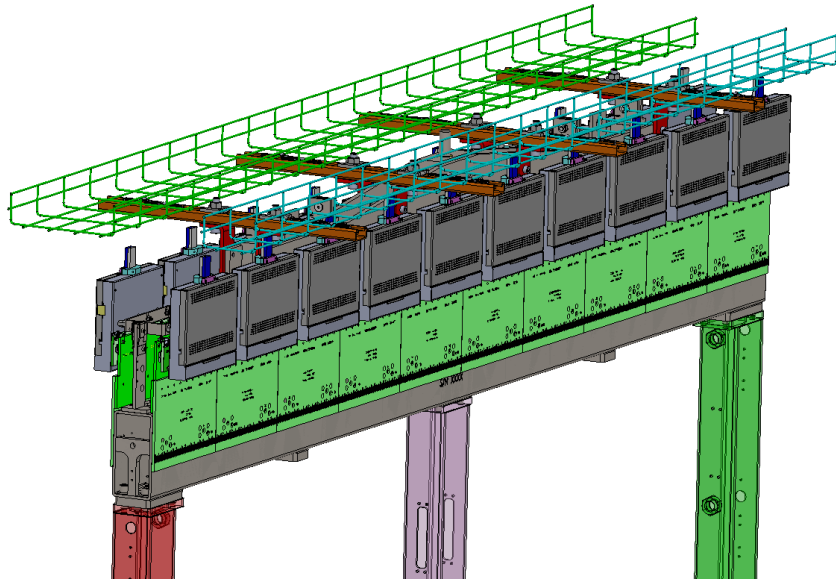


Figure 2.15: The head region of an APA frame showing the 10 wire board stacks on each side, 20 FE motherboard boxes, and the cable tray mounted above.

voltages from the cryostat feedthroughs to the CR boards, interface boards providing connection between CR boards and CE boxes, filtering of the wire-bias voltages through CR boards in order to suppress potential introduction of electronics noise, and an overall grounding scheme and electrical isolation scheme for each APA. The last item is particularly important in order to reach the low electronics noise levels required. See Chapter 3 for information on all of these aspects of the FE electronics system.

2.3.2 Photon Detection System

While the design of the PDS is still under development, it is expected that it is integrated into the APA frame to form a single unit for the detection of both ionization charge and scintillation light. Cables for the PDs must also be accommodated in the APA frame design. Figure 2.16 shows the interface for a light-guide bar based PDS as has been deployed in ProtoDUNE-SP. Individual bars were inserted through 10 slots left on the side steel tubes of the frame. Rails mounted in the APA frame, as shown in Figure 2.7, support the bars in their final positions.

Similar to that of the CE, the interface between the PDS and anode plane assemblies covers a wide range of topics, including the hardware design and production, testing, integration, installation, and commissioning. Depending on the final design of the PDS, the geometry of the APA, including access slot dimensions, locations, and number, may require modification. Any proposed changes by the PDS consortium must be evaluated by the APA consortium to understand structural impacts or interferences with other components. The electrical interface includes a grounding scheme and electrical insulation. Due to the strict requirements on the noise from the CE, the electrical interface must be defined together with the SP electronics consortium.

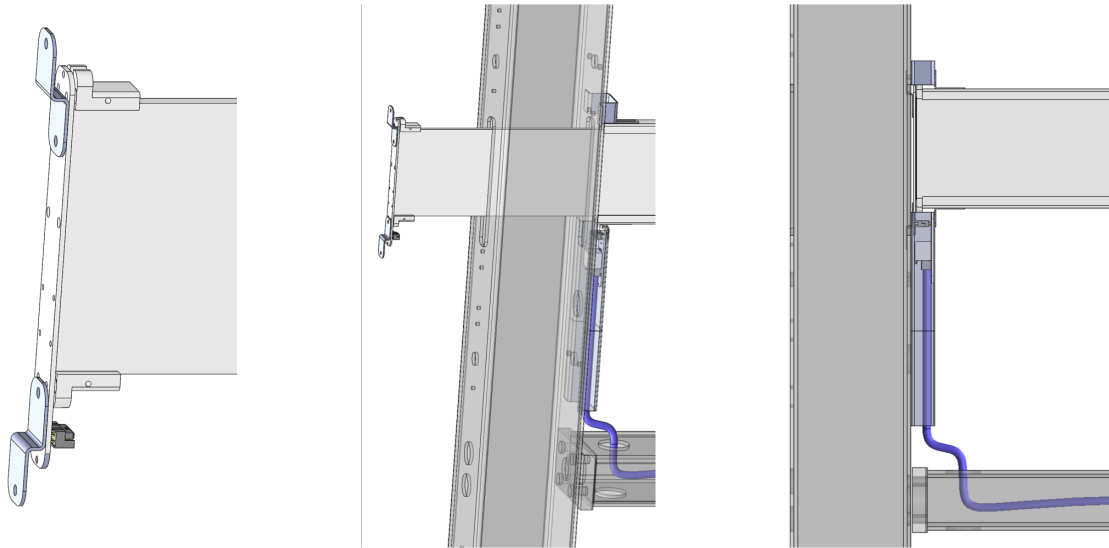


Figure 2.16: Installation of a light-guide bar photon detector module into the available slots in the APA frame. Also shown is a concept for routing PDS cables through the rib tubes of the APA frame and up the central vertical tube section.

For more information on the photon system, see Chapter 5

2.3.3 APA-to-APA Connections and Cable Routing

The TPC readout electronics require that the APA frames must be electrically isolated. The left panel of Figure 2.17 shows the current conceptual design for mechanically connecting the two anode plane assemblies in a vertical stack while maintaining electrical isolation. The green elements are an insulating panel and bolt sleeve made from G10.

Cable routing schemes for both the TPC electronics and PDS are actively being developed. A concept currently under evaluation is to run the cables of the PDS inside the crossing rib tubes to the central beam tube of the APA frames to get to the top. The CE signal and power cables also need to be routed so that the head end of the lower APA in the two-APA assembly can be reached. The current concept is to route the electronics cables inside the two side beams of the APA frames. The right panel of Figure 2.17 depicts such a cable routing scheme. To fully accommodate the cables from two anode plane assemblies, using larger hollow tube sections is under consideration. The final design is in progress, and prototyping is planned for later this year to verify a cabling and installation solution.

2.4 Production and Assembly

Design, construction, and testing of the DUNE SP module anode plane assemblies is overseen by the APA consortium. The APA consortium takes a *factory style* approach to the construction

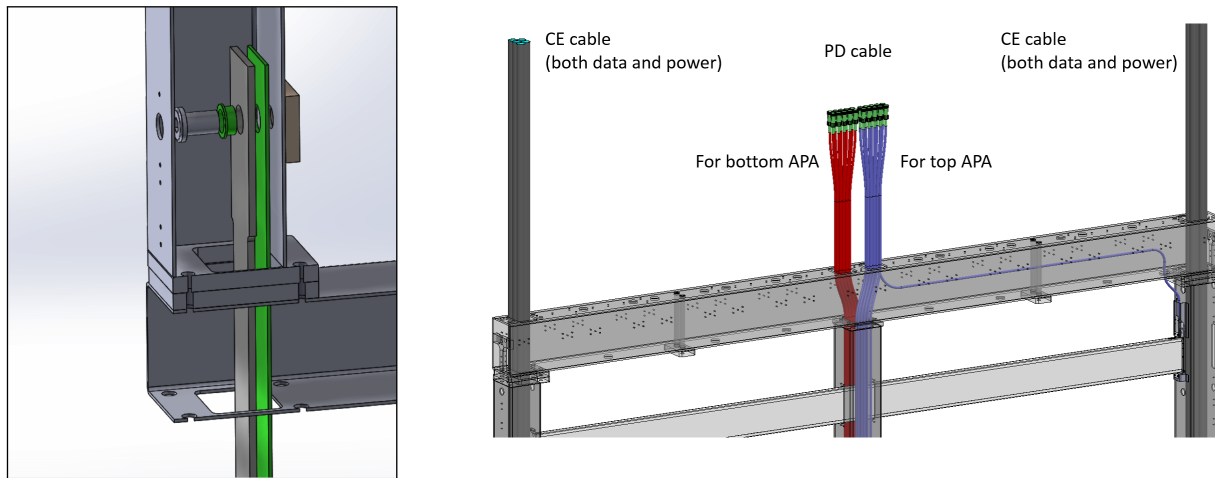


Figure 2.17: Left: Conceptual design for the APA-to-APA connection. The green insulator pieces act to electrically isolate the two frames, as required by the FE electronics. Right: A concept for TPC electronics and PDS cable routing. Photon detector cables would go through the central beam and be distributed inside the supporting tubes of the APA frame. CE cables (both data and power) from the bottom APA electronics would go through the outside tubes to reach the top of the stack.

with multiple factories being planned in the USA and UK. This approach allows the consortium to produce anode plane assemblies at the rate required to meet overall construction milestones and at the same time reduce risk to the project if any location encounters problems that slow the pace of production.

The starting point for the APA production plan for the SP modules is the experience and lessons learned from ProtoDUNE-SP construction. For ProtoDUNE-SP, anode plane assemblies have been constructed both at the Physical Sciences Laboratory (PSL) at the University of Wisconsin in the USA and at Daresbury Laboratory in the UK. APA construction for DUNE is also envisaged to be done at USA and UK collaborating institutions, and assuming construction begins in 2021, a minimum of six production lines is required to build 150 anode plane assemblies within 2.5 years for the first 10 kt SP module.

Based on the ProtoDUNE-SP experience, we estimate that each APA requires approximately 50 shifts (eight-hour intervals) of effort to construct, with a mix of engineering, technical, and scientific personnel. This estimate involves only the wiring stages of production, and assumes that completed frames and all other hardware necessary for construction are ready to go at the factories. Currently an APA can be completed in 64 shifts. Several improvements to the process and tooling are planned that will bring this down to the required 50 shifts. The production model assumes that factories run two shifts per day and that two weeks per year are devoted to maintenance of equipment.

Each production line is centered around a wire winding robot, or *winder*, that enables the continuous wrapping of wire on a 6 m long frame. The winder can also be used to make wire tension measurements by replacing the winding head with a laser photodiode system that then can determine an individual wire's natural frequency and hence its tension. A production line also requires two process carts. These carts support the APA and are used during various steps in the construc-

tion process, e.g., continuity testing, board epoxy installation, etc. A production line, therefore, requires a means of lifting the APA in and out of the winder. A gantry-style crane has been used for ProtoDUNE-SP construction.

Having multiple APA production sites in two different countries presents quality assurance and quality control (QA/QC) challenges. Key among the requirements of production is that every APA be the same, regardless of where it was constructed. To achieve this goal we are building on ProtoDUNE-SP experience where six identical anode plane assemblies were built, four in the USA and two in the UK. This was achieved by using the same tooling, fabrication drawings, assembly and test procedures, and identical acceptance criteria at both sites. This uniform approach to construction for DUNE is necessary, and the APA consortium is developing the necessary management structure to ensure that each factory and production line follows the agreed upon approach to achieve APA performance requirements.

2.4.1 Facility Plans

Construction of SP module anode plane assemblies is planned to take place in both the USA and the UK. Daresbury Lab in the UK will house multiple production lines, one of which already exists from ProtoDUNE-SP. In the USA, it is anticipated that production lines will be set up at the University of Chicago, Yale University, and the already existing production facility at the University of Wisconsin, PSL. At least eight APA production lines spread over multiple facilities will provide some margin on the production schedule and provide backup in the event that technical problems occur at any particular site. The space requirements for each production line are driven by the large size of the APA frames and the winding robot used to build them. The approximate dimensions of a class 100,000 clean space needed to house winder operations and associated tooling is 175 m². The estimated requirement for inventory, work in progress, and completed anode plane assemblies is about 600 m². Each facility also needs temporary access to shipping and crating space of about 200 m². Possible floor layouts at each institution are currently in development. Adequate space is available at each site and commitments have been expressed by the institutions for its use on DUNE.

The University of Wisconsin has space available within the Physical Sciences Lab Rowe Technology Center. A portion of the facility has been used for the past two years for the ProtoDUNE-SP project. There is approximately 20,000 ft² (1850 m²) available for DUNE and the possibility exists to expand the current clean tent to house another production line.

ProtoDUNE-SP construction has also taken place at Daresbury Lab. The current facility cannot accommodate multiple production lines, but the “Inner Hall” on the Daresbury site has been identified as an area that is sufficiently large to be used for DUNE APA construction. It has good access and crane coverage throughout. Daresbury Laboratory management have agreed that the area is available, but investment is needed to establish a safe working environment. Preparation work for the construction area is underway to clear the current area of existing facilities, obsolete cranes, and ancillary equipment. Also planned is the renovation of a plant room to be used for storage and as a shipping area. This work is ongoing. The production factory is being designed to hold four winding machines and associated process equipment and tooling.

The Enrico Fermi Institute at the University of Chicago and the Wright Laboratory at Yale University each have the needed infrastructure to house up to two APA production lines. Development work that is relevant for local planning at each site has begun at those institutions, as well.

2.4.2 Assembly Procedures and Tooling

The central piece of equipment used in APA production is the custom-designed wire winder machine, shown in use in Figure 2.18. An important centerpiece of the winder machine is the wiring head. The head releases wire as motors move it up and down and across the frame, controlling the tension in the wire as it gets laid. Currently, the head then positions the wire at solder connection points for soldering by hand. The fully automated motion of the winder head is controlled by software, which is written in the widely used numerical control G programming language. The winder also includes a built-in vision system to assist operators during winding, which is currently used at winding start-up to find a locator pin on the wire boards. In the current scheme used for ProtoDUNE-SP, during the winding process an APA moves on and off the winder machine multiple times for wiring, soldering, testing, etc.



Figure 2.18: Left: Partially wired ProtoDUNE-SP APA on the winding machine at Daresbury Lab, UK. Right: Partially wired ProtoDUNE-SP APA on the winding machine during wire tension measurements at University of Wisconsin, PSL.

Two large process carts, shown in Figure 2.19, are used to move anode plane assemblies around the assembly facility. One process cart with regular casters remains in the assembly area and is maintained at a particular height that coordinates with other construction tooling such as jack stands and platform ladders. A second process cart has been fitted with specialized 360° rotating casters that allow the process cart loaded with a fully assembled APA to maneuver corners during the journey from the assembly area to the shipping/packing location.

Before wiring can begin, the first operation with a bare frame is to install the grounding mesh.

In the ProtoDUNE-SP design, a large jig is needed to hold the mesh in place for gluing. Once the jig is leveled sufficiently to the frame, a mesh sheet is laid into place and hold down bars are iteratively moved and repositioned until the mesh is flat and tight. The outside edge of the mesh panel then gets epoxied, and the jig and hold down bars remain in place for a 12 hour epoxy cure cycle. This process is then repeated for the next three shifts until all four panels of mesh have been attached to the bare APA frame. As described below, changes to this lengthy procedure are being considered for DUNE anode plane assemblies.

Another custom construction jig is needed for installing the wire combs that hold the wires at intermediate points above the four cross beams of the APA. Currently there are two jigs that can be loaded and installed at a time, and each installation requires a six-hour epoxy cure cycle.



Figure 2.19: (Left) APA being moved around a production facility on the process cart. (Right) APA frame with the grounding mesh already installed is shown sitting on a process cart. Two technicians are using a custom jig to place the wire combs above a horizontal cross beam on the APA.

2.4.3 Material Supply

Ensuring the reliable supply of raw materials and parts to each of the factories is critical to keeping APA production on schedule through multiple years of construction. Here the consortium institutions play a pivotal role taking on the responsibility for the delivery of APA sub-elements to

each of the factories. Supplier institutions have responsibility for the sourcing, inspection, cleaning, testing, quality assurance, and delivery of hardware to each of the factories.

- **Frame construction:** We envision two sources of frames, one in the USA and one in the UK. The institutions responsible will rely on many lessons learned from ProtoDUNE-SP. The effort requires specialized resources and skills including a large assembly area, certified welding capability, large scale metrology tools and experience, and large scale tooling and crane support. Two approaches are under consideration for sourcing; one is a total outsource strategy with an industrial supplier, the other is to procure all of the major machined and welded components and then assemble and survey in-house. Material suppliers have been identified and used with good results on ProtoDUNE-SP.
- **Mesh supply and construction:** Elsewhere in this proposal we describe the current mesh installation procedure. However, our ProtoDUNE-SP experience leads us to believe that moving to smaller self-supporting *window screen* panels may save assembly time and improve overall APA quality. An excellent source of mesh exists and was used on ProtoDUNE-SP.
- **Wire procurement:** Wire is a significant element in the assembly of an APA. There is approximately 24 km| of wire wound on each unit. Through ProtoDUNE-SP an excellent supplier has worked with us to provide wire that is of high quality and wound on spools that we provide. These spools are then used directly on the winder head with no additional handling or re-spooling required. Wire samples from each spool are strength tested prior to use.
- **Comb procurement:** An institution will work with either our existing comb supplier or find additional suppliers that can meet our requirements. The ProtoDUNE-SP supplier has been very reliable.
- **Wire wrapping board procurement:** One or more consortium institutions will take on the responsibility of wire-wrapping board supply. The side and foot boards are unique to suppliers as they have electrical traces and provide wire placement support through a separately bonded tooth strip. There are 276 boards per APA, or 41,400 needed for 150 anode plane assemblies. The institutions that have responsibility for boards will spend time working with multiple vendors to reduce risk and ensure quality.
- **Capacitor resistor boards:** These boards are unique given their thickness, HV components, and leakage current requirements. A reliable source of bare boards was found for ProtoDUNE-SP. Assembly and testing was performed at PSL. We will conduct a more exhaustive search of vendors that are willing to take on assembly and testing for the 3000 plus boards needed for DUNE.
- **Winders and tooling:** We propose that PSL and Daresbury work together to supply tooling and winding machines for additional production lines at new locations and for additional lines in-house. This is a natural collaboration that has been in place for nearly two years on ProtoDUNE-SP.

2.4.4 Planned Improvements to Production Process

Based on our ProtoDUNE-SP experience, we have identified several potential improvements to tooling and process that allow the anode plane assemblies to be constructed in a more efficient and reliable manner, including:

- **Wiring head design:** Efforts to improve winder head performance are already underway. We envision improved tension control, continuous tension feedback, improved clutch, and an improvement to the compensator mechanism all leading to better, more consistent, and more reliable winder performance. The current winding head uses a magnetic clutch mechanism that is manually adjusted to increase or decrease the tension of the wire as it is wound around the APA. The clutch regularly needs adjustment as the diameter of the wire on the spool reduces during the winding process. In addition, if the mechanism is run from a cold start, it has been observed that the tension changes after ~ 10 minutes of running. Experience winding the ProtoDUNE-SP anode plane assemblies has shown that it is difficult to maintain the target tension within tolerances (5 ± 1 N for ProtoDUNE-SP).

A solution to this issue is to design a winder head with active tension control. This can be achieved by replacing the magnetic clutch with a servo motor and introducing a potentiometer on a dancer arm for the feedback loop (see Figure 2.20). This only works if there are no signal losses when transferring the winding head to the compensator latching mechanism and back. The system can be driven in torque mode and compensates for any wire spool changes. It must be able to operate from a cold start. This development is well underway and tests are currently being carried out.

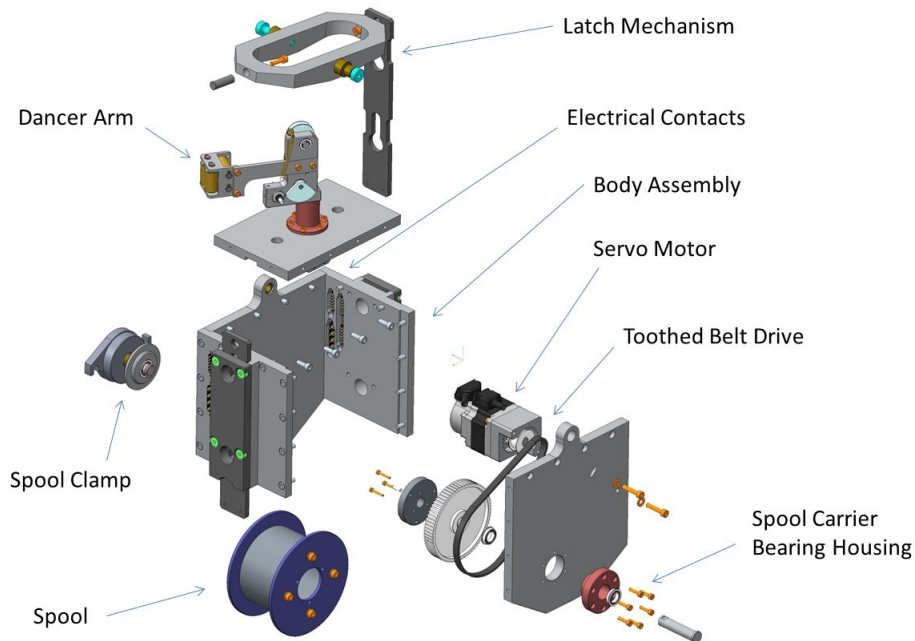


Figure 2.20: Exploded view of winder head with active tension control.

- **Winder interface arm design:** The current winder interface only allows one-half of a wire

plane to be wired at a time. The APA frame must be moved to the process cart where the interface arms are flipped 180° to wind the second half of the wire plane. A new design concept, illustrated in Figure 2.21, allows the winder head to pass from one side to the other in a nearly continuous fashion without removal from the winding machine. The interface frames are replaced at either end by retractable linear guided shafts. These can be withdrawn to allow passing of the winding head around the frame over the full height of the frame. These shafts have conical ends and locate in shafts that are fixed to the internal frame tube to provide guided location. This design change does not alter the design of the frame. The design also allows for rotation in the winding machine, so that it should also be possible to carry out board installation and gluing & soldering in the winding machine. This eliminates the need to transfer the APA to the process cart for the whole of the production operation, which is inherently a safer and faster production method as it cuts down the amount of handling of the APA.

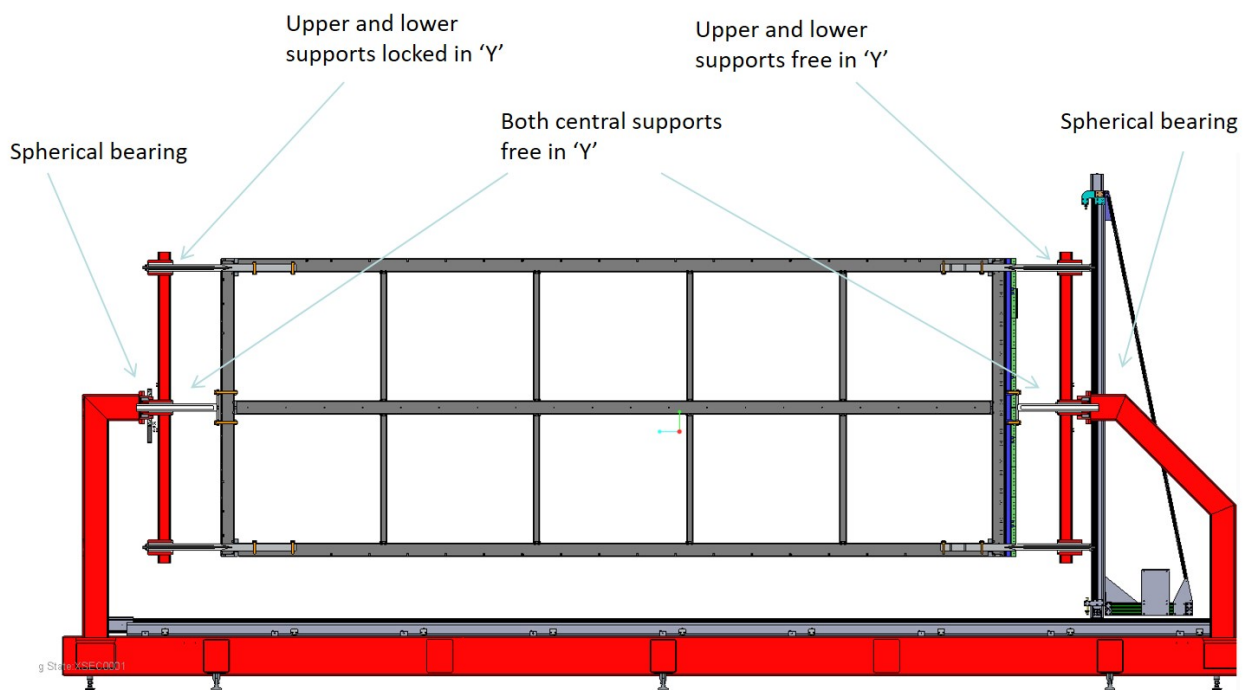


Figure 2.21: Work is ongoing to modify the wiring machine design to allow an APA frame to be rotated without removing it from the frame. This would reduce the required handling of the frame during fabrication and speed production substantially.

- **Modular mesh panels:** The current approach to mesh installation is slow and cumbersome. We will improve this aspect of construction by moving toward a modular window screen design that improves the reliability of the installed mesh (more uniform tension across the mesh), and allows much easier installation on the APA frame.
- **Epoxy process improvements:** There are many epoxy application steps during the construction process. These steps require careful work that takes many hours between winding each successive wire plane. We already have concepts for improved epoxy application jigs from ProtoDUNE-SP, and we will investigate whether epoxy pre-forms or accelerated heat curing can yield time or reliability improvements.

- Automated soldering: Every solder joint on the six ProtoDUNE-SP anode plane assemblies was done by hand. We will investigate automated soldering techniques to improve process and reduce the amount of manual effort required.
- Wire tension measurement techniques: Verifying wire tension is an important, but time consuming process during construction. The current technique utilizes a laser photodiode tool mounted on the winder to measure tension one wire at a time. This takes many hours for each wire plane. Techniques are under development by collaborators at the University of Manchester to electronically measure groups of 20 or more wires at one time. This technique provides much faster tension measurements and shorter turnaround between wire planes.
- Winder maintenance plan: The approach to winder maintenance used during ProtoDUNE-SP construction was not well formed. As a result, winding machine problems that can be traced back to lack of routine maintenance occurred from time to time, which shut the production line down until a repair or maintenance was performed. We will formulate a routine and preventive maintenance plan that minimizes winder downtime during APA production.

2.4.5 Quality Assurance and Quality Control in APA Production

A key input to quality assurance (QA) for the APA design and manufacturing procedures is the experience with ProtoDUNE-SP, including upcoming operations and data analysis results from the detector. Much has already been learned regarding design, component testing, and fabrication procedures that will go into formulating the detailed design and plans for the APA construction project over the next year. The set of final design drawings and detailed procedures documentation generated over the next year leading to the TDR represent an important element of the QA plan for the fabrication of the anode plane assemblies.

Summaries of all QA testing performed for elements used in the final design of the anode plane assemblies will also be prepared for the TDR. Much data already exists, and again, ProtoDUNE-SP will provide valuable additional information regarding the robustness of the detector components and construction.

2.4.5.1 Incoming Inspections

Some components require inspection and quality control (QC) checks prior to use on an APA, including:

- Frame components: If the APA steel frames are produced in-house, then upon receipt of the rectangular hollow section steel for the frames, a selection procedure is followed to choose the sections of the steel most suited to achieving the geometrical tolerances.
- Wire testing: The CuBe wire is provided on spools from the supplier. Samples from each spool are strength tested prior to use on an APA.

- Circuit boards: All circuit boards that get installed on an APA are inspected for dimensional accuracy prior to being routed through various epoxy and cleaning processes as they are prepped for assembly. Inspection results are documented, and if anomalies are found, an electronic non-conformance report is written.
- CR and G -plane bias board testing: Acceptance tests of these boards include leakage current measurements (<0.5 nA) and continuity tests on each channel. This test is performed at room temperature. ProtoDUNE-SP was used to perform design validation on over 100 boards that were cycled and tested at LN temperature. No failures were seen during these tests.

2.4.5.2 APA Acceptance Tests

The following are examples of quality control data to be collected for each APA during production:

- Frame flatness: A laser survey is performed to measure the flatness of the assembled bare frame. Three sets of data are compiled into a map that shows the amount of bow, twist, and fold in the frame. Each of these parameters is compared to an allowable amount that does not cause wire plane-to-plane spacing to be out of tolerance (± 0.5 mm). A visual file is created for each APA from measured data. A final frame survey is completed after all electrical components have been installed, and the as-built plane-to-plane separations are measured to verify the distance between adjacent wire planes.
- Mesh to frame connection: To confirm sufficient electrical contact between these two components a resistance measurement is taken in each of 20 zones of mesh bounded by the outside frame perimeter and the four cross beam ribs. This measurement is completed immediately after mesh install, prior to any winding.
- Wire tension: The tension of each wire is measured after each new plane of wires is installed on an APA. The optimal target tension is still under discussion (was 5 N in ProtoDUNE-SP), as are the necessary tolerances. ProtoDUNE-SP data, where the tensions have substantial variation, will provide important data for quantifying the impacts of varying tensions.

2.4.5.3 Documentation

Each APA is delivered with a traveler document in which specific assembly information is gathered, initially by hand on a paper copy, then entered into an electronic version for longer term storage. The traveler database contains a detailed log of the production of each APA, including where and when the APA was built and the origin of all parts used in its construction.

As assembly issues arise during the construction of an APA, they are gathered in an issue log for each APA, and separate short reports are created to provide details of what caused the occurrence, how the issue was immediately resolved, and what measures should be taken in the future to ensure the specific issue has a reduced risk of occurring.

2.5 Integration and Installation

Completed anode plane assemblies are shipped from the APA production sites to an integration and test facility (ITF) for integration with the TPC FE electronics and PDs. The ITF location is not decided, but facilities near the SURF site are being considered. Activities at the ITF include extensive QC testing to ensure the functioning of the fully integrated anode plane assemblies. Once checked, the anode plane assemblies are repackaged for final transport to SURF. Each APA, still in its transport crate, are hung from the Ross Shaft cage by a sling and transported underground where it is stored in a waiting area. Pairs of anode plane assemblies must be linked in their vertical configuration and cables ran from both the lower and upper anode plane assemblies in an area just outside the cryostat. Once completed, the pair enters through the temporary construction opening (TCO) onto the DSS and is moved into its final position. Final checkout tests are performed once the anode plane assemblies are in place.

The integration with the PDs is expected to be done at the Integration Facility. An alternative plan entailing PDS installation at the APA production sites is also under consideration. The TPC FE electronics are installed at the ITF and the exact installation sequence will be developed with the electronics consortium.

A conceptual layout of the space required at the Integration Facility is being developed. An overhead crane is needed to lift anode plane assemblies out of their shipping crate and maneuver them through the facility. Most of the handling areas need to be embedded in a class 100,000 clean tent. Finally, a cold box will be available for QC testing of the electronics once installed on the APA (see Section 2.5.3.1).

2.5.1 Transport and Handling

Custom designed crates are used for transport between the production sites and the ITF, and between the ITF and SURF. The design of the crates is still being finalized, but there are currently two possible approaches. The first is to use less expensive, disposable crates for transport to the ITF and fewer, more expensive crates for transport underground, which are reused between the ITF and underground. The second option is a single crate that is used for all transport stages. The transport underground requires a design that allows a 180° rotation of the crate.

The handling of the anode plane assemblies at the ITF and underground is done with overhead cranes. Once the anode plane assemblies are repackaged in the crates, they are loaded on a truck, driven to the mine, transported to the cage, secured on the sling under the cage (see figure 2.22), lowered down and moved to the underground storage area.

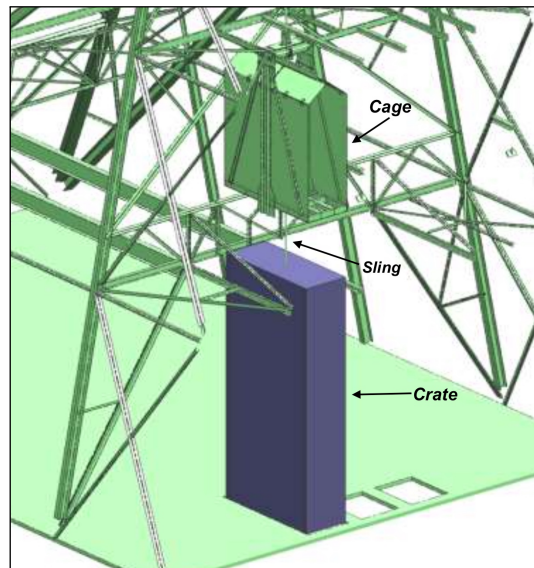


Figure 2.22: The APA crate (in blue) is brought underground with a sling under the elevator cage (the green box at the top of the figure). The insertion into the crate at the surface is done from the back of the cage, but the extraction underground must be done from the front of the cage. The APA crate must, therefore, be able to be rotated by 180° in the sling.

2.5.2 APA-to-CPA Assembly and Installation in the Cryostat

Once underground, there will be a small storage area for stockpiling anode plane assemblies (see Figure 2.23). When ready for installation, each APA is extracted from its crate, inspected and rotated to be lowered into the area just outside of the TCO in the cryostat. Two anode plane assemblies are lowered in front of the TCO where they are linked and cabled. The details of the cabling are still being finalized, but the main option is currently to pass all the cables inside the APA frame tubes (see Section 2.3.3).

Finally, when the two anode plane assemblies are fully cabled, they are placed onto the DSS inside the cryostat (see bottom right of Figure 2.23) and moved to their location in the cryostat where final integration tests are performed. For more information on the detector support structure and installation into the cryostat, see Chapter 8.

2.5.3 Quality Assurance and Quality Control in Integration and Installation

The QC related to integration and installation has two main testing campaigns, one at the Integration Facility (ITF) and one once the anode plane assemblies are installed into their location in the cryostat. Some details are still under development by the installation and integration team within the APA consortium.

A dedicated database for QC is required to keep track of all the components for all the anode plane assemblies at the different stages of the integration and installation. A simple and practical

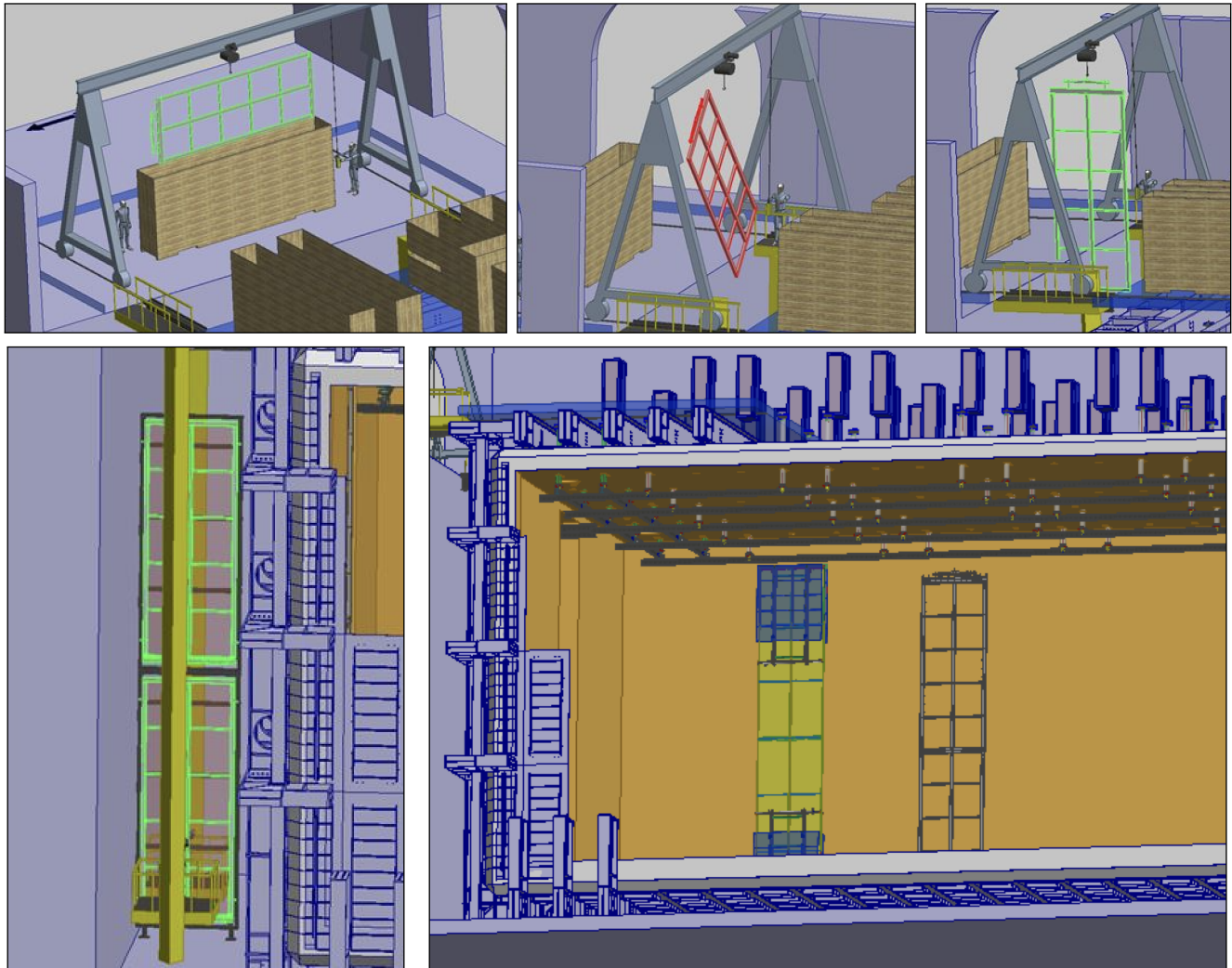


Figure 2.23: (Top row) Handling of an APA in the underground storage area where the anode plane assemblies are extracted from the crates, inspected, and readied for installation in the cryostat. (Bottom row) A pair of anode plane assemblies are brought into the space just outside the TCO to be linked and cabled, then connected to the DSS and moved into their final position inside the cryostat.

method of tagging critical parts in the APA is also under development for efficient integration.

The QA related to integration and installation is heavily based on the ProtoDUNE-SP experience and at this point no dedicated QA protocol is developed. The full development is done by the installation and integration team in the APA consortium.

2.5.3.1 Quality Control at the Integration Facility

All the active detector components are shipped to the ITF for integration and for testing, where more time is available to perform tests. This step is critical for ensuring high performance of the integrated anode plane assemblies. The exact time scale of APA testing needs to be finalized based on information from the production sites and on the installation schedule.

After unpacking an APA at the ITF, a thorough visual inspection is performed. Tension measurements are made for a sample of around 350 wires (representing $\sim 10\%$ of the wires). The default technique is the laser method that has been used for ProtoDUNE-SP. The method works well, but is time consuming, so alternative methods that use voltage measurements are also being pursued to reduce the measuring time. Such improved methods could allow a larger number of wires (even the full APA) to be measured.

Tension values are recorded in the database and compared with the original tension measurements performed at the production sites. Definite guidance for the acceptable tension values will be available to inform decisions on the quality of the APA. Clear pass/fail criteria will be provided as well as clear procedures to deal with individual wires laying outside the acceptable values. This guidance will be based on the ProtoDUNE-SP experience, where the tension of some wires have changed during the production to installation process. In addition, a continuity test and a leakage current test is performed on all the wires and the data is also recorded in the database.

Once the electronics are installed by the electronics consortium, dedicated testing of the APA readout is performed. The integrated APA is inserted in the cold box so that the electronics performance can be tested adequately. Strict guidance is provided for assessing the pass/fail criteria for each APA during these tests. Here too, guidance from ProtoDUNE-SP and development tests will guide the exact criteria. Close collaboration with the electronics consortium is necessary.

When all the tests have been successfully performed and more than 99% of the channels are confirmed functional, the APA is tagged as “good” and prepared for shipment to SURF.

2.5.3.2 Quality Control Underground

There are three opportunities to test the anode plane assemblies underground: in the storage area, once secured in front of the TCO, or once positioned at their final location in the cryostat. The latter is the most important and it may save time to perform the final tests once the full *APA-CPA-APA-CPA-APA* wall is installed (cathode plane assemblies are described in Chapter 4).

This brings the risk that if serious problems are found, anode plane assemblies are harder (more time-consuming) to move out.

The anode plane assemblies are unpacked in the storage area underground (see Figure 2.24). Space in this area is very limited and only visual inspection is performed during unpacking. If clear defects are visible, the APA is returned to the ITF for further investigation.

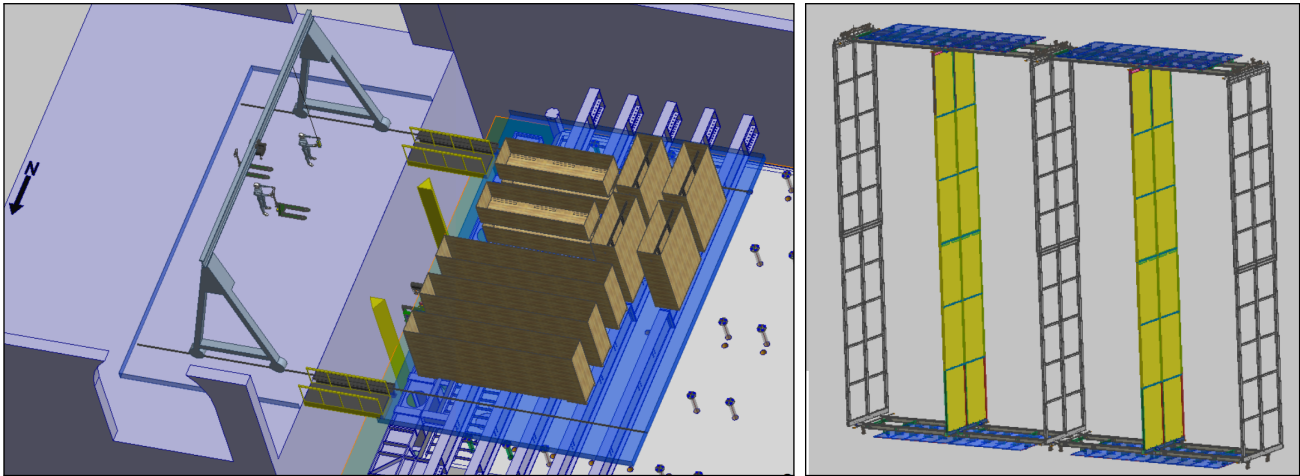


Figure 2.24: Left: A schematic of the layout for the storage and unpacking area underground. Right: A schematic of the layout of a full APA-CPA-APA-CPA-APA wall installed in the cryostat.

Pairs of anode plane assemblies (top and bottom) are lowered in front of the TCO to be linked and cabled. Once the cabling is finished a connection test is performed to ensure adequate cabling. Due to the very restrictive space near the TCO (see Figure 2.23), no additional tests other than visual inspection are performed at that time, and the cabled and linked anode plane assemblies are positioned in their final location in the cryostat.

The current goal is to install a full APA-CPA-APA-CPA-APA wall every week (see Figure 2.24, right). After each wall is installed, the night crew has time for final testing of the installed APA. There are currently two testing models, one where the night crew tests APA pairs as they are installed (every two days), and the other model where the night crew tests the full wall at once. The decision between the two models will be made when accurate estimates of the time needed for the testing become available.

The tests are the same described above at the ITF. Tension on a smaller set of wires is measured ($\sim 5\%$, potentially more if a quicker tension method is developed) to ensure that the installation operations did not alter the anode plane assemblies. Since the complete integration is now done, a full readout test can be performed. Short runs are taken with the data acquisition (DAQ) system to ensure that the readout is fully operational. The details of these tests still need to be developed to provide efficient assessment of the integrated anode plane assemblies. If an APA appears to have more than 1% of the channels not functioning, the APA is sent back to the ITF.

2.5.3.3 Quality Assurance

We will rely on the ProtoDUNE-SP experience to assess most of the QA protocols. The dedicated QA plan during production should ensure that the anode plane assemblies meet the requirements and the installation steps should not modify them. The control of the quality of each wire along the installation steps will ensure fully functioning anode plane assemblies. The detailed QA program is currently under development by the installation and integration group in the APA consortium.

2.6 Safety

Building on the experience of ProtoDUNE-SP, a full safety analysis will be performed and a set of safe work procedures developed for all stages of the fabrication process before the start of DUNE APA production. In the final design of the winding machine, central to the production process, safety must be taken into account right from the design stage and must be kept in mind at all stages in the life of the machine: design, manufacture, installation, adjustment, operation, and maintenance. Handling of the large, but delicate frames is a major challenge and safe procedures will be developed for all phases of construction, including frame assembly, wiring, transport, and integration and installation in the cryostat.

At the factory sites, safety is ultimately the responsibility of the host institutions, and all local rules and regulations must be followed. However, common job hazard analyses can be performed and documents prepared for many shared aspects of the tooling and activities. In addition, safety will be an important element of production readiness reviews that are conducted for the project overall and for the factory sites individually.

2.7 Organization and Management

2.7.1 APA Consortium Organization

The APA consortium comprises 21 institutions, of which 13 are from the USA, seven from the UK, and one from the Czech Republic. The consortium is organized along the main deliverables, which are the final design of the APA and the APA production and installation procedures. Since the two main centers for APA construction are expected to be located in the USA and the UK, there are usually two leaders of each working group, representing the main stakeholders (Figure 2.25). This is particularly important to ensure that common procedures and tooling are developed.

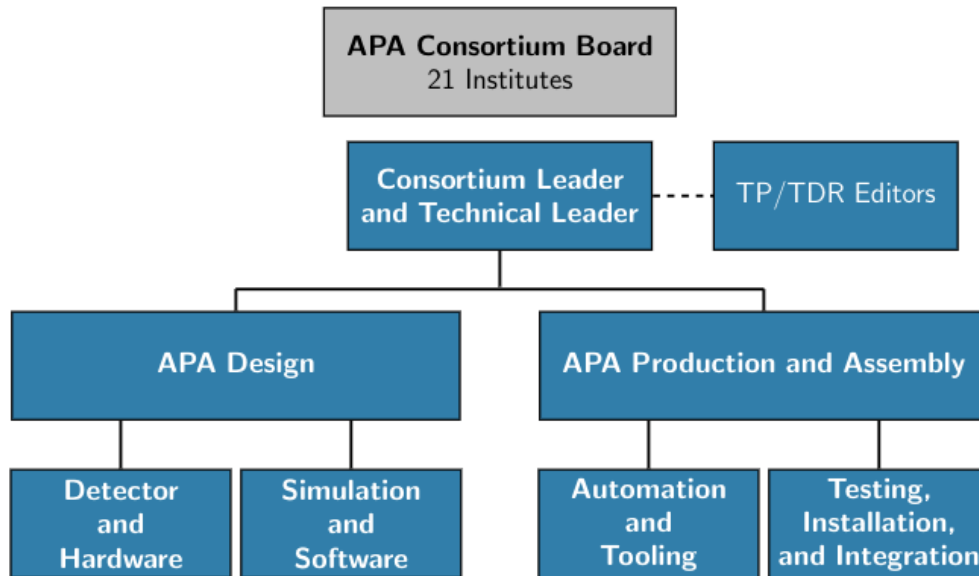


Figure 2.25: APA Consortium organizational chart

2.7.2 Planning Assumptions

The planning assumptions are based on having eight to nine APA assembly lines, at different locations in the UK and the USA. We assume about one year of setup time for the factories. It will take of the order 50 shifts to construct a single APA. Assuming a multi-shift system, we will be able to construct the 150 anode plane assemblies required for one SP module within about two years.

2.7.3 WBS and Responsibilities

Here, we only discuss the top-level WBS elements, which are (1) design, engineering and R&D, (2) production setup, (3) production, (4) integration, and (5) installation.

The validation of the design is mainly a responsibility of the university groups and BNL, while engineering and the production setup will be developed at PSL in Madison (USA) and Daresbury Laboratory (UK), where the anode plane assemblies for ProtoDUNE-SP have been built, with contributions from university groups. In addition to PSL and Daresbury Laboratory, the University of Chicago and Yale University have been identified as candidate sites for the production. The production sites will require significant contributions from university groups during the production process.

In total, we expect half of the anode plane assemblies to be produced in the USA and half in the UK. The steel for the frames is most likely to be bought from a single vendor. The assembly of the frames will be performed in the USA and the UK separately. The options to assemble the frames in house or in collaboration with industrial partners are still being explored.

Other significant components include on-APA electronics boards. Design modifications relative to ProtoDUNE-SP are the responsibility of BNL. The boards will be produced by industry, while the testing will be distributed among consortium institutions. The shipping of the anode plane assemblies is the responsibility of the production factories in the USA and the UK. The integration and installation are a joint responsibility of the Consortium, with ANL providing the interface with the technical coordination group.

2.7.4 High-level Milestones and Schedule

The high-level milestones for the period 2018 to 2024 are given in Table 2.5 for the periods before and after the TDR. The final design of the anode plane assemblies to be proposed in the TDR will be informed by the experience of the ProtoDUNE-SP APA production and performance, which will be reviewed in early 2019. Additional design considerations that cannot be directly tested through ProtoDUNE-SP, such as the two-APA assembly and the related cabling issues, will require a full test with cabling of a two-APA assembly also in early 2019. The production schedule, the required number of assembly lines, and the location of the production factories will depend on the improvements of the wire winding procedures, which will formally be reviewed in January 2019. The post-TDR milestones are driven by the high-level international project milestones and are based on a schedule with one year factory preparation and about two years of APA construction time.

Table 2.5: APA design and construction milestones

Date	Milestone
Pre-TDR	
December 2018	Test two-APA assembly
January 2019	Formal review of complete modifications to the winder design
February 2019	Formal review of ProtoDUNE-SP APA performance
February 2019	Complete assembly test of FD prototype APA
March 2019	Decision on location of factories and required number of assembly lines
March 2019	APA cost estimate for SP module
March 2019	APA schedule for SP module
April 2019	APA section of TDR delivered
Post-TDR	
2020	Preparation of APA factories
2021 – 2023	Construction of anode plane assemblies
2022/3	Installation of anode plane assemblies in SP module 1
2024	Commissioning of SP module 1

Chapter 3

TPC Electronics

3.1 TPC Electronics (CE) System Overview

3.1.1 Introduction

DUNE single-phase time projection chamber TPC electronics hardware signal processing takes place inside the LAr, in boards that are directly mounted on the anode plane assembly (APA); accordingly, the TPC readout electronics are referred to as the cold electronics (CE). The electronics are mounted inside the LAr to exploit the fact that charge carrier mobility in silicon is higher and that thermal fluctuations are lower at LAr temperature than at room temperature. For CMOS (complementary metal-oxide-semiconductor) electronics, this results in substantially higher gain and lower noise at LAr temperature than at room temperature [2]. Mounting the front-end electronics on the APA frames also minimizes the input capacitance. Furthermore, placing the digitizing and multiplexing (MUX) electronics inside the cryostat reduces the total number of penetrations into the cryostat and minimizes the number of cables coming out of the cryostat. As the full TPC electronics chain for the SP module includes many components on the warm side of the cryostat as well, the DUNE consortium designated to organize development of this system is called the DUNE *Single-Phase TPC Electronics* consortium. It is sometimes referred to as the CE consortium for short.

The overall noise requirement drives the choice of architecture of the TPC electronics. This requirement is difficult to establish precisely, but it is clear that the lower the electronic noise is, the greater the physics reach of the DUNE experiment will be. An equivalent noise charge (ENC) of less than approximately $1000e^-$ is required for satisfactory reconstruction of accelerator neutrino interactions, but a lower noise level will yield significantly better two-track separation and primary vertex resolution, and thus higher efficiency and/or lower background for identifying electron neutrino interactions. Setting the noise level requirement for the DUNE SP module more precisely is an ongoing effort.

The noise level enabled by having the front-end electronics in the cold (roughly half as much noise at LAr temperature than at room temperature) greatly extends the reach of the DUNE physics program. Decreasing the noise level allows for smaller charge deposits to be measurable, which acts as a source of risk mitigation in the case that the desired drift field can not be reached or the electron lifetime in the detector is lower than desired (due to the electronegative impurities in the detector), and also increases the reach of low-energy physics measurements such as those associated with stellar core-collapse supernova burst neutrinos. Finally, the low noise level allows the experiment to utilize low-energy ^{39}Ar beta decays for the purpose of calibration in the DUNE SP module. The noise level requirement of $\text{ENC} < 1000 e^-$ will allow for the use of ^{39}Ar beta decays in calibrations at the DUNE SP module.

In order to retain maximum flexibility to optimize reconstruction algorithms after the DUNE data is collected, the SP module electronics are designed to produce a digital record that is a representation of the waveform of the current produced by charge collection/induction on the anode wires. Each anode wire signal is input to a charge sensitive amplifier, followed by a pulse shaping circuit and an analog-to-digital converter (ADC). In order to minimize the number of cables and cryostat penetrations, the ADCs as well as the amplifier/shapers are located in the LAr, and digitized data from many wires are merged onto a much smaller set of high speed serial links.

3.1.2 System Description, Scope and Current Status

The CE signal processing is implemented in application-specific integrated circuits (ASICs) using CMOS technology. The CE is continuously read out, resulting in a digitized ADC sample from each APA channel (wire) up to every 500 ns (2 MHz sampling rate).

Each individual APA has 2560 channels that are read out by 20 front-end mother boards (FEMBs), with each FEMB enabling digitized wire readout from 128 channels. One cable bundle connects each FEMB to the outside of the cryostat via a CE signal cable flange located at the CE feedthrough at the top of the cryostat, where a single flange services each APA, as shown in Figure 3.1. Two CE signal flanges are located on each feedthrough, together accounting for all electronics channels associated with a pair of anode plane assemblies (upper and lower, vertically arranged). Each cable bundle contains wires for low-voltage (LV) power, high-speed data readout, and clock or digital-control signal distribution. Eight separate cables carry the TPC wire bias voltages from the signal flange to the APA wire bias boards, in addition to the bias voltages for the field cage termination electrodes and for the electron diverters. An additional flange on the top of each feedthrough services the photon detection system (PDS) cables associated with the APA pair.

The components of the CE system are the following:

- front-end mother boards (FEMBs), on which the ASICs are mounted, which are installed on the anode plane assemblies;
- cables for the data, clock and control signals, LV power, and wire bias voltages between the APA and the signal flanges (cold cables);

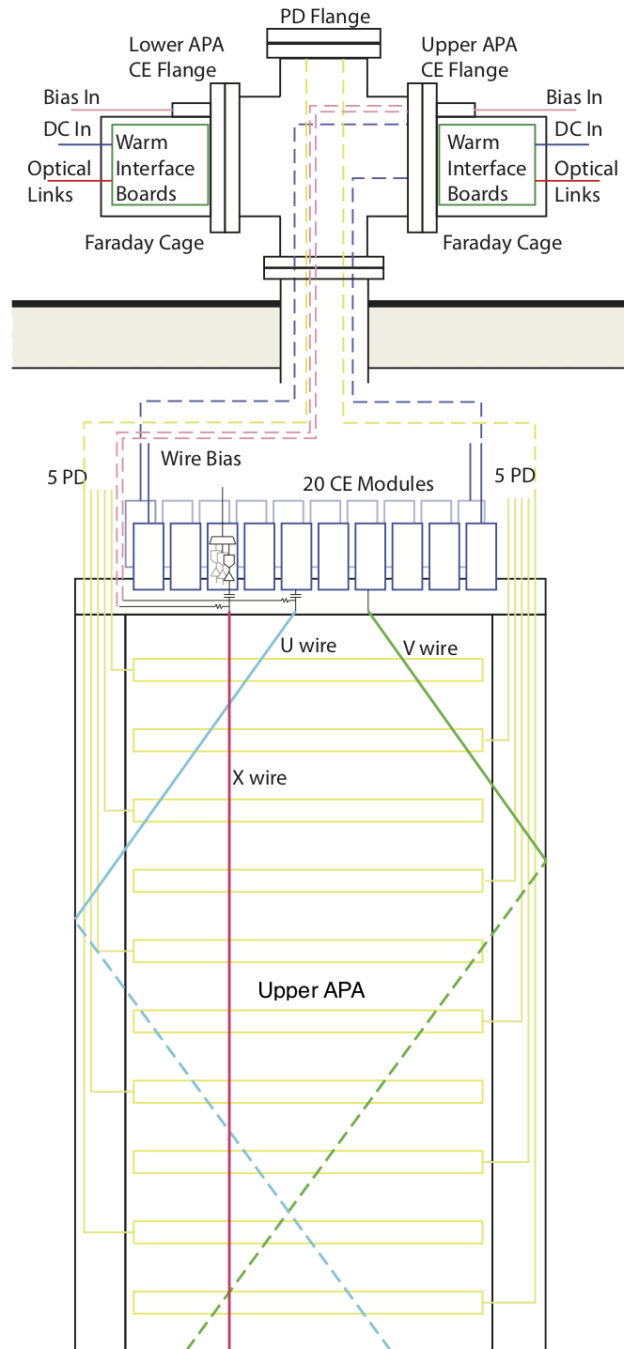


Figure 3.1: Connections between the signal flanges and APA. Only the upper APA of the hanging APA pair, described in Section 2.2.2, and its connection paths are shown. The lower APA shares the PD flange with the upper APA but has a separate TPC readout flange. A *CE module* consists of all CE associated with 128 channels of digitized readout.

- signal flanges with a CE feedthrough to pass the data, clock and control signals, LV power, and APA wire-bias voltages between the inside and outside of the cryostat, in addition to the corresponding cryostat penetrations and spool pieces;
- warm interface electronics crates (WIECs) that are mounted on the signal flanges and contain the warm interface boards (WIBs) and power and timing cards (PTCs) for further processing and distribution of the signals entering and exiting the cryostat;
- cables for LV power and wire bias voltages between the signal flange and external power supplies (warm cables); and
- LV power supplies for the CE and bias-voltage power supplies for the anode plane assemblies.

Table 3.1 lists the component type, the quantity required for each type and the number of channels per component of each type.

Table 3.1: TPC electronics components and quantities for a single APA of the DUNE SP module.

Element	Quantity	Channels per element
Front-end mother board (FEMB)	20 per APA	128
FE ASIC chip	8 per FEMB	16
ADC ASIC chip	8 per FEMB	16
COLDATA ASIC chip	2 per FEMB	64
Cold cable bundle	1 per FEMB	128
Signal flange	1 per APA	2560
CE feedthrough	1 per APA	2560
Warm interface board (WIB)	5 per APA	512
Warm interface electronics crate (WIEC)	1 per APA	2560
Power and timing card (PTC)	1 per APA	2560
Power and timing backplane (PTB)	1 per APA	2560

The baseline design for the SP module TPC electronics calls for three types of ASICs to be located inside of the LAr:

- a 16-channel front-end (FE) ASIC for amplification and pulse shaping, referred to as LArA-SIC in the following;
- a 16-channel 12-bit ADC ASIC operating at 2 MHz; and
- a 64-channel control and communications ASIC, referred to as COLDATA in the following.

The FE ASIC has been prototyped and is close to meeting requirements (discussed in Section 3.1.3). Another prototype to address issues in the version deployed in ProtoDUNE-SP is expected in the spring of 2018. Key portions of the control and communications ASIC (also referred to as the COLDATA ASIC) have been prototyped and meet requirements. However, it has been determined that the BNL-designed P1-ADC ASIC now being used in ProtoDUNE-SP does not meet

requirements, and accordingly, its development has been terminated. A new ADC ASIC (referred to as the cold ADC ASIC) is being developed by an LBNL-Fermilab-BNL collaboration and first prototypes are expected by the end of summer 2018. The first full prototype of the controls and communication ASIC is also expected to be available for testing by the end of summer 2018.

In order to maximize the probability of developing a complete design for cold TPC FE electronics in a timely fashion, an alternative solution is also being investigated, a single 64-channel ASIC that will consolidate all three functions described above. This design is being done at SLAC and first prototypes are expected in summer 2018. An ADC solution in the form of a developmental ADC chip for an upgrade of the ATLAS detector provides an additional backup option; this option will be explored further if the performance of the other two ADC solutions being considered do not meet the requirements for DUNE.

While the higher charge carrier mobility at LAr temperature than at room temperature is central to the improved performance of CE, it also leads to the *hot carrier effect*. In n-type MOS transistors, the carriers (electrons) can acquire enough kinetic energy to ionize silicon in the active channel. This charge can become trapped and lead to effects (including threshold shifts) similar to those caused by radiation damage. This effect can cause MOS circuits to age much more quickly at LAr temperature than at room temperature, reducing performance and potentially causing failure. In order to mitigate this effect, the maximum E field in transistor channels must be lower than the field that can be reliably used at room temperature. This is accomplished by using transistors that are fabricated with longer than typical length and operated at reduced bias voltage. Any commercial circuits that are used in the LAr must be carefully tested to ensure that they will perform well for the expected 20-year lifetime of DUNE.

A series of tests are planned to demonstrate that the CE system design will meet DUNE requirements. These include two system tests: one using the ProtoDUNE-SP *cold box* at CERN, and one using a new small LArTPC at Fermilab. The latter will also accommodate one half-length DUNE PD, and will provide a low-noise environment that will allow one to make detailed comparisons of the performance of the new ASICs. It will also enable the study of interactions between the TPC readout and other systems, including the PD readout and the high voltage (HV) distribution. These test facilities are discussed in more detail in Section 3.5.2. Plans are also being made for a second period of data taking for the ProtoDUNE-SP detector, with final anode plane assemblies including the final ASICs and FEMBs replacing the current prototypes. This second run of ProtoDUNE-SP is planned for 2021-2022.

3.1.3 System Requirements

In addition to the noise requirement (less than $1000 e^-$), several additional requirements determine most of the other important TPC electronics specifications. These are:

- The FE peaking time must be in the range 1 to 3 μs . This requirement is derived primarily from the time required for drifting charges to travel from one plane of anode wires to the next.

- The FE must have an adjustable baseline. This requirement reflects the fact that the signal from induction wires is bipolar while the signal from the collection wires is mostly unipolar.
- The ADC sampling frequency must be 2 MHz. This value is chosen to match a FE shaping time of 1 μ s (approximate Nyquist condition) while minimizing the data rate.
- The system must have a linear response up to an impulse input of at least 500,000 e^- . This roughly corresponds to the charge collected on a single wire from one stopping proton and two more highly ionizing protons, all assumed to have trajectories at 45° with respect to the beam axis. This number was chosen so that saturation will occur in less than 5% of beam related events. Studies are ongoing (including an evaluation of LArIAT [3] data and simulation studies) to better understand this requirement.
- The dynamic range of the system must be at least 3000:1. This number is given by the ratio between the maximum signal for no saturation and 50% of the lowest possible noise level. It implies a 12-bit ADC.
- The ADC must not contribute significantly to overall FE noise. This requirement is dependent on the gain of the FE, but for each gain setting translates into requirements on ADC parameters including non-linearity and noise.
- The power dissipated by the electronics located in the LAr must be less than 50 mW/channel. Lower power dissipation is desirable because the mass of the power cables scales with the power. Studies are ongoing to understand if the amount of power dissipated by the electronics should be minimized further due to potential complications from argon boiling; in principle this should not be a problem because the CE boxes housing the FEMBs are designed to channel bubbles to the APA frames.

Finally, all electronics located in the LAr must be highly reliable because it will not be possible to access the CE for repair once the cryostat is filled with LAr. Studies are ongoing to quantify the impact of failures in the TPC and electronics, including single wire failures, and failures of groups of 16, 64, or 128 channels.

3.2 System Design

3.2.1 Grounding and Shielding

In order to minimize system noise, the CE cables for each APA enter the cryostat through a single CE flange, as shown in Figure 3.1, creating, for grounding purposes, an integrated unit consisting of an APA frame, FEMB ground for all 20 CE modules, TPC flange, and warm interface electronics. To accomplish this, the input amplifiers on the FE ASICs have their ground terminals connected to the APA frame. All power-return leads and cable shields are connected to both the ground plane of the FEMB and to the TPC signal flange.

The only location where this integrated unit makes electrical contact with the cryostat, which defines *detector ground*, is at a single point on the CE feedthrough board in the TPC signal flange where the cables exit the cryostat. Mechanical suspension of the anode plane assemblies is accomplished using insulated supports. To avoid structural ground loops, the APA frames described in Chapter 2 are insulated from each other.

Filtering circuits for the APA wire-bias voltages are locally referenced to the ground plane of the FEMBs through low-impedance electrical connections. This approach ensures a ground-return path in close proximity to the bias-voltage and signal paths. The close proximity of the current paths minimizes the size of potential loops to further suppress noise pickup.

Signals associated with the PDS, described in Chapter 5, are carried directly on shielded, twisted-pair cables to the signal feedthrough. The cable shields are connected to the cryostat at the PD flange shown in Figure 3.1, and to the PCB shield layer on the PDs. There is no electrical connection between the cable shields and the APA frame.

3.2.2 Connections from Wire to Front-End

Each side of an APA includes four wire layers as described in Section 2.2. Electrons passing through the wire grid must drift unimpeded until they reach the X -plane collection layer. The nominal bias voltages are predicted to result in this electrically transparent configuration, and are given in Section 2.2.

The filtering of wire bias voltages and AC coupling of wire signals passing onto the charge amplifier circuits is done on capacitance-resistance (CR) boards that plug in between the APA wire-board stacks and FEMBs. Each CR board includes single RC filters for the X - and U -plane wire bias voltages. In addition, each board has 48 pairs of bias resistors and AC coupling capacitors for X -plane wires, and 40 pairs for the U -plane wires. The coupling capacitors block DC while passing AC signals to the CE motherboards. A schematic diagram of the ProtoDUNE-SP APA wire bias subsystem is illustrated in Figure 3.2.

Clamping diodes limit the input voltage received at the amplifier circuits to between $1.8\text{ V} \pm U_D$, where U_D is the breakdown voltage of the diode, $\sim 0.7\text{ V}$. The amplifier circuit has a 22 nF coupling capacitor at input to avoid leakage current from the protection clamping diodes.

Bias resistance values should be at least $20\text{ M}\Omega$ to maintain negligible noise contributions. The higher value helps to achieve a longer time constant for the high-pass coupling networks. Time constants should be at least 25 times the electron drift time so that the undershoot in the digitized waveform is small and easily correctable. However, leakage currents can develop on PC boards that are exposed to high voltages over extended periods. If the bias resistors are much greater than $50\text{ M}\Omega$, leakage currents may affect the bias voltages applied to the wires. The target value of $50\text{ M}\Omega$ was used in ProtoDUNE-SP.

The bias-voltage filters are RC low-pass networks. Resistance values should be much smaller than the bias resistances to control crosstalk between wires and limit the voltage drop if any of the wires

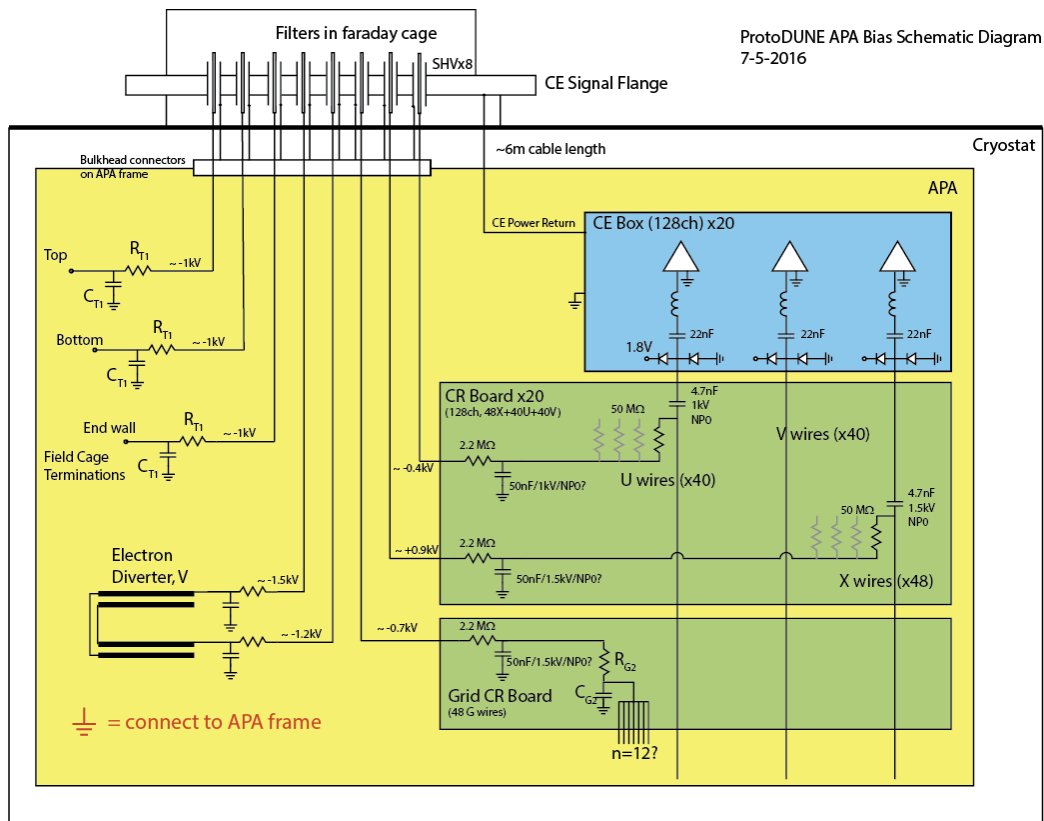


Figure 3.2: ProtoDUNE-SP APA wire bias schematic diagram, including the CR board.

becomes shorted to the APA frame. The value of $2.2\text{ M}\Omega$ was used in ProtoDUNE-SP. Smaller values may be considered for the SP module although a larger filter capacitor would be required to maintain a given level of noise reduction. The target value of 47 nF was used in ProtoDUNE-SP for the filter capacitors.

3.2.3 Front-End Mother Board (FEMB)

3.2.3.1 Overview

Each APA is instrumented with 20 FEMBs. The FEMBs plug into the APA CR boards, making the connections from the wires to the charge amplifier circuits as short as possible. Each FEMB receives signals from 40 *U* wires, 40 *V* wires, and 48 *X* wires. The baseline FEMB design contains eight 16-channel FE (LArASIC) ASICs, eight 16-channel Cold ADC ASICs, and two COLDATA control and communication ASICs (see Figure 3.3). The FEMB also contains regulators that produce the voltages required by the ASICs and filter those voltages. The LArASIC inputs are protected by diodes and a series inductor.

The ProtoDUNE-SP version of the FEMB (which uses a single field programmable gate array (FPGA) on a mezzanine card instead of two COLDATA ASICs) is shown in Figure 3.4.

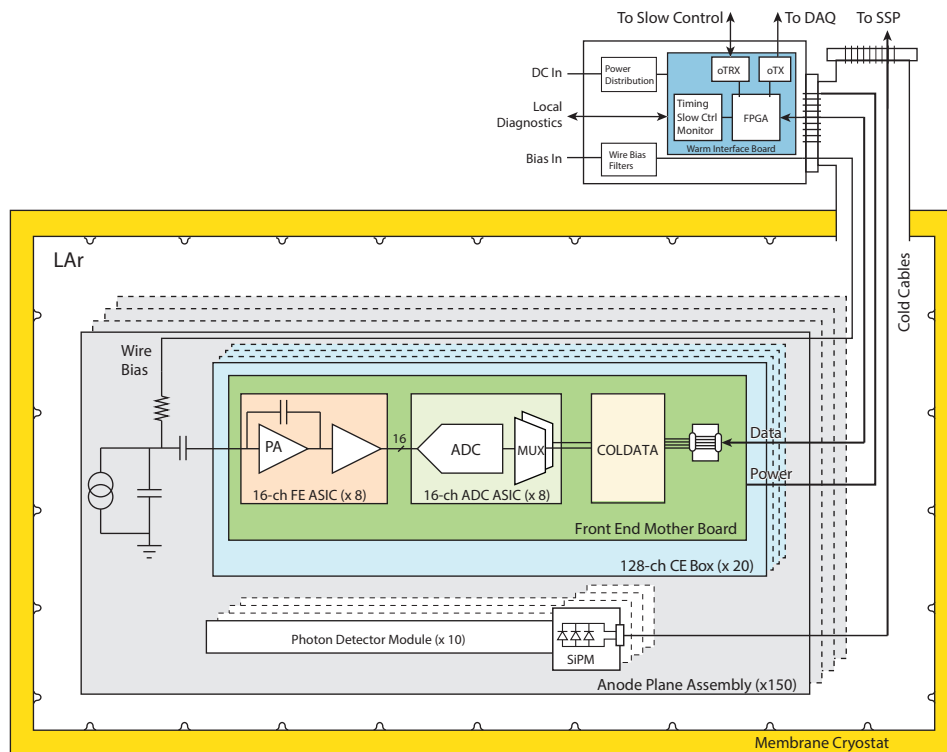


Figure 3.3: The baseline CE architecture. The basic unit is the 128-channel FEMB. Note that only one CE flange is shown to simplify the illustration. Note that SSP stands for *SiPM Signal Processor* (see Chapter 5).

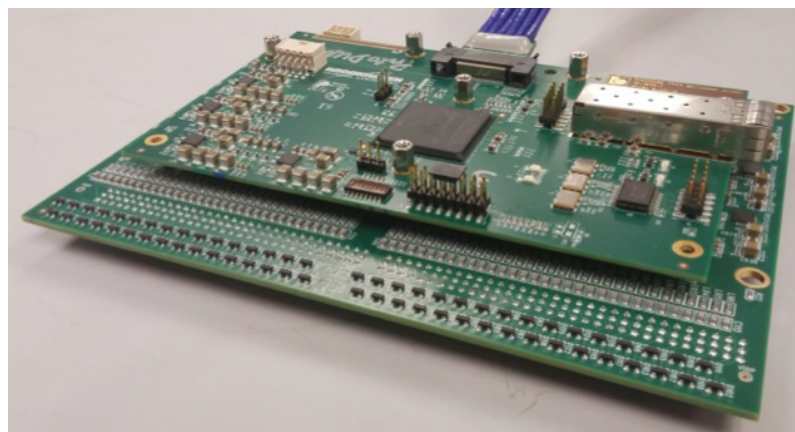


Figure 3.4: The complete FEMB assembly as used in the ProtoDUNE-SP detector. The cable shown is the high-speed data, clock, and control cable.

3.2.3.2 Front-End ASIC

The LArASIC receives signals from the CR board and provides a means to amplify and shape the current signals originally coming from the TPC wires; the shaping serves as an anti-aliasing filter for the TPC signals. Each LArASIC channel has a charge amplifier circuit with a programmable gain selectable from one of 4.7, 7.8, 14 or 25 mV/fC (corresponding to full-scale charge of 300, 180, 100 and 55 fC), a high-order anti-aliasing filter with programmable time constant (semi-Gaussian with peaking time 0.5, 1, 2, and 3 μ s), an option to enable AC coupling, and a baseline adjustment for operation with either the collecting (200 mV nominal) or the non-collecting (900 mV nominal) wires.

Figure 3.5 (left) shows the simulated pulse response for all gains and peaking times and both baselines. Note that the gain is independent of the peaking time; the same amount of charge produces the same peak voltage signal regardless of the peaking time.

Shared among the 16 channels in the LArASIC are the bias circuits, programming registers, a temperature monitor, an analog buffer for signal monitoring, and the digital interface. The power dissipation of LArASIC is about 6 mW per channel at 1.8 V supply voltage.

The LArASIC is implemented using the TSMC 180 nm CMOS process.¹ The charge sensitive amplifier uses a very large p-channel field effect transistor (PFET) with a width of 20 mm and a length of 270 nm followed by a dual cascode stage, a pulse shaping network, and a baseline restoration circuit.

Each channel also implements a high-performance output driver that can be used to drive a long cable, but which is disabled when interfaced to an ADC ASIC to reduce the power consumption. The ASIC integrates a band-gap reference (BGR) to generate all the internal bias voltages and currents. This guarantees a high stability of the operating point over a wide range of temperatures, including cryogenic temperatures. The ASIC is packaged in a commercial, fully encapsulated plastic QFP 80 package.

Each FE LArASIC channel is equipped with an injection capacitor which can be used for test and calibration and can be enabled or disabled through a dedicated register. The injection capacitance has been measured to 0.5% using a calibrated external capacitor. The measurements show that the calibration capacitance is extremely stable, changing from 184 fF at room temperature to 183 fF at 77 K. This result and the measured stability of the peaking time demonstrate the high stability of the passive components as a function of temperature. Channel-to-channel and chip-to-chip variation in the calibration capacitor are typically less than 1%.

Prototype LArASICs have been evaluated and characterized at room temperature and LN (77 K) temperature. During testing the circuits have been cycled multiple times between the two temperatures and operated without any change in performance. Figure 3.5 (right) shows the measured injection pulse response overlaid with the baseline subtracted for one full APA (2560) electronics channels from ProtoDUNE-SP FEMB attached to a ProtoDUNE-SP APA in a shielded environ-

¹TSMC 0.18-micron Technology™, Taiwan Semiconductor Manufacturing Company Ltd., <http://www.tsmc.com/english/dedicatedFoundry/technology/0.18um.htm>.

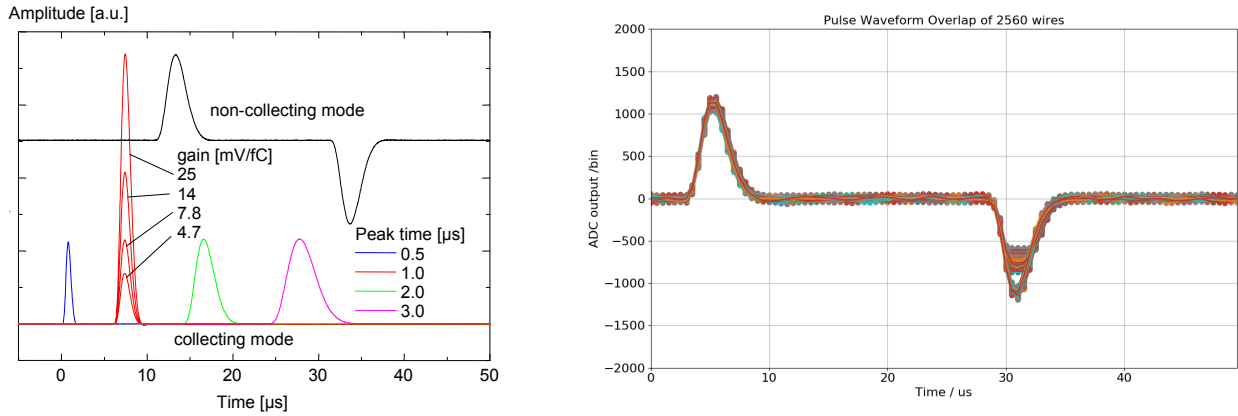


Figure 3.5: Simulated FE response to an instantaneous injected charge for all gains and peaking times and both baselines (left); also shown are measured calibration pulse response overlays for 2560 electronics channels (baseline subtracted) attached to a ProtoDUNE-SP APA (right). Note that the truncated negative pulses are due to effects of saturation associated with the collection plane threshold being close to the lower ADC boundary.

ment at approximately 180 K. This contains 1600 induction (high-baseline) and 960 collection (low-baseline) channels, the latter of which saturate the negative pulse at the low end of the FE output. The spread in saturation values between -500 and -750 ADC bins is due to the variation in relative position of the FE baseline to the low end of the FE output in the ProtoDUNE-SP version of the LArASIC.

3.2.3.3 Cold ADC

The baseline option for the DUNE cold ADC is a new 16-channel low-noise ADC ASIC intended to read out the LArASIC preamps in the SP module CE. The ADC is 12 bits and digitizes each channel at a rate of 2 MHz. The ADC accepts single-ended or differential inputs, and outputs a serial data stream to COLDATA, the SP module digital serializer chip. The ADC ASIC is implemented using 65 nm CMOS technology. The ASIC uses a conservative, industry standard design along with digital calibration. A block diagram of the ADC ASIC is shown in Figure 3.6. The design and testing of the baseline ADC ASIC is being carried out by a collaboration of scientists and engineers at BNL, Fermilab, and LBNL.

Each cold ADC receives 16 single-ended voltage outputs from a single LArASIC chip. The voltage is buffered and then sampled at a rate of 2 MHz. The analog samples are multiplexed by eight and digitized by calibrated 12 bit pipelined ADCs operating at 16 MHz. The ADC uses the well-known pipelined architecture with redundancy to reduce the impact of component non-idealities on the linearity of the ADC [4]. The linearity of the raw output samples from the ADCs is improved using an on-chip calibration. The corrected ADC output is then multiplexed onto eight LVDS channels and sent to COLDATA for further aggregation and transmission via a copper link to the warm

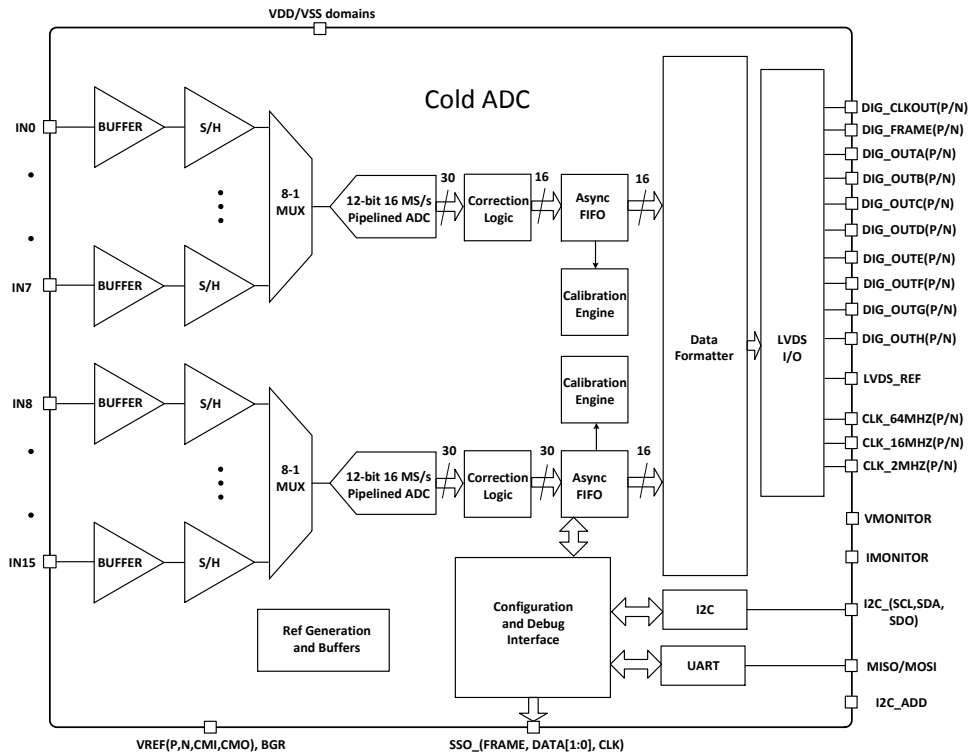


Figure 3.6: Baseline cold ADC ASIC block diagram.

electronics sitting outside the cryostat.

The ADC ASIC is designed for low-noise operation, with a noise specification of 175 μV RMS. This noise specification was chosen to ensure that LArASIC will dominate the overall noise performance of the channel.

The ADC is digitally calibrated using the proven Soenen-Karanicolas algorithm [5, 6]. The algorithm exploits the observation that in a pipelined ADC with redundancy, the ADC nonlinearity is caused almost entirely by errors in the closed-loop interstage gain [4]. Traditionally, the ADC output bits are assumed to be in radix two and are simply combined to generate the ADC output. However, due to unavoidable non-idealities such as finite op-amp gain and capacitor mismatch, the true radix of each stage is slightly different from two. The extent to which the true radix is different from two leads to DNL and INL in the ADC transfer characteristic. The Soenen-Karanicolas algorithm provides a way to measure the radix of a given stage by forcing events at the decision boundaries and using the following stages of the ADC to record the stage’s response. The radix is then decomposed into a set of weights and during normal operation the ADC output is converted from the true radix to radix two using pipelined digital adders. This way, static linearity can be greatly improved without any post-processing required. To provide additional ease-of-use, all calibration hardware (including test signal generation) is included on the ADC ASIC. To control power dissipation, the stages of the ADC are scaled in area to take advantage of the fact that the accuracy requirements of the stages decline down the pipeline [7].

To reduce the number of pads and to improve performance, all required reference voltages and

currents are generated internally by a resistor-programmed reference generator on the ASIC.

The cold ADC is highly configurable (see Table 3.2) and includes two redundant slow control interfaces for configuration (either UART or I2C). The configurability of the chip is included primarily to reduce risk by providing a high degree of flexibility and observability. First, many of the components on the ASIC can be bypassed and their functions assumed at the board level if desired. For example, the ADC reference voltages can be supplied externally and the input buffers can be bypassed. Second, the ADC digital calibration algorithm can be implemented externally with the calculated stage weights loaded back into the chip using the configuration interface. Third, various internal voltages and currents can be monitored and test data can be introduced at various parts of the digital processing to observe the function of the ASIC. Lastly, the bias point of the analog circuits in the ASIC can be adjusted to compensate for expected component variations between room temperature and LAr temperature.

Table 3.2: Baseline cold ADC ASIC configurability.

BLOCK	Configurability	Comment
Input Buffer	Single-ended/differential, bypass, bias current adjust	Reduces design risk
Sample-and-hold Amplifiers	Multiplexer freeze, bias current adjust	Simplifies evaluation of prototype
ADC	Bias currents, clock edge fine adjustment, sync and test modes	Simplifies evaluation of prototype and reduces risk
References	All reference voltages can be adjusted in 8 mV increments; all references can be powered down and external voltages used	Reduces design risk
Calibration	Number of stages and amount of digital filtering; all calibration commands can be implemented through configuration interface for offline calibration; known data can be injected at various points for testing	Simplifies evaluation of prototype and reduces risk
Output Monitor	Various internal bias voltages and currents can be sent off-chip for evaluation	Simplifies evaluation of prototype

3.2.3.4 COLDDATA ASIC

The COLDDATA ASIC is responsible for all communication between the CE on FEMBs and electronics located outside the cryostat. The COLDDATA ASIC is being designed by engineers from Fermilab and Southern Methodist University. Each FEMB contains two COLDDATA ASICs. COLDDATA receives command and control information; it provides clocks to the cold ADC ASICs and relays commands to the LArASIC front-end and to the cold ADC ASICs to set operating modes and initiate calibration procedures. COLDDATA receives data from the ADC ASICs, reformats these data, merges data streams, formats data packets, and sends these data packets to the warm electronics using 1.28 Gbps links. These links include line drivers with pulse pre-emphasis. All the components of COLDDATA, with the exception of the line drivers and of the interface to the ADC,

have been implemented in the CDP1 prototype ASIC and demonstrated to work as designed both at room temperature and at 77 K. A block diagram of COLDATA is shown in Figure 3.7.

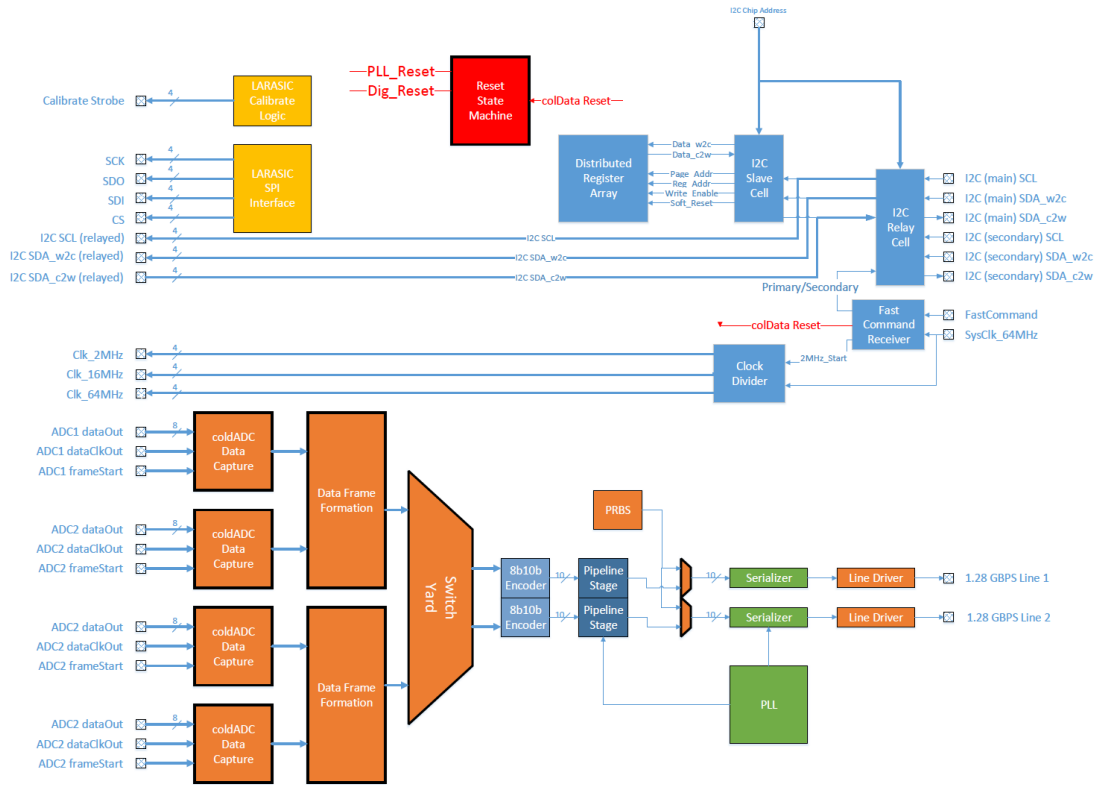


Figure 3.7: Block diagram of COLDATA ASIC design.

Both COLDATA and cold ADC are implemented in TSMC 65 nm CMOS² using cold transistor models produced by Logix Consulting³. Logix made measurements of Fermilab-supplied TSMC 65 nm transistors at a variety of temperatures (including room temperature and LN₂ temperature). They extracted and provided to Fermilab SPICE⁴ models as a function of temperature. A special library of standard cells, based on these SPICE models and using a minimum channel length of 90 nm, was developed by members of the University of Pennsylvania and Fermilab groups. This library was designed to eliminate the risk posed by the hot carrier effect. The digital sections of COLDATA and cold ADC use these standard cells and were synthesized from RTL (register-transfer level) using automatic place and route tools.

3.2.3.5 Cold Electronics Box

Each FEMB is enclosed in a mechanical CE box to provide support, cable strain relief, and control of gas argon bubbles in the LAr from the FEMB attached to the lower APA (which could in

²TSMC 65 Nanometer Technology™, Taiwan Semiconductor Manufacturing Company Ltd., <http://www.tsmc.com/english/dedicatedFoundry/technology/65nm.htm>.

³Logix Consulting™, <http://www.lgx.com/>

⁴SPICE™, is a general-purpose circuit simulation program for nonlinear DC, nonlinear transient, and linear AC analyses. <https://bwrccs.eecs.berkeley.edu/Courses/IcBook/SPICE/>.

principle lead to discharge of the HV system). The CE box, illustrated in Figure 3.8, is designed to make the electrical connection between the FEMB and the APA frame, as defined in Section 3.2.1. Mounting hardware inside the CE box connects the ground plane of the FEMB to the box casing. The box casing is electrically connected to the APA frame via twisted conducting wire (not shown in Figure 3.8). This is the only point of contact between the FEMB and APA, except for the input amplifier circuits connected to the CR board, which also terminate to ground at the APA frame, as shown in Figure 3.2.



Figure 3.8: Prototype CE box used in ProtoDUNE-SP.

3.2.4 Additional FEMB/ASIC Designs

In addition to the baseline FEMB and ASIC designs discussed in Section 3.2.3, two other FEMB and ASIC options are currently under consideration. There is one official alternative design, the SLAC nEXO three-chip *CRYO* ASIC, and one fallback option for the ADC ASIC, the Columbia University ATLAS-style ADC ASIC. These options are described in Section 3.2.4.1 and Section 3.2.4.2, respectively.

3.2.4.1 nEXO CRYO ASIC

The SLAC CRYO ASIC differs from the baseline three-chip design in that it combines the functions of an analog preamplifier, ADC, and data serialization and transmission for 64 wire channels, into a single chip. It is based on a design developed for the nEXO experiment⁵ and differs from it only in the design of the preamplifier, which is modified to account for the higher capacitance of the DUNE SP module wires compared to the small pads of nEXO. The FEMBs constructed using this chip would use only two ASICs, compared to the 18 (eight FE, eight ADC and two COLDATA) needed in the baseline design. This drastic reduction in part count may significantly improve FEMB reliability, reduce power, and reduce costs related to production and testing.

Figure 3.9 shows the overall architecture of the CRYO ASIC, which will be implemented in 130 nm CMOS. It comprises two identical, 32-channel blocks. The current signal from each wire is amplified

⁵Enriched Xenon Observatory, <https://www-project.slac.stanford.edu/exo/about.html>.

using a preamplifier with pole zero cancellation and an anti-alias fifth-order Bessel filter applied. Provisions are also made for injection of test pulses. Gain and peaking time are adjustable to values similar to those of the baseline design.

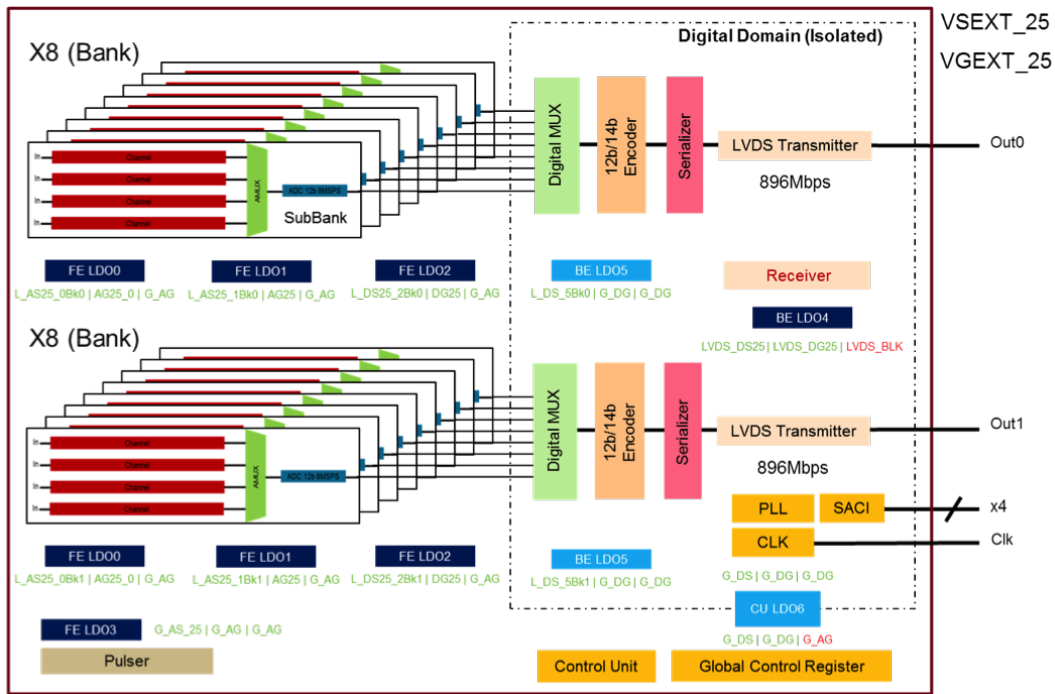


Figure 3.9: Overall architecture of the CRYO ASIC.

The ADC uses 8 MHz successive approximation registration (SAR), so that four input channels are multiplexed onto a single ADC. The data serialization and transmission block employs a custom 12b/14b encoder, so that 32 channels of 12-bit, 2 MHz data can be transmitted with a digital bandwidth of only 896 Mbps, which is significantly less than the required bandwidth of the baseline, which is 1.28 Gbps.

One key concern with mixed signal ASICs is the possibility of interference from the digital side causing noise on the very sensitive preamplifier. Fortunately, there are well established techniques for substrate isolation described in the literature [8], which have been successfully employed in previous ASICs produced by the SLAC group.

The infrastructure requirements for a CYRO ASIC-based system are similar to those of the baseline option. However, in most cases, somewhat fewer resources are needed:

- A single voltage is needed for the power supply. This is used to generate two supply voltages using internal voltage regulators.
- The output digital bandwidth on each of the four lines in an FEMB is 896 Mbps. This is lower than the baseline option due to the custom 12b/14b encoder of the CRYO chip.
- The warm interface is different. Only a single clock is needed (56 MHz) and the configuration protocol is the SLAC ASIC Control Interface (SACI) [9] rather than I2C.

The first prototype of the CRYO ASIC is in the final design and simulation stages. Simulation-based studies have already been performed; at $0.8\ \mu\text{s}$ peaking time and an input capacitance of $200\ \text{pF}$ (similar to that expected in the DUNE SP module), the ENC is approximately $500\ e^-$. This noise level is similar to that expected with the baseline FE and ADC ASIC design in LAr with the same input capacitance. Submission to the ASIC foundry is imminent and the first prototypes should be received by summer 2018. They will first be tested in an existing test stand at SLAC. Subsequent tests are planned for a small test TPC at Fermilab and on an APA in the ProtoDUNE-SP cold box; these test facilities are described in Section 3.5.2.

3.2.4.2 ATLAS ADC ASIC

An alternative ADC solution is to adapt the ADC chip under development for the ATLAS LAr calorimeter readout upgrade for the high luminosity LHC. The main ATLAS requirements are given in Table 3.3. Adapting the chip to the SP module needs would require doubling the number of channels per chip as well as adapting the output architecture. These are both relatively simple changes compared to the overall complexity of the chip.

Table 3.3: Performance requirements for the ATLAS-style ADC ASIC.

Parameter	Specification
Channels/chip	eight preferred, four minimum
Sampling Frequency	40 MHz
Dynamic Range	14 bits
Precision	11 ENOB
Power	< 100 mW/channel at 40 MHz
Input	2 V differential
Output	E-link interface operating at 640 Mbps

To achieve a 14 bit dynamic range, each analog channel is comprised of two main sections: a dynamic range enhancement (DRE) block that determines the most significant two bits of the 14 bit digital code, followed by a 12 bit SAR block. The input signal to the DRE block is sampled on two paths, one with unity gain and the other of gain four. A comparator determines which gain to use. The signal from the selected DRE gain is presented at the DRE output, which is connected to the input of the 12 bit SAR ADC block. The DRE design has been carefully optimized so that its output preserves the required 12 bit performance.

Following current state-of-the-art ADC development techniques, a two-stage SAR architecture is used, exploiting the high speed of the technology while maintaining the SAR input capacitance at a reasonable value. Since capacitor matching in this technology might not meet the precision required, the ADC will use bit redundancy, i.e., determine more bits than its actual output, and the redundant bits will be used to both calibrate the ADC and produce correct output codes. Such procedures are well understood and applied to both pipeline [10] and SAR [11] ADCs using foreground or background calibration techniques. Details of the SAR design are shown in Figure 3.10.

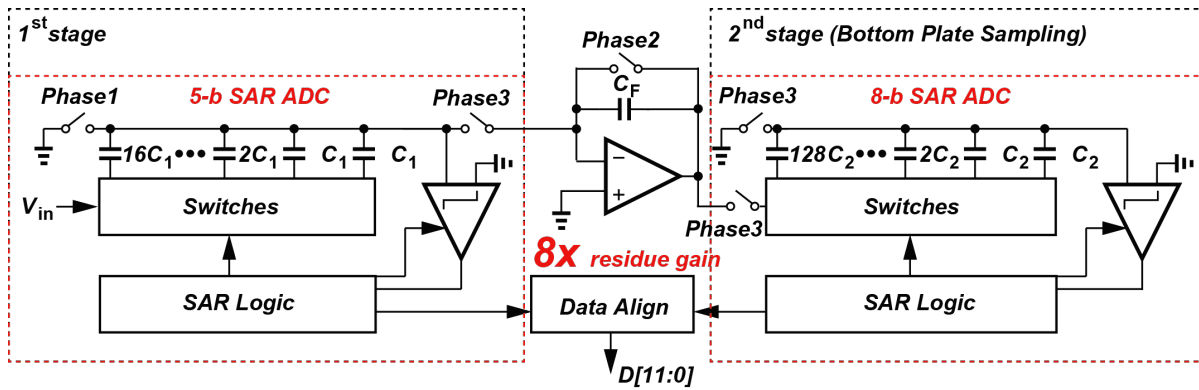


Figure 3.10: Block diagram depicting the two-stage SAR design of the ATLAS ADC ASIC.

An ADC test chip, dubbed COLUTA65V1, was designed and submitted for fabrication in May 2017 and received in September of 2017. The DRE and SAR blocks of the COLUTA65V1 were first tested independently. Measurements were made of the SAR precision using the sine-wave fast Fourier transform method. An effective number of bits (ENOB) of 11.6 bits at 20 MHz (after calibration) was obtained. Both DRE and SAR were successfully integrated with negligible degradation in performance. The COLUTA65V1 chip was also tested at 2 MHz and shown to work as designed, meeting the requirement for the SP module. Tests of an updated design in liquid nitrogen are planned for spring 2018. Additional tests associated with meeting power requirements will be carried out if this ADC option is further pursued.

3.2.5 Cold Electronics Feedthroughs and Cold Cables

All cold cables originating from inside the cryostat connect to the outside warm electronics through PCB board feedthroughs installed in the signal flanges that are distributed along the cryostat roof. The TPC data rate per APA, with an overall 32:321 MUX and eighty ~ 1 Gbps data channels per APA, is sufficiently low that the LVDS signals can be driven over copper twin-axial transmission lines. Additional transmission lines are available for the distribution of LVDS clock signals and I²C control information, which are transmitted at a lower bit rate. Optical fiber is employed externally from the WIBs on the signal flange to the data acquisition (DAQ) and slow control systems described in Chapter 6 and Chapter 7, respectively.

The design of the signal flange includes a four-way cross spool piece, separate PCB feedthroughs for the CE and PDS cables, and an attached crate for the TPC warm electronics, as shown in Figure 3.11. The wire bias voltage cables connect to standard SHV (safe high voltage) connectors machined directly into the CE feedthrough, ensuring no electrical connection between the wire bias voltages and other signals passing through the signal flange. Each CE feedthrough serves the bias, power, and digital I/O needs of one APA.

Data and control cable bundles are used to send system clock and control signals from the signal flange to the FEMB, stream the ~ 1 Gbps high-speed data from the FEMB to the signal flange. Each FEMB connects to a signal flange via one data cable bundle, leading to 20 bundles between one APA and one flange. Each data bundle contains 12 low-skew twin-axial cables with a drain

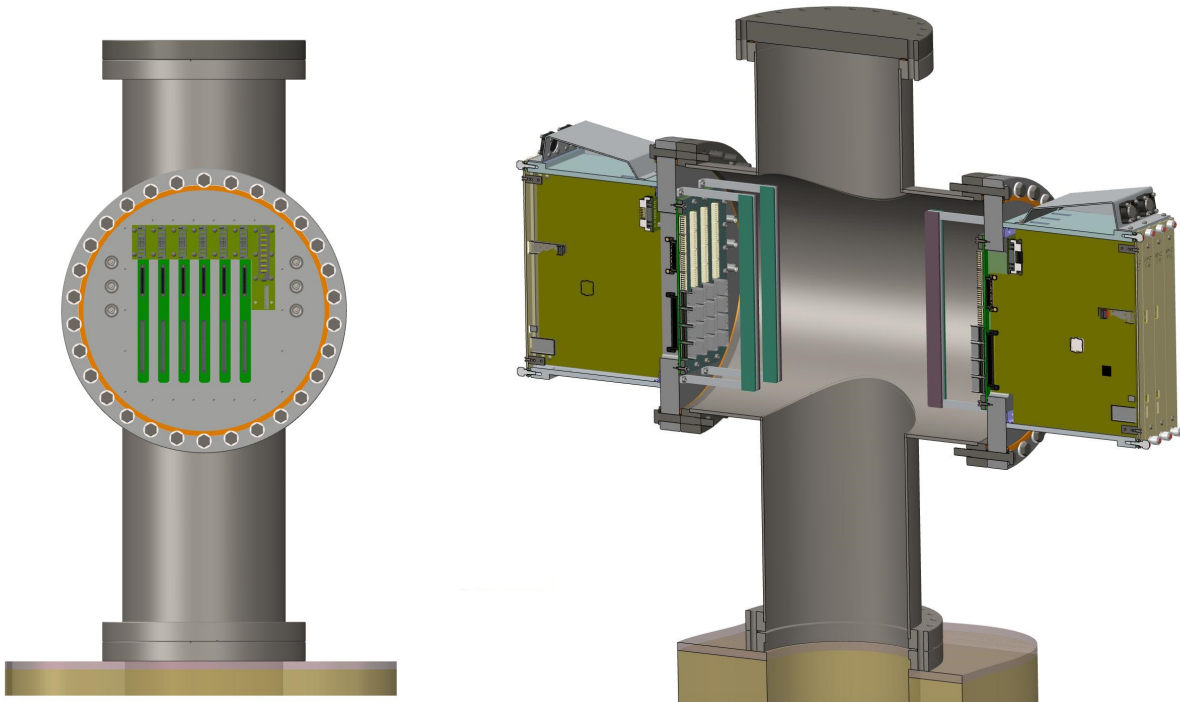


Figure 3.11: TPC CE feedthrough. The WIBs are seen edge-on in the left panel, and in an oblique side-view in the right panel, which also shows the warm crate for a SP module in a cutaway view.

wire, to transmit the following differential signals:

- four 1.28 Gbps data (two from each COLDATA);
- two 64 MHz clocks (one input to each COLDATA);
- two fast command lines (one input to each COLDATA);
- three I²C-like control lines (clock, data-in, and data-out); and
- one multipurpose LArASIC output (temperature, reference voltage, or analog test output).

The LV power is passed from the signal flange to the FEMB by bundles of 20AWG twisted-pair wires. Half of the wires are power feeds; the others are attached to the grounds of the input amplifier circuits, as described in Section 3.2.2. For a single FEMB, the resistance is measured to be $<30\text{ m}\Omega$ at room temperature or $<10\text{ m}\Omega$ at LAr temperature. Each APA has a copper cross section of approximately 80 mm^2 , with a resistance $<1.5\text{ m}\Omega$ at room temperature or $<0.5\text{ m}\Omega$ at LAr temperature.

The bias voltages are applied to the X -, U -, and G -plane wire layers, three field cage (FC) terminations, and an electron diverter, as shown in Figure 3.2. The voltages are supplied through eight SHV connectors mounted on the signal flange. RG-316 coaxial cables carry the voltages from the signal flange to a patch panel PCB which includes noise filtering mounted on the top end of the APA.

From there, wire bias voltages are carried by single wires to various points on the APA frame, including the CR boards, a small PCB mounted on or near the patch panel that houses a noise filter and termination circuits for the field cage voltages, and a small mounted board near the electron diverter that also houses wire bias voltage filters.

3.2.6 Warm Interface Electronics

The warm interface electronics provide an interface between the CE, DAQ, timing, and slow control systems, including local power control at the flange and a real-time diagnostic readout. They are housed in the WIECs attached directly to the CE flange. The WIEC shown in Figure 3.12 contains one power and timing card (PTC), five warm interface boards (WIBs) and a passive power and timing backplane (PTB), which fans out signals and LV power from the PTC to the WIBs. The WIEC must provide a Faraday-shielded housing, robust ground connections from the WIBs to the detector ground described in Section 3.2.1, and only optical fiber links to the DAQ and slow control in order to mitigate noise introduced at the CE feedthrough.

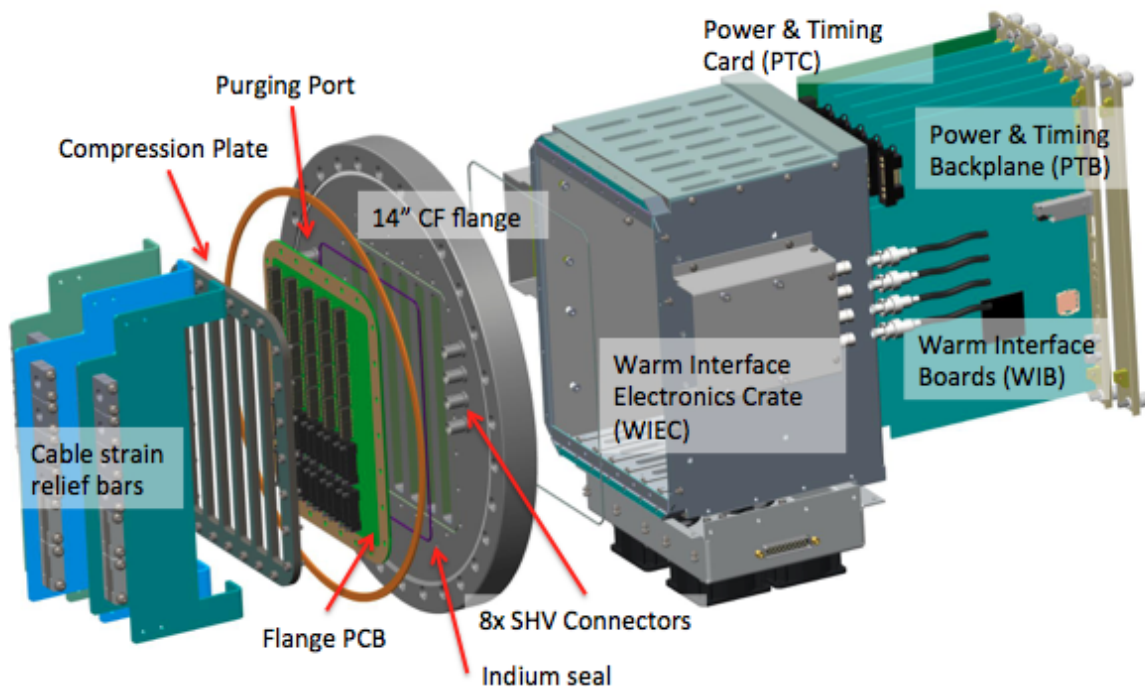


Figure 3.12: Exploded view of the CE signal flange for ProtoDUNE-SP. The design will be very similar for the SP module CE signal flange (with two CE signal flanges per feedthrough).

The WIB is the interface between the DAQ system and four FEMBs. It receives the system clock and control signals from the timing system and provides for processing and fan-out of those signals to the four FEMBs. The WIB also receives the high-speed data signals from the four FEMBs and transmits them to the DAQ system over optical fibers. The data signals are recovered onboard the WIB with commercial equalizers. The WIBs are attached directly to the TPC CE feedthrough on the signal flange. The feedthrough board is a PCB with connectors to the cold signal and LV power cables fitted between the compression plate on the cold side, and sockets for the WIB

on the warm side. Cable strain relief for the cold cables is supported from the back end of the feedthrough.

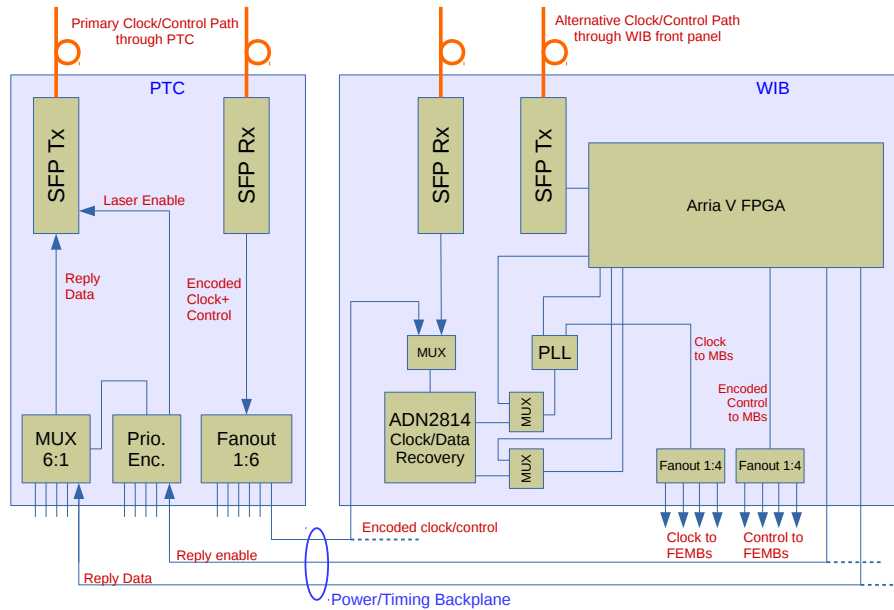


Figure 3.13: Power and timing card (PTC) and timing distribution to the WIB and FEMBs used in ProtoDUNE-SP.

The ProtoDUNE-SP PTC provides a bidirectional fiber interface to the timing system. The clock and data streams are separately fanned out to the five WIBs as shown in Figure 3.13. The PTC fans the clocks out to the WIB over the PTB, which is a passive backplane attached directly to the PTC and WIBs. The received clock on the WIB is separated into clock and data using a clock-data separator. Timing endpoint firmware to receive and transmit the clock is integrated in the WIB FPGA (the Altera Arria V⁶ was used for ProtoDUNE-SP). The SP module timing system, described in Section 6.2.6, is a development of the ProtoDUNE-SP system, and expected to require the nearly identical functionality at the WIB endpoint.

The PTC also receives 48 V LV power for all cold electronics connected through the TPC signal flange: one PTC, five WIB, and 20 FEMB. The LV power is then stepped down to 12 V via a DC-DC converter onboard the PTC. The output of the PTC converters is filtered with a common-mode choke and fanned out on the PTB to each WIB, which provides the necessary 12 V DC-DC conversions and fans the LV power out to each of the cold FEMBs supplied by that WIB, as shown in Figure 3.14. The output of the WIB converters is further filtered by a common-mode choke. The majority of the power drawn by a full flange is dissipated in the LAr by the cold FEMB.

As shown in Figure 3.15, the WIB is capable of receiving LV power in the front panel and distribut-

⁶Altera Arria™, V FPGA family, <https://www.altera.com/products/fpga/arrisa-series/arrisa-v/overview.html>.

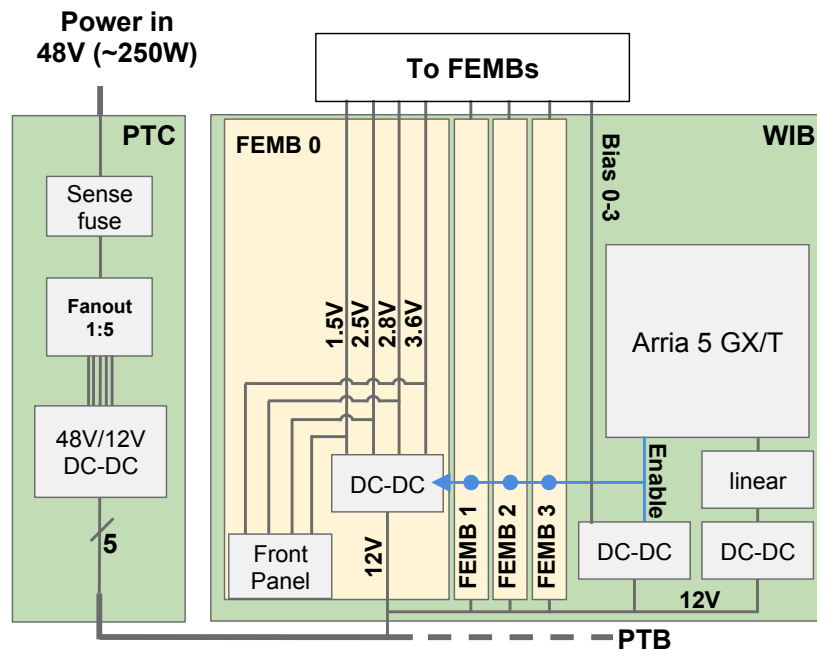


Figure 3.14: LV power distribution to the WIB and FEMBs implemented for ProtoDUNE-SP. This will be modified for the SP module to provide the required voltage or voltages depending on which ASICs are used on the FEMBs. In particular the voltages to the FEMB 0 to 3 will change as the ProtoDUNE-SP FPGA is replaced by COLDATA.

ing it directly to the FEMB, bypassing all DC/DC converters. It can also receive the encoded system timing signals over bi-directional optical fibers on the front panel, and process these using either the on-board FPGA or clock synthesizer chip to provide the clock required by the CE. The baseline ASIC design currently uses 8b/10b encoding; if the SLAC CRYO ASIC is selected for the DUNE SP module, 12b/14b encoding will be used instead of 8b/10b.

The FPGA on the ProtoDUNE-SP WIB is an Altera Arria V GT variant, which has transceivers that can drive the high-speed data to the DAQ system up to 10.3125 Gbps per link, implying that all data from two FEMB (2×5 Gbps) could be transmitted on a single link. The FPGA has an additional Gbps Ethernet transceiver I/O based on the 125 MHz clock, which provides real-time digital data readout to the slow control system.

3.2.7 External Power and Supplies

As implemented for ProtoDUNE-SP, a fully loaded WIB (one WIB plus four FEMBs) requires 12V and draws up to approximately 4 A. The full electronics for one APA (one PTC, five WIBs, and 20 FEMBs) requires 12V and draws approximately 20 A, for a total power of approximately 240 W, as described in Section 3.2.6. The SP module implementation should require much less power as the FPGA will be replaced by the COLDATA chips.

As the LV power is delivered at 48V to the PTC, each LV power mainframe is chosen to bracket

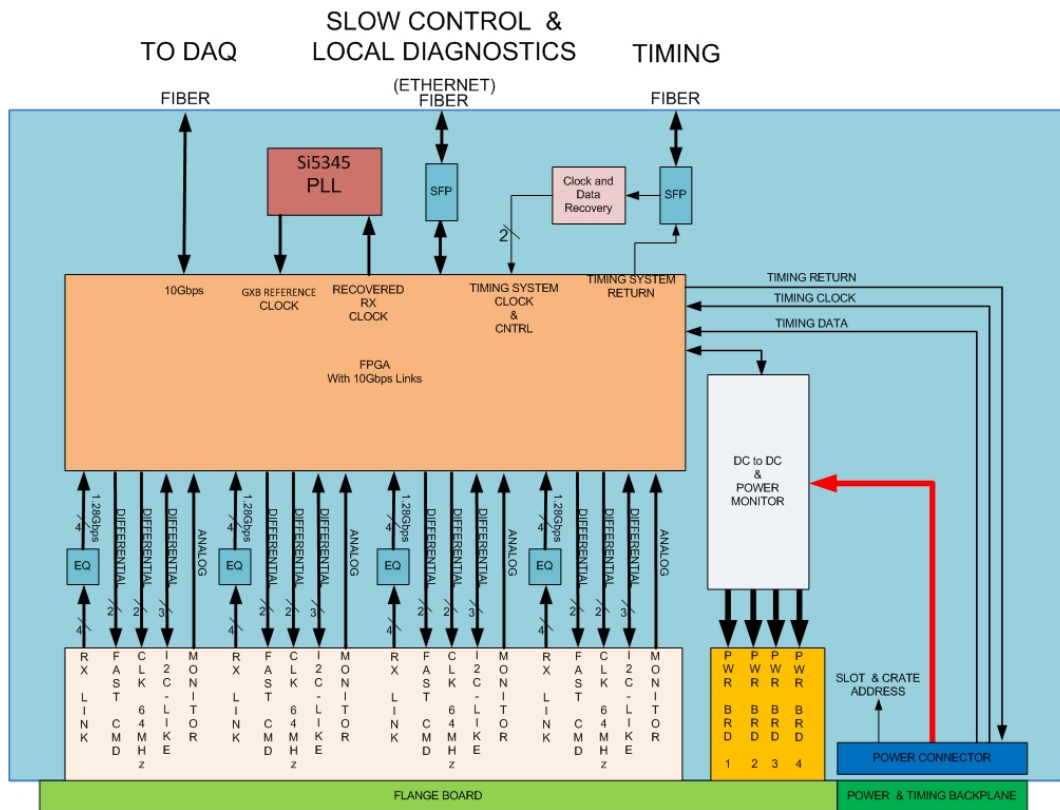


Figure 3.15: Warm interface board (WIB). Note that front panel inputs include a LEMO connector and alternate inputs for LV power and timing.

that value; each has roughly 30 to 60V, 13.5 A, 650 W maximum capacity per APA. Using 10AWG cable, a 0.8 V drop is expected along the cable with a required power of 306 W out of 650 W available. This leaves a significant margin that allows for larger distances between the power supplies and the warm interface crates than the 20 m in ProtoDUNE-SP.

Four wires are used for each module; two 10AWG, shielded, twisted-pair cables for the power and return; and two 20AWG, shielded, twisted-pair cables for the sense. The primary protection is the over-current protection circuit in the LV supply modules, which is set above the 20 A current draw of the WIEC. Secondary sense line fusing is provided on the PTC. The LV power cable uses FCI micro TCA⁷ connectors, shown in Figure 3.16.

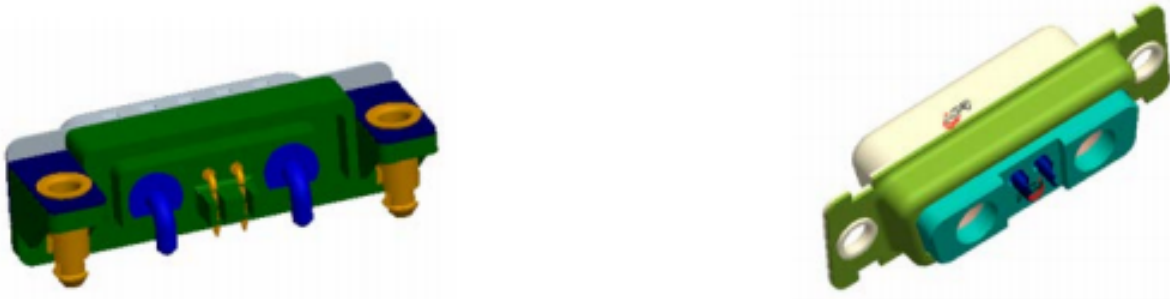


Figure 3.16: FCI microTCA power connector at the PTC end of the cable.

Bias voltages for the APA wire planes, the electron diverters, and the last FC electrodes are generated by supplies which are the responsibility of the TPC Electronics consortium. The current from each of these supplies is expected to be very close to zero in normal operation. However, the ripple voltage must be carefully controlled to avoid injecting noise into the front-end electronics. RG-58 coaxial cables connect the wire bias voltages from the mini-crate to the standard SHV connectors machined directly into the CE feedthrough, so there is no electrical connection between the LV power and data connectors and wire bias voltages.

Optical fibers are used for all connections between the WIECs, which act as Faraday-shielded boxes, and the DAQ and slow control systems. The WIB reports its onboard temperature and the current draw from each FEMB to the slow control system, while the current draw for each APA is monitored at the mainframe itself.

3.3 Production and Assembly

A single SP module requires 3000 FEMBs, 750 WIBs, and 50 PTCs. A total of 3300 FEMBs, 900 WIBs, and 60 PTCs will be built.

If the three-ASIC FEMB solution is chosen (the baseline option), then two ASIC production contracts will be required, one for LArASIC (180 nm CMOS) and one for the cold ADC and

⁷MicroTCA™ (Micro Telecommunications Computing Architecture (μ TCA)) vertical card-edge connectors, Amphenol ICC, <https://www.amphenol-icc.com/product-series/micro-tca-card-edge.html>.

COLDATA (65 nm CMOS). If the one-ASIC FEMB solution is chosen, only one ASIC production contract will be required.

In either case, all ASICs will be packaged in plastic quad flat-pack (PQFP) or thin quad flat-pack (TQFP) surface mount packages. No wafer probing will be done before the chips are packaged. Rather, the wafers will be diced and all chips located more than ~ 10 mm from the outside of the wafer will be selected for packaging. The packaged parts will be tested by DUNE collaborators (see Section 3.6) before being assembled onto printed circuit boards.

All printed circuit boards will be fabricated and tested by qualified vendors. Circuit boards will also be assembled by qualified vendors. The completed boards will be acceptance tested by DUNE collaborators promptly after assembly.

All cable assemblies (including terminations) will be fabricated and tested by qualified vendors. At least a fraction of the cable assemblies will be retested by DUNE collaborators promptly after purchase.

3.4 Interfaces

3.4.1 Overview

Some of the components designed and built by the CE consortium are mounted on or need to work together with detector components provided by other DUNE consortia. Interface documents have been developed to ensure that the boundaries between systems are fully understood and that no detector components are missed or not properly defined when organizing the detector construction project into consortia. These interface documents are a work-in-progress. With time they will evolve into a very detailed definition of mechanical and electrical interfaces, including in some cases the description of data transmission protocols. These interface documents include a list of the responsibilities of each consortium during the R&D, design, and prototyping phases, and discuss all of the procedures to be followed during the integration of detector components and the following testing and commissioning process. In some cases multiple consortia (APA, PDS, HV, cryogenic instrumentation and slow controls (CISC), and DAQ) can be involved, depending on the complexity and maturity of the test setup.

The most important interfaces for the CE consortium are with the APA and DAQ consortia, followed by those with PDS, HV, and CISC. One of the most important aspects of all these interfaces is the enforcement of appropriate grounding rules and of the physical separation between electrical circuits to minimize the noise and crosstalk between different detector components. Different anode plane assemblies should be electrically insulated, and the same should apply for the PDS and the CE readout of the anode plane assemblies. The flanges on the feedthroughs are used to provide, separately for the two anode plane assemblies and for the PDS, the reference voltage for all the detector elements. The flanges are electrically connected to the cryostat structure that acts as the detector ground. The same approach has to be implemented for the CISC instrumentation

in the LAr.

The two most complex interfaces to the TPC electronics subsystem, the interfaces to the anode plane assemblies and DAQ, are discussed below.

3.4.2 APAs

The CE consortium provides all of the electronics used for reading out the charge collection and induction signals produced on the APA wires by particles that ionize the LAr. The APA consortium is responsible for all of the printed circuit boards mounted on the APA frame holding the anode wires. These boards provide filtering of the wire bias voltages, connection of the bias voltages to the wires and AC or direct coupling of the wire signals to the FEMBs built by the CE consortium. The cold boxes containing the FEMBs are also mounted on the anode plane assemblies and are connected electrically to the CR boards. The CE consortium is responsible for providing the bias voltage to the anode plane assemblies, and also the bias voltage for the electron diverters and the FE termination electrodes (these last two items are part of the interface with the HV consortium).

A crucial aspect of the interface between the CE and APA consortia is the choice of routing for the cables that provide power, control, and readout for the bottom APA. Studies are ongoing to understand whether it is feasible to route these cables inside the APA frames of the two stacked anode plane assemblies, and whether it is necessary to modify the size of the APA frame in order to achieve this goal. Mockups of the APA frames will be used for routing tests together with ProtoDUNE-SP cables, under the assumption that there will be minimal changes in the cross section of cables between ProtoDUNE-SP and DUNE (we expect to be able to remove one of the seven pairs of power lines used in ProtoDUNE-SP, when the FPGA on the FEMB is replaced by the COLDATA ASIC). Before spring 2019 we expect to perform a realistic test of the cable insertion in a pair of stacked anode plane assemblies using mechanical prototypes (i.e., without wires) of the APA. We are also investigating the possibility of routing the cables for the bottom APA outside the field cage, which increases significantly the length of the cables for the central APA; this also complicates the installation procedure and the engineering of the support structures inside the cryostat.

3.4.3 DAQ

There are two components in the definition of the interface between the CE and DAQ consortia. The first one is a decision on whether to implement any firmware and buffering related to the trigger decision inside the WIB, or instead transmit the data as they are produced from the FEMBs, possibly with some serialization taking place in the WIB. For the SP module we have chosen to adopt the latter option, which minimizes the requirements on the FPGA inside the WIB, and also reduces the power and cooling requirements for the WIEC. Based on this decision, the interface between the CE and DAQ consortia is defined by the fiber plant used to transmit the data from the WIBs to the DAQ components housed in the central utility cavern (CUC), and to broadcast the clock and controls in the opposite direction. Only optical links are used in the

connection with the DAQ, which guarantees that the DAQ electronics will not induce any noise on the APA wires.

The interface is fully defined with the selection of the number and type of optical fiber links, their speed, and the type of connectors. The FPGA inside the WIB can be used to reformat the data with changes to the headers and trailers that include time stamps and geographical addresses of the FEMBs. It can also be used to serialize the data from multiple COLDATA ASICs into a single stream. In the simplest scheme each electrical link from the FEMB is routed to a single optical fiber, transmitting data at 1.28 Gbps. Depending on the availability and cost of transmitters capable of sending data at higher speeds data from multiple electrical links (four, eight, or more) could be serialized onto a single link. Using higher transmission speeds reduces the number of links that are needed, possibly reducing the cost of the DAQ part of the detector. The use of links with speeds of 5 Gbps or larger may present the drawback that the data has to be deserialized on the CUC side, depending on the availability of resources for the extraction of trigger primitives on the DAQ boards. The final choice of the number of fibers, link speed, and matching between FEMBs and DAQ processing units in the CUC should be the result of a cost optimization process that can be delayed until the technical design report (TDR).

Another aspect of the interface between the DAQ and the CE consortia is the transmission of clock and command signals. In ProtoDUNE-SP, a single fiber carries this information to the PTC card at each CE flange, which then re-broadcasts the information to the five WIBs, using the WIEC backplane. For the SP module, we foresee the possibility of transmitting the information directly to each WIB, the functionality for which is already implemented in the ProtoDUNE-SP WIB, as shown in Figure 3.13.

The final aspect of the interface between the DAQ and the CE is the definition of the format of the data transmitted by the CE to the DAQ. This format has been defined previously for ProtoDUNE-SP. Some changes are needed for DUNE to accommodate a larger number of anode plane assemblies.

3.5 Quality Assurance

3.5.1 Initial Design Validation

The quality assurance (QA) program for the DUNE SP module electronics has been ongoing for several years. The QA program started with the appropriate design choices for operation in LAr, including the measurement of transistor properties, and later continued with tests of all of the cold components, cables, feedthrough and flange mechanicals, and warm electronics for suitability with respect to the SP module requirements. The current focus of the QA program is the instrumenting of the ProtoDUNE-SP detector with 120 FEMB (960 of each of the current FE and ADC ASIC designs) and six full APA readout chains as described in Section 3.2. There are aspects of the DUNE design that are not going to be fully validated in the 2018 ProtoDUNE-SP data taking and that will require additional confirmation. Some aspects of the detector, e.g., the use of stacked anode

plane assemblies with long cables routed possibly through the APA frames, and the integration and installation procedure, will have to be demonstrated in independent tests. The ASICs and FEMBs used for the SP module will be an evolution of the current ProtoDUNE-SP ones. Below we focus mostly on the electronics and on system tests to demonstrate that the final design meets the SP module specifications, but plans are being made to test all the detector components and their assembly and installation prior to the submission of the TDR.

The existing LArASIC design will be revised from the ProtoDUNE-SP version. Several issues, including pedestal uniformity and baseline restoration in the existing LArASIC, have been addressed by BNL in a spring 2018 submission. The new design will be tested at BNL and other sites to verify that the issues have been resolved. All new ASIC designs, including the new cold ADC, COLDATA, and CRYO will be tested first at the component level, both at room temperature and at LAr (or LN₂) temperature. The next step will be to modify the FEMB to accommodate the new ASICs. Tests of the new FEMBs (at least two versions) will be followed by small-scale system tests as described below, and plans are being made to test three full-scale anode plane assemblies with the final ASIC(s) and FEMBs in a second run in the ProtoDUNE-SP cryostat. The cold data and LV cables used in ProtoDUNE-SP have been selected to be candidates for the SP module baseline design, and tests are in progress to demonstrate that they can successfully transmit the high-speed data over the longest possible cable length in the SP module. It should be noted that the current schedule for the SP module construction, which is discussed in Section 3.9.4, foresees the possibility of two more iterations in the design of the ASICs and the FEMBs, including the time for performing system tests.

The updates to the SP module cryostat penetrations and spool pieces, as well as the warm interface electronics, are expected to be small iterations on the already existing system for ProtoDUNE-SP. Prototypes will be ordered in small batches and tested at the responsible institutions for the different components. After individual testing, integrated system tests including other SP module components will be critical to validate that the performance of the CE meets the DUNE far detector (FD) requirements. Issues identified in the integrated system tests will be fed back into the design requirements of the individual components.

3.5.2 Integrated Test Facilities

DUNE will plan for system tests of the baseline and alternative option in both the CERN cold box and a small test TPC at Fermilab. The cold box tests establish performance of the electronics coupled to a full-scale APA in a correctly grounded environment, but in a gaseous environment no colder than 150 K, and without TPC drift or HV. The small test TPC will provide tests in an operational LArTPC but at much smaller scale, with quick turn around (two to four weeks) for changing components and refilling. The 40% APA at BNL employs liquid nitrogen instead of LAr, does not integrate the CE with the PDS, and has no TPC drift. However, it allows for quick turn-around and is located very close to where the development is happening (BNL and Fermilab), and is thus invaluable for initial board and component testing.

Generic board and component testing often includes measurement of (1) the baseline noise level and frequency spectrum, (2) the response to the calibration input signal provided on the FEMB, and

(3) the response to cosmic rays in a TPC. Measurements are often done at both room temperature and liquid nitrogen or argon temperature in three configurations: nothing attached to the inputs, dummy capacitive load attached to the inputs, and an APA attached to the inputs as the capacitive coupling of long wires is subtly different than a dummy capacitor with the equivalent capacitance of a single wire. Measurements specific to the characterization of the ADC performance, such as integral nonlinearity (INL) and differential nonlinearity (DNL) determination, are done before the ADC is mounted on the FEMB.

3.5.2.1 Cold Box at CERN

A cold box at CERN used in electronics tests for ProtoDUNE-SP is available for electronics testing in cold nitrogen gas. The cold box is designed to cycle one full-size APA with the full set of 20 FEMB through gaseous nitrogen temperatures around 150 K to check out the APA performance prior to installing the APA into the ProtoDUNE-SP cryostat. It is designed to be a Faraday cage, using the same grounding and shielding scheme that is implemented for the ProtoDUNE-SP cryostat. It is read out by a complete CE system for a single APA, including a CE flange and fully-loaded WIEC with five WIBs and one PTC.

Preliminary results from the ProtoDUNE-SP cold box indicate that the noise performance of the TPC readout will satisfy the DUNE FD noise requirements of $\text{ENC} < 1000 e^-$ on SP module-length wires. These measurements suggest that the noise level in LAr would be around $500 e^-$ and $600 e^-$ for the collection and induction plane channels, respectively; this is well below the requirement. The ENC and temperature of the second ProtoDUNE-SP APA delivered to CERN in the cold box are shown in Figure 3.17.

3.5.2.2 ProtoDUNE-SP

ProtoDUNE-SP is intended to be a full slice of the SP module as close as possible to the final DUNE SP design. It contains six full-size anode plane assemblies instrumented with 20 FEMBs each for a total readout channel count of 15,360 digitized sense wires. Critically, the CE on each APA is read out via a full CE readout system, including a CE flange and WIEC with five WIBs and one PTC. Each APA also has a full PD readout system installed. Five of the six ProtoDUNE-SP anode plane assemblies have been validated in the cold box at CERN, and then installed in the ProtoDUNE-SP cryostat, while the last APA was installed after passing only room temperature tests. Any issues that are discovered either during the cold box tests or the ProtoDUNE-SP commissioning and data-taking will be incorporated into the next iteration of the system design for the SP module.

In addition to the tests described in Section 3.5.2.1, tests have also been done on the ProtoDUNE-SP APA to check for any additional noise introduced on the TPC wire readout by operating the PDS or enabling the wire bias HV system. So far, no significant increase in the noise on the APA wire readout has been observed when operating these other systems.

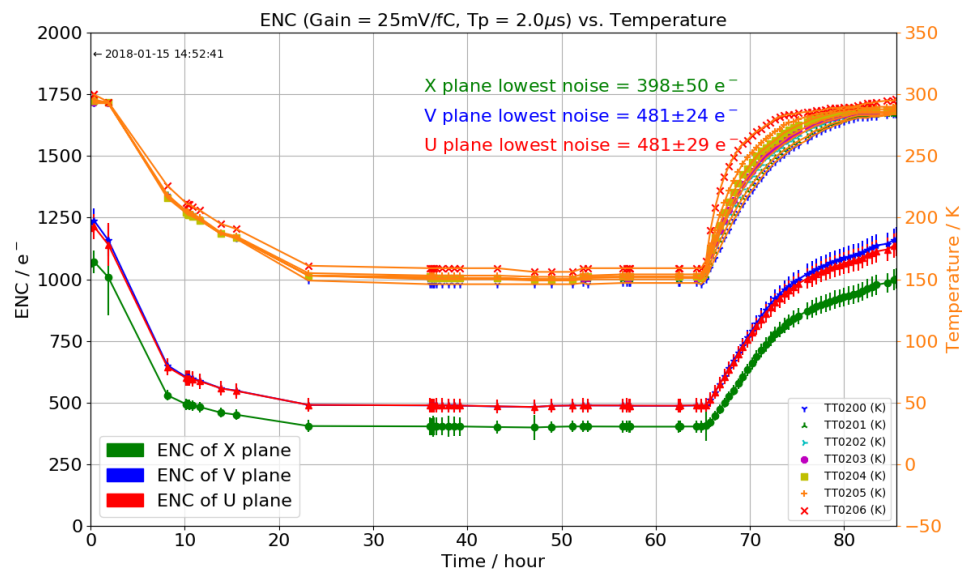


Figure 3.17: ENC in electrons (left axis) for the wrapped induction wires (red and blue curves) and straight collection wires (green curve) as well as the temperature in degrees Kelvin (right axis) for the temperature sensors in the CERN cold box (orange curves) as a function of cold cycle time in gaseous nitrogen for ProtoDUNE-SP APA2. At the lowest temperature of 160 K, the wrapped wires measured $480e^-$ noise and the straight wires $400e^-$. This noise level is consistent with all other ProtoDUNE-SP anode plane assemblies tested in the cold box.

The anode plane assemblies and the readout electronics will be different from the ones used in ProtoDUNE-SP; for this reason, plans are being made for re-opening the ProtoDUNE-SP cryostat and replacing three of the six anode plane assemblies with final DUNE prototypes that will also include the final versions of the ASICs and FEMBs. A second period of data-taking with this new configuration of ProtoDUNE-SP is being planned for 2021-2022. This will also allow for another opportunity to check for interference between the readout of the APA wires and the PDS.

3.5.2.3 Small Test TPC at Fermilab

A small test TPC is essential to qualify the different prototype ASICs, offering quick turn around for changing components and refilling; this allows one to study the response of the electronics to signals from cosmic-ray muons. A new reduced-size APA will be constructed with many similarities to the DUNE APA design. The APA will be half the width of a DUNE APA (along the beam direction) or 1.3 m, with half the number of readout channels. This amounts to 10 FEMBs with a total of 1280 channels. The height will be significantly reduced from the DUNE APA height of 6 m to about 1.25 m, and the wire lengths will be reduced by the same factor. The ProtoDUNE-SP CR boards will be used, and the APA will accommodate a single half-length PD. The TPC will have the APA in the center and a cathode on either end, creating two drift volumes with drift distance 0.3 m each. The TPC will be installed in the cryostat with the wire planes parallel to the floor to optimize the orientation of the cosmic ray tracks. It will be instrumented with a full readout chain of ProtoDUNE-SP electronics, specifically the cables, feedthrough flange, WIB, PTC, and warm interface crate. Initially, ProtoDUNE-SP FEMBs will be used for commissioning, and later FEMBs with prototype ASICs will be swapped in.

The TPC electronics and photodetector will be read out through a slice of the ProtoDUNE-SP DAQ. This system will provide a low-noise environment that will allow one to make detailed comparisons of the performance of the new ASICs. It will also enable the study of interactions between the TPC readout and other systems, including the PD readout and the HV distribution, to exclude the possibility that one system generates noise on another one when both are being operated.

The APA will be housed in a new LAr cryostat at Fermilab located in the Proton Assembly Building that complies with the DUNE grounding and shielding requirements, and connected to an existing recirculation system for argon purification. The cryostat will be a vertical cylinder, with an inner depth of 185 cm and an inner diameter of 150 cm. With the cryogenic connections on the upper portion of the cylinder, the flat top plate will have penetrations dedicated to readout and cryogenic instrumentation. The target date for the fabrication of new FE motherboards is fall of 2018, and these will house the latest version of the FE ASIC, the first prototype of COLDATA, and various ADC prototypes (including the SLAC CRYO ASIC). The new APA and the new cryostat will be completed on the same timescale so that tests in both the ProtoDUNE-SP cold box at CERN and the test TPC at Fermilab can be completed and analyzed prior to the submission of the TDR.

3.5.2.4 Additional Test Facilities

For CE development, testing prototypes at room temperature is the first step, as many problems can be identified quickly and without the expense of cryogenics. A quick access test stand with the FEMB connected to an APA inside a shielded environment that is in the same location as the FEMB and ASIC development is invaluable for rapid progress. Two such facilities are available to DUNE: the shielded room at Fermilab and the 40% APA test stand at BNL. In addition, a test dewar design developed by Michigan State University, referred to as the Cryogenic Test System (CTS), allows for additional testing of the FEMBs and ASICs in LN₂.

The shielded room at Fermilab (see Figure 3.18) is 2.5 m tall, and 2 m on each side, with a double layer of copper mesh in the walls, floor and ceiling, plus a solid metal plate in the floor all electrically connected to create a Faraday cage. A flexible AC distribution and isolated grounding configuration offers the ability to easily ground the shielded room and refer the associated electronics to either a building ground or a detector ground. In addition to evaluating different grounding schemes for the anode plane assemblies, capacitive coupling issues can be studied by varying the distance between the floor and a copper plate positioned underneath. This room has uniquely easy access to the setup through a shielded door, and a person can remain inside safely with the door closed and probe the electronics directly while operating in a shielded environment. Currently mounted inside are two anode plane assemblies from the 35 ton prototype with adapter boards to connect ProtoDUNE-SP electronics. This installation satisfies the ProtoDUNE-SP grounding and shielding guidelines. A rough demonstration of the shielding adequacy for our purposes is the measured noise level of 800 ENC for ProtoDUNE-SP prototype FEMBs. The same noise level was measured at room temperature in the 40% APA at BNL for the same FEMBs.



Figure 3.18: Picture of the shielded room at Fermilab.

The 40% APA at BNL is a 2.8 m × 1.0 m three-plane APA with two layers of 576 wrapped (*U* and

V) wires and one layer of 448 straight (X) wires. It is read out by eight ProtoDUNE-SP FEMBs with the full 7 m ProtoDUNE-SP length data and LV power cables, four on the top and four on the bottom. The readout uses the full CE system for ProtoDUNE-SP, with a prototype CE flange and WIEC, two WIBs and one PTC, as shown in Figure 3.19. Detailed integration tests of the CE readout performance while following the DUNE grounding and shielding guidelines have been done at the 40% APA. Additional input capacitance (equivalent to longer wire length) have been added to a subset of channels to project the ENC performance from the 40% APA teststand to the ProtoDUNE-SP and SBND detectors. The results from the 40% APA indicate that, if the new ADC performs as expected, the full CE system as installed on the test stand at BNL will have a noise level in LAr around $500 e^-$ and $600 e^-$ for the collection and induction plane channels, respectively, in line with the CERN cold box tests described in Section 3.5.2.1.



Figure 3.19: Left: one side of the 40% APA with four FEMBs. Right: the full CE feedthrough and flange.

To facilitate testing of individual components and printed circuit boards, members of the Michigan State group have developed the CTS (see Figure 3.20). This system allows a device under test to be cooled down in nitrogen gas, immersed in LN_2 for testing, and then warmed back to room temperature in a nitrogen gas. This process avoids the condensation of water from air that can otherwise interfere with the tests or damage the test equipment. A total of nine CTSs will be built and used at consortium member institutions.

3.6 Quality Control

Once there is a final design that clearly satisfies the requirements and constraints, given all of the testing at the device and system level described above, it will be necessary to put in place procedures and controls to ensure that the production CE parts will continue to fully satisfy the requirements and constraints. This set of quality control (QC) procedures, based on the experience gained with ProtoDUNE-SP, can only be sketched at this point without yet knowing, for instance, yield statistics on the final ASICs. Nevertheless, it is possible to put forward a general plan based upon long-established good practice.

All of the custom ASICs will be packaged by a commercial vendor. All custom printed circuit



Figure 3.20: Cryogenic Test System: an insulated box is mounted on top of a commercial LN₂ dewar. Simple controls allow the box to be purged with nitrogen gas and LN₂ to be moved from the dewar to the box and back to the dewar.

boards will be produced by qualified vendors to at least IPC class 2⁸ standards; the same standard will apply to all commercial assembly of those boards. All commercial parts will be procured from known, reliable vendors and manufacturers and qualified for use at LN temperatures. Depending upon the actual yield of the custom packaged chips it may or may not be necessary to individually test those chips prior to assembly onto printed circuits, and the use of an automated cryogenic test station is being considered. In any event, all custom printed circuits delivered by the assembler will be run through a full functional test sequence at a DUNE institution and then subjected to a powered burn-in period of one or more weeks at elevated temperature followed by a second functional test sequence. Depending upon experience with pre-production assemblies, this burn-in may also include a temperature cycling step. All cables will be fully tested for continuity and lack of shorts either by the assembler or at a DUNE institution prior to installation. Cable testing may also include impedance and electrical length verification. All discrete CE parts will be serial-numbered and a production database will record the specifics for each part and each test sequence.

However, as much of the SP module TPC electronics will operate in a cryogenic environment, which differs from typical commercial experience, it will be necessary to add additional cryogenic testing steps to the above list for all of the ASICs and circuit boards that will be subject to those cryogenic conditions. Based upon current experience, the expectation is that repeating the functional test sequence with the board under test immersed in LN₂ should be sufficient. It may be useful to subject a small sample of such boards to the stress of multiple cycles between room

⁸ "Acceptability of Printed Boards", IPC(R), IPCA-600F, Association Connecting Electronics Industries™, <http://www.ipc.org>.

and LN₂ temperatures; this will allow one to understand how much margin is available against failure due to stress caused by thermal cycling for each production batch.

Handling of CE components at DUNE institutions must follow standard IPC class 2 good practice for cleanliness, electrostatic discharge protection, and environmental conditions. Boards, cables, and other CE components must be stored in qualified storage facilities and all shipments of boards and other components will be in qualified shipping containers and shipped via qualified shippers.

3.7 Installation, Integration, and Commissioning

3.7.1 Installation and Integration with APAs

The installation and commissioning of the detector components built or purchased by the CE consortium takes place both prior to and after the insertion of the anode plane assemblies in the detector cryostat, with testing performed after each step, to avoid the need for rework that could cause significant delays. The installation and initial commissioning of the CE electronics is likely to be on the critical path for the completion of the SP module and the amount of time available for testing and possibly repairing or replacing components after their installation is going to be very limited. Cold tests of the complete anode plane assemblies for the entire detector require the availability of at least two independent cold boxes at the integration facility. To reduce the number of failures in these tests, all CE components will be qualified for operation in LAr prior to their installation.

After the completion of the cryostat, the spool pieces that house all of the cables for the CE, PDS, and HV consortia (with the exception of the high-voltage feedthrough for the cathode planes) are installed and leak tested. This includes the installation of the crossing tube cable support and of the flanges that provide the cold-to-warm interface for all of the cables. In parallel, the racks that house the CE and PDS electronics components on the top of the cryostat and the corresponding CISC and detector safety system monitoring, controlling, and interlock hardware can be installed. Cable trays between different spool pieces belonging to a set of six anode plane assemblies and two cathode plane assemblies (CPAs) can also be put in place. Readout fiber bundles between the spool pieces and the central utility cavern used for the readout of the wire information from the anode plane assemblies can also be put in place. In the meantime, inside the cryostat, all of the cable trays used to support the CE and PDS cables, and to accommodate the slack of the cables, can be put in place.

In parallel, the 20 FEMBs required to read out the wires from one APA are installed with their shielding box onto the APA and connected to the CR boards. This work will be performed at the integration facility (or facilities), because there will not be enough space to perform this type of work in parallel on multiple anode plane assemblies in the detector cavern. Once the FEMBs are installed, a temporary set of cables will be used to connect each FEMB to a temporary power, control, and readout system to ensure that all the wires can be properly read out. All anode plane assemblies will then be inserted into a cold box similar to the one used at CERN for ProtoDUNE-

SP and tested at a temperature of ~ 150 K. Once these tests are completed, the temporary cables are disconnected and the APA is prepared for shipment to SURF. It is not considered feasible to transport the top APA from the integration facility to the detector cryostat with the CE cables already installed. For the bottom APA the final cables can be installed only after the two anode plane assemblies are joined together in the so-called *toaster* area just outside of the detector cryostat.

Further work on the CE components installed on the anode plane assemblies is performed after the anode plane assemblies are transported to the clean area outside the cryostat at SURF. All of the cables that provide power and control and are used to read out the 20 FEMBs associated with the top and bottom anode plane assemblies need to be installed; the cables that connect to the SHV boards that are used to distribute the bias voltage to the APA wires, electron diverters, and FC termination electrodes need to be installed as well. The cables for the bottom APA need to be routed through the frames of the anode plane assemblies, an operation that can be performed only after the two anode plane assemblies are mechanically coupled inside the toaster area. Quick tests are performed after the installation of the final cables to ensure that the detector has not been damaged in the transport and that all cable connections have been performed correctly. Only then can the anode plane assemblies be moved to their final positions inside the detector cryostat. At that point, the CE and PDS cables can be routed through the spool piece and connected to the respective flanges and strain reliefs. The flanges are then moved to the final position on the spool pieces and leak tests and electrical connectivity tests can be performed. Then the bottom plate of the crossing tubes, along with its additional strain relief for the CE and PDS cables, can be put in place; the final slack of the cables are also arranged in the cable trays attached to the supports inside the cryostat. After the cabling work is completed, the WIECs for a pair of anode plane assemblies can be installed on the spool piece and more testing of the entire power, control, and readout chain can be performed: first with local control, and later after connection of the readout and timing and control fibers to the WIBs using the final DAQ system. The installation of the next row of anode plane assemblies will begin only when all of these tests have been completed, with a requirement that all FEMBs are properly read out from the DAQ, allowing at most for a 0.1% fraction of non-working channels.

A total of seven months is available in the schedule for the installation of the 25 rows of anode plane assemblies and cathode plane assemblies. The current plans foresee that six anode plane assemblies and two cathode plane assemblies are installed and tested in one week before moving on to the next set. As soon as another set of anode plane assemblies and cathode plane assemblies is in place, any replacement of components or rework of connections inside the cryostat becomes very difficult or impossible. This requires that all readout tests be performed very quickly after each step in the installation. The schedule foresees four work days each week for the installation work (in two eight-hour shifts). The testing activities may require that work is performed in parallel, i.e., that the CE components of a pair of anode plane assemblies are tested while another pair is being installed and/or connected to the powering, control, and readout system. It is also likely that the testing work may require a more extended working schedule (six or seven working days per week). More complex tests, involving the reading out of multiple rows of anode plane assemblies, will continue throughout the entire period (eight months) during which all the detector components are installed inside the cryostat. Final tests should be performed reading out the entire detector through the DAQ system prior to the closure of the temporary construction opening (TCO) and before starting to fill the cryostat with argon and cooling down. There will be a hiatus in the

commissioning activities during the filling of the cryostat, during which the conditions of the detector will continue to be monitored. The commissioning at LAr temperature most likely will be possible only after the cryostat is completely full of LAr.

3.7.2 Commissioning and Calibration

Directly following the installation of the instrumented anode plane assemblies into the cryostat, commissioning of the TPC electronics will commence, and will be carried out both before and after the LAr fill; the former establishes whether or not the installation procedure led to impairment of the electronics, and the latter checks that the cryogenic electronics do not experience failures in the cold LAr.

As described in Section 3.7.1, the electronics checkout prior to LAr fill will begin as soon as the first APA is installed; that is, installation and testing will proceed in parallel. This has the advantage of informing the installation of subsequent anode plane assemblies, and thus minimizing the total number of electronics channels lost during the installation process. Items to be checked during the commissioning process include the noise level on every channel, dead or noisy (high RMS) channels, cross-talk across neighboring wires or neighboring channels in the electronics, pick-up noise (including spatial dependence in the detector) if present, and noise coherent across channels sharing common electronics (e.g., the same FEMB). These measurements will be performed first during the tests in the cold box. Repeating these measurements prior to filling the cryostat with LAr will allow for final repairs or replacements for all the CE components prior to the closure of the TCO. This will also give an opportunity to intervene on noise or electronics issues that would become evident when reading out the entire detector at once, before proceeding with the LAr fill.

Once every APA is installed and tested as described above, the cool-down process and LAr fill will be carried out. Monitoring of noise levels and dead/noisy channel count will be done continuously during this process. After the LAr fill, another electronics checkout similar to the one described above will be carried out. Any electronics issues identified during this procedure will be fixed before continuing, if possible. The wire bias HV and cathode HV will then be brought up, with noise studies repeated after each subsystem is turned on. With the wire bias HV and cathode HV up, one can then utilize ionization signals (e.g., from ^{39}Ar beta decays) to distinguish between different possible issues that might impair the readout of a given channel, such as a short between the wire planes (which would alter the wire field response on nearby wires) and a problem with the electronics.

Both during the commissioning phase of the experiment and during normal operations, it may be desired to perform an in situ calibration of one or more parts of the TPC electronics chain. These calibrations will utilize a combination of noise data and data collected while a calibration pulser (internal DAC on the FE ASIC) is periodically injecting charge into the TPC electronics channels. Calibrations of interest include determining the gain and shaping time of every electronics channel in the TPC (as the FE ASICs may experience changes in these quantities in the cold) and characterizing the linearity of the ADC ASICs in the cold. With the updated ADC ASIC design, it is not expected that nonlinearity of the ADCs will be a significant issue (see Section 3.2.3.3

for a discussion of the on-chip calibration that is used), but it is important to verify this with data collected in the experiment. Specific in situ calibration algorithms are being studied at ProtoDUNE-SP, and will be further developed there and in the other electronics test facilities described in Section 3.5.2. Experience from MicroBooNE and other running LArTPC experiments will be very useful in informing TPC electronics calibration procedures for the DUNE SP modules.

3.8 Safety

The TPC electronics will be built and handled in such a way as to ensure the safety of both personnel and equipment. The team will work closely with the project Technical Coordination organization to make sure that all applicable safety procedures are followed and documented.

The instrumentation of the TPC electronics will include multiple printed circuit boards and cabling. The cabling includes the high-voltage wire bias distribution, low-voltage power and signals. Each of these elements will require attention to relevant safety standards and solutions will be subject to the review of the project Technical Coordination organization.

All printed circuit boards will be designed such that the connectors and copper-carrying traces are rated to sustain the maximum current load. In the case of the low-voltage warm electronics, all boards will be fused following prescribed safety standards. The cold electronic low-voltage boards inside the cryostat will not be fused because these boards will be inaccessible during operations and fire is not a danger once the cryostat is filled with LAr. Special precautions must be taken during installation and commissioning of the CE prior to the cryostat being filled with LAr. The TPC electronics group will work with the project Technical Coordination to implement this.

All cabling and connectors will be selected such that they meet or exceed the possible ampacity and voltage ratings of the connected power supplies. In the case of HV wire bias distribution, all accessible warm connectors will be SHV type connectors, which limit the possibility of a touch potential that could shock a person. In the cold, many of the HV connections will be open soldered connections. Care will be taken to ensure personnel safety should these connections need to be energized while the APA is exposed. However, it is not anticipated that APA wire bias will be powered by more than 50 V unless the APA is enclosed within a Faraday shield.

Finally, the safety of the equipment must be taken into account during production, initial checkout, installation, and cabling. Proper electrostatic discharge (ESD) procedures will be followed at all stages, including use of ESD safe bags for storage and ESD wrist straps used by personnel when handling the cards. The TPC electronics will also make use of shorting connectors on all cables which are attached to the printed circuit cards, but not attached at the opposite end. During installation, multiple long cables will be attached to front-end boards, but will not be attached to the connectors on the flanges for some period of time. Detailed procedures for the use of cable-shortening connectors will be written and used.

Finally, the handling of the APA and attached front-end electronics must follow ESD safe handling procedures whenever the APA is moved from one ground reference to another, or after it has been

left in a “floating” state for any period of time. Whenever the APA is moved and could encounter a step potential, a connection must be made through a slow discharge path that equalizes the APA frame potential to the new environment. Again, ESD safe-handling rules will be documented and followed.

3.9 Organization and Management

3.9.1 Single-Phase TPC Electronics Consortium Organization

For the moment the CE consortium does not have a formal substructure with coordinators appointed to oversee specific areas. This is in part due to the current focus on ASIC development; informal subgroups exist that are following the design of the various ASICs. A BNL collaborator is currently leading the design of the new version of LArASIC, and in parallel following the studies of commercial ADCs for SBND, which is using the same ASIC. Collaborators from LBNL, BNL, and Fermilab are working on the design of a new ADC ASIC with 65 nm technology. Collaborators from Fermilab and SLAC, respectively, are overseeing the development of the new COLDATA ASIC and the adaptation of the nEXO CRYO ASIC for use in DUNE. A new working group is tasked with studying reliability issues in the CE components and preparing recommendations for the choice of ASICs, the design of printed circuit boards, and testing. This working group will consider past experience from cryogenic detectors operated for a long time (ATLAS LAr calorimeters, NA48 liquid krypton calorimeter, HELIOS), from space-based experiments (FERMI/GLAST), and the lessons learned from ProtoDUNE-SP construction and commissioning. Input from other fields will also be sought. Later this working group will develop the QC program for the CE detector components, starting from the ProtoDUNE-SP experience. It is planned to reassess the structure of the group in a few months, with a likely split between components inside and outside the cryostat, a new group responsible for testing, and various contact people for calibration, physics, software and computing, and integration and installation.

The main decision that the consortium has to face in the next 12 to 18 months is the choice of ASICs to be used in the DUNE FEMBs. A first decision will be taken early in Summer 2018, when it will be determined whether or not system tests, beyond those planned by the SBND collaboration, should be performed for commercial ADC chips and for the ATLAS ADC. In February 2019, following tests performed with a ProtoDUNE-SP APA in the cold box at CERN and with a small TPC in LAr at Fermilab, a list of options will be prepared for presentation in the TDR. Only ASICs that satisfy the DUNE performance and reliability requirements will be included in this list of options. A final choice for the ASICs to be used in DUNE should be taken in summer 2019, prior to the DOE CD-2/CD-3b review. Physics performance, reliability, and power constraint considerations will be taken into account when making this choice, which will go through the Executive Board approval procedure.

3.9.2 Planning Assumptions

Plans for the CE consortium are based on the overall schedule for DUNE that assumes that the first anode plane assemblies will be fully populated with electronics and tested in spring 2022, with the installation of the anode plane assemblies inside the cryostat beginning in May 2023. Plans are being made for replacing three of the six anode plane assemblies of ProtoDUNE-SP with the final DUNE anode plane assemblies including final ASICs and FEMBs, and for a second period of data-taking in 2021-2022. The integration of the anode plane assemblies for the first cryostat with the electronics should be finished by October 2023, and their installation in the cryostat by January 2024. This requires integrating two anode plane assemblies per week over a span of 21 months, which allows for a ramp-up period at the beginning and a contingency of two to three months at the end. This defines the time window for the completion of the R&D program on the ASICs. A set of ASICs (or a single ASIC) meeting all the DUNE requirements has to be fully qualified by fall 2020, such that pre-production ASICs and the corresponding FEMBs can be assembled and tested in spring 2021, launching the full production in summer 2021.

Meeting this timeline requires that the development of the ASICs, and in particular of the newly designed ones (the SLAC CRYO ASIC, the joint LBNL-BNL-Fermilab cold ADC, and COLDATA) are prototyped by the end of summer 2018, with testing completed by the end of 2018. This would allow for a second round of prototyping, if necessary, in the first half of 2019. It also leaves room for a possible third design iteration and qualification of ASICs and FEMBs between the end of 2019 and fall 2020. The FEMBs used for ProtoDUNE-SP will likely have to be redesigned to house a new ADC and to replace the FPGA used in ProtoDUNE-SP with the COLDATA ASIC. Multiple variants of this board will be necessary, depending on the success of the various ADC R&D projects being currently pursued. These design changes will be made in the second half of 2018. Additional FEMB prototypes will be designed and fabricated depending on the outcome of the initial testing of the SLAC CRYO ASIC. A second iteration of FEMB prototype(s) will be necessary in 2019, when the final ASICs (that may have a different channel count from the first round of prototypes) will become available.

It is assumed that apart from the ASICs, where rapid development is still required, and the FEMBs, which have to be redesigned to accommodate the new ASICs, most of the detector components to be delivered by the CE consortium will require only minor changes relative to the ProtoDUNE-SP components. For this reason the modifications of these other detector components will be delayed until 2019 or 2020, which will also help with the funding profile. Exceptions will be made for further development in test stands, for cabling studies, and for conceptual studies of automated testing assemblies, rack space assignment, and the interface to the DAQ system.

3.9.3 WBS and Responsibilities

A preliminary work breakdown structure (WBS) has been prepared for the activities of the CE consortium. The WBS is split in a time-ordered fashion between activities related initially to design, R&D, and engineering, then to production setup, and finally to the production, integration, and installation phases for the SP module to be installed in the first DUNE cryostat. The latter

three sets of activities could be repeated for the construction of additional SP modules. Physics and simulation activities are to proceed in parallel to the detector design and construction activities. Within each phase (starting with the design and ending with the installation), the WBS foresees work packages that cover system engineering, installation of the detector components inside the cryostat (including all ASICs, FEMBs, cables, and corresponding support structures and cryostat penetrations), and the detector components installed on top of the cryostat (including the warm interface electronic crates with their boards, the LV and bias-voltage power supplies with their crates, and all of the associated cables and infrastructure). This matches the current plan for the future group structure of the CE consortium. In addition, a separate work package covers the development and support of the testing facilities and the related software in order to provide these activities with the effective supervision that is required in order to meet the reliability requirements of the DUNE experiment.

All of the institutions currently interested and committed to the construction of the detector components that are a responsibility of the CE consortium are from the USA and are supported by a single funding agency, the Department of Energy. For this reason, the exact role of the individual institutions in the activities of the consortium has not been defined, except for the currently ongoing ASIC development. The role of each institution will be defined prior to the submission of the TDR.

3.9.4 Timeline and Key Milestones

A preliminary list of milestones indicating the current planning for the completion of the design, R&D, and engineering phase, and then later for the production setup and the production, integration, and installation activities is shown in Table 3.4. This list of milestones corresponds to a scenario in which only two iterations in the design of the ASICs and FEMBs are required, and results in a float of nine months for the integration of the CE with the anode plane assemblies. In the case that a third iteration is required, the availability of the ASICs and FEMBs could introduce a delay in the overall schedule of the SP module. A detailed schedule of all of the activities will be prepared in the coming months, with the goal of having a better estimate of the critical path for the project under different assumptions on the number of design iterations for the ASICs and FEMBs.

Table 3.4: Milestones of the Cold Electronics consortium.

Date	Milestone
Jun 2018	Submission of first version of all custom ASICs
Oct 2018	Bench test of first version of all custom ASICs
Feb 2019	System tests of first version of all ASICs and FEMBs
Feb 2019	Conceptual design of fibers and cabling plant
Feb 2019	Demonstrate cable routing through APA frames
May 2019	Submission of second version of all custom ASICs
Dec 2019	System tests of second version of all ASICs and FEMBs
Mar 2020	Revise design of WIBs and crates
Jun 2020	Revise design of cryostat penetrations
Sep 2020	Revise design of detector components outside the cryostat
Nov 2020	Launch pre-production of ASICs and FEMBs
Jun 2021	Integrate CE with pre-production anode plane assemblies
Jul 2021	Availability of all test stands for ASICs and FEMBs
Jul 2021	Availability of vertical slice test with final production components
Oct 2021	Launch pre-production of all detector components
Mar 2022	Begin integration of CE on production anode plane assemblies
Nov 2022	Integration of CE on anode plane assemblies 50 % complete
Nov 2022	Launch production of cryostat penetrations
Nov 2022	Launch production of warm interface electronic crates and boards
Jun 2023	Start detector installation in the cryostat at SURF
Oct 2023	Complete integration of CE on anode plane assemblies
Jan 2024	Complete APA installation at SURF
Feb 2024	Complete initial tests of detector prior to TCO closing

Chapter 4

High Voltage System

4.1 High Voltage System Overview

4.1.1 Introduction

A liquid argon time-projection chamber (LArTPC) requires an equipotential cathode plane at high voltage (HV) and a precisely regulated interior E field to drive electrons from particle interactions to sensor planes. In the case of the DUNE single-phase technology, this requires vertical cathode planes, called cathode plane assemblies (CPAs), held at HV; vertical anode planes, called anode plane assemblies (APAs), described in Chapter 2.1; and formed sets of conductors at graded voltages surrounding the the central drift volume, collectively called the field cage. The field cage (FC) consists of portions on the top and bottom of the drift volume (called the top field cage (top FC) and bottom field cage (bottom FC), respectively), and along the sides, called endwall field cages (endwall FCs).

The SP time projection chamber (TPC) construction is shown in Figure 4.1. The drift fields transport the ionization electrons towards the anode plane assemblies at sides and center. One should note that the HV systems for the SP and DP TPC concepts share components with similar designs. These include the FCs profiles and supporting FRP beams as well as the voltage divider boards. More details can be found in Volume 3: Dual-Phase Module Chapter 4.

The HV consortium provides systems that operate at the full range of voltages, maximum to ground, inside the TPC volume. As a result, its systems constitute a large fraction of the total internal structures of the TPC itself, the principal exception being the anode plane assemblies and the photon detection system (PDS). In addition, the HV system largely bounds the useful fiducial volume of the experiment, and thus plays a key role in determining the event rate for all DUNE physics processes. Mechanical and structural concerns are integrated with electrical design to meet the requirements.

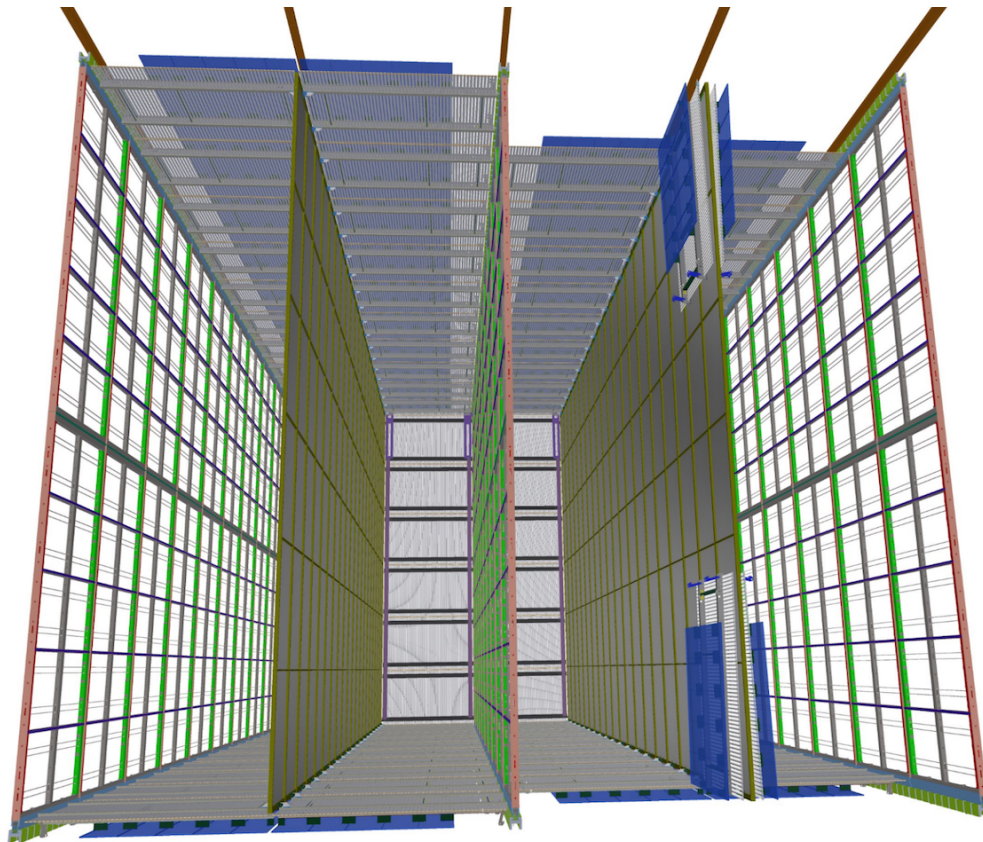


Figure 4.1: A schematic of a SP module showing the three APA arrays (at the far left and right and in the center, spanning the entire detector module length) and the two CPA arrays, occupying the intermediate second and fourth positions. The top and bottom FC modules are shown in blue; the endwall FCs are not shown. On the right, the front top and bottom FC modules are shown folded up against the CPA panels to which they connect, as they are positioned for shipping and insertion into the cryostat. The cathode plane assemblies, anode plane assemblies and FCs together define the four drift volumes of the SP module.

Two possible anode-cathode plane configurations exist for the fixed DUNE maximum electron drift length: cathode planes facing cryostat wall (C-A-C-A-C) or anode planes facing the cryostatic wall (A-C-A-C-A). The latter configuration keeps most of the cathode plane surfaces far away from the grounded cryostat walls, reducing electrostatic breakdown risks and decreasing the total energy stored in the electric field to 800 J.

In this configuration, energy is mostly stored in the high E field region between the field cage and the nearby grounded conductors. In an unexpected HV breakdown, the entire 400 J associated with one cathode could be released into a small volume of material, possibly causing physical damage. It is difficult to predict the distribution of energy along a discharge path. A conservative approach treats this energy as a risk to the TPC and the cryostat membrane. Mitigating this risk entails slowing down the energy release as much as possible to minimize the potential damage by subdividing the FC into electrically isolated modules, and constructing the cathode with highly resistive material.

Previous large LArTPCs (ICARUS, MicroBooNE) have used continuous stainless steel tubes as electrodes. Electrically, linking such electrodes to span more than 100 m in total length increases the stored energy each electrode has, and increases the risk of damaging the field cage components in a HV discharge.

Having the FC divided into mechanically and electrically independent modules eases the construction and assembly of the FC, and also greatly restricts the extent of drift field distortion caused by a resistor failure on the divider chain of a FC module.

If the cathode is made of metal, a HV discharge can cause the electrical potential of the entire cathode surface to swing from its nominal bias (e.g., -180 kV) to 0 V in nanoseconds. This would induce a large current into the analog front-end (FE) amplifiers connected to the sensing wires on the anode plane assemblies (mostly to the first induction wire plane channels). Internal study (docdb 1320) has shown that this surge of current would overwhelm the internal ESD protection in the FE ASICs. To reduce this induced current, we chose to construct the cathode out of material with high resistivity. Figure 4.2 shows the release of stored energy in time and the voltage distribution of a section of the cathode at one moment in time. To minimize the induced current to the amplifiers, the surface resistivity should be raised until the ionization current from the TPC starts to cause significant voltage drop along the cathode. In the DUNE FD the current is dominated by ^{39}Ar decay, and we can tolerate surface resistivity well above $1\text{ G}\Omega/\text{sq}$.

The SP HV system may have modifications if problems are identified in the present design in ProtoDUNE-SP. Issues identified in earlier testing form the basis of an ongoing R&D program.

4.1.2 Design Requirements

The HV system is designed to meet the physics requirements of the DUNE experiment. These are both physical requirements (such as E fields that allow robust event reconstruction) and operational (a system that avoids over-complication so as to maximize the time that the detector can collect neutrino events). An important collection of the requirements affecting HV is shown in Table 4.1.

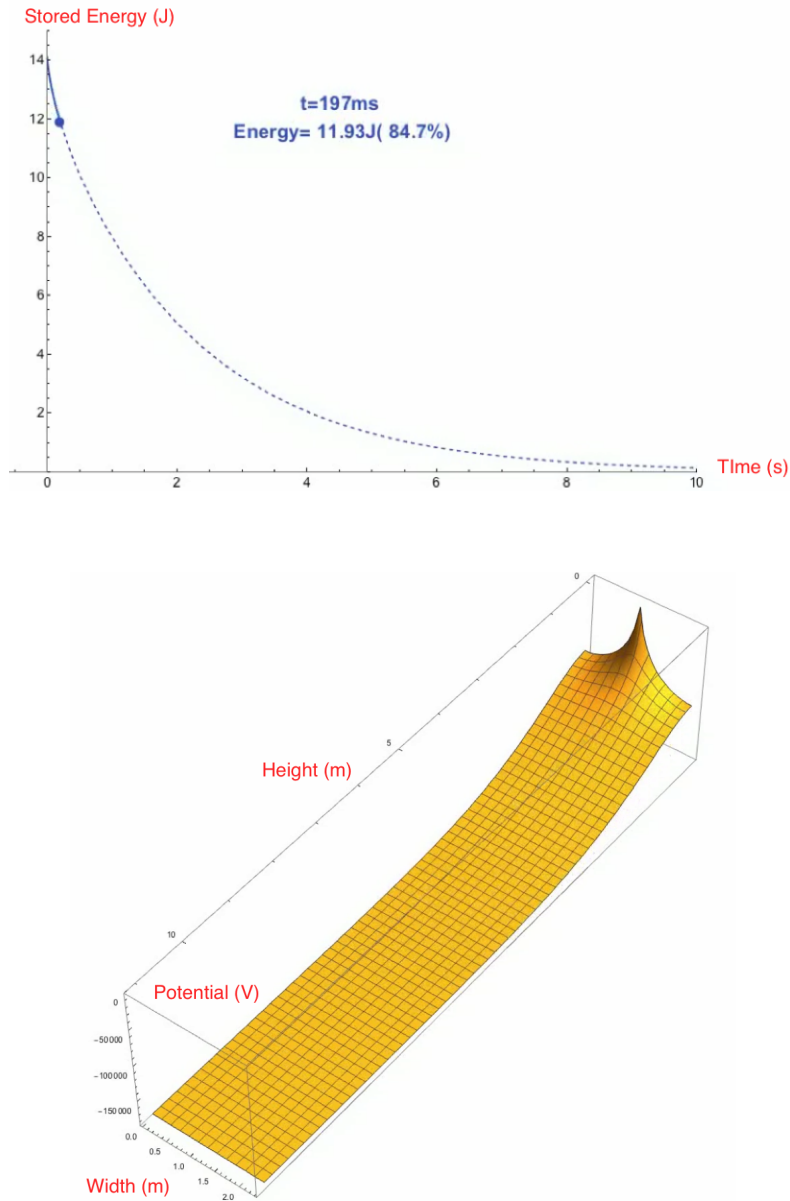


Figure 4.2: Bottom: Simulated CPA Discharge event on a highly resistive cathode surface ($1 \text{ G}\Omega/\square$), showing the voltage distribution on a section of the cathode ($2.3 \text{ m} \times 12 \text{ m}$) 0.2 ms after the discharge. Top: Time dependence of removal of stored energy.

Table 4.1: HV system requirements

No.	Requirement	Physics Requirement Driver	Requirement	Goal
1	Establish uniform minimum E field in TPC drift volume.	Limit recombination, diffusion, and space charge impacts e , μ , p particle ID. Establish constant drift velocity and adequate S/N on induction planes for tracking.	>250 V/cm	500 V/cm
2	Do not exceed maximum E field in liquid argon (LAr) volume.	Avoid damage to detector to enable data collection over long periods.	30 kV/cm	as low as reasonably achievable (ALARA)
3	Minimize power supply ripple	Keep readout electronics free from external noise, which confuses event reconstruction.	0.9 mV	0.9 mV
4	Maximize power supply stability.	Maintain ability to reconstruct data taken over long period. Maintain high operational uptime to maximize experimental statistics.		
5	Provide adequate resistivity to create acceptable decay constant for discharge of the cathode surface and FC.	Avoid discharge damage to detector module or electronics to enable data collection over long periods.	1 M Ω /sq	1 G Ω /sq
6	Provide redundancy in all HV connections.	Avoid single point failures in detector module that interrupt data collection.	Two-fold	Four-fold

4.1.3 Scope

The scope of the HV system includes the selection and procurement of materials for, and the fabrication, testing, delivery and installation of systems to generate, distribute, and regulate the voltages that create a stable and precise E field within a DUNE SP module.

The HV system consists of components both exterior and interior to the cryostat. The voltage generated at the HV power supplies passes through the cables, filters, and the HV feedthrough into the cryostat. From the voltage delivery into the cryostat, it is further distributed by components that form part of the TPC structure. These components are:

- HV power supply;
- Top FC, bottom FC, and ground planes (GPs);
- Endwall FC.

The TPC has two cathode plane assemblies *arrays*, that span the length and height of the SP module, as shown in Figure 4.1. Given the modular design, each array is assembled a set of 25 adjacent CPA *planes*, which in turn are constructed of smaller pieces. Each plane is a set of two adjacent *panels* (full height, half length, as measured along the detector module length). Each panel consists of three stacked *units*, approximately 4 m high by 1.2 m long. The units each consist of two half-height vertically stacked resistive panels enclosed within a FR4¹ frame.

An installation rail supports the panels from above through a single mechanical link.

The sides of the drift volumes on both sides of the CPA plane are covered by the FC and endwall FC modules to define a uniform drift field of 500 V/cm, with a increasing potential over 3.5 m from the HV CPA (−180 kV) to ground potential at the APA sensor planes. The cathode bias is provided by an external HV power supply through an HV feedthrough connecting to the CPA plane inside the cryostat. The FC modules come in two distinct types: the top and bottom (FC), which run the full length of the detector module, and the endwall FCs, which complete the detector at either end. The modules of both systems are constructed from an array of extruded aluminum open profiles supported by FRP² (fiber-reinforced plastic) structural beams. A resistive divider chain connects adjacent metal profiles to provide a linear voltage gradient between the cathode and anode planes. The top FC and bottom FC modules are nominally 2.3 m wide by 3.5 m long. At the ends, the endwall FC modules are 3.5 m wide by 1.5 m in height.

Structurally, the frames of the cathode and field cages are made from materials with similar thermal expansion coefficients, minimizing issues of differential thermal expansion. The field cage frames support aluminum profiles but these are restrained at only one location and are allowed to float within the frame. The endwall FCs modules, each 1.5 m high by 3.5 m wide (along the drift volume dimension), stack eight units high to cover the 12 m height of the TPC. Extensive tests have been

¹NEMA grade designation for flame-retardant glass-reinforced epoxy laminate material, multiple vendors, National Electrical Manufacturers Association™, <https://www.nema.org/pages/default.aspx>.

²Fiber-reinforced plastic, a composite material made of a polymer matrix reinforced with fibers, many vendors.

performed of mechanical and electrical properties of materials used in the HV system. These are fully documented elsewhere

The cathode plane assemblies and anode plane assemblies support the top FC and bottom FC modules, whereas installation rails above the anode plane assemblies and cathode plane assemblies support the endwall FC modules. A ground plane consisting of tiled, perforated stainless steel sheets runs along the outside surface of each of the top FC and bottom FC, with a 20 cm clearance.

Tables 4.2 and 4.3 contain summaries of terminology and parts.

Table 4.2: HV Cathode Plane Components

Component and Quantity	Length (z)	Height (y)	Per SP module
CPA array (2 per SP module)	58 m	12 m	2
CPA plane (25 per CPA array)	2.3 m	12 m	50
CPA panel (2 per CPA plane)	1.2 m	12 m	100
CPA unit (3 per CPA panel)	1.2 m	4 m	300
CPA RP (2 per CPA unit)	1.2 m	2 m	600

Table 4.3: HV Field Cage Components

Component	Count	Length (z)	Width (x)	Height (y)	Submodule:	Grand Total
FC (Top/Bottom Field Cage)	200	2.3 m	3.5 m	-	57	200
FC-Profiles (per FC)	57	2.3 m	-	-	-	11400
Ground Plane Modules (per FC)	5	2.3 m	0.7 m	-	-	1000
EW-Plane (Endwall Field Cage)	2	-	14.4 m	12 m	4	2
EW (per EW-Plane)	4	-	3.5 m	12 m	8	8
EW-Modules (per EW)	8	-	3. m	1.5 m	57	64
EW-Profiles (per EW-Module)	57	-	-	1.5 m	-	3648

4.2 HV System Design

4.2.1 High Voltage Power Supply and Feedthrough

The HV delivery system consists of

- two power supplies,
- HV cables,
- filter resistors, and

- HV feedthroughs into the cryostat.

For HV delivery, two power supplies are used to generate the voltage, one for each CPA array. This separated setup more easily accommodates different running conditions and helps isolate any instabilities. The cryostat design has two feedthrough ports for each CPA array, one at each end of the cryostat. The spare, downstream port provides redundancy against any failure of the primary HV delivery system.

Each CPA connects to two drift volumes in parallel, presenting a net resistance of $1.14 \text{ G}\Omega$ to each supply. At the nominal 180 kV cathode voltage, each power supply must provide 0.16 mA .

The planned power supply model for the SP module is similar to the power supply³ used on ProtoDUNE-SP, with a maximum output voltage of 200 kV and a maximum current draw of 0.5 mA . An option is an existing 300 kV , 0.5 mA model from the same vendor. The HV cables are commercially available models compatible with the selected power supplies.

Filter resistors are placed in between the power supply and the feedthrough. Along with the cables, these resistors reduce the discharge impact by partitioning the stored energy in the system. The resistor-cable assembly also serves as a low-pass filter reducing the 30 kHz voltage ripple on the output of the power supply. With filtering, such supplies have been used successfully in other LArTPC experiments, such as MicroBooNE and ICARUS.

Figure 4.3 provides a sample schematic of the HV supply circuit.

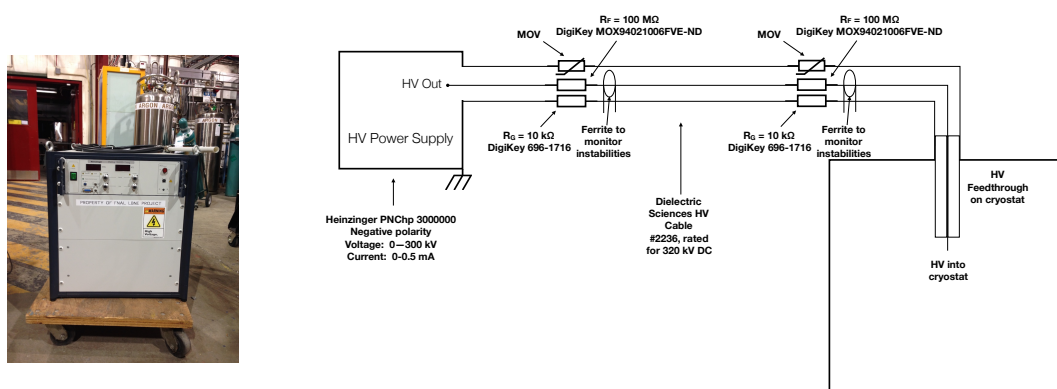


Figure 4.3: Right: A schematic showing the HV delivery system to the cryostat (Credit: SEL). One of the two filters sits near the power supply; the other sits near the feedthrough. Left: A Heininger power supply (Credit: H. Wang).

The requirement on low electronics noise sets the upper limit of residual voltage ripple on the

³Heininger, PNC HP200000 HV power supply, Heininger™ Power Supplies, <http://www.heininger.com/>.

cathode to be 0.9 mV. Typically, commercial supplies specify that the ripple variation is limited to 0.0001 % around an absolute precision in nominal voltage of plus or minus 50 mV. Assuming cable lengths of 30 m and 3 m between the filters themselves, and between the filter and feedthrough, respectively, resistances as low as a few M Ω yield the required noise reduction according to calculations and experience.

The current plan for the filters is a cylindrical design. Here each end of an HV resistor is electrically connected to a cable receptacle. The resistor must withstand a large over-power condition. Radially out from the resistor is an insulator, for which other designs have used transformer oil or ultra-high molecular weight polyethelene (UHMWPE). The outer case of the filter is a grounded stainless-steel shell. The current filter design is shown in Figure 4.4.

The HV feedthrough is based on the successful ICARUS design, which has been adapted for ProtoDUNE-SP. The voltage is transmitted by a stainless steel center conductor. On the warm side of the cryostat, this conductor mates with a cable end. Inside the cryostat, the end of the center conductor has a spring-loaded tip that contacts a receptacle cup mounted on the cathode, delivering HV to the field cage. The center conductor of the feedthrough is surrounded by UHMWPE. A drawing is shown in Figure 4.4.

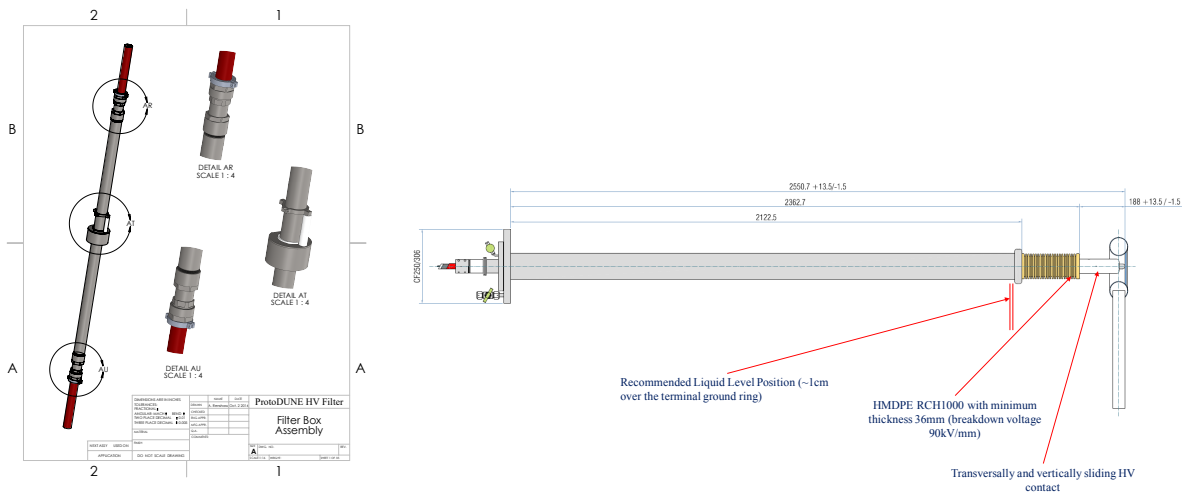


Figure 4.4: Left: Drawing of a HV filter (Credit: A. Renshaw). Right: HV feedthrough drawing (Credit: F. Sergiampietri).

The upper bound of operating voltage on a feedthrough is, to first order, set by the maximum E field on the feedthrough. This E field is reduced by increasing the insulator radius. For the target voltage, the feedthrough uses a UHMWPE cylinder of approximately 15 cm diameter. In the gas space and into at least 15 cm of the liquid, the insulator is surrounded by a tight-fitting stainless steel ground tube. The ground tube has a 25 cm Conflat (an industry standard) flange welded on for attachment to the cryostat.

Outside of the cryostat, the HV power supply and cable-mounted toroids will monitor the HV. The power supplies typically have sensitivities down to tens of nA in current read-back capability and are able to sample the current and voltage every 300 ms. The cable-mounted toroids are sensitive to fast changes in current; the polarity of a toroid's signal indicates the location of the current-

drawing feature as either upstream or downstream of it. Experience from the 35 ton prototype installation suggested sensitivities to changing currents with a timescale between $0.1\ \mu\text{s}$ to $10\ \mu\text{s}$, providing information on the timescale of any current changes.

Inside the cryostat, pick-off points near the anode will monitor the current in each resistor chain. Additionally, the voltage of the GPs above and below each drift region can be equipped to diagnose problems via a high-value resistor connecting the GP to the cryostat. In the 35 ton prototype, such instrumentation provided useful information on HV stability and where any stray charge was flowing.

Both commercial and custom HV components must be rated for sufficient voltage and satisfy tests to meet the requirements summarized in Table 4.1. Further details on these tests are in Section 4.5.

The resistances in the filters, in combination with the capacitances between the HV system and the cathode, determine the attenuation of the tens of kHz ripple from the power supply. The filters are designed such that the ripple is reduced to an acceptable level when installed in the complete system, thus satisfying requirement (3) that the power supply ripple is minimized.

4.2.2 Cathode Plane Assembly (CPA)

The CPA provides a constant potential surface at $-180\ \text{kV}$ for the SP module. It receives its HV from the feedthrough that makes contact with the HV bus mounted on the CPA frame through an attached donut assembly attached to the frame, as shown in Figure 4.5. The CPA also provides HV to the first profile on the top and bottom FC elements and to the endwall FCs as well. Details on the electrical connections are found in Section 4.2.4.

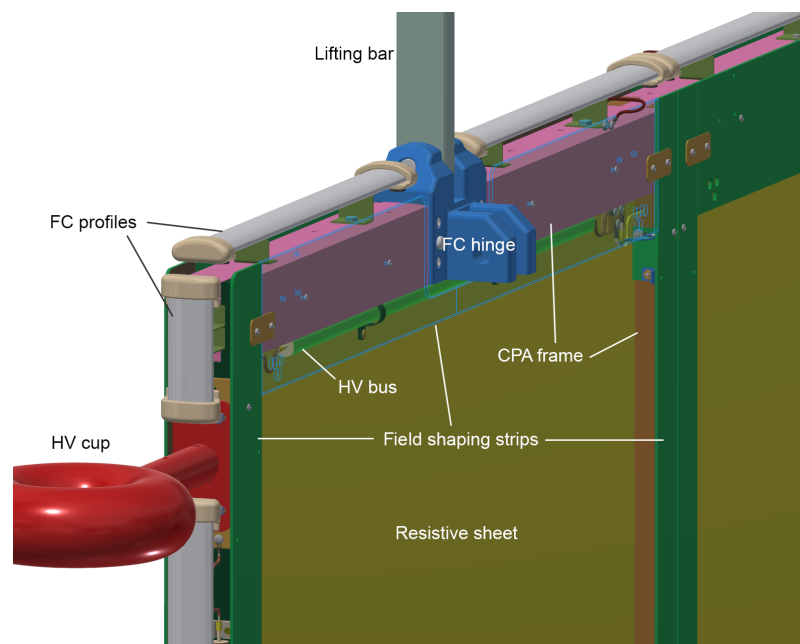


Figure 4.5: HV input donut connection to CPA.

Ideally, the cathode would be constructed from a large thin resistive sheet. However, inside the cryostat, there is a moderate convective flow of the LAr that can produce a small pressure difference across the cathode surface. To maintain the position and flatness of the cathode, the cathode surface must be reinforced for stiffness. This is accomplished using 6 cm thick FR-4 frames at 1.2 m intervals. Since FR4 is a good insulator at cryogenic temperature with a different dielectric constant than LAr, the presence of the frame causes a local E field distortion that can become pronounced if the frame surface charges up as a result of ionization in the TPC. To minimize this distortion, a resistive field shaping strip is placed on the cathode frame and biased at a different potential. Figure 4.6 illustrates the drift field uniformity improvement with the field shaping strips.

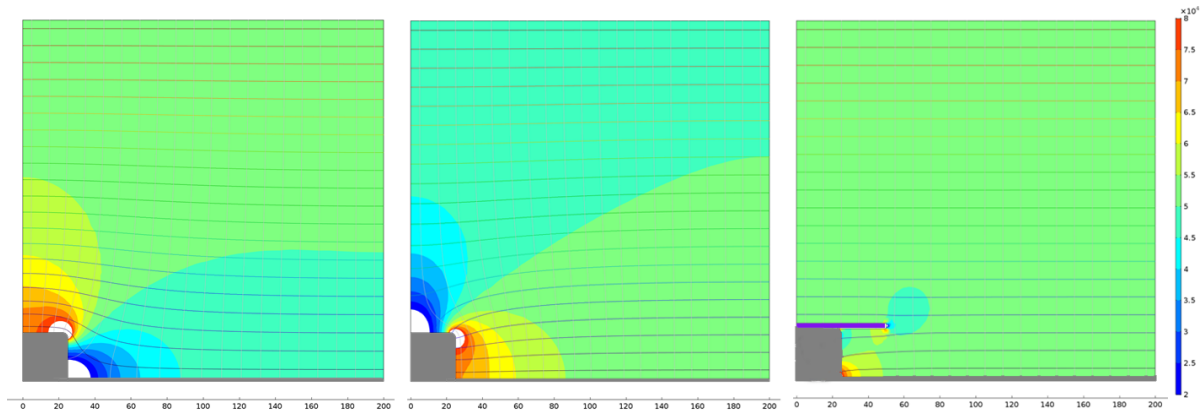


Figure 4.6: A comparison of three cathode cross sections to illustrate the benefit of the FSS. Both equipotential lines (horizontal) and E field lines (vertical) are shown. The amplitude of the E field is shown as color contours. Each color contour is a 10% step of the nominal drift field. The gray rectangles represent the frame and the resistive sheet in each case. Left: a conductive/resistive frame similar to that of ICARUS or SBND; Middle: an insulating frame with the insulating surfaces charged to an equilibrium state; Right: an insulating frame covered with a field shaping strip (purple) and biased at the optimum potential.

The cathode plane assemblies' constant potential surfaces are resistive panels (CPA RPs) composed of a thin layer of carbon-impregnated Kapton⁴ laminated to both sides of a 3 mm thick FR4 sheet of 1.2 m × 2 m size. The surface resistivity of the CPA RPs is required to be greater than 1 MΩ/square in order to provide for slow reduction of accumulated charge in the event of a discharge. A goal of 1 GΩ/square for DUNE CPA RPs extends the protection from discharges in the condition of anticipated higher stored energy at DUNE, compared to prototypes. Other HV components of the CPA include FSS mounted to the CPA frames, edge aluminum profiles to act as the first elements of the field cage, and cable segments forming the HV bus. Careful inspection of these items during the assembly process ensures that no sharp points or edges are present. The surface resistivity of the CPA RPs and the FSS are checked multiple times during assembly – first when the resistive panels and strips are received and after assembly into CPA units on the table. Coated parts that do not meet the minimum surface resistivity requirement are replaced. This ensures that requirement (5) on Table 4.1 is satisfied. Figure 4.7 shows a completed ProtoDUNE-SP CPA panel on the production table ready for lifting into vertical position for mounting on its trolley.

All electrical connections on the CPA and between the CPA and other HV system components

⁴DuPont™, Kapton® polyimide film, E. I. du Pont de Nemours and Company, <http://www.dupont.com/>.

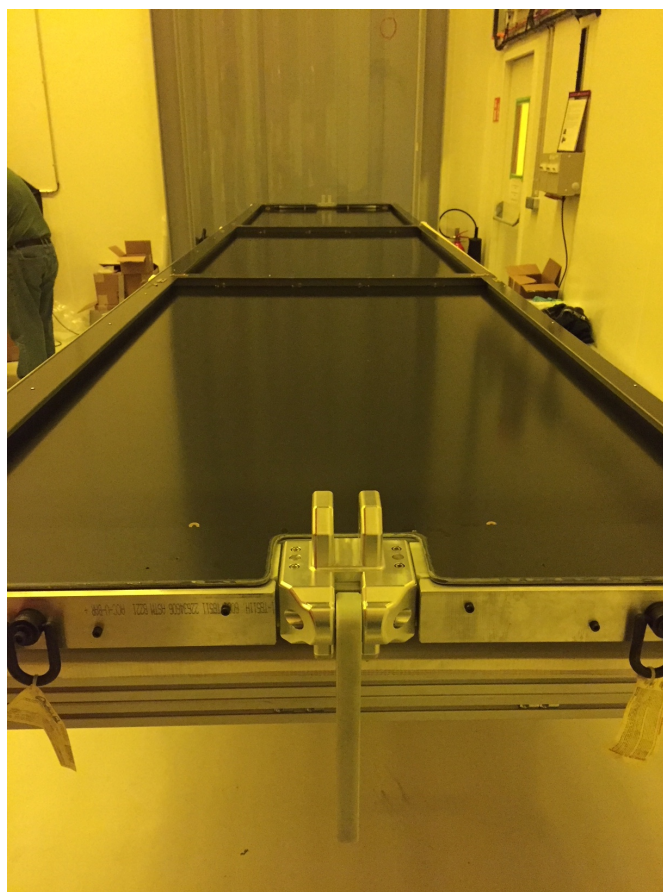


Figure 4.7: Completed ProtoDUNE-SP CPA panel on production table.

(top, bottom, and endwall FCs) are redundant by at least a factor of two. Connections between RPs in a CPA unit are four-fold redundant. The HV connection from the HV power supply is a closed loop around the CPA which can sustain at least one broken connection without loss of the cathode plane HV. This ensures compliance with requirement (6) of Table 4.1.

The CPA frames are required to support, in addition to the HV components, the top FC and bottom FC units attached to both sides of the CPA panel. The arrangement and deployment of these components will be the same as in ProtoDUNE-SP.

4.2.3 Field Cages

4.2.3.1 General Considerations

A uniform E field is required to drift ionization electrons towards the anode plane assemblies. The FCs consisting of field shaping electrodes form a band surrounding the top, bottom, and ends of the active drift volume. The electrodes are biased at different potentials to establish a uniform field inside the LAr volume. The SP module will use extruded aluminum profiles as a cost-effective way to establish the equipotential surfaces.

For safe and stable operation of the LAr cryogenic system, the cryostat must have a small fraction of its volume filled with gaseous argon, commonly referred to as the ullage. Since we want to make good use of the LAr in the cryostat, the top boundary of the TPC, the upper FC, is not very far from the ullage. There are many grounded metallic components in the ullage with sharp features. The E field near these conductors could easily exceed the breakdown strength of gaseous argon. To prevent such breakdowns in the argon gas, a GP is added above the upper FC electrodes at a safe distance and below the liquid surface to shield the high E field from entering the gas ullage. The need for such shielding diminishes toward the APA end of the FC due to the lower voltages on the FC profiles in that region. Therefore the GP on the top only covers about 70 % of the CPA side of the FC, leaving extra room for cable routing near the anode plane assemblies. On the bottom of the cryostat, a similar set of GPs is planned to prevent breakdown, in the liquid, to cryogenic pipings and other sensors with sharp features. No GPs are planned beyond the two endwall FCs since there is sufficient clearance in those regions.

The shape of the electrodes is critical as it determines the strength of the E field between a given profile and its neighboring profiles, as well as other surrounding parts, including the APA, which is electrically at ground. Electric fields need to be well below 30 kV/cm to satisfy design requirement (2) and enable safe TPC operation [12].

The commercially available profiles used for ProtoDUNE-SP, and forming the SP module design, are estimated to lead to E fields of up to 12 kV cm⁻¹ under the configuration and operating voltage assumptions. Figure 4.8 illustrates results from an E field calculation.

The profiles ends are equipped with UHMW polyethylene caps to reduce the risk of arc formation. These caps are designed to have sufficient wall thickness (6 mm) to withstand the full voltage across

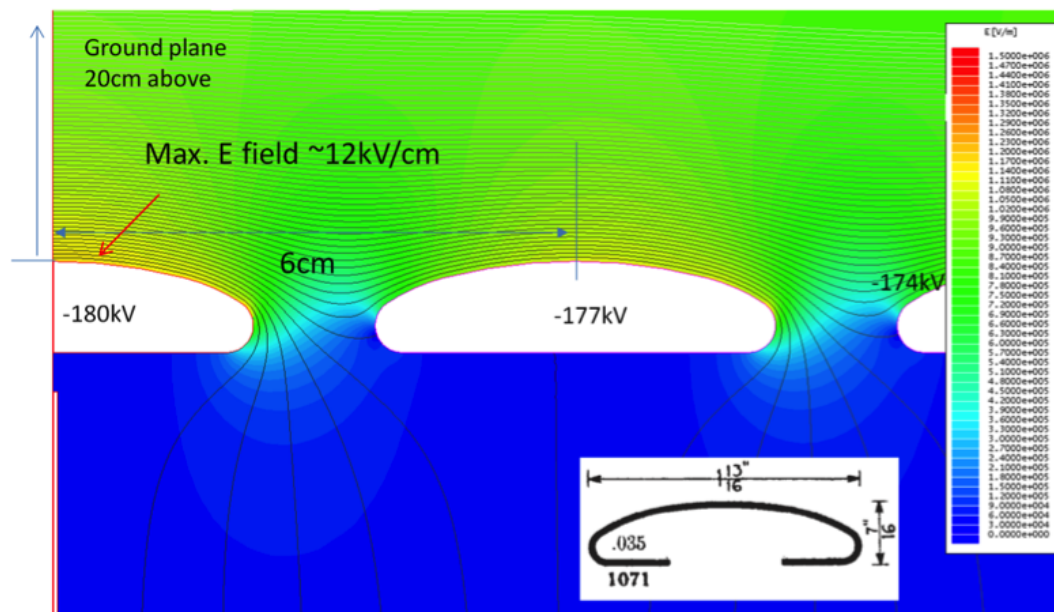


Figure 4.8: E field map (color) and equipotential contours of an array of roll formed profiles biased up to -180 kV and a ground clearance of 20 cm (Credit: BNL CAD model).

their walls.

The aluminum profiles are attached to fiber-reinforced plastic (FRP) pultruded structural elements, including I-beams and box beams. Pultruded FRP material is non-conductive and strong enough to withstand the FC loads in the temperature range of -150 C and 23 C, as certified by vendors. Testing of the FRP joints were conducted at liquid nitrogen temperatures (see DocDb 1504). The strength of the material increased over room temperature tests which provides confidence in the material behavior at LAr temperature. Tests of FRP joints at LN temperature showed that the strength of the material increases at cryogenic temperature relative to room temperature, providing confidence in FRP material behavior at LAr temperature. The FRP material meets class A standards for fire and smoke development established by the International Building Code characterized by ASTM E84⁵

As discussed in Section 4.1.1, the field cage modules are of two types: the top and bottom FC and the endwall FC, both of which are described below. A resistive divider chain interconnects all the aluminum profiles to provide a linear voltage gradient between the cathode and anode planes. The top and bottom modules are nominally 2.3 m wide by 3.5 m long. A GP, in the form of tiled, perforated stainless steel sheet panels, is mounted on the outside surface of the T/B field cage module with a 20 cm clearance. The top and bottom FC modules are supported by the cathode plane assemblies and anode plane assemblies. The endwall FC modules are 1.5 m tall by 3.5 m long. They are stacked eight units high (12 m), and are supported by the installation rails above the anode plane assemblies and cathode plane assemblies.

The FCs are designed to produce a uniform field with understood characteristics. The current (i.e.,

⁵Standard Test Method for Surface Burning Characteristics of Building Materials, ASTM International, https://compass.astm.org/EDIT/html_annot.cgi?E84+18.

ProtoDUNE-SP) FC design has a large gap between the endwall FC module and its neighboring top and bottom modules to allow the latter to swing pass the endwall FC during the FC deployment. This gap causes the largest known distortion in the drift field in the TPC. Figure 4.9 shows the extent of the distortion in this limiting scenario. In ProtoDUNE-SP, the gap produces two regions (of total LAr mass 20 kg) in the TPC near both bottom corners that suffer 5 % E field distortions.

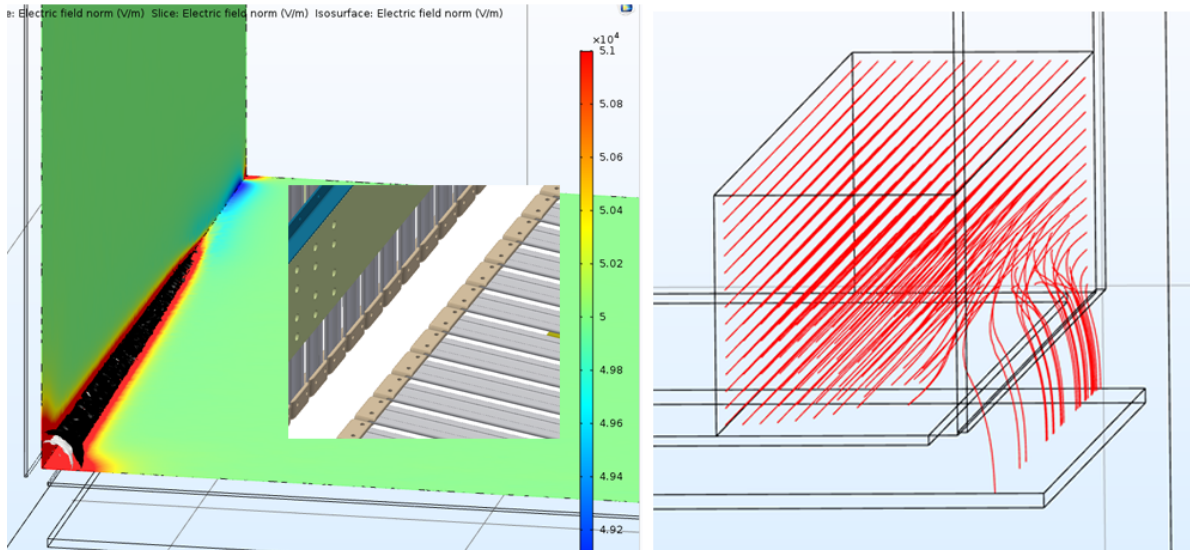


Figure 4.9: E field at a corner between the bottom and endwall FC modules, showing effects of a 7 cm gap. Left: the extent of 5% E field non-uniformity boundary (black surface, contains less than 10 kg of LAr) and 10% non-uniformity boundary (white surface, contains ~ 6 kg of LAr) inside the TPC's active volume. The inset is a view from the CAD model. Right: electron drift lines originating from the cathode surface.

The FCs are designed to meet the system requirements specified in Table 4.1. All components other than the aluminum profiles, GPs, and electronic divider boards are made of insulating FRP and FR4 materials, and the end of each profile is covered with a UHMWPE end cap, to allow the system to reach the design TPC E field (requirement 1). The profiles have been carefully modeled to study the resulting E field, and small-scale laboratory tests have been conducted to ensure that the maximum E field does not approach 30 kV cm^{-1} (requirement 2). These design features are expected to avoid sparking, and thus to draw very small stable currents, which should produce a consistent load on the power supply (requirements 3, 4, and 5). Finally, all voltage divider boards provide redundant paths for establishing the profile-to-profile potential differences, and two redundant boards provide the connection from the FCs modules to the CPA (requirement 6).

4.2.3.2 Top and bottom field cages

The top FC and bottom FC modules are 3.5 m long, which is set by the length of the two 15.2 cm (6 in) FRP I-beams that form the primary support structure of the modules. The I-beams are connected to each other by three 7.6 cm (3 in) FRP cross beams. The connections between the longitudinal and cross I-beams are made with L-shaped FRP braces that are attached to the I-

beams with FRP spacer tubes, and secured with FRP threaded rods, FRP hex-head nuts, and custom-machined FR4 washer plates.

The modules are 2.3 m wide, which corresponds to the length of the aluminum profiles, including the UHMW polyethylene end caps. Profiles are secured to the FRP frame using custom-machined double-holed stainless steel slip nuts that are slid into and electrically in direct contact with the Al profiles such that they straddle the webbing of the 15 cm I-beams, and are held in place with screws that penetrate the I-beam flanges. The profile offset with respect to the FRP frame is different for modules closest to the endwall FCs, and modules in the center of the active volume.

Each top FC and bottom FC module holds five ground planes, which are connected to the outside (i.e., the non-drift side) of the module. The GPs are positioned ~ 20.5 cm above the profiles, and are pushed to the CPA side of the module, leaving the last 14 profiles (88 cm) on the APA side of the module exposed. Between the GPs and the 15 cm I-beams are standoffs made of short sections of 10.2 cm (4 in) FRP I-beams, which are connected with FRP threaded rods and slip nuts. The electrical connection between the ground planes is made with copper strips.

The connections between the top and bottom modules and the cathode plane assemblies are made with aluminum hinges, 2.54 cm (1 in) in thickness, that allow the modules to be folded in to the CPA during installation. The hinges are electrically connected to the second profile from the CPA. The connections to the anode plane assemblies are made with stainless steel latches that are engaged once the top and bottom modules are unfolded and fully extended toward the APA.

The voltage drop between adjacent profiles is established by voltage divider boards that are screwed into the drift volume side of the profiles. A custom-machined nut plate is used that can be inserted into the open slot of each profile and twisted 90° to lock into position. Two additional boards to connect the modules to the cathode plane assemblies were screwed into the last profile on the CPA-side of the module. This system is also described in Section 4.2.4. A fully assembled module is shown in Figure 4.10.

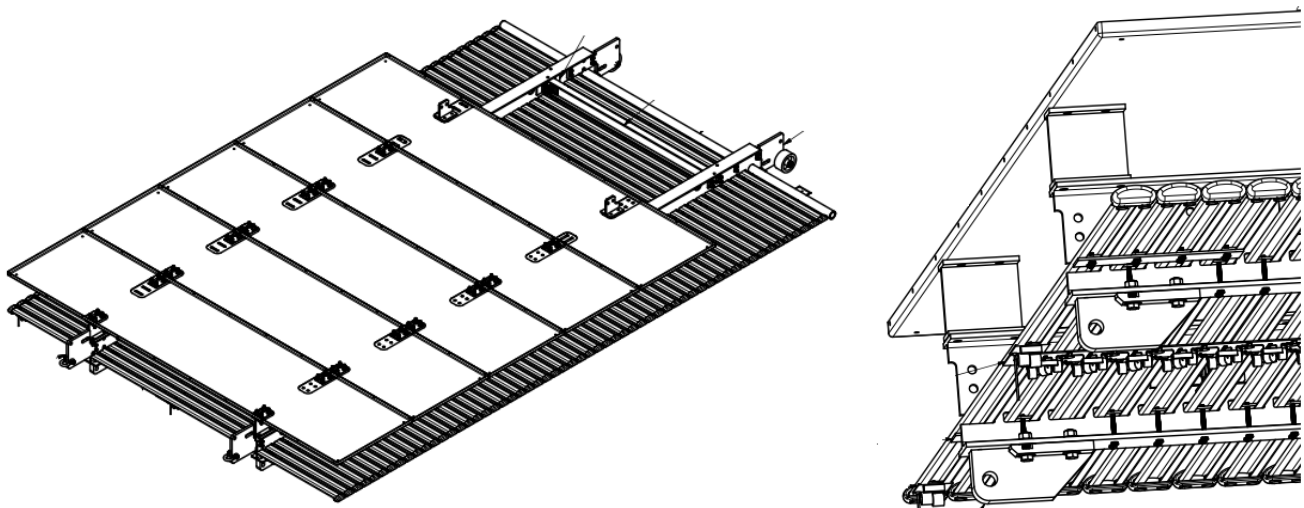


Figure 4.10: The fully assembled modules with ground planes are shown (left), as well as a close up of a CPA end as viewed from the bottom (drift) side of the module.

Between any two adjacent nodes of the resistor divider chain are two $5\text{ G}\Omega$ resistors, and three serially connected metal oxide varistors (MOVs) in parallel. The nominal voltage drop is 3 kV between each node. An open resistor on the divider chain would approximately double the voltage across the remaining resistor to 6 kV . This will force the varistors in parallel to that resistor into conduction mode, resulting in a voltage drop of roughly 5 kV ($1.7\text{ kV} \times 3$), while the rest of the divider chain remains linear, with a slightly lower voltage gradient. Because the damage to the divider would be local to one module, its impact to the TPC drift field is limited to region near this module. This is part of the intention of the modular design. An example of a simulated E field distortion which would be caused by a failed resistor is shown in Figure 4.11.

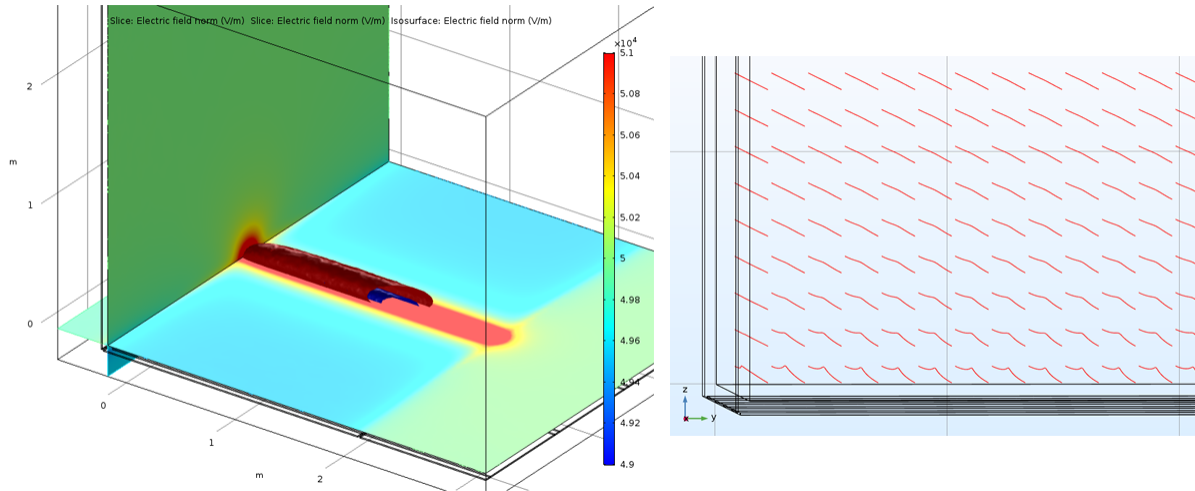


Figure 4.11: Simulated E field distortion from one broken resistor in the middle of the voltage divider chain on one bottom field cage module, emphasizing the need for redundancy. Left: Extent of E field non-uniformity in the active volume of the TPC. the green planes mark the boundaries of the active volume inside the field cage. The partial contour surfaces represent the volume boundaries where E field exceeds 5% (dark red, contains less than 100 kg of LAr) and 10% (dark blue, contains less than 20 kg of LAr) of the nominal drift field. Units are V m^{-1} in the legend. Right: electron drift lines connecting the CPA to APA in a bottom/end wall field cage corner. The maximum distortion to the field line is about 5 cm for electrons starting at mid drift at the bottom edge of the active volume.

The effect of the non-uniformity in resistor values can also be scaled from this study. A 2% change in a resistor value (1% change from the $2R$ in parallel) would give about 1.5% of the distortion from a broken resistor, i.e. less than 1 mm of transverse distortion in track position, with no noticeable drift field amplitude change inside the active volume.

4.2.3.3 Endwall field cages (EWFC)

Each of the four drift volumes has two endwall FCs, one on each end. Each endwall FC is in turn composed of eight endwall FC modules. There are two different types of endwall FC modules, each of which comes in a *regular* and in a *mirrored* configuration to account for mounting constraints and to match the detector geometry. Figure 4.12 illustrates the layout for the topmost and the other panels, respectively.

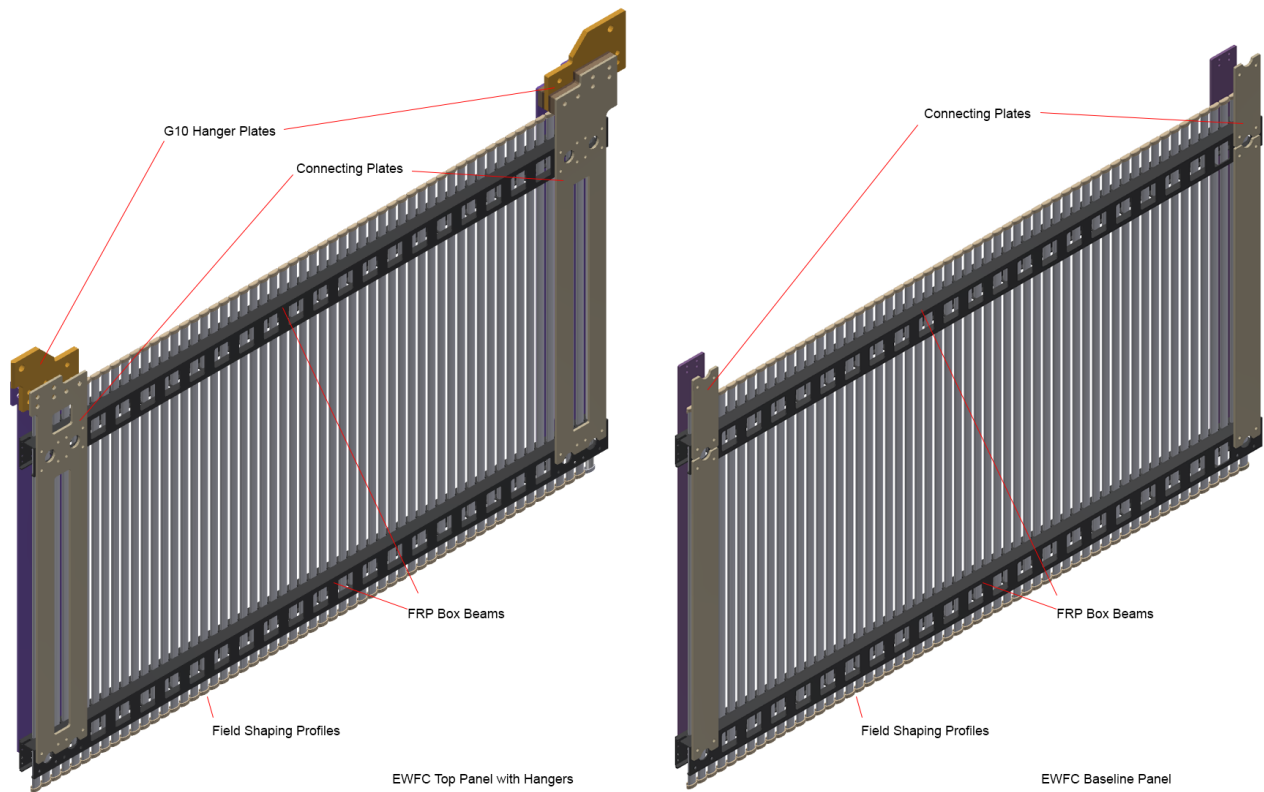


Figure 4.12: Left: Uppermost panel of the endwall FC. Right: Non-uppermost endwall FC panel.

Each endwall FC module is constructed of two FRP box beams which are 3.5 m long. The box beam design also incorporates cutouts on the outside face to minimize charge build up. Box beams are connected using 1.27 cm (0.5 in) thick FRP plates. The plates are connected to the box beams using a shear pin and bolt arrangement. The inside plates facing the active volume are connected using special stainless steel slip nuts and stainless steel bolts. The field-shaping profiles are connected to the top box beam using stainless steel slip nuts, an FRP angle, and two screws each. The profiles are connected to the bottom box beam with a slip nut that is held in place by friction.

4.2.4 Electrical Interconnections

Electrical interconnections are needed among the HV delivery system, CPA planes, FC modules, and termination boards on the APA modules, as well as between resistive dividers and the field-forming elements on the cathode plane assemblies and FCs. Redundancy is needed to avoid single points of failure. Some connections must be insulated in order to avoid creating a discharge path that might circumvent the discharge mitigation provided by the resistive CPA surface and FC partitioning. Certain connections must be flexible in order to allow for FC deployment, thermal contraction, and motion between separately supported cathode plane assemblies. Figure 4.13 shows a high-level overview of the interconnections between the HV, CPA, and FC modules.

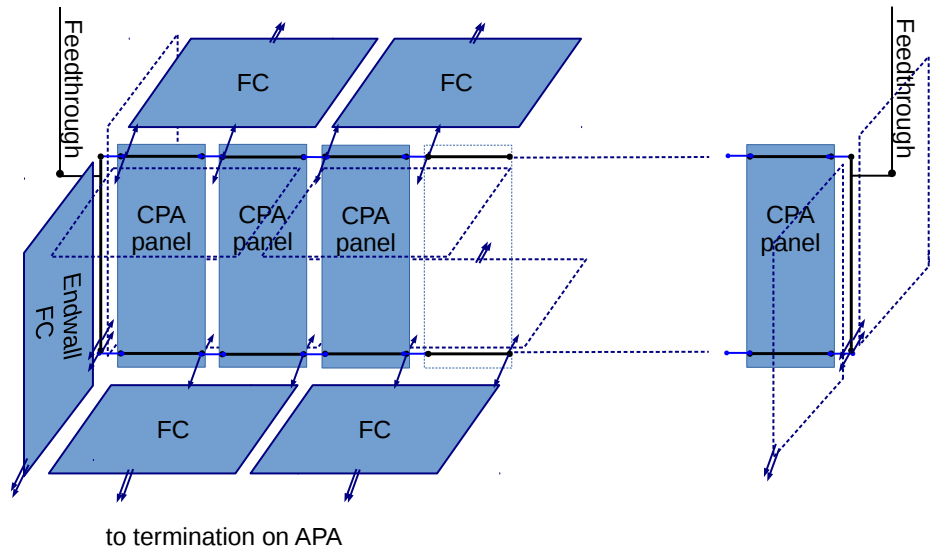


Figure 4.13: High-level topology of the HV interconnections

High voltage feedthroughs connect to cups mounted on the CPA frame that attach to a HV bus running through the cathode plane assemblies. HV bus connections between CPA panels are made by flexible wires through holes in the CPA frame. The HV bus is a loop in order to mitigate risk of a single point failure; feedthroughs at each end of each CPA plane mitigate risk of a double-break failure. Voltage dividers on each CPA panel bias the field shaping strips and the resistive dividers on the top and bottom FCs. CPA-to-FC connections are made using flexible wire to accommodate FC deployment. To further increase redundancy, two CPA panels connect to each top or bottom field cage, and two connections are also made to each endwall FC. Resistor divider boards attach directly to the interior side of the FC profiles with screws. A redundant pair of flexible wires connects a circuit board on the last profile of each FC to a bias-and-monitoring board mounted on the corresponding APA.

Short sections of flexible wire at the ends of each HV bus segment attach to screws in brass tabs on the CPA resistive panels (CPA RPs). Vertical HV bus segments on the outer ends of each CPA plane connect the top and bottom HV buses to complete the loop. Solid wire is used to connect resistive panels within a CPA panel.

Each FC module is as electrically independent as possible in order to mitigate discharge. However, only the bottom module of each endwall can make connections to the HV bus and APA, so each endwall module is connected to its upper neighbor at its first and last profiles using metal strips.

All flexible wires have ring or spade terminals and are secured by screws in brass tabs. Spring washers are used with every electrical screw connection in order to maintain good electrical contact with motion and changes of temperature.

Table 4.4 summarizes the interconnections required.

The redundancy in electrical connections described above meets requirement (6). The HV bus and interconnections are all made in low field regions in order to meet requirement (2). The HV bus

Table 4.4: HV System Interconnections

Connection	Method
HV cup to HV bus	wire to screw in HV cup mount on CPA frame
HV bus between CPA panels	wire between screws in brass tabs
HV bus to FSS	wire to circuit board mounted on FSS
FSS to top FC and bottom FC	wire to circuit board on first FC profile, two per FC module
HV bus to endwall FC	wire to circuit board mounted on first FC profile, two per endwall
FC divider circuit boards	directly attached to profiles using screws
FC to bias and monitoring termination	redundant wires from board mounted on last FC profile
HV bus to CPA panels	brass tab on CPA resistive panel
CPA RP interconnections	solid wire between screws in brass tabs
Endwall FC module interconnections	metal strips, first and last profiles only

cable is rated at the full cathode HV such that even in case of a rapid discharge of the HV system no current can flow to the cathode or FC except at the intended contact points, preserving the ability of the resistive cathode and FCs to meet requirement (5).

4.3 Production and Assembly

4.3.1 Power Supplies and Feedthroughs

Power supplies will be commercially procured, for example through Heinzinger. The HV cable is commercially available.

The power supply is tested extensively along with the controls and monitoring software. Features to be included in the software are:

- The ability to ramp, or change the voltage. The rate and an ability to pause the ramp shall be included. In previous installations, the ramp rate was typically between 60 to 120 V/s.
- An input for a user-defined current limit. This parameter is the current value at which the supply reduces the voltage output to stay below the current limit. The current-limiting is done in hardware.
- An input for a trip threshold. At this current reading, the program would reduce the voltage output through software. In previous experiments, the trip function in software would set the output to 0 kV.

Additionally, the software should record the current and voltage read-back values with a user-defined frequency, as well as any irregular current or voltage events.

The HV feedthroughs, filters, and splitter are custom devices. One feedthrough option is to use the ProtoDUNE-SP design and similar procurement. HV splitters are already on hand if they are desired.

4.3.2 Cathode Plane Assemblies

The component parts of the CPA are produced by commercial vendors for the following items:

- manufactured FR4 RP frames packed into three CPA unit kits making up a CPA panel,
- carbon-impregnated Kapton coated resistive panels (RPs) and FSS,
- HV cable segments and wire jumpers making up the CPA HV bus and RP interconnects,
- machined brass tabs for connecting RPs, HV Bus, and FSS, and
- top, bottom, and exterior edge profiles and associated connection hardware.

The above items are packaged into CPA panel kits by the vendors and are sent to the assembly factories, the locations of which will be determined later. The basic construction unit for an assembly factory is a pair of CPA panels so that shipment to SURF from an assembly factory consists of two CPA panels that are paired on site to form a CPA plane.

The most basic element of the CPA is an RP mounted in a machined slot in the top, bottom and sides of FR4 frames. There are three different types of these CPA RP elements – an upper, which has as its top frame the CPA mounting bracket and top FC hinge, a middle, and a lower, which has as its bottom frame a bottom FC hinge. Two such CPA RP elements are bolted together and pinned to form a shipment CPA unit of size 1.2m × 4m. These CPA units are assembled horizontally on a smooth, flat table to meet the dimensional requirements of CPA construction. In addition to the frames and RPs, FSS strips are mounted on the exposed sides of the FR4 frames, aluminum profiles are attached to the top and bottom of the upper and lower elements, and cables are attached to the RPs to form segments of the HV bus. The shipment CPA unit comes in three varieties in order to make a full 12m tall CPA Panel. These are : (1) an upper CPA RP element attached to a middle element, (2) two middle elements connected, and (3) a middle element attached to a lower element. The CPA unit order in the shipping crate from top to bottom is middle-and-lower, middle-and-middle, and upper-and-middle. For the 10kt SP module, there are 100 upper elements, 100 lower elements and 400 middle elements that make up the 100 CPA panels of the TPC. A comparison of a 6m ProtoDUNE-SP CPA panel and a 12m ProtoDUNE-SP panel is shown at Ash River Laboratory in Minnesota, USA, in Figure 4.14.



Figure 4.14: A 12 m DUNE-SP CPA mockup panel and a smaller 6 m ProtoDUNE-SP panel mockup at Ash River.

4.3.3 Field Cages

4.3.3.1 Top and Bottom Field Cages

The FRP and FR4 components of the top FCs and bottom FCs will be commercially produced by firms that specialize in the machining of fiberglass components for electrical applications, as was successfully done for ProtoDUNE-SP. All parts are machined in the absence of water and cleaned with a lacquer thinner. Machined edges, other than small circular holes, are coated with translucent epoxy. The stainless steel and aluminum components will be produced in local university and commercial machine shops. Voltage divider boards and FC and CPA connection boards will likely be fabricated by university groups.

The FRP frame assembly primarily consists of fastening together FRP I-beams with FRP threaded rods and hex nuts, which are secured with a limited and specified torque, to avoid damage to the threads. A detailed view of one of these connections is shown in Figure 4.15.

Prior to sliding each profile into the FRP frame, the holes should be covered with Kapton tape to avoid damage to the profile coating. An end cap is attached to each profile using plastic rivets, and then the profiles are aligned against an alignment fixture running the length of the FC. After securing each profile to the frame, the tension in the mounting screws is adjusted to remove any angular deflection in the extended portion of the profile.

The ground planes are attached to the 10 cm stand-off I-beam sections with threaded rods and a machined plate. The copper strips are connected to adjacent modules at the same locations. Care must be taken to avoid bending the corners of the GPs toward the profiles, particularly on the

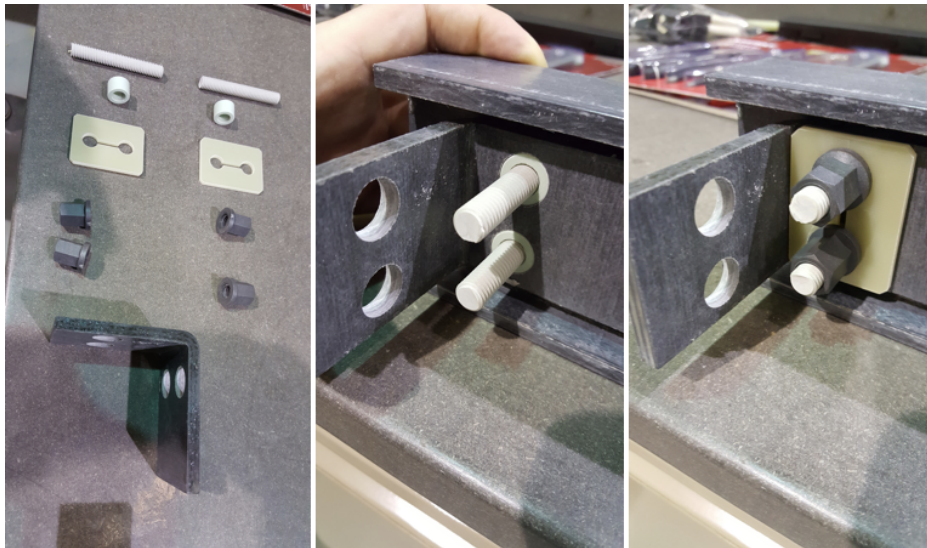


Figure 4.15: The above figure shows the procedure for connecting the cross beams to the main I-beams for the top FC. Left: The components of each connection, which (from top to bottom) are the threaded rods, the spacer tubes, washer plates, the hexagonal nuts, and an L-shaped FRP brace. An intermediate stage (middle) and final stage (right) of the assembly are also shown."

CPA side of of the module.

4.3.3.2 Endwall Field Cages

All FRP plates are commercially cut to shape by water jet. The cut outs in the FRP box beams are also cut by water jet. Holes that accommodate G10 bushings are reamed in a machine shop. FRP frames are pre-assembled to ensure proper alignment of all FRP parts and matching of holes. The profiles are not inserted at this stage. The FRP modules are hung off of each other by means of interconnecting FRP plates to ensure accurate alignment.

Next, parts are labeled and the frames are taken apart. All components are cleaned by pressure washing or ultrasonic bath. All cut FRP surfaces are then coated with polyurethane, which contains the same main ingredient as the FRP resin, allowing it to bond well to the FRP fibers. Final panels are constructed from cleaned and inspected parts. In order to ease assembly, which requires access to both sides of a module, a dedicated assembly table has been manufactured that allows convenient module rotation.

Figure 4.16 shows a partially assembled endwall FC FRP frame on the assembly table.

The FRP box beams are sandwiched between 1.27 cm (0.5 in) thick FRP panels which are held on one side by means of G10 bushings and rods with square nuts as shown in Figure 4.17. On the other side M10 stainless steel bolts engage with large slip nuts that are inserted into the Al profiles. The profiles are pulled towards a 2.5 cm thick FRP plate (red in Figure 4.17) on the inside of the box beam.

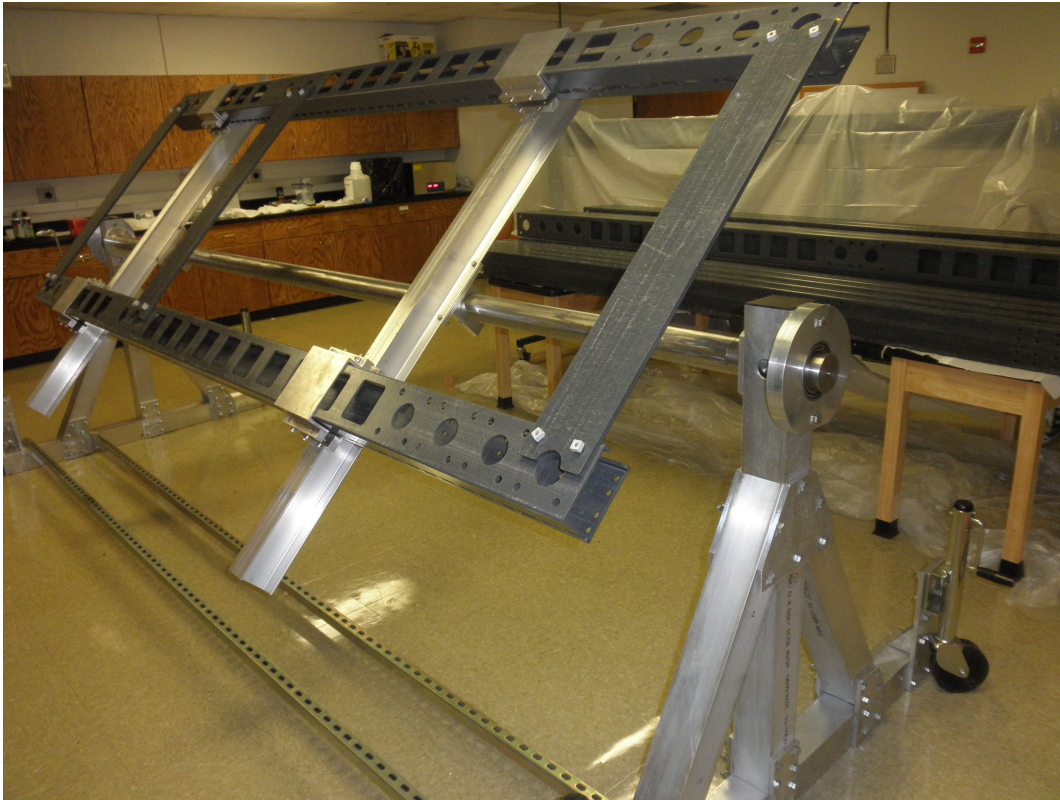


Figure 4.16: Assembly table with partially assembled endwall FC module (Credit: LSU)

Aluminum profiles are inserted into the cutouts of the box beams and attached with screws and stainless steel slip nuts to brackets that are mounted on the FRP box beams. After this, the resistive divider boards are mounted to the profiles using brass screws that engage with stainless steel slip nuts inside the profiles.

4.3.4 Electrical Interconnections

All electrical fasteners and wires used on the CPA and FC are produced to specification by commercial vendors and packaged with the CPA or FC modules. As discussed above (4.3.2, 4.3.3), this includes the HV cable segments, as well as wire jumpers, machined brass tabs, etc.

Circuit boards for HV interconnections are produced and tested at the university shops according to the same design used for ProtoDUNE-SP. The FC voltage dividers were produced for ProtoDUNE-SP at Louisiana State University, and the boards for CPA frame bias and CPA-FC connections were produced at Kansas State University. Both institutions have created custom test apparatus for verifying proper operation of the boards at full voltage and over-voltage conditions. Production and testing could be scaled up by the required order of magnitude at these institutions, or shared with other institutions, whichever best meets the needs of the project. Each board is free of solder flux and flux-remover.



Figure 4.17: Top and center endwall FC module frames hanging. (Credit: LSU)

4.4 Installation, Integration and Commissioning

4.4.1 Transport and Handling

The power supply, cables, filters, and feedthroughs are sent to the site in standard shipping crates. Handlers wear gloves when handling insulators that are between HV and ground. Surfaces can be cleaned with alcohol and allowed to dry.

CPA panels are shipped in crates to the SURF site. The 12 m CPA panels are disassembled into their three CPA units, loaded into the crates with all hardware needed to complete the CPA panel assembly at the SURF site. Each shipment should consist of two crates which contain the two CPA panels that will be paired to form a CPA plane. There will be very little room for storage at the SURF site, so it is important to ship CPA panels in this way so that final assembly, integration, and installation can proceed as soon as components are received.

Top FC and bottom FC modules will either be fully assembled at university production sites and shipped to SURF ready for installation into the mine, or the components will be fabricated and quality control (QC) inspected at university sites before being shipped to SURF for final assembly, as was done for the ProtoDUNE-SP modules at CERN. Crate design for top FC and bottom FC modules will depend strongly on whether the GPs remain attached to the modules, as in the ProtoDUNE-SP design, or if the GPs are, instead, connected directly to the cryostat. In the former case, if fully assembled top FCs and bottom FCs modules with attached GPs are transported to the underground area, the complexity of the crates is significantly enhanced, as it is difficult to fully support a module on all sides while allowing for tipping of the crate. Hence, it may be necessary for GPs to be installed underground in either design scenario. Thus far, only single fully assembled top FCs and bottom FCs modules have been crated for shipment, but more complex designs that will allow for multiple modules (without installed ground planes) will be developed.

The endwall FCs sections each consisting of eight modules are shipped in two separate shipping crates each containing four modules in an upright and vertical orientation. As was done for ProtoDUNE each endwall FCs module will be individually wrapped in plastic and can be extracted from the crate by means of an overhead crane and spreader bar. Extracted modules will be rotated into horizontal position using the ledge on a dedicated assembly table. The module side showing steel bolts should be on top for final QC.

The HV bus segments, FSS bias boards, and interconnection wires will be integrated with the CPA units before shipment, while CPA panel interconnections and FSS connection tabs will be packaged and shipped with the CPA panels for integration on site. FC divider boards will be attached to FC modules during FC assembly as described in 4.3.3. The CPA-to-FC and FC-to-APA boards will be shipped separately and attached just before each FC is hoisted onto its CPA panel in order to avoid risk of damage to exposed boards on the ends of the FCs during shipment and handling.

4.4.2 Installation and Integration

Upon arriving at the SURF site, The CPA shipping crate is unpacked with the middle/lower CPA unit placed in a vertical stand on the floor of the so-called toaster region, an area in the DUNE detector cavern between the cryostat endwall and the cavern wall set aside for installation functions. Next, the middle-middle CPA unit is removed and vertically attached to the middle-lower Unit. Finally, the upper-middle CPA unit is removed and attached. This assembly makes up a CPA panel. The CPA panel is lifted and vertically attached to its trolley with an FR4 hangar. Two CPA panels are paired to form a CPA plane which then forms the unit for attachment of the FCs. Figure 4.18 shows on the left a two-Panel CPA plane mounted on its trolleys in the clean room at ProtoDUNE-SP, waiting for installation of the top FC and bottom FC units.

It should also be noted that the CPA panels on each end of each CPA array are special – they have aluminum profiles along the exterior side to form the first element of the field cage. They also contain parts of the HV bus mounted on the CPA frames. The HV bus forms a continuous loop from the HV Input through the top of the 25 CPA planes, down the far external side, back along the bottom and up the external side back to the HV Input.



Figure 4.18: Left: Completed ProtoDUNE-SP CPA plane ready for FC attachment. Right: Two completed CPA-FC assemblies in the ProtoDUNE-SP cryostat. The top and bottom FCs with their GPs attached are visible to the right of the cathode plane in their folded-up pre-installation position.

There are a total of 50 CPA panel pairs (CPA planes) arranged in the SP module in two rows of 25 each. After the panels are paired, FC units are attached folded against the CPA and the full CPA-FC assembly is placed in the SP module cryostat through the access door. Figure 4.18 shows on

the right two completed CPA-FC assemblies on their beam in the ProtoDUNE-SP cryostat. Upon deployment of the folded top and bottom FC units, and after the final endwall FC installations, the TPC FC is complete.

To assemble the endwall FC, the modules are rotated vertically in the assembly area, then placed in a stand designed to hold the 120 kg pieces vertically. The top FC is lifted and moved above the next module in the vertical stand where the two are bolted together and any electrical connections are made. The two modules are then lifted up and aligned above the following module. The modules are again bolted, electrically connected and raised and aligned above the next piece. This process is repeated until all eight modules are hanging together. Once the bolting and electrical connections have been completed on the last piece, the continuity of all the grounding connections of the endwall FC are checked.

The completed endwall FC section is then moved over to the installation beam where its spreader bar is attached to the installation system. It is then rolled into the cryostat and located on the appropriate beam for installation into the TPC.



Figure 4.19: Completed endwall in process of installation into ProtoDUNE-SP cryostat.

4.4.3 Interfaces

Among TPC components there are internal interfaces between the CPA and FC; the CPA and HV, and the FC and HV. In addition there are significant interfaces with systems from other consortia.

The interfaces with the HV system include the electrical connections with the HV cup, HV bus, and FC, interconnecting the panels within the CPA, and propagating the HV bus between adjoining cathode plane assemblies. A selection of the mechanical interfaces are as follows:

- Metal contact plates on the cathode surface at each corner, with two captive screws in each, used for making electrical contact with the HV bus and the resistor board for the frame field strips;
- Through holes for the 3 mm diameter cable in the sides of each frame adjacent to the contact plates to allow interconnection of the HV bus between cathode plane assemblies;
- A means of securing the HV bus cable in place;
- Through-holes near the centers of the top and bottom frames for connecting the top FC and bottom FC elements to the cathode, with corresponding metal contact plate on the cathode surface;
- Between the CPA and the FC the interface at the hinge joint ensures that the CPA and FC are properly located relative to each other.

Since these interfaces occur within the design group that is constructing the TPC there is close coordination and communication between the CPA, FC and HV groups to ensure that all requirements are met and that the components all fit together.

The interfaces between the CPA system and the HV system, and the interfaces among the CPA-FC-HV systems are shown in integration drawings and documented in the project documentation system.

The various components in the HV system also have interfaces with components from other systems. These interfaces are formally defined by interface documents.

Key interfaces between the HV and other systems are summarized in Table 4.5.

4.5 Quality Control (QC)

Power supplies used in a SP module will be tested before installation. Output voltages and currents must be checked on a known load.

The feedthrough and filters should be tested at the same time, preferably with the planned power supply. The feedthrough must be tested to hold the required voltage in TPC-quality LAr ($\tau \geq 1.6$ ms) for several days. The ground tube submersion and E field environment of the test setup should be comparable to the real field cage setup or more challenging (e.g., the test liquid level can be lower than that in the SP module but not higher). Additionally, the feedthrough must be leak-tight to satisfy cryogenics requirements.

Table 4.5: Key HV System Interfaces to Other Systems

Interface to	Description
DSS	Support, positioning, and alignment of all CPA, FC modules inside the cryostat both warm and cold
APA	FC support (top, bottom, and end wall) on APA frames; Mounting of field cage termination filter boards and FC failsafe terminations; Mounting of the electron diverter boards.
TPC Elec.	FC termination wire connectors on CE feedthrough flange, FC termination wires routed with CE cables
PDS	Mounting of PD calibration flash diffusers and routing of their fibers to cathode plane assemblies; Possible TPC coated reflector foil on CPAs.
Facility	Locations and specifications of the HV Feedthrough ports; gas and LAr flow velocities and patterns.
Calibration	FC openings for the calibration laser heads
Cryogenic Instrumentation & Slow Control.	HV vs. LAr level interlock, sensor locations in high field regions, cold/warm camera coverage, HV signal monitoring, etc.
Integration Facility	Storage buffer, inspections/tests, repackage for underground delivery
Physics / Software	Requirements: range of operating drift field, uniformity of the drift field; Supply detector geometry and E field map.

CPA QC consists of forms that are filled out as part of the various procedures from initial assembly at factories to the final testing of connections in the DUNE cryostat. A group of QC forms filled out during initial panel unit assembly travels in the shipping crate with the panel. At SURF, CPA panel and CPA plane assemblies have their own set of QC forms for CPA assembly and for CPA-FC integration. Finally, before top and bottom FC deployment, a final check of all electrical connections on the CPA and between the CPA and the top, bottom, and endwall FCs is completed.

Before assembly and shipment of top FC and bottom FC, each FRP component is subjected to inspection. Each of the beams is checked for flatness, torsion, and structural and surface defects, such as cracks or fractures, layer separation, thermal decomposition, and evidence of water-induced bloating. Any scratching or grooving of the surface layer can be remediated by coating with commercially available epoxy.

For the endwall FCs, each box beam and all FRP stock will be inspected prior to assembly for dimensions, deformations, surface scratches and delamination defects. If the inspection is not passed, the parts will be rejected. Preliminary assembly of endwall FCs modules will take place in a high-bay area under full crane access. After assembly, individual endwall FCs modules will be hung off each other in pairs of two to test the interconnections of the modules. Hanging will be performed in a top-down sequence consistent with space constraints (maximum three at once). This process will be repeated for all endwall FCs. All parts will be labeled to uniquely identify their position. After disassembly, all parts are cleaned before being moved into the clean room, where they will be inspected again. Final assembly will occur in a dedicated clean laboratory space.

Each panel will undergo mechanical and quality control tests before shipping. Electrical QC tests will be performed after assembly of all aluminum profiles and resistor divider chains and again prior to installation of the endwall FCs into the cryostat. These tests will be performed with a pico-ammeter to measure the nominal resistance between profiles while grounding neighboring profiles not involved in any particular measurement.

Once at SURF, all endwall FCs panels shall be inspected visually after unpacking and prior to installation. Electrical tests will be repeated at various stages of the staging and installation process. The tests will be again be performed with a pico-ammeter to measure the nominal resistance between profiles while grounding neighboring profiles.

During electrical interconnections local assembly, quality control inspection checklists for CPA, FC, and interconnections will be adapted from ProtoDUNE-SP checklists for CPA panels, HV bus segments, interconnection wires, and resistor boards. These checklists include physical inspection for defects and resistance tests. For maximum traceability, checklists may be both filed in an electronic logbook and sent in hard copy along with the components tested.

For the electrical interconnections QC at SURF, expected resistances have been modeled at all stages of CPA+FC integration. The height of the cathode plane assemblies make it best to catch a faulty connection as early as possible. This will be achieved by quickly checking resistances for expected values between CPA panels and between CPA panels and field strips as CPA unit subassemblies are added. Profile-to-profile field cage resistances will be checked upon reception and rechecked immediately before attaching to cathode plane assemblies underground. Once all four FCs are attached to a CPA, resistances between selected FC profiles and the HV bus will be measured, checked against expected values, and recorded. Continuity of the HV bus between cathode plane assemblies will be checked at top and bottom as each CPA is connected to its neighbor inside the cryostat.

4.6 Safety

Safety is central to the design of the HV system. In all phases including fabrication, installation, and operations, safety will be the highest priority. There will be documented assembly, testing, transport, and installation procedures. Particular attention was paid to these topics in the design of ProtoDUNE-SP with explicit concern to a design that is identical to the SP module design, the most critical of which are also noted in the preliminary HV risk assessment, which is under development.

The structural and electrical designs for the single-phase (SP) HV are based on designs that were vetted and validated in the ProtoDUNE-SP construction, which is currently in its final phase of deployment at CERN. Previously, Fermilab HV tests implemented a full-voltage and full-scale HV feedthrough, power supply, filtering, and monitoring system, along with the HV connection cup and arm, after completing full safety reviews. These devices worked as designed and are essentially reproduced in both ProtoDUNE-SP and the SP module.

When operating the FC at its full operating voltage there is a substantial amount of stored energy. The design of the CPA is centered around storing charge at the highest voltage on a resistive surfaces to limit the power dissipated during a power supply trip or other failure which unexpectedly drops the HV. This design has been successfully tested at full voltage over 2 m^2 surfaces at full voltage and will soon be tested at larger scale in ProtoDUNE-SP.

Integral to the SP FC design, both in ProtoDUNE-SP and the SP module, is the concept of pre-assembled modular panels of field-shaping conductors with individual voltage divider boards. The structural design and installation procedures used in ProtoDUNE-SP were selected to be compatible with use at the Far Detector site and were vetted by project engineers, engineering design review teams, and CERN's safety engineers. Some revisions to these designs are expected based on lessons learned in installation and operations; these revisions will be reviewed both within the Project and by Fermilab ES&H personnel. The overall design is on solid footing.

Assembly of the FC panels and resistor-divider boards will involve collaboration technical, scientific, and student labor and does not present unusual industrial hazards. The HV consortium will work closely with each assembly site to ensure that procedures meet both Fermilab and institutional requirements for safe procedures, personal protective equipment, environmental protection, trained materials handling, and training. The vast majority of production part fabrication will be carried out commercially and shipping will be contracted through approved commercial shipping companies. Prior to approving a site as a production venue, each site will be visited and reviewed by an external safety panel to ensure best practices are in place and maintained.

4.7 Organization and Management

4.7.1 HV System Consortium Organization

The consortium consolidates all the institutions that are participating in the design, construction and assembly of the HV systems for both ProtoDUNE-SP and ProtoDUNE-DP. It is currently composed of US institutions and CERN, presently the only non-USA participant. As in the case of ProtoDUNE, CERN is heavily committed to a significant role in terms of funding, personnel, and the provision of infrastructure for R&D and detector optimization. Moreover, CERN will be responsible for a significant fraction of subsystem deliverables; as such it is the intention of CERN to attract additional European institutions into the consortium. The consortium organization structure includes a leader (currently from CERN), a technical lead (currently from BNL), a technical design report (TDR) editor (currently from Fermilab), and a HVS design and integration lead (currently from ANL).

In the HV consortium organization, each institution is naturally assuming the same responsibilities as for the developments of ProtoDUNE-SP. The consortium is organized into working groups addressing the design and R&D phases and the hardware production and installation.

- WG1. Design optimization for SP module and DP module; assembly, system integration,

detector simulation, physics requirements for monitoring and calibrations.

- WG2. R&D activities, R&D facilities.
- WG3. SP-CPA: Procurement, in situ QC, resistive panels, frame strips, electrical connections of planes; QC, assembly, shipment to assembly site; QC.
- WG4. dual-phase (DP) cathode.
- WG5. FC modules.
- WG6. HV supply and filtering, HV power supply and cable procurement, R&D tests, filtering and receptacle design and tests.

Merging of SP and DP groups is envisaged for the working groups where synergies are being identified: HV feedthroughs, voltage dividers, aluminum profiles, FRP beams, and assembly infrastructure.

4.7.2 Planning Assumptions

The present baseline design for all elements of the SP module (CPA, top/bottom top FC, bottom FC, endwall FC and HV distribution) follows the ProtoDUNE-SP design as it has been produced and is being assembled. It is also assumed that no major issues in the HV operation of ProtoDUNE-SP will be encountered and therefore that the basic HV concepts are sound.

However some design modifications/simplifications are envisaged to be implemented to take into account the different height of the CPA and the endwall FC modules and to adapt the installation procedure to the underground environment.

Additional design modifications could be expected if the ProtoDUNE-SP test run (as well as tests at Fermilab using the 35 t cryostat) identifies weaknesses in the present baseline option.

ProtoDUNE-SP is the testbed to understand and optimize detector element assembly, installation sequence, integration as well as requirements in manpower, space and tooling, and schedule.

4.7.3 High-level Cost and Schedule

Table 4.6: DRAFT- HV system R&D program and Milestones to lead to CD-2 approval.

WBS	Task Name	Start	Finish
1.5	CD-2 DOE Review	10/4/19	10/4/19
7	HV system		
7.1	Finalize SP FC design	06/27/18	09/30/19
7.2	Finalize SP cathode design	06/27/18	09/30/19
7.3	Run SP HV design integration test	01/01/18	12/31/19
7.4	HV TDR - submit for internal review	03/29/19	03/29/19
7.5	CPA procurement	09/21/21	12/06/22
7.6	ground plane procurement	08/08/22	12/06/22
7.7	Assemble and test voltage dividers	08/08/22	12/06/22
7.8	FC procurement	03/11/22	12/06/22
7.9	Production readiness reviews	01/02/23	01/07/23
7.10	Cryostat ready for TPC installation	05/01/23	05/01/23
7.11	CPA assembly	01/31/23	07/25/23
7.12	Top-bottom FC assembly	01/31/23	07/25/23
7.13	Endwall FC assembly	01/05/23	04/23/23

Chapter 5

Photon Detection System

5.1 Photon Detection System (PDS) Overview

5.1.1 Introduction

The photon detection system (PDS) is an essential subsystem of a DUNE SP module. The detection of the prompt scintillation light signal, emitted in coincidence with an ionizing event inside the active volume, allows the determination of the time of occurrence of an event of interest with much higher precision than charge collected from ionization in the TPC. This capability is most critical for the primary DUNE science objectives that are uncorrelated with the timing signal from the neutrino source at Fermilab, such as proton decay and neutrinos from a supernova neutrino burst (SNB), and for the ancillary science program including measurements of neutrino oscillation phenomena using atmospheric neutrinos. A number of scientific and technical issues impact the SP and DP PDS in a similar way, and the consortia for these two systems cooperate closely. See Volume 3: Dual-Phase Module, Chapter 5.

Timing information from the photon detector (PD) and TPC systems allows determination of the drift time of the ionizing particles. Knowledge of the drift time provides localization of the event inside the active volume and provides the ability to correct the measured charge for effects that depend on the drift path length, purity of LAr, or for specific locations in the detector if there are non-uniformities. This correction is important for the reconstruction of the energy deposited by the ionizing event. In addition to allowing optimum track reconstruction, scintillation light measured by the system may also be used as a trigger and for improved calorimetric measurement in combination with charge measurement.

Table 5.1 summarizes the high-level system performance requirements for the PDS necessary to achieve the DUNE science objectives. The first row provides a requirement to ensure high efficiency and good energy resolution for proton decay and atmospheric neutrinos. The second row targets core collapse SNB neutrinos, but specifies only a timing measurement for event localization

(in conjunction with the TPC drift time measurement). However, a consensus has emerged in the collaboration that the current requirements do not fully exploit the potential for LAr scintillation light to contribute to the energy reconstruction of events, in particular for lower energy events such as from SNBs (10-100 MeV). In response, the third row is a proposed requirement to measure the energy in scintillation light from SNB events near the peak of the spectrum (~ 10 MeV) with a precision similar to that of the ionization measurement. The combined measurement of ionization charge and scintillation light has been shown to improve the determination of the energy deposition of an event. Table 5.2 shows the corresponding photon detection light yield, timing and spatial separation requirements. To achieve a 10% calorimetric measurement with light requires approximately ten times higher light yield for the PDS than the original requirement.

To achieve these requirements, there is an ongoing intense R&D program to investigate methods that maximize the photon detection efficiency of the PDS within the constraints of the SP TPC design. All three of the photon collector options described in this chapter could meet the original performance requirements, albeit with different event efficiency, but one, the ARAPUCA, has highest potential to perform the low energy calorimetric measurements at the desired precision. It also has the highest efficiency for SNB events and provides higher spatial granularity for background rejection.

Table 5.1: PDS performance requirements to achieve the primary science objectives (under review).

Requirement	Rationale
The far detector (FD) PDS shall detect sufficient light from events depositing visible energy >200 MeV to efficiently measure the time and total intensity.	This is the region for nucleon decay and atmospheric neutrinos. The time measurement is needed for event localization for optimal energy resolution and background rejection.
The FD PDS shall detect sufficient light from events depositing visible energy <200 MeV to provide a time measurement. The efficiency of this measurement shall be adequate for SNB events.	Enables low energy measurement of event localization for SNB events. The efficiency may vary significantly for visible energy in the range 5 MeV to 100 MeV.
(Proposed) The FD PDS shall detect sufficient light from events depositing visible energy of 10 MeV to provide an energy measurement with a resolution of 10%.	Enables energy measurement for SNB events with a precision similar to that from the TPC ionization measurement.
The FD PDS readout electronics shall record time and signal amplitude from the photo-sensors with sufficient precision and range to achieve the key physics parameters.	The resolution and dynamic range needs to be adjusted so that a few-photoelectron signal can be detected with low noise. The dynamic range needs to be sufficiently high to measure light from a muon traversing a TPC module.

5.1.2 Design Considerations

Scintillation Light: LAr is known to be an abundant scintillator and emits about 40 photons/keV when excited by minimum ionizing particles[13], in the absence of external E fields. In the presence

Table 5.2: PDS performance requirements (under review).

Parameter	Value
(Current) Minimum detector response per MeV energy deposition (Light Yield).	1 pe/MeV for events at the center of the TPC and no less than 0.5 pe/MeV at all points in the fiducial volume.
(Proposed) Minimum detector response per MeV energy deposition (Light Yield).	10 pe/MeV for events at the center of the TPC and no less than 5 pe/MeV at all points in the fiducial volume.
Minimum requirements on energy deposition, spatial separation, and temporal separation from other events, for which the system must associate a unique event time (<i>flash matching</i>).	10 MeV, 1 m, 1 ms respectively.

of E fields the yield is reduced due to recombination; for the nominal DUNE SP module field of 500 V/cm the yield is approximately 24 photons/keV [14].

As depicted in Figure 5.1, the passage of ionizing radiation in LAr produces excitations and ionization of the argon atoms that ultimately results in the formation of the excited dimer Ar_2^* . Photon emission proceeds through the de-excitation of the lowest lying singlet and triplet excited states, $^1\Sigma$ and $^3\Sigma$ to the dissociative ground state. The de-excitation from the $^1\Sigma$ state is very fast and has a characteristic time of the order of $\tau_{fast} \simeq 6$ ns. The de-excitation from the $^3\Sigma$, state is much slower with a characteristic time of $\tau_{slow} \simeq 1.3$ μsec , since it is forbidden by the selection rules. In both decays, photons are emitted in a 10 nm band centered around 127 nm, which is in the Vacuum Ultra-Violet (VUV) region of the electromagnetic spectrum [15]. The relative intensity of the fast and slow components is related to the ionization density of LAr and depends on the ionizing particle: 0.3 for electrons, 1.3 for alpha particles and 3 for neutrons [16]. This phenomenon is the basis for the particle discrimination capabilities of LAr exploited by many experiments that have the capacity to separate the two components, for DUNE the greatest significance relates to a pending decision on treatment of light signals.

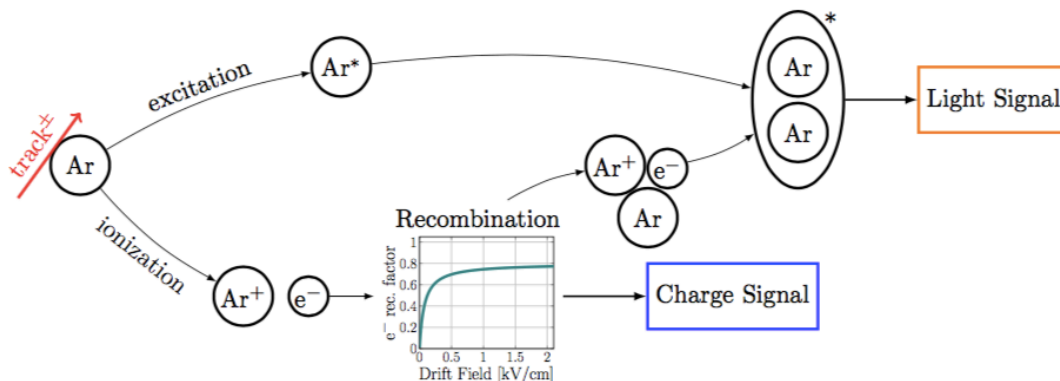


Figure 5.1: Schematic of scintillation light production in argon.

In massive LArTPCs, a cost-effective approach is to use photon collector systems that collect light from large areas and attempt channel it in an efficient way towards much smaller photosensors that

produce an electrical signal. This paradigm for the detection of LAr scintillation light depends on the use of chemical wavelength shifters since most currently available commercial (cryogenic) large area photosensors are not directly sensitive to VUV radiation, primarily due to the lack of transparency of fused silica and glass optical windows.

³⁹Ar: The long-lived cosmogenic radioisotope ³⁹Ar has a natural abundance with an activity of approximately 1 Bq/kg and undergoes beta decay with a mean beta energy of 220 keV with an endpoint of 565 keV. In the 10 kt FD modules this leads to a rate of more than 10 MHz of very short (~1 mm) tracks uniformly distributed throughout the detector module, each of which produces several thousand VUV scintillation photons. This continuous background impacts the data acquisition (DAQ), trigger and spatial granularity required of the PDS.

Wavelength Shifter: The most widely used wavelength shifter used in combination with LAr is tetra-phenyl butadiene (TPB)¹, which absorbs VUV photons and re-emits them with a spectrum centered around 420 nm, close to where most commercial photosensors have their maximum quantum efficiency for photoconversion. Though TPB has been utilized quite extensively with great success, there are recent publications that warrant caution. For example, until recently the conversion efficiency of TPB in coating was taken to be high, approaching or even exceeding 100% (possible by multi-photon emission), however a recent arXiv paper [17] refutes this previously referenced result. Using much of the same equipment but replacing a damaged reference photodiode, the authors (including an author of the previous paper) report a measurement for the quantum efficiency of 40% for incident 127 nm light. Another recent paper [18] reports that some methods used to coat surfaces with TPB suffered loss of the TPB coating in LAr, whereas there is no measurable effect if the fluor is dissolved in a polymer matrix. These developments will be followed carefully and highlight the importance of the ongoing R&D and prototype program.

Physical Constraints: The physical dimension of the PD system is constrained by the need to fit within the innermost wire planes of the anode plane assemblies (APAs) and to be installed through slots in the APA mechanical frame after it is wound (see Section 2.2). Individual PD modules will be restricted to be within an envelope in the form of a long, thin box. At the time of preparation of this proposal the dimensions were 14.6 cm × 9.6 cm × 212.7 cm, but it is anticipated that the size of the slot in the APA will be increased by about 25% (the long dimension of the modules will remain the same). There will be ten PD modules per APA, for a total of 1500 modules.

5.1.2.1 Photon Collectors

The core modular elements of the PDS are the large area photon collectors that convert incident 127 nm scintillation photons into photons in the visible range (>400 nm), which in turn are converted to an electrical signal by compact (silicon photomultipliers (SiPMs)). As detailed in Section 5.3, since the size and cost of currently available SiPMs are not well matched to meeting the performance requirements in the large-volume SP module, the photon collector design aims to maximize the active VUV-sensitive area of the PD module while minimizing the necessary photocathode (SiPM) coverage. In the following we will distinguish between the terms photon *collection* efficiency and photon *detection* efficiency (PDE). Collection efficiency is the number of

¹1,1,4,4-Tetraphenyl-1,3-butadiene, supplier: Sigma-Aldrich®, <https://www.sigmaaldrich.com/>.

visible photons delivered to the SiPMs divided by the number of VUV photons incident on the PD module active area; this parameter is used to report results of calculations or simulations of predicted device performance independent of the SiPM used. Detection efficiency is the number of detected photoelectrons from the SiPM(s) divided by the number of VUV photons incident on the PD module active area; this is generally the result of a direct measurement unless the detailed performance of the SiPM is known and divided out. The effective area of a PD module is another useful figure-of-merit that is defined to be the photon detection efficiency multiplied by the photon collecting area of a PD module.

Three different designs of PD photon collector modules have been developed and are being considered by the SP PD consortium. The baseline design, ARAPUCA², is a relatively new concept that is scalable and has the potential for the best performance of the three designs by a significant factor. It is functionally a light trap that captures wavelength-shifted photons inside boxes with highly reflective internal surfaces where they are eventually detected by SiPMs. There are also two alternative designs based on the use of wavelength-shifters and light guides coupled to SiPMs. Both have undergone more development than ARAPUCA, but their performance meets the basic physics requirements with only a limited safety margin and are not easily scalable within the geometric constraints of the SP module. Figure 5.2 shows a 3D model of the SP TPC with a zoom in to the anode plane where the three candidates photon collector technologies are visible for illustration – in the final detector module there will be a single type.

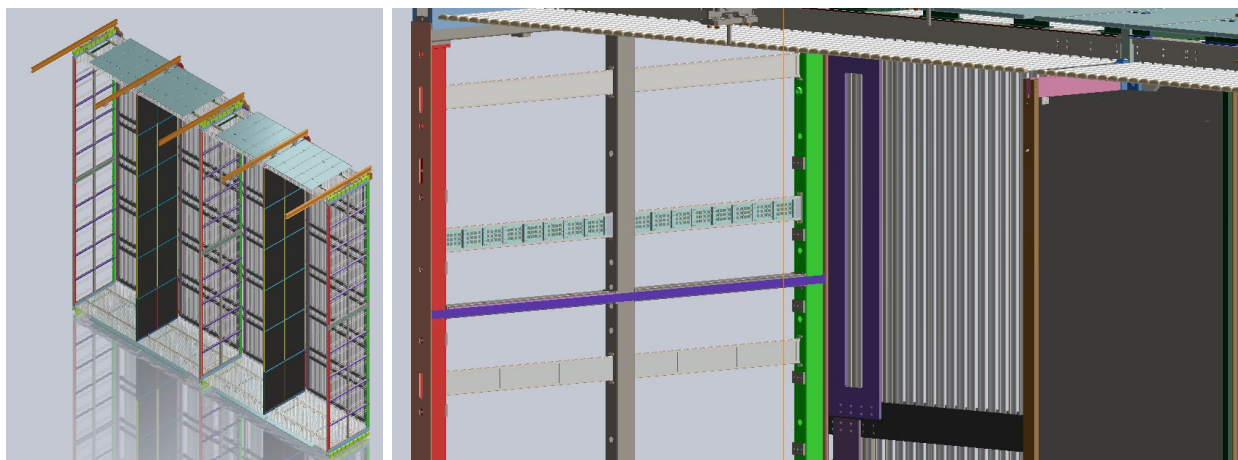


Figure 5.2: 3D model of PDs in the APA. The model on the left shows the full width of the TPC with the configuration APA-CPA-APA-CPA-APA. The figure on the right shows a zoom in to the top far side of the TPC where three candidates photon collector technologies are visible for illustration – in the final detector there will be a single type.

ARAPUCA Option: The first large-scale implementation of an ARAPUCA module, in ProtoDUNE-SP, is composed of an array of sixteen ARAPUCA cells each one acting as an individual detector element. This configuration allows for finer spatial segmentation along the detector bar than is the case for the light guide designs. The ProtoDUNE-SP ARAPUCA design collects light from one side of the box through an optical window formed by a dichroic filter deposited with a layer of pTP³ wavelength shifter on the external surface. This shifts the incident VUV light to a near-visible

²*Arapuca* is the name of a simple trap for catching birds originally used by the Guarani people of Brazil.

³p-TerPhenyl, supplier: Sigma-Aldrich®.

frequency that is able to pass through the filter plate to the interior of the box.

In the ProtoDUNE-SP version of the device, the inner surface of the box opposite the window houses an array of SiPMs that covers a small fraction of the area of the window (2.8-5.6%), surrounded by a foil of a highly reflective material coated with a second wavelength shifter, TPB. The TPB converts the light passing through the filter to a wavelength that is reflected by the filter. It has been shown in simulation and in prototypes that a large fraction of these trapped photons, reflecting from the filter and the lined walls of the box, will eventually fall on a SiPM and be detected. The X-ARAPUCA described in Section 5.3.1.3, is a promising variant of the concept that uses a wavelength shifter-doped plate between two dichroic filter windows with SiPMs on the narrow sides of the cell; in addition to viewing scintillation light from both sides as needed for the central APA, it is expected to provide a higher light collection efficiency.

The ARAPUCA concept is relatively recent – it was first proposed in 2015 and accepted for installation in ProtoDUNE-SP in mid-2016. A series of tests in LAr have been performed with an evolving prototype design that resulted in detection efficiency measurements ranging from 0.4% to 1.8%, demonstrating the potential for substantially higher performance than the light guide designs. Monte Carlo (MC) simulations show that detection efficiencies at the level of several per cent could be reasonably reached with improvements to the basic design. While the results of the experimental tests are encouraging, a deeper understanding of the optical phenomena involving emission and scattering on wavelength-shifter coated surfaces is needed to optimize the design.

Light Guide Options: The fundamental idea of this approach is to convert VUV scintillation light to visible wavelengths on (or near) the surface of an optical light guide, which then guides some fraction of the converted light by total internal reflection to SiPMs mounted on one or both ends of the guide.

Several approaches were investigated and narrowed down to the two most promising ones based a set of comparative measurements taken simultaneously in LAr [19]. These two have been improved over several years and have reached a reasonable level of maturity and reliability. The *dip-coated* light guides are pre-treated commercially-cut acrylic bars that are dip-coated with a solution of TPB, acrylic, and toluene. When the toluene evaporates it leaves a thin film of TPB embedded in the acrylic matrix on the surface of the bar. In the *double-shift* light guides, the conversion and guiding processes of the photons are decoupled. The first conversion is in a radiator plate, which is an ultraviolet transmitting UVT-acrylic plate coated with pure TPB through a spraying process. It is positioned just above a commercial WLS-doped bar that absorbs the blue light produced by TPB and re-emits it in the green; a fraction of this green light propagates down the bar.

Both bar designs have demonstrated attenuation lengths for the trapped light along the long dimension of the bar comparable to the length of the bars themselves, which ensures a reasonable uniformity along the beam direction. Preliminary measurements of both designs with readout at just one end indicate an photon detection efficiency range of 0.1% to 0.25% averaged along the length of the bar. Up to a factor of four higher detection efficiency might be achieved with straightforward enhancements, such as: SiPM at both ends of the bars; higher PDE SiPM; and coating the long edges of the bars with reflective foils.

5.1.2.2 Wavelength Shifter-Coated Cathode Plane

Since the PD modules are installed only on the anode plane, light collection is not uniform over the entire active volume of the TPC. A possible solution to improve this is to install a reflective foil coated with wavelength shifter on the cathode. This would increase the light yield of the detector and could enable calorimetric measurements based on light emitted by the ionizing particles. It may also be possible to remove the ^{39}Ar background through PD-supplied timing cuts, a background that may otherwise cause a huge counting rate for events near the anode plane. This option would require good visible light sensitivity for the photon collectors, which is not the case for current light collector options. The capability could be incorporated in a variety of ways but with an impact on the direct light measurement. This option has yet to be formally adopted by the PD consortium but is under study through MC simulations and the mechanical feasibility is being discussed with the high voltage (HV) consortium.

5.1.2.3 Silicon Photosensors

In each photon collector concept, the final stage of converting a visible wavelength photon into an electrical signal is performed by a SiPM. The device must operate reliably for many years at LAr temperatures. Experience with a promising early candidate that failed in later batches, due to an unadvertised change in the fabrication process, emphasizes the importance of a multi-source approach with active engagement of potential vendors to develop a device expressly for cryogenic operation. Currently, there are ongoing investigations of MPPCs (multi-pixel photon counters) produced by Hamamatsu⁴ (Japan) including a model specifically designed for cryogenic operation, and a device developed for operation in LAr by FBK⁵ (Italy) in collaboration with the DarkSide experiment.

5.1.2.4 Readout Electronics

For prototype development and for ProtoDUNE-SP, a waveform digitizer has been developed that enables a thorough investigation of the photosensor signals, particularly as we investigate the impact of electrically ganging multiple SiPMs. The design of the readout electronics for the final system will be strongly influenced by the outcomes of MC simulations that are in progress. Of particular interest is the extent to which pulse shape capabilities are important to maximizing sensitivity to low energy neutrino interactions from SNBs. Initial MC simulations suggest that it may not be necessary to fully digitize the SiPM waveforms in order to achieve the PD performance requirements. Charge integration electronic readout systems, which offer the promise of significantly lower cost and smaller cabling harnesses, are under investigation and are expected to be the baseline solution. A lower-cost waveform digitization based on lower sampling rate commercial electronics will be investigated as a potential backup option in case our evolving understanding of the requirements necessitates collecting waveform data from the SiPMs.

⁴Hamamatsu™ Photonics K.K., <http://www.hamamatsu.com/>.

⁵Fondazione Bruno Kessler™, <https://www.fbk.eu>.

The size of currently available SiPMs is far smaller than the spatial granularity required for the experiment so the output of individual devices will be electrically summed (ganged) to reduce the electronics channel count. This will be achieved either by simply connecting together the output of multiple devices, passive ganging, or using active components, active ganging, if the signal is too degraded for the passive approach. Both approaches are under investigation.

5.1.2.5 R&D Priorities

Since the light guide designs are comparatively well understood, the need for an improved understanding of the potential ARAPUCA performance drives the strategy for the R&D program that will be carried out before the technical design report (TDR) (mid-2019). An intense effort is underway to demonstrate that an implementation of the ARAPUCA concept will increase the light yield of the SP module by a factor of five to ten with respect to the light guides; resources (personnel and funding) are being sought by the consortium to achieve this. Since the ARAPUCA approach demands a larger number of SiPMs than the light guides, a related high priority is demonstration of active ganging of a sufficient number of devices with adequate S/N properties.

It is anticipated that by the time of the TDR, the consortium will present ARAPUCA as a baseline design for the photon collector with one alternative design for risk mitigation.

5.1.3 Development and Evaluation Plans

The performance of the different photon collection options will be evaluated at several facilities available to the consortium. Relative and absolute measurements will be performed at both room and cryogenic temperatures.

The most comprehensive set of data will come from the fully instrumented modules in the ProtoDUNE-SP experiment currently under construction at CERN, which will start operations in the last third of 2018. All three photon collector designs are present in ProtoDUNE-SP: 29 double-shift guides, 29 dip-coated guides, and two ARAPUCA arrays. The TPC will provide precise reconstruction in 3D of the track of any ionizing event inside the active volume and matching the track with the associated light signal will enable an accurate comparison of the relative detection efficiencies of the different PD modules. In principle, absolute calculations are possible using MC simulations, but currently some of the optical parameters that regulate VUV light propagation in LAr are poorly known, which will limit the precision of this approach. A plan will be developed to address this limitation.

ProtoDUNE-SP will also provide a long-term test of full-scale PD modules for the first time so it may be possible to quantify any deterioration in their performance such as the loss of TPB from the coating noted previously. More broadly, aging effects in various detectors technologies, such as scintillator and photomultiplier tubes (PMTs), are well documented, and knowledge of such effects is required at the design stage so that the photon detection performance will meet minimum requirements for the whole life of the experiment.

An R&D program will be executed in parallel with the ProtoDUNE-SP operation since additional comparative measurements will be needed, particularly for the newer ARAPUCA concept, prior to establishing the baseline design for the TDR. Several facilities are accessible to the consortium that will allow testing of smaller scale prototypes of the modules (or sections of them). These include: the cryogenic facilities at Fermilab, Colorado State University and Universidade Estadual de Campinas (UNICAMP); and facilities for precision optical measurements and cryogenic testing of photosensors at Fermilab, Indiana University, Northern Illinois University, University of Iowa, Syracuse University, UNICAMP, and Institute of Physics in Prague.

A critical issue for large experiments are the interfaces between the subsystems. PD modules and interfaces with the APA system and cold electronics will be conducted using cryogenic gaseous nitrogen in cold box studies at CERN, using a test stand developed for testing of ProtoDUNE-SP components prior to installation into the detector. A full-scale ProtoDUNE-SP APA has been fabricated, and will be instrumented with cold electronics (CE) and PDs, allowing the interfaces to be carefully studied.

In addition, a small-scale TPC is planned for cold electronics testing at FNAL, and will be instrumented with as many as three 1/2-length PD modules to provide triggering information for the TPC and to continue interface studies with the APA and cold electronics. It is envisioned that up to three test cycles will be performed prior to the TDR, allowing testing and continued development of the ARAPUCA concept.

5.2 Photon Detector Efficiency Simulation

The potential physics performance of PD designs will be evaluated using a full simulation, reconstruction, and analysis chain developed for the LArSoft framework. The goal is to evaluate the performance in physics deliverables for each of the photon collector designs under consideration. The metrics evaluated will include efficiency for determining the time of the event (t_0), timing resolution, and calorimetric energy resolution for three physics samples: SNB neutrinos, nucleon decay events, and beam neutrinos. However, the development of analysis tools to take advantage of this full simulation chain is fairly recent, so this proposal will only include one test case: t_0 -finding efficiency for SNB neutrinos versus the effective area of the photon collectors (see Section 5.1.2.1).

The first step in the simulation specific to the PDS is the simulation of the production of light and its transport within the volume to the PDs. Argon is a strong scintillator, producing 24,000 γ s/MeV at our nominal drift field. Even accounting for the efficiency of the PDs, it is prohibitive to simulate every optical photon with GEometry ANd Tracking, version 4 (Geant4) in every event. So, prior to the full event simulation, the detector volume is voxelized and many photons are produced in each voxel. The fraction of photons from each voxel reaching each photosensor is called the visibility, and these visibilities are recorded in a 4-dimensional library (akin to the photon maps used in the DP module simulation described in Volume 3: Dual-Phase Module Chapter 6. This library includes Rayleigh scattering length ($\lambda = 55$ cm[20]), absorption length ($\lambda = 20$ m), and the measured collection efficiency versus position of the double-shift light-guide bars. When a particle is simulated, at each step it produces charge and light. The light produced is distributed

onto the various PDs using the photon library as a look-up table and the early (6 ns) plus late (1.6 μ s) scintillation time constants are applied. Transport time of the light through the LAr is not currently simulated, but is under development.

The second step is the simulation of the electronics response. For now, the SiPM signal processor (SSP) readout electronics used for PD development and in ProtoDUNE-SP is assumed (see Section 5.3.6). Waveforms are produced on each channel by adding an SiPM single-photoelectron response shape for each true photon. In addition, other characteristics of the SiPM are included such as dark noise, crosstalk and afterpulsing, based on data from device measurements. Dark noise, at a rate of 10 Hz for each of the three SiPMs on each channel is included by the addition of extra single-photoelectron waveforms. Crosstalk (where a second cell avalanches when a neighbor is struck by a photon generated internal to the silicon) is introduced by adding a second photoelectron 16.5% of the time when an initial photoelectron is added to the waveform. Additional uncorrelated random noise is added to the waveform with an RMS of 0.1 photoelectron. The response of the SSP self-triggering algorithm, based on a leading-edge discriminator, is then simulated to determine if and when a 7.8 μ s waveform will be read out, or in the case of the simulation it will be stored and passed on for later processing.

The third step is reconstruction, which proceeds in three stages. The first is a “hit finding” algorithm that searches for peaks on individual waveforms channel-by-channel, identifying the time based on the time of the first peak and the total amount of light collected based on the integral until the hit goes back below threshold. The second step is a “flash finding” algorithm that searches for coincident hits across multiple channels. All the coincident light is collected into a single object that has an associated time (the earliest hit), an amount of light (summed from all the hits), and a position on the plane of the anode plane assemblies (y - z) that is a weighted average of the positions of the photon collectors with hits in the flash. The final step is to “match” the flash to the original event by taking the largest flash within the allowed drift time that is within 240 cm in the y - z plane. Since the TPC reconstruction is still in active development, especially for low-energy events, we match to the true event vertex of the event in the analyses presented here. This is a reasonable approximation since the position resolution of the TPC will be significantly better than that of the PDS.

Figure 5.3 (top) shows the efficiency for determining t_0 for events in a typical SNB spectrum using the tools above. The changes in effective areas that would correspond to alternative photon collection designs are achieved by simply scaling up the total efficiency of the simulated double-shift light guide design shown here. The differences in attenuation behaviors within the bars are a second-order effect relative to the total amount of light collected. The efficiency for finding t_0 for these events increases, but less than linearly as the performance of the light collectors is improved. Figures 5.3 (bottom-left) and 5.3 (bottom-right) show how the efficiency varies as a function of neutrino energy and distance from the anode plane for three chosen points. These algorithms are still in development so there is potential for improvement in the performance as development continues.

If the correct flash is identified for a SNB event, the resolution on t_0 is excellent, as shown in Figure 5.4 – for 95% of the events, the time is identified from the prompt light and the timing resolution is better than 100 ns, well within a single TPC time tick. In the remaining 5% of cases where a correct flash is matched, the t_0 is biased towards later times (with respect to the true

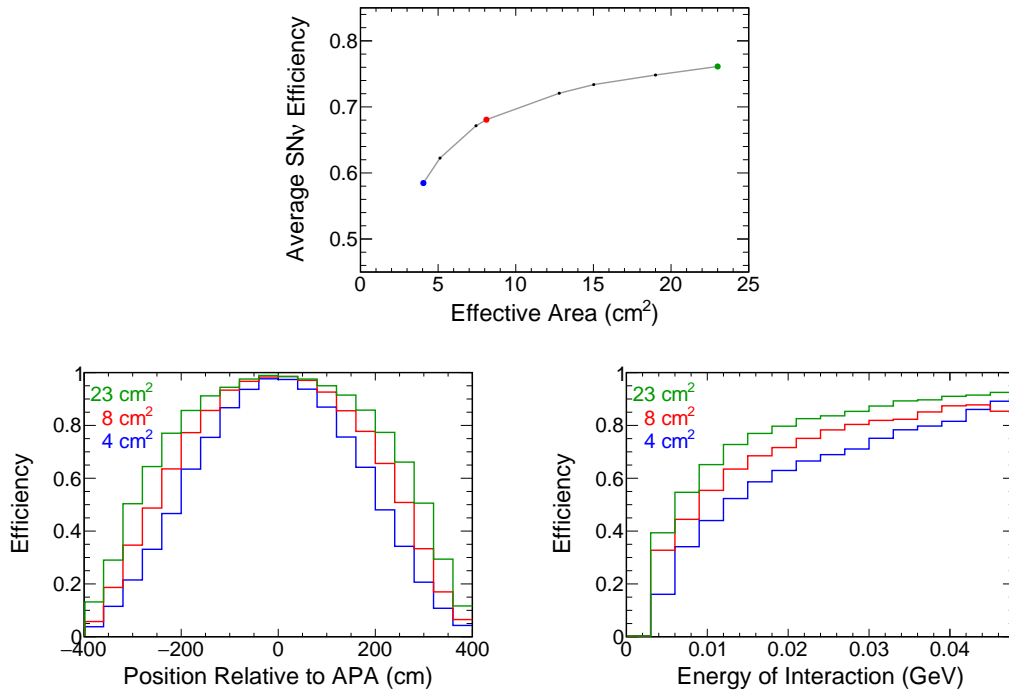


Figure 5.3: Preliminary estimates of the efficiency for finding t_0 for core collapse SNB events vs. the effective area (top), distance from the anode plane (bottom-left), and neutrino energy (bottom-right).

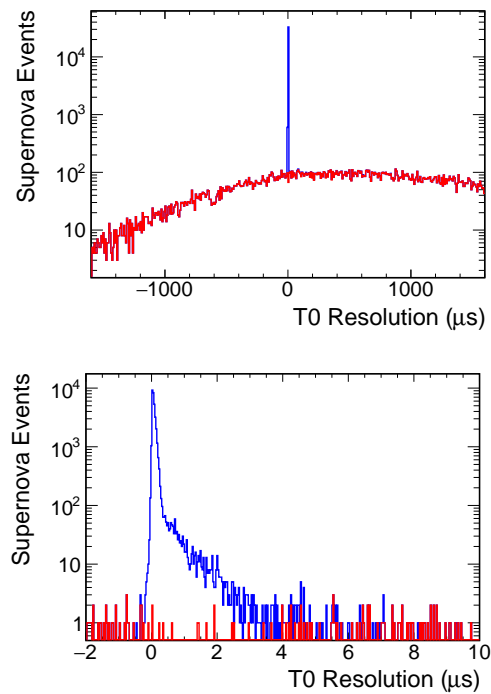


Figure 5.4: Resolution on t_0 for SNB events. These are based on simulation with effective light collector area of 4 cm², which corresponds to the photon detection efficiency of 0.23% measured for a double-shift light guide module.

event time) by a few μs , driven by the late light time constant. If the wrong flash is identified the t_0 found is essentially randomly distributed in the drift time.

This preliminary study shows that each of the PD options, with effective area per module currently estimated to be in the range 4 to 22cm^2 , will be able to determine the event t_0 with reasonable efficiency and it illustrates the benefit of higher photon detection efficiency.

5.3 Photon Detection System Design

The principal task of the SP module PDS is to measure the VUV scintillation light produced by ionizing tracks in the TPC within the geometrical constraints of the APA structure. A commercially available compact solution for photon measurement is the SiPM, however, the response of the devices, which typically peaks in the visible range ($>400\text{nm}$) is not well-matched to incident 127nm scintillation photons, so a wavelength shifter or some sort must be employed. In addition, even though production cost and key performance parameters have improved significantly in recent years, the cost of the readout electronics (channel count) and the SiPMs needed to meet the physics requirements of the PDS would be prohibitive.

The photon collector must optimize the costs of various components of the system while meeting the performance requirements. In practice, this consists of collecting VUV photons over an area of hundreds of square-meters (viewing the entire 10 kt LAr fiducial mass), converting the photons to longer wavelengths and guiding them onto SiPMs that are typically $\text{O}(\text{cm}^2)$. For reference, an array of 48 SiPMs demonstrated a detection efficiency of 13%, corresponding to an effective area of 2.2cm^2 . This array, tested in the Fermilab TallBo LAr facility, consisted of twelve 4×4 units of $3\text{mm}\times 3\text{mm}$ sensL C-series coated with $100\ \mu\text{g}/\text{cm}^2$ of TPB.

A challenge for the PDS is that a full set of requirements is not yet fully defined for one of the priority physics topics, SNB neutrinos. So the designs strive to demonstrate that at minimum the requirements for the accelerator neutrino program, atmospheric neutrinos and nucleon decay will be met, while maintaining the flexibility to adjust to the greater demands for the SBN physics.

At the time of the interim design report (IDR) there are three photon collector options under consideration; Figure 5.2 shows how they are incorporated into the TPC anode plane assembly by an identical modular mounting scheme. In the following we summarize the design and development status for each photon collector option⁶.

5.3.1 Photon Collector: ARAPUCA

The ARAPUCA is a device based on a new approach to LAr scintillation photon detection where the effective photon detection area is increased by trapping photons inside a box with highly reflective internal surfaces until reflections guide them to a much smaller SiPM [21].

⁶For the TDR there will be a baseline design and at most one alternative.

Photon trapping is achieved through a novel use of wavelength-shifting and the technology of the dichroic shortpass optical filters. These commercially available filters are created by using multilayer thin films that in combination have the property of being highly transparent to photons with a wavelength below a tunable cut-off while being almost perfectly reflective to photons with wavelength above the cut-off. Such a filter coated with either one or two different wavelength-shifters, depending on the detailed implementation, forms the entrance window to a flat box with internal surfaces covered by highly reflective acrylic foils except for a small fraction of the surface that is occupied by active photosensors (SiPMs).

To act as a photon trap, the wavelength-shifter deposited on the outer face of the dichroic filter must have its emission wavelength *less* than the cut-off wavelength of the filter, below which transmission is typically greater than 95%. These photons pass through the filter where they encounter a second wavelength-shifter, either on the inner surface of the filter or coated on the reflecting inner surfaces of the box, with an emission spectrum greater than the cut-off wavelength. For these photons the reflectivity of the filter is typically greater than 98%, so they will reflect off the filter surface (and the inner walls) and so be trapped inside the box with a high probability to be incident on an SiPM before being lost to absorption. The concept is illustrated in Figure 5.5, in this example the filter cut-off is 400 nm.

The net effect of the ARAPUCA is to amplify the active area of the SiPM used to readout the trapped photons. It is easy to show that, for small values of SiPM coverage of the internal surface, the amplification factor is equal to $A = 1/(2(1-R))$, where R is the average value of the reflectivity of the internal surfaces; for an average reflectivity of 0.95 the amplification factor is equal to ten.

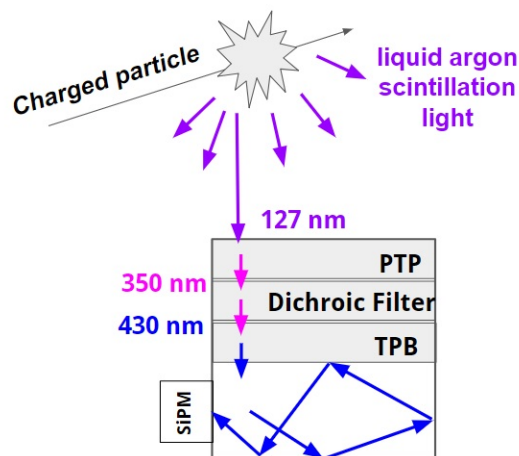


Figure 5.5: Schematic representation of the ARAPUCA operating principle.

5.3.1.1 Prototype Measurements

ARAPUCA prototypes with different configurations have been tested in LAr at multiple facilities. In each case, the first wavelength shift of 127 nm scintillation photons down to 350 nm that can

pass through the filter substrate was performed by p-TerPhenyl (pTP) evaporated onto the outside of a dichroic filter window.

The first prototype was made of PTFE with internal dimensions of $3.5\text{ cm} \times 2.5\text{ cm} \times 0.6\text{ cm}$ with a window formed from a dichroic filter with dimensions of $3.5\text{ cm} \times 2.5\text{ cm}$ and wavelength cut-off at 400 nm. TetraPhenyl-Butadiene (TPB) was evaporated onto the internal side of the filter where it absorbs the shifted 350 nm photons and reemits around 430 nm. Trapped light is detected by a single $0.6\text{ cm} \times 0.6\text{ cm}$ sensL SiPM mod C60035⁷. The device was installed inside a vacuum tight stainless-steel cylinder closed by two CF100 flanges. The cylinder was deployed inside a LAr open bath, vacuum pumped down to a pressure around 10^{-6} mbar and then filled with one liter of ultra-pure LAr⁸.

Scintillation light emission was produced by an alpha source⁹ installed in front of the ARAPUCA immersed in LAr. Signals were read out through an Aquiris¹⁰ PCI board and stored on a computer. Figure 5.6 shows photographs of the ARAPUCA and cryogenic system at the Brazilian Synchrotron Light Laboratory (LNLS).



Figure 5.6: ARAPUCA test at the Brazilian Synchrotron Light Laboratory

The detection efficiency of the ARAPUCA was calculated by determining the number of photoelectrons detected corresponding to the end point of the α spectrum and comparing it with the expected number of photons impinging on the acceptance window for that particular energy value ($\sim 4.3\text{ MeV}$). This depends only on known properties of LAr and on the solid angle subtended by the ARAPUCA window. A detection efficiency at the level of 1.8% was measured, consistent with MC expectations for the this configuration[22].

The next several prototypes were tested under cryogenic conditions at Fermilab. The first, performed in mid-2016 at the Proton Assembly Building (PAB) at the ScENE cryogenic test facility, had dimensions of $5.0\text{ cm} \times 5.0\text{ cm} \times 1.0\text{ cm}$ with a dichroic window of $5.0\text{ cm} \times 5.0\text{ cm}$ with a cut-off of 400 nm which was deposited with pTP and TPB. However, in this case, two of sensL SiPMs mod

⁷<http://sensl.com/products/c-series/>

⁸Argon 6.0, less than 1 ppm total residual contamination.

⁹A ^{238}U -Al alloy in the form of a metallic foil, with alpha particle emission of 4.267 MeV.

¹⁰Aquiris High-Speed Digitizer products; <http://www.acqiris.com/>.

C60035 were installed inside the box. The ARAPUCA was again deployed inside a vacuum-tight cryostat filled with ultrapure LAr. An ^{241}Am alpha source was positioned in front of the window of the device 5 cm from its center. The efficiency of the ARAPUCA was estimated taking into account that the alpha particles from this source have a monochromatic energy of about 5.4 MeV. The estimated efficiency in this case was approximately 1%, a factor two below the expected value; this is attributed to the sub-optimal quality and uniformity of the pTP and TPB films, and to the lack of reflectivity of the inner PTFE surfaces in this early prototype.

The next set of tests was performed at the beginning of 2017 at the PAB, but using the TallBo facility, which is large enough to allow testing of several devices at a time. Eight different ARAPUCA cells with filters from different manufacturers, different reflectors, and different dimensions were tested. Scintillation light was again produced by alpha particles emitted by an ^{241}Am source mounted on a holder that could be moved with an external manipulator in order to place it in front of each prototype. The detection efficiencies of these ARAPUCAs ranged from 0.4% to 1.0%.

The most recent measurements were performed in the TallBo facility at the end of 2017 with an array of eight ARAPUCAs together with two reference bars (double-shift light guide design). The data analysis for the ARAPUCA array is currently underway.

5.3.1.2 ARAPUCA in ProtoDUNE-SP

Two arrays of ARAPUCA modules will be operated inside ProtoDUNE-SP to test the devices in a large-scale experimental environment and allow direct comparison of their performance with the light guide designs.

Each ProtoDUNE-SP ARAPUCA module array is composed of sixteen cells where each cell is an ARAPUCA box with dimensions of 8 cm \times 10 cm; half of the cells have twelve SiPMs installed on the bottom side of the cell and half have six SiPMs. The SiPMs have active dimensions 0.6 cm \times 0.6 cm and account for 5.6% (12 SiPMs) or 2.8% (6 SiPMs) of the area of the window (7.8 cm \times 9.8 cm). The SiPMs are passively ganged together, so that only one readout channel is needed for each ARAPUCA grouping of 12 SiPMs (the boxes with six SiPMs are ganged together to form 12-SiPM units) so a total of 12 channels is required per array. Studies are underway to investigate active ganging that would permit combining signals from multiple boxes, as required to reduce the number of electronics channels and cables under the working assumption that the SP PDS is restricted to four readout channels per PD module. The total width of a module is 9.6 cm, while the active width of an ARAPUCA is 7.8 cm, the length is the same as the light guide modules (210 cm). The first ARAPUCA array installed in ProtoDUNE-SP is shown in Figure 5.8. If the ARAPUCA cells achieved the same detection efficiency as earlier prototypes (1.8%), the effective area of an ARAPUCA module will be approximately 23 cm².



Figure 5.7: Full-scale ARAPUCA for ProtoDUNE-SP during assembly. SiPMs are visible in the sixteen cells before the installation of reflecting foils, coated filter windows, and readout cabling.

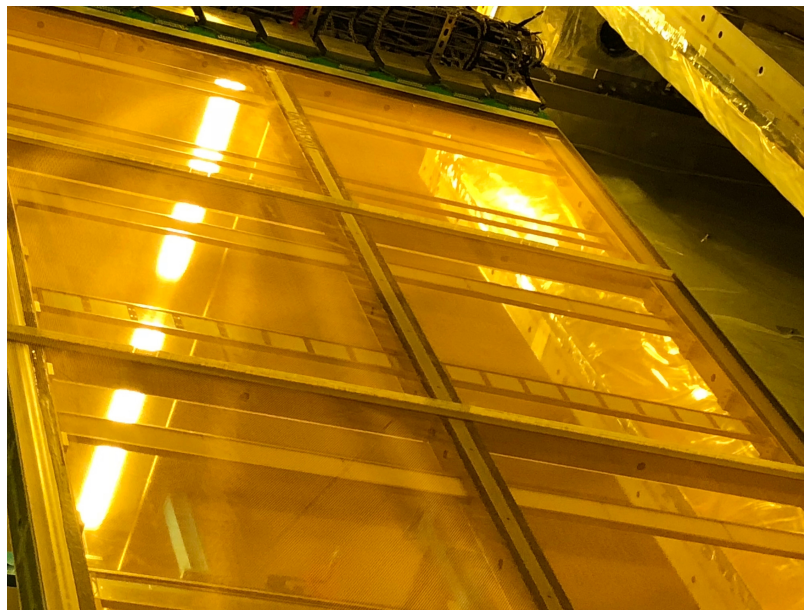


Figure 5.8: ARAPUCA array in ProtoDUNE-SP.

5.3.1.3 X-ARAPUCA

X-ARAPUCA represents an alternative line of development with the aim of further improving the collection efficiency, while retaining the same working principle, mechanical form factor and active photo-sensitive coverage. X-ARAPUCA is effectively a hybrid solution between the ARAPUCA and the wavelength-shifting light guide concepts, where photons trapped in the ARAPUCA box are shifted and transported to the readout via total internal reflection in a short light guide placed inside the box. This solution minimizes the number of reflections on the internal surfaces of the box and thus the probability of photon loss. Simulations suggest that this modification will lead to a significant increase of the collection efficiency, to around 60%, so the photon detection efficiency including the SiPM response could approach 20%.

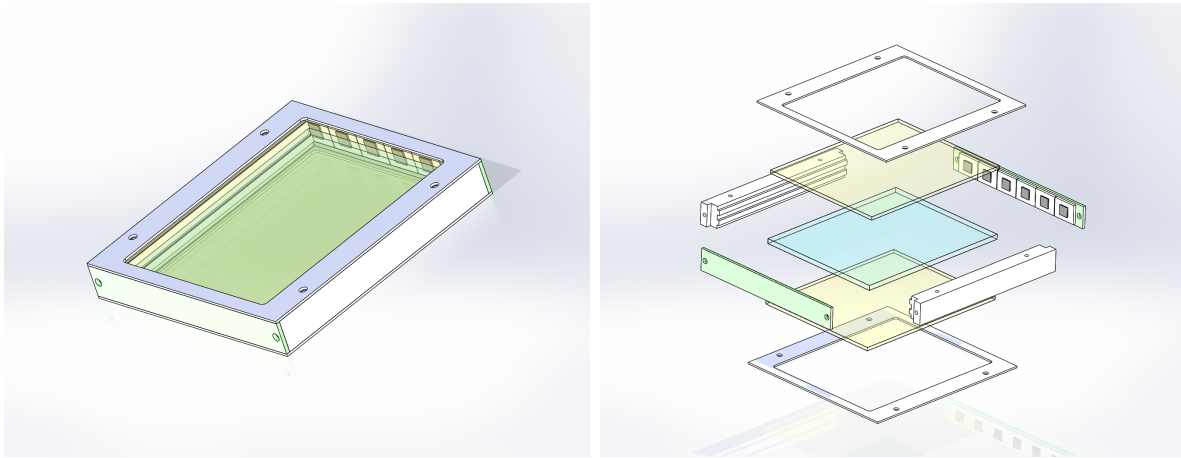


Figure 5.9: X-ARAPUCA design: assembled cell (left), exploded view (right). The size and aspect ratio of the cells can be adjusted to match the spatial granularity required for a PD module.

In the X-ARAPUCA design, Figure 5.9, the inner shifter coating/lining over the reflective walls of the box is replaced by a thin wavelength-shifting light guide slab inside the box, of the same dimensions of the acceptance filter window and parallel to it. The SiPM arrays are installed vertically on the sides of the box, parallel to the light guide thin ends. In this way a fraction of the photons will be converted inside the slab and guided to the readout, other photons, e.g., those at small angle of incidence below the critical angle of the light guide slab, after conversion at the slab surface will remain trapped in the box and eventually collected as for the standard ARAPUCA.

A full-sized X-ARAPUCA prototype is under development. The light guide is a 3 mm thick TPB-doped acrylic plate. Two readout boards, each with several passively ganged SiPMs in a strip configuration, are mounted along the thin edges of the box and their ganged signals are combined into a single channel readout. The aspect ratio of the cells can be adjusted to match the required spatial granularity for the PD module.

5.3.1.4 ARAPUCA Configuration in DUNE 10 kt

The modular arrangement of the SP module TPC calls for a configuration across the width of the cryostat starting with an APA plane against one cryostat wall, and following with anode plane

assemblies and cathode plane assemblies (CPAs) arranges as follows: APA-CPA-APA-CPA-APA. This means that the central APA will collect charge and see scintillation light from LAr volumes on both sides, whereas those by the wall collect from only one side. While the ARAPUCA modules deployed in ProtoDUNE-SP collect light from only one direction, several ARAPUCA configurations under development are capable of collecting light from both sides (including the X-ARAPUCA concept). The optimal configuration of ARAPUCA modules has not yet been determined, but the basic design allows for both single-sided and double-sided cells with no impact on the APA design.

5.3.2 Photon Collector: Dip-Coated Light Guides

The dip-coated light guide design is mechanically the simplest of the three options. Figure 5.10 illustrates the process by which LAr scintillation photons are converted and detected in this approach. VUV scintillation photons incident on the bar are absorbed and wavelength-shifted to blue (~ 430 nm) by the TPB-based coating on the surface of the bar. A portion of this light is captured in the bar and guided to one end through total internal reflection where it is detected by an array of SiPMs, whose PDE is well-matched to the blue light. Dimensions of the bars in ProtoDUNE-SP are: $209.3\text{ cm} \times 8.47\text{ cm} \times 0.60\text{ cm}$. Since the bar is coated on all sides, in the SP module it can be employed both in the wall anode plane assemblies as well as in the center APA array where scintillation light approaches from two drift volumes.

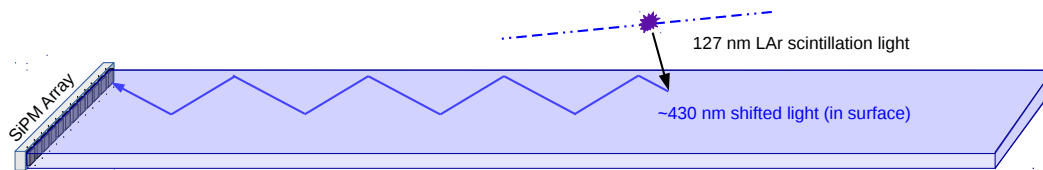


Figure 5.10: Schematic of scintillation light detection with dip-coated light guide bars.

The dipping process and coating formula have undergone a series of development iterations [23], with the bars undergoing extensive testing at both room and cryogenic temperatures. As a part of the production process, the attenuation of each dip-coated light guide bar is measured at room temperature in a dark box with a UV LED; 80% of the bars measured have an attenuation length in air of 6 m or greater. Attenuation measurements on full-length bars have not yet been performed in LAr, but a model presented in [23] predicts effective attenuation lengths greater than 2 m [24]. The general features of this model were validated by measurements using ^{210}Po alpha sources in the TallBo cryogenic test stand at FNAL.

A further validation of the bar performance came from a set of measurements taken in the TallBo cryostat containing the four initial candidate photon collector technologies using alpha sources and tracked cosmic ray muons, allowing side-by-side comparisons [19]. As a result, the two approaches that showed the highest promise, dip-coated and double-shift light guides (described in the next section), were continued for further development since these had similar photon detection efficiency, $\sim 0.1\%$, that was significantly higher than the other two.

A simple improvement to the bar performance is to read out both ends of the bar rather than a

single end as is the case for bars deployed in ProtoDUNE-SP. In addition, test bars have been produced with a higher TPB-to-acrylic ratio, which may have a higher conversion efficiency without introducing a reduction in attenuation length. These improvements could increase the photon detection efficiency of the dip-coated light guide by more than a factor of two.

5.3.3 Photon Collector: Double-Shift Light Guides

In the early implementations of the dip-coated light guide development there was a strong dependence of the light yield along the length of the bar, presumed to be due to the impact of the coating on the total internal reflection efficiency. In an effort to mitigate this effect, the double-shift light guide design decouples the process of converting VUV photons to optical wavelengths from the transportation of photons along the bars. This is achieved by positioning an array of acrylic plates coated with TPB in front of a high-quality commercial polystyrene light guide doped with a second wavelength-shifting compound.

Figure 5.11 illustrates the double-shift light guide concept. VUV scintillation photons incident on the acrylic plates are converted to blue wavelengths (~ 430 nm) and a fraction of these blue photons penetrate the light guide and are converted to green (~ 490 nm). The re-emission of these green photons, taken to be a Lambertian distribution (isotropic luminance), leads to some becoming trapped by total internal reflection within the light guide and transported to the end of the light guide where they are detected by an array of SiPMs.

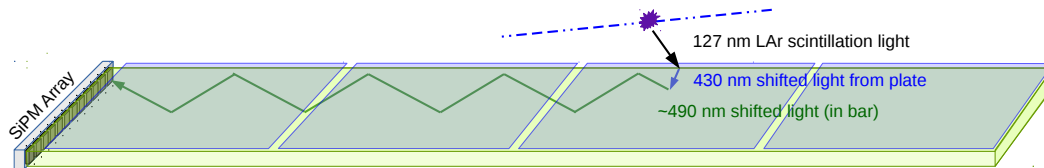


Figure 5.11: Schematic of the double-shift light guide concept.

The radiator plates are formed by spray-coating TPB on the outer surface of acrylic plates, as described in Section 5.4.1.3. A full-scale double-shift light collector module consists of six radiator plates mounted on each face of the wavelength-shifting light guide (12 plates total). The 210 cm \times 8.6 cm light guide is fabricated by Eljen Technologies¹¹ and consists of a polystyrene bar doped with the EJ-280 wavelength shifter. EJ-280 features an absorption spectrum that is well matched to the TPB emission spectrum so wavelength-shifted photons emitted from the plates are absorbed with good efficiency.

For most of the testing and the ProtoDUNE-SP modules, the SiPM array used 0.6 cm \times 0.6 cm sensL C-series MicroFC-60035-SMT SiPMs. These were originally selected since they were a good match for the TPB emission spectrum on the dip-coated bars. However, they have a photon detection efficiency between 20%–35% across the emission spectrum of the EJ-280 wavelength shifter, compared to up to 40% at the peak, so selecting a different device with a better-matched photon detection efficiency would improve the performance of the double-shift design.

¹¹<http://www.eljentechnology.com>

The double-shift light guide design has undergone a series of development iterations to improve its performance, carried out at Indiana University (IU) and at Fermilab’s cryogenic and vacuum test facility in the PAB. Comparative testing of light guide designs at PAB in mid-2015 demonstrated the viability of the double-shift light guide concept [25]. An improved design similar to that deployed at ProtoDUNE-SP was studied at the Blanche test stand at Fermilab in September of 2016 with a complementary component-wise analysis program at IU afterward, as detailed in [26]. The attenuation characteristics of this light guide were measured at IU, while the detection efficiency for incident LAr scintillation photons was measured with a vacuum-ultraviolet (VUV) monochromator at IU and using scintillation light from cosmic rays at the Blanche test stand.

Analysis of the double-shift light guide’s attenuation properties determined an attenuation profile in LAr characterized by a double-exponential function of the form $f(z) = A \exp(-z/\lambda_A) + B \exp(-z/\lambda_B)$ with z the distance from the instrumented end and parameters $A = 0.29$, $\lambda_A = 4.3$ cm, $B = 0.71$, and $\lambda_B = 225$ cm [26]. The effective attenuation length of 2.25 m is comparable to the width of an APA when the double-shift light guide is deployed in LAr.

Using both direct measurement with the monochromator and scintillation light, the photon detection efficiency of this detector was determined to be 0.48% at the end close to the SiPM readout. The total effective area for detecting VUV scintillation photons in this module can be determined by integrating the product of this efficiency and the attenuation function over the area of the detector, yielding an effective area $A_{eff} = 4.1$. This corresponds to an effective area for detecting VUV scintillation photons of 4.1 cm² per module per drift volume, which corresponds to overall 0.23% photon detection efficiency for events occurring on one side of the APA. Since the radiator plates are deployed on both faces of the light guide, modules in the center APA array are sensitive to scintillation light from the two drift volumes on either side.

There are several ways that the current design could be improved. The double-shift light guide deployed in the ProtoDUNE-SP anode plane assemblies is constrained to read out at a single end. Proposed changes to the APA size and cabling routing scheme for the SP module would allow for a second array of SiPMs at the opposite end of the light guide, which would almost double the performance of the photon detection system. A SiPM with a wavelength-dependent PDE that is better matched to the EJ-280 emission spectrum would also improve the efficiency. Simulations of the transport of light within the light guide suggest that applying a highly reflective coating to the long, narrow inactive sides of the light guide would improve the attenuation function and increase the effective area of the light guide module. These effects combined lead to a potential increase of the effective area up to four times the current prototypes, approaching 1% detection efficiency.

5.3.4 Additional Techniques to Enhance Light Yield

Though we anticipate that the designs described in the previous sections will meet the PD performance requirements we do not yet have final designs and so we have also considered options for enhancing the light yield if that becomes necessary. Some of the initial ideas, such as deploying a large array of Winston-cone style reflectors focusing light onto SiPMs throughout the entire area enclosed by the APA frame, would require a significant change in the APA production and assembly planning and so will become increasing untenable. However, one option being investigated in

parallel with the photon collector modules design is to convert the scintillation light falling on the cathode plane into the visible wavelengths, which in turn illuminates photon detectors embedded in the APA, as is currently envisioned.

A motivation for this approach is that, due to geometric effects, the baseline PDS design will result in some non-uniformity of light collection along the drift direction. Light emitted from interactions close to the anode plane assemblies has an order of magnitude larger chance of being detected compared to interactions close to the CPA. This effect can be mitigated by installing wavelength-shifter (TPB) coated dielectric reflector foils on the cathode planes. Light impinging on these foils is wavelength-shifted into visible wavelengths and reflected from the underlying foils. This light can subsequently be detected by photon detectors placed in the anode plane assemblies provided they are sensitive to visible light (which is not the case for the current photon collector modules). Fig. 5.12, shows that if the APA photon collectors are capable of recording both direct scintillation light and the visible light from the CPA, there is an enhancement of the total light collection close to the cathode (black points), which will increase the detection efficiency in that region. Another benefit is the increase in uniformity - this can enable calorimetric reconstruction with scintillation light, which would enhance the charge-based energy reconstruction as well as increase the efficiency of triggering on low energy signals. Introducing the foils on the cathode may also enable drift position resolution using only scintillation light. This requires the photon detectors to be able to differentiate direct VUV light from re-emitted visible light (e.g. two different PD detector types) and good enough timing of arrival of first light.

Coated reflector foils are manufactured through low-temperature evaporation of TPB on dielectric reflectors e.g. 3M DM2000 or Vikuiti™ ESR. Foils prepared in this manner have been successfully used in dark matter detectors such as WArP[27]. Recently they have been shown to work in LArTPCs at neutrino energies, namely in the LArIAT test-beam detector [28]. In LArIAT they have been installed on the field-cage walls and, during the last run, on the cathode.

The necessity to record both VUV and visible photons in the photon collectors would require a change in the current design but is conceptually possible. For example, if the cathode plane were coated with tTP, some of the ARAPUCA modules could be constructed without the pTP coating on the outer surface of the filter and benefit from the same photon trapping effect but these cells would no longer be sensitive to direct scintillator light. Understanding the impact of these competing effects on the physics is under study by the simulation group and the feasibility of coating the cathode with a dielectric medium is being investigated with the DUNE HV consortium.

5.3.5 Silicon Photosensors

The SP module PDS uses a multi-step approach to scintillation light detection with final stage of conversion into electrical charge performed by silicon photomultipliers (SiPM). Robust photon detection efficiency, low operating voltages, small size and ruggedness make their use attractive in the SP design where the photon detectors must be accommodated inside the APA frames. As implemented in ProtoDUNE-SP, there are twelve $6\times 6\text{ mm}^2$ SiPMs per bar and 6 to 12 per ARAPUCA box. With this configuration, a 10 kt SP module with 150 anode plane assemblies, each with 10 PD modules, would contain 18,000-36,000 (single or double-ended readout) SiPMs

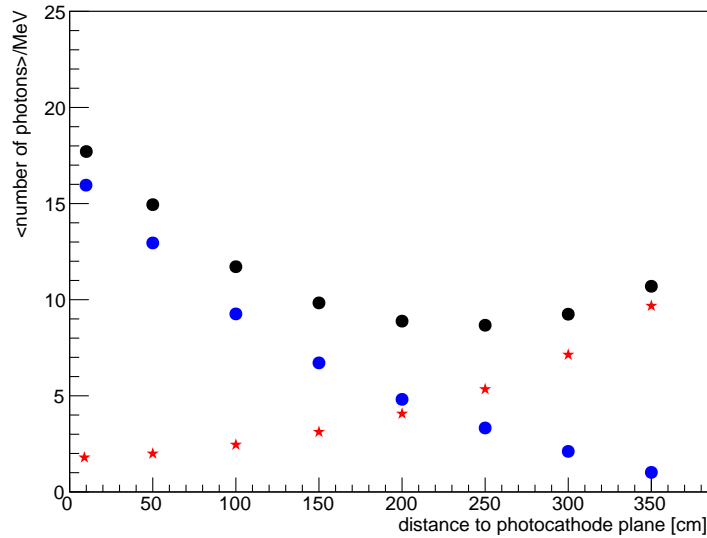


Figure 5.12: Predicted light yield in with WLS-coated reflector foils on the CPA. Blue points represent direct VUV light impinging on the PDs assuming a 0.42% photon detection efficiency and 70% wire mesh transmission; red stars - represent scintillation light that has been wavelength-shifted and reflected on the CPA assuming the same photon detection efficiency. Black points show the sum of these two contributions (which would require twice the number of PD modules in the current APA configuration).

for the light guide designs and 10-20 times more for the higher granularity ARAPUCA design. This corresponds to approximately 1-13 m² of active SiPM surface area.

The following summarizes the most salient guiding principles and requirements for this SiPM-based photodetection system.

- The full suite of SiPM requirements (number of devices, spectral sensitivity, dynamic range, triggering, zero-suppression threshold etc.) is determined by the physics goals and the photon collection implementation. As discussed in Section 5.1.1, the requirements for SNB neutrinos are not yet fully established however, R&D carried out to date indicates that devices from several vendors have the performance characteristics close to that needed for the PDS (see Table 5.3). Nearly one thousand of several types of these devices are used in the ProtoDUNE-SP PD¹², which will provide an excellent test bed for evaluating and monitoring SiPM performance in a realistic environment over a period of months.
- A key requirement is to ensure the mechanical and electrical integrity of these devices in a cryogenic environment. However, currently, catalogue devices for most vendors are certified for operation only down to -40°C . It is essential to be in close communication with vendors in the design, fabrication and SiPM packaging certification stages to ensure that the device will be robust and reliable for long-term operation in a cryogenic environment. Two sources have expressed interest to engage with the consortium in this fashion with the goal of having the vendor warranty the product for our application: Hamamatsu Photonics K.K., a large

¹²ProtoDUNE-SP PDS uses 516 sensL MicroFC-60035C-SMT, 288 Hamamatsu MPPC 13360-6050CQ-SMD with cryogenic packaging, 180 Hamamatsu MPPC 13360-6050VE.

well-known commercial vendor in Japan and Fondazione Bruno Kessler (FBK) in Italy, an experienced developer of solid state photosensors that typically licenses its technology and which is partnering with the DarkSide collaboration to develop a devices with very similar requirements as DUNE. Contact with other vendors and experiments using this technology in a similar environment is being pursued.

- Comparative performance evaluation of promising SiPM candidates from multiple vendors will need to be carried out in parallel over the next year. This evaluation will need to address inherent device characteristics (gain, dark rate, x-talk, after-pulsing etc), which are common to all three photon collector options, along with ganging performance, form factor, spectral response, and mechanical mounting options that may have different optimization for the two light guide design and ARAPUCA. Experience acquired from ProtoDUNE-SP construction and operation will inform QA/QC plans for the full detector, which will need to be delineated in detail.
- The optimal SiPM may depend on the photon collector option selected. All options currently being considered involve shifting the 127 nm LAr scintillation light to longer wavelengths, but each may present a different spectral distribution to the SiPM. In this case, final selection of the SiPM might be delayed to allow an optimal match to the photon collector. However, we would not expect this fine-tuning to be more than a 15-20% effect, so it is not a driving factor.
- For the light guide photon collector designs, the SiPM packaging should allow for tileable arrays to be constructed to facilitate high packing efficiency across the end of the bars and efficient space utilization inside the APA frame.
- Current candidate SiPMs have an area of less than 1 cm^2 , a much finer granularity than needed. In addition, the cold feedthrough size and space in the anode plane assemblies for cable runs limits the number of PD signal and power cables. These constraints, and other considerations, imply that the signal output of SiPMs must be electrically ganged. The degree of ganging depends on the photon collectors technology and currently ranges from six SiPMs for the light guides to 48 or more for the ARAPUCA modules. Whether simple passive-ganging (wiring the outputs together) will suffice or if active-ganging (with active components) is under investigation as a joint responsibility of the photon sensor and electronics working groups (see Section 5.3.6.1 for more details).
- The terminal capacitance of the sensors strongly affects the signal-to-noise when devices are ganged in parallel and so is a factor in SiPM selection, and may ultimately determine the maximum number of individual sensors that can be ganged this way.

Table 5.3: Candidate Photosensors Characteristics.

	Hamamatsu	sensL	KETEK	Advansid
Series part #	S13360	DS-MicroC	PM33	NUV-SiPMs
Vbr range	48 V to 58 V	24.2 V to 24.7 V	27.5 V	24 V to 28 V
Vop range	Vbr + 3 V	Vbr +1 V to +3 V	Vbr+2V to +5 V	Vbr +2 V to +6 V
Temp. dependence	54 mV/K	21.5 mV/K	22 mV/K	26 mV/K
Gain	1.7×10^6	3×10^6	1.74×10^6	3.6×10^6
Pixel size	50 μm	10 μm to 50 μm	15 μm to 25 μm	40 μm
Sizes	2x2 mm	1x1	3x3	4x4
	3x3 mm	3x3		3x3
	6x6 mm	6x6		
Wavelength	320 to 900 nm	300 to 950 nm	300 to 950 nm	350 to 900 nm
PDE peak wavelength	450 nm	420 nm	430 nm	420 nm
PDE @ peak	40%	24% to 41%	41% at Vov=5 V	43%
DCR @0.5PE	2 to 6 MHz	0.3 kHz to 1.2 MHz	100 kHz at Vovr=5 V	100 kHz/mm ²
Crosstalk	< 3%	7%	15%	< 4% (correlated noise)
Afterpulsing		0.20%	<1%	<4%
Terminal capacitance	1300 pF	3400 pF	750 pF	800 pF
Lab experience	Good experiences from Mu2e and ARAPUCA	Crack at LN2 temps. after specifications change		

5.3.6 Electronics

5.3.6.1 Introduction

The PD design requires the readout system to collect and process electrical signals from photosensors reading out the light collector bars, to provide interface with trigger and timing systems to support data reduction and classification, and to enable data transfer to offline storage for physics analysis.

The readout system must enable the measurement of the t_0 of non-beam events with deposited energy above 10 MeV. This capability will also enhance beam physics, by recording interaction time of events within beam spill to help separate against potential cosmic background interactions. Two main methods of data collection are currently considered: self-triggered integrated charge readout and wave form digitization. Charge integration appears to be a likely candidate at this point in our development, as it offers the potential for a simpler, commercially available charge integration circuit and perhaps a smaller, less-expensive cable plant to read it out. Physics simulation studies are currently underway to determine if pulse-shape discrimination will be required, which would provide the capability to record both prompt and delayed components of scintillation light (characteristic times of 6 ns and $1.3 \mu\text{s}$), the latter consisting mostly of single photoelectrons and thus place stringent requirements on signal-to-noise performance. The photon detector collects a limited amount of light, so it could be beneficial to collect the light from both excited states. Since this requirement has not yet been established the option is kept open in the electronics design.

All photon collector options require some level of electrical ganging of the SiPMs, either passive direct connection of the SiPM outputs or active (cold signal summing and possibly amplification). To that end we desire a system where the ganging is maximized to minimize the electronics channel count while maintaining adequate redundancy and granularity, as well as readout system performance. This represents a significant interface between the electronics, photosensor and light collector designs, and will be a main focus of our development and optimization work up to the TDR.

Technical factors that affect performance of the ganging system are the characteristic capacitance of the SiPM and the number of SiPMs connected together, which together dictate the signal to noise ratio and affect the system performance and design considerations. Selection of the ganging option will include passive or active solutions, where the active circuitry may require cold components such as an amplifier in the LAr volume. Design options with active cold components will need to address issues of power dissipation and potential risks of single-point failures of multi-channel devices inside the cryostat. In the case of passive ganging, analog signals are transmitted outside of the cryostat for processing and digitalization. Successful demonstrations of passive ganging at LAr temperatures have been made for groups of four and twelve 6x6 mm Micro-FC-60035C-SMT C series, and groups of 2, 4, 8, and 12 Hamamatsu MPPCs (S13360-6050PE) at 25°C, -70°C and 77K. Active ganging has been demonstrated for an array of 12 sensL 4x4 arrays of 3 mmx3 mm sensL C-series SiPMs (48 in all) and 72 SiPMs mounted in a hybrid combination of passive and active ganging using 6 mmx6 mm MPPCs with a low noise operational amplifier—this design combines 12 active branches into the op-amp, where each branch has six MPPCs in a

parallel passive-ganging configuration.

Typically, arrival time and total charge are the key parameters to be obtained from a detector. Extraction of these parameters is possible using analog or digital systems. Charge preamplifiers will be connected to the output of the detector to integrate current producing a charge proportional output. In the case of digital systems an amplifier is needed to adjust the detector output signal level to the input of an analog-to-digital converter (ADC). In both systems, performance parameters related to sampling rate, number of bits, power requirements, signal to noise ratio, and interface requirements should be evaluated to arrive to selected solution. Pulse shapes can be fully analyzed to improve detection of a new physics but it will have an important impact on the digitalization frequency.

5.3.6.2 ProtoDUNE-SP Electronics

A dedicated photon-detector readout system, presented schematically in Figure 5.13(left), was developed for ProtoDUNE-SP, which will be operational in the second half of 2018. Twenty-four custom SiPM Signal Processor (SSP) units were produced to read out the 58 light guide and 2 ARAPUCAs photon collectors. An SSP contains of twelve readout channels packaged in a self-contained 1U module; four SSPs are shown in Figure 5.13(right).

A passive ganging scheme with three SiPMs ganged together was chosen for the light guides (4 SSP channels for each bar) and groups of twelve SiPMs are passively ganged for the two ARAPUCA modules (12 SSP channels per module). The unamplified analog signals from the SiPMs are transmitted to outside the cryostat for processing and digitization over an approximately 25 m cable to the SSP outside the cryostat. Each channel receives the SiPM signal into a termination resistor that matches the characteristic impedance of the signal cable followed by a fully-differential voltage amplifier and a 14-bit, 150-MSPS ADC that digitizes the SiPM signal waveforms.

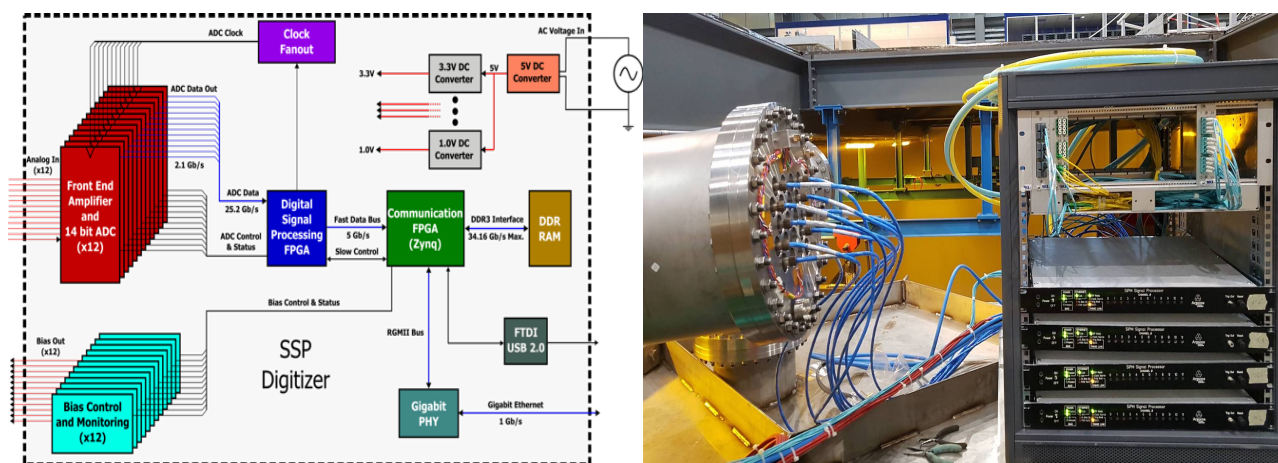


Figure 5.13: Block diagram of the ProtoDUNE-SP PD readout module (left). PD readout system operational at ProtoDUNE-SP (right).

In the standard mode of operation, the module performs waveform capture, using either an external or internal trigger. In the latter case the module self-triggers to capture only waveforms

with an amplitude greater than a specified threshold. In ProtoDUNE-SP the photon readout is configured to read waveforms when triggered by a beam event, or to provide header information when self-triggered by cosmic muons. The header portion summarizes pulse amplitude, integrated charge, and time-stamp information of events. The SSP for ProtoDUNE-SP uses Gb Ethernet communication implemented over an optical interface. The 1 Gb/s Ethernet supports full TCP/IP protocol.

The module includes a separate 12-bit high-voltage DAC for each channel to provide bias to each SiPM. Currently there are two DAC options: one with a voltage range of 0 V to 30 V, used with the sensL SiPMs (17 of the 24 SSP units); and the other with a range 0 V to 60 V for use with the Hamamatsu MPPCs (seven of the 24 SSP units). The SSP provides a trigger output signal from internal discriminators in firmware based on programmable coincidence logic, with a standard ST fiber interface to the central trigger board (CTB). Input signals are provided to CTB from the beam instrumentation, the SSPs, and the beam TOF system. The CTB receives timing information from the ProtoDUNE-SP timing system and the CTB trigger inputs are distributed to the experiment via the timing system. To that end, the SSP implements the timing receiver/transmitter endpoint hardware to receive trigger inputs and clock signals from the timing system.

5.3.6.3 Electronics Next Steps

Although the requirements for the electronics system are not all fully established, it not expected that the system requires novel high-risk techniques and can be developed and fabricated well within the schedule for the PDS. In the latter half of CY18, ProtoDUNE-SP test beam and cosmic-ray muon data analysis will provide evaluation of the readout system implemented in ProtoDUNE-SP and the PD Photon Sensor and Simulation groups will provide essential guidance on optimization of performance and cost.

As identified in Section 5.3.5, the most important near term R&D program will be to optimize the ganging scheme including choice of SiPM and cable types. The first objective is to demonstrate that an ensemble of 48 to 72 Hamamatsu 6 mm×6 mm MPPCs can be summed into a single channel by a combination of passive and active ganging. This board will also measure the photoelectron collection efficiency when the SiPMs are coated with TPB as a reference for ARAPUCA measurements with a similar ganging level (the summing board is the same size as the ProtoDUNE-SP ARAPUCA backplane to facilitate the comparisons). Charge processing requires a charge preamplifier ideally located within the cold environment, so the design must take into consideration the failure risks and the power dissipated into the environment.

The timing resolution, minimum threshold and dynamic range requirements for the system are dictated by the physics requirements. These are well known for the higher energy physics (>200 MeV) but, as noted elsewhere in this document, are still evolving for lower energy. Currently, a timing resolution of $1\mu\text{s}$ is called for and the sampling rate and number of sample bits is estimated based on this. For this task some digital process such as a sample interpolation may be proposed, enhancing the recorded raw sample time precision. The light sensitivity and the dynamic range requirement will determine the number of bits and the sample rate required by either waveform or charge collection methods. In both cases, the signal to noise ratio and the power consumption must

be estimated. With this data from ProtoDUNE-SP and the ganging studies, the choice between waveform readout and integrated charge readout will be made taking into account DAQ readout and trigger requirements.

5.4 Production and Assembly

5.4.1 Photon Collector Production

5.4.1.1 ARAPUCA

Although the individual cell dimensions may differ, the basic design of the ARAPUCA-based PD modules for the first SP module is similar to that of the two prototypes produced for ProtoDUNE-SP. Here we describe the production and assembly envisaged based on that experience.

Each ProtoDUNE-SP ARAPUCA module is shaped as a bar with external dimensions of $207.3\text{ cm} \times 9.6\text{ cm} \times 1.46\text{ cm}$, which allows for it to be inserted between the wire planes through 10 slots the APA. The module currently contains sixteen basic ARAPUCA cells, each one with an optical window with an area of $7.8\text{ cm} \times 9.8\text{ cm}$ and internal dimensions of approximately $8\text{ cm} \times 10\text{ cm} \times 0.6\text{ cm}$. The SiPMs are mounted on the backplane of the cell, which in ProtoDUNE-SP, allows for two different configurations of either 12 or 6 passively-ganged SiPMs.

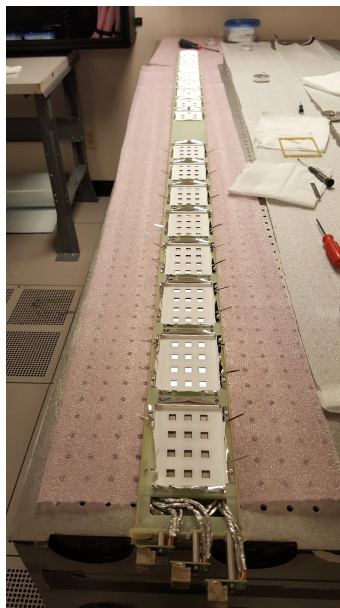


Figure 5.14: ProtoDUNE-SP ARAPUCA modules during assembly prior to installation of the dichroic filters; SiPMs and TPB coated reflector are visible.

The internal surface of the box is lined with a dielectric mirror foil¹³ laser cut with openings at the

¹³3M Vikuiti™ ESR - <http://multimedia.3m.com/mws/media/1932940/vikuiti-tm-esr-application-guidelines.pdf>

locations of the SiPMs; these are visible in Figure 5.14, which shows an ARAPUCA during assembly prior to installation of the optical windows. The backplane SiPM boards for the ProtoDUNE-SP modules were designed at CSU and produced by an external USA vendor¹⁴; the SiPMs were soldered on the boards using a reflow oven at CSU. Before mounting into the ARAPUCA module they were tested at room and LN2 temperatures. It is anticipated that the production of the boards for SP modules will be done outside the USA.

The optical window of each box is a dichroic filter with cut-off at 400 nm. While the filters used for the ProtoDUNE-SP prototypes have been acquired from Omega Optical Inc.¹⁵, other vendors are being considered for the DUNE production¹⁶. Prior to coating, the filters are cleaned according to the procedures given by the manufacturer using isopropyl alcohol. Since the most likely vector for scratching/damaging the coating is dragging contaminated wipes across the surface, new clean lint free wipes are used for each cleaning pass on the surface. Clean filters are then baked at 100°C for 12 hours. The Vikuiti™ foils do not need to be cleaned and baked since they have a protective film that is removed just before the evaporation.

The filters are coated on the external side facing the LAr active volume with pTP, while the internal dielectric mirror side is coated with TPB. The coatings for the ProtoDUNE-SP modules have been made at the Thin Film facility at Fermilab using a vacuum evaporator. Each coated filter was dipped in LN2 to check the stability of the evaporated coating at cryogenic temperature. For ProtoDUNE-SP PD production the evaporation process will be performed at UNICAMP in Brazil, where a large vacuum evaporator with an internal diameter of one meter is now available. The conversion efficiency of the film deposited on the filters or on the Vikuiti™ foils will be measured with a dedicated set-up that will use the 127 nm light produced by a VUV monochromator.

5.4.1.2 Dip-Coated Light Guides

To produce the full-size ProtoDUNE-SP dip-coated light guide bars, the production methods initially developed at MIT for 50.8 cm (20 in) dip-coated light guide bars were scaled up for a facility at FNAL. For ProtoDUNE-SP production four steps will remain essentially the same:

1. Cut and polished UVT acrylic bars are annealed at 180°F in a temperature-controlled oven to prevent subsequent crazing.
2. The TPB-based coating mixture is prepared in a fume hood and poured into an upright vessel located inside a larger enclosed volume.
3. A mechanized system dips the annealed bars into the coating solution where they soak and are then hung to dry in a low humidity environment established through a dry nitrogen purge of the enclosed volume.
4. The coated acrylic bars are placed in a dark box and their attenuation length in air is

¹⁴Advanced Circuits Inc.; www.4pcb.com.

¹⁵<http://www.omegafilters.com/>

¹⁶ASHAI -Japan, Andover-USA, Edmunds Optics-USA

measured with a UV LED that is scanned along the length of the bar.

The coating solution consists of four components in the following ratios: 100 mL 99.9% pure toluene; 25 mL 200 proof ethanol; 0.2 g UVT acrylic pellets; 0.2 g scintillation grade TPB. The TPB and UVT acrylic pellets are first dissolved in a flask filled with toluene and mixed overnight with a teflon-coated magnetic stir bar. Then the ethanol is mixed into the coating solution before it is poured into the dipping vessel. This will produce an optically transparent, TPB-embedded coating, which adheres well to the surface of the bar and has a smooth surface.

A picture of the oven used for annealing, the fume hood used for mixing the coating, the vessel used for dipping, and the dark box used for measuring attenuation lengths for the production of dip-coated light guides for ProtoDUNE-SP is shown in Figure 5.15. These same production methods would also be used for the SP modules, but scaled up to dip and scan multiple bars at the same time. Additionally, multiple production sites would be built to produce dip-coat light guide bars for the SP modules.

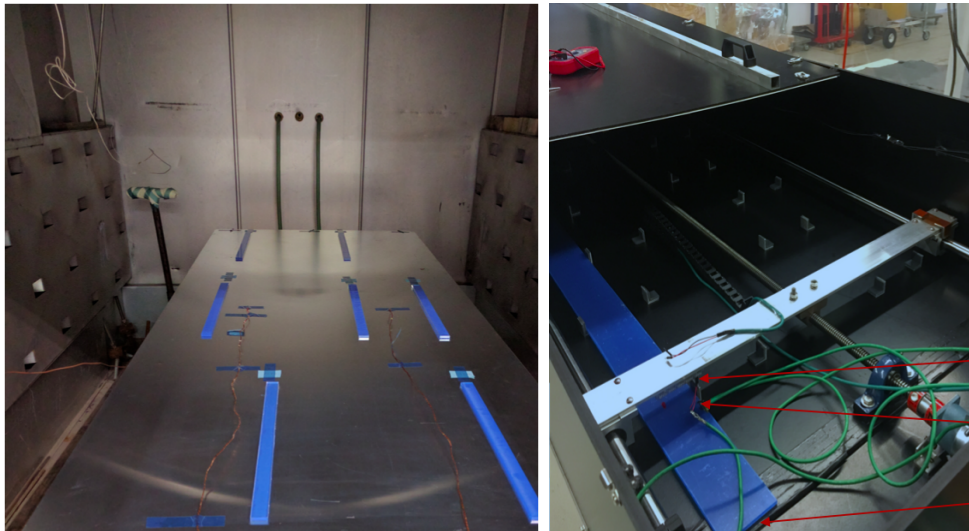


Figure 5.15: ProtoDUNE-SP dip-coated light guide bars production: annealing oven (left); dark box (right)

5.4.1.3 Double-Shift Light Guides

The production and assembly of the double-shift light guide modules has two main components; the wavelength-shifting plates and the EJ-280 light guides. Many of the production, quality assurance, and assembly procedures developed for the double-shift light guide design deployed at ProtoDUNE-SP would remain the same for the SP modules.

WLS Plates Sheets of 0.166 cm (0.0625 in) thick UVT acrylic purchased from McMaster-Carr¹⁷ are laser-cut into 77 cm × 9 cm templates with two 34.2 cm × 8.6 cm plates per template (Figure 5.16 (top)).

¹⁷<https://www.mcmaster.com>.

Each template also includes three small 3.81 cm×2.54 cm pop-out tabs on either side of and between the two plates. After the acrylic templates are coated with TPB these tabs are separated from the plate and tested in a VUV monochromator to determine the quality of the coating on the two associated plates.



Figure 5.16: A laser-cut acrylic template holding two plates and three test tabs (top). TPB-coated acrylic plates after spraying during fabrication of parts for ProtoDUNE-SP (bottom).

Scintillation grade ($\geq 99\%$) TPB is dissolved in dichloromethane (DCM) at a ratio of 5 g TPB per 1000 g DCM. The solution is applied to the templates using a high-volume low-pressure (HVLP) sprayer system under a fume hood. The relatively small number of plates manufactured for ProtoDUNE-SP were sprayed by a technician to approximate an established standard coating thickness measured to have an acceptably high VUV photon conversion efficiency. Figure 5.16(bottom) shows the HVLP spray-coating mount with a coated acrylic template. Two plates and three test tabs can be seen in the HVLP mounting frame. A second sprayed template has been broken at one of the midpoint cuts and positioned in the photo. For ProtoDUNE-SP production, the spray-coating process will be automated or commercialized to accommodate the large-scale production necessary for the SP modules.

After spraying, the acrylic templates are baked in a vacuum oven at 80°C overnight, just below the glass transition point of acrylic. The softened acrylic partially absorbs the TPB into the surface, better affixing the wavelength-shifting coating. Uneven heating during the baking process described above can deform the coated plates, but this is minimized by careful oven fixturing to ensure even heating. After baking, the dimensions of the samples are measured and only plates within the production tolerance are accepted for further testing. To ensure adequate and uniform performance of the coated plates, the conversion efficiency is tested using a VUV monochromator. During ProtoDUNE-SP production, plates were fabricated and tested using a McPherson¹⁸ VUV monochromator with deuterium lamp source to study performance at 127 nm. The full plates were too large for the sample chamber VUV monochromator system, so the testing tabs on either side of each plate were used to constrain the plate's performance. Only plates that exhibit a relative efficiency above an acceptance threshold are shipped to the assembly facility for deployment along

¹⁸<http://mcphersoninc.com>.

a light guide. For ProtoDUNE-SP, a threshold was chosen to accept plates that were comparable or superior to those studied at the Blanche test stand [26] described previously.

WLS-Doped Light Guides The EJ-280 light guides are fabricated and cut to length by Eljen Technologies. Upon receipt, each light guide is unpacked, visually inspected for defects, checked for dimensional tolerance, and scanned using a 430 nm LED to determine its attenuation length in air (Figure 5.17). Since the index of refraction for ~ 500 nm light in LAr is larger than in air and the critical angle for trapping by total internal reflection is correspondingly lower, so attenuation scans of sample light guides were made in both air and LAr (using a movable Am-241 α source) to quantify the correlation between measurements in air and in LAr. Attenuation lengths longer than ~ 5 meters measured in the darkbox correspond to attenuation lengths in LAr longer than ~ 2 meters. An acceptance threshold of 5 meters measured at both ends of an EJ-280 light guide in the darkbox ensures adequate attenuation performance for the modules deployed in the SP modules.

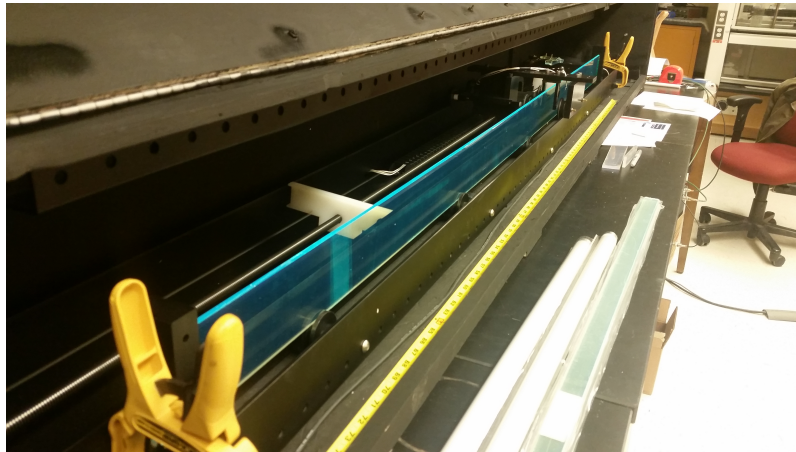


Figure 5.17: EJ-280 light guide in a dark box for attenuation scan QA at Indiana University (prepared for ProtoDUNE-SP).

Visual inspection of light guides received for ProtoDUNE-SP found multiple instances of fogging or mottling on the surface and within the bulk of some light guides. However, these features did not appear to impact the attenuation properties or uniformity during darkbox scans. Acceptance of light guides for shipment to the assembly facility was based on the metrology and attenuation results.

5.4.2 Photon Detector Module Assembly

Final assembly planning for PD modules is guided by the assembly of 60 ProtoDUNE-SP PD modules (representing multiple units of all three varieties) at the Colorado State University assembly facility. ProtoDUNE-SP assembly will occur at one or more assembly facilities, to be determined prior to submission of the TDR. Several features of this are common to all three types of module, and these aspects will be covered in this section.

5.4.3 Incoming Materials Control

All materials for PD module assembly will be delivered with a previously generated QC traveller (in the case of materials custom fabricated for DUNE) or will have an incoming materials traveller generated immediately upon receipt of the component (for commercial components). These travellers will be scanned upon receipt at the assembly facility, and the data stored in the DUNE QC database. Materials will either arrive with a pre-existing DUNE inventory control batch/lot number, or will have one assigned prior to entering the assembly area. Bar code labels attached to storage containers for all components in the assembly area will facilitate traceability throughout the assembly process.

Immediately upon receipt all materials will undergo an incoming materials inspection, including confirmation of key dimensional tolerances as specified on the incoming materials documentation for that component. The results of these inspections will be included on the traveller for that batch/lot and entered into the database.

In the case of discrepancy, the deviation from nominal will be recorded in an exception section of the traveller, as well as the resolution of the discrepancy.

5.4.4 Assembly Area Requirements

Assembly will occur in a class 100,000 or better clean assembly area. Photosensitive components (TPB coated surfaces) are sensitive to near-UV light exposure, and will be protected by blue-filtered light in the assembly area (>400 nm or better filters¹⁹); it has been determined that this level of filtering is sufficient to protect coated surfaces during exposures of up to several days. For exposures of weeks or months, such as in the ProtoDUNE cryostat assembly area, a higher cut-off yellow filter is used²⁰. The requirement for light exposure is to be revisited prior to ProtoDUNE-SP production.

Exposure of photosensitive components will be strictly controlled. Work flow will be restricted to ensure no component exceeds a total exposure of 8 hours to filtered assembly area lighting (including testing time).

5.4.5 Component Cleaning

All components will be cleaned as appropriate, following manufacturer's specifications and DUNE materials test stand recommendations. Cleaning procedures will be written for all incoming materials, and completion of these procedures noted in the appropriate travellers.

¹⁹For example, GAMTUBE T1510 from GAM Products, Inc., <http://www.gamonline.com/catalog/gamtube/index.php>.

²⁰F007-010 Amber with Adhesive - http://www.epakelectronics.com/uv_filter_materials_flexible.htm.

5.4.6 Assembly Procedures

Following the example of the ProtoDUNE-SP experience, detailed, step-by-step written procedure documents will be followed for each module, and a QC traveller for each module is completed and recorded in the database. ProtoDUNE-SP experience suggests that a two-person assembly team is necessary and sufficient for all three currently-considered versions of the light collector modules. Our current assembly plan envisions two 2-person teams operating at the same time, with a fifth person acting as shift leader. The shift leader is not directly involved in assembly, but rather acts as a QC officer responsible primarily for ensuring distributing materials to the assembly teams (documenting the batch/lot numbers for each detector on the relevant module travelers) and ensuring that documented assembly procedures are followed.

Assembly fixtures mounted to 2.4 m long flat optical tables will be used to support and align PD components during assembly. All workers handling PD components will wear gloves, hair nets, shoe covers, and clean room disposable lab jackets at all times.

5.4.7 Post-Assembly Quality Control

Post-assembly QC planning is currently based on ProtoDUNE-SP experience, modified as appropriate for larger-scale production. Each module will go through a series of go-no gauges designed to control tolerances of critical interface points. Following this, each module will be inserted into a test APA support model, representing the tightest slot allowed by APA mechanical tolerances. Next, each module will be scanned at a fixed set of positions (to be determined prior to the TDR) with 275 nm UV LEDs. The detector response at each position will be read out using PD readout electronics, and the data compared to pre-established criteria. Figure 5.18 is a photograph of the scanner used for ProtoDUNE-SP modules. These performance data will serve as a baseline for the module, and will be compared against those taken in an identical scanner shortly before installation into the APA, as in the ProtoDUNE-SP experience. All data collected will be recorded to the module traveler and to the DUNE QC database. As a final QC check, post-assembly immersion into a LN₂ cryostat followed by a repeat scan of each PD module (as in ProtoDUNE-SP) is being considered.

5.4.8 APA Frame Mounting Structure and Module Securing

PD modules are inserted into the APA frames through ten slots (five on each side of the APA frame) and are supported inside the frame by stainless steel guide channels. The slot dimensions for the ProtoDUNE-SP APA frames were 108.0 mm × 19.2 mm wide (see Figure 5.19(top)). These dimensions are expected to increase by about 20% in the next round of APA design revisions, allowing for larger PD modules. The guide channels are pre-positioned into the APA frame prior to applying the wire shielding mesh to the APA frames, and are not accessible following wire wrapping. Following insertion, the PD modules are fixed in place in the APA frame using two stainless steel captive screws, as shown in Figure 5.19(bottom).



Figure 5.18: PD module scanner.

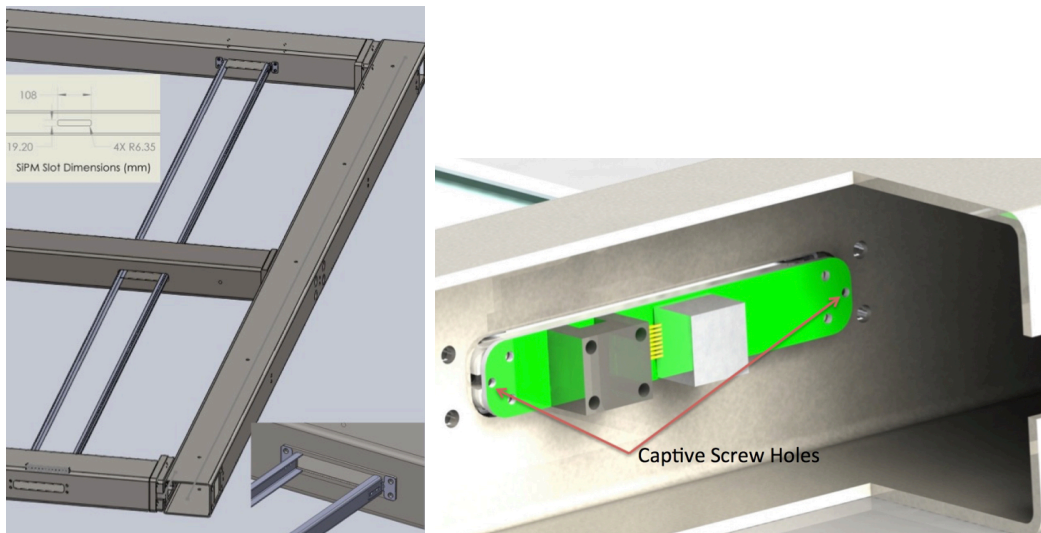


Figure 5.19: PD mounting in APA frame: Rails (top) and securing to the frame with captive screws (bottom).

5.4.8.1 Cryogenic thermal contraction

Bar-style PD modules are structurally composed of primarily polycarbonate, polystyrene and acrylic, which have significantly different shrinkage factors compared to the stainless steel APA and PD support frames (see Table 5.4).

Table 5.4: Shrinkage of PD module materials for a 206°C temperature drop

Material	Shrinkage Factor (m/m)
Stainless Steel (304)	2.7×10^{-3}
FR-4 G-10 (In-plane)	2.1×10^{-3}
Polystyrene (Average)	1.5×10^{-2}
Acrylic and Polycarbonate (Average)	1.4×10^{-2}

These differences in thermal expansion (or contraction, in this case) are an important factor during design of the PD module supports. Mitigation of these contractions is detailed in Table 5.5.

Thermal expansion coefficients (CTEs) for the fused-silica filter plates (1.1×10^{-4} m/m for a 206°C temperature drop) informed the materials selection for the ProtoDUNE ARAPUCA modules. The frame components for the ARAPUCA were fabricated from FR-4 G-10, resulting in a shrinkage of the stainless steel frame structure relative to the frame of approximately 1.2 mm along the long (~ 2 m) axis of the bar. The shrinkage of the frame relative to the filter plate is < 0.2 mm. Both these relative shrinkage factors are accounted for in the dimensions and tolerances of the design.

Table 5.5: Relative Shrinkage of PD components and APA frame, and mitigations.

Interface	Relative shrinkage	Mitigation
PD Length to APA width	PD shrinks 25.7 mm Relative to APA frame	PD affixed only at one end of APA frame, free to contract at other end
Width of PD in APA Slot	PD shrinks 1.2 mm relative to slot width	PD not constrained in C-channels. C channels and tolerances designed to contain module across thermal contraction range
Width of SiPM mount board (<i>Hover board</i>) to stainless steel frame	Stainless frame shrinks 0.06 mm more than PCB	Diameter of shoulder screws and FR-4 board clearance holes selected to allow for motion
Width of SiPM mount board relative to polycarbonate mount block	Polycarbonate block shrinks 1 mm more than PCB	Allowed for in clearance holes in SiPM mount board

5.4.8.2 PD Mount frame deformation under static PD load

FEA modeling of the PD support structure was conducted to study static deflection prior to building prototypes. Modeling was conducted in both the vertical orientation (APA upright, as installed in cryostat) and also horizontal orientation. Basic assumptions used were fully-supported fixed end conditions for the rails, with uniform loading of 3X PD mass (5 kg) along rails. Figure 5.20 illustrates the rail deflection for the APA in the horizontal (left) and vertical (right) orientations. Prototype testing confirmed these calculations.

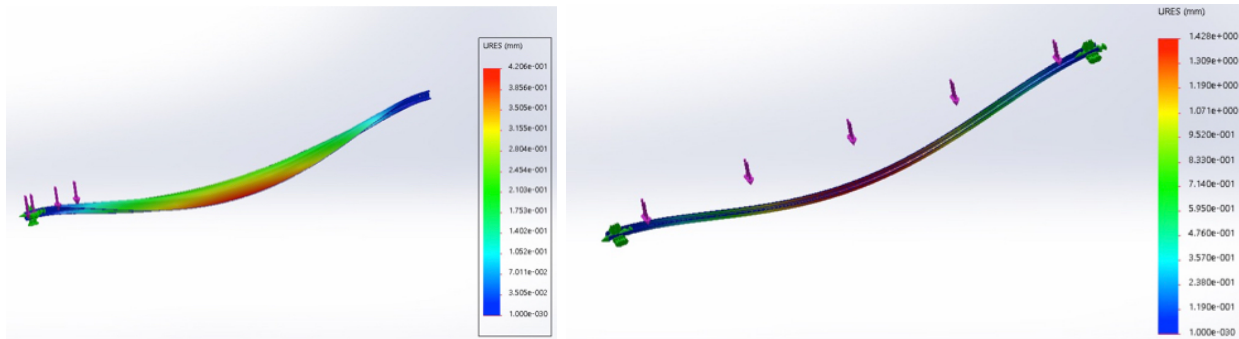


Figure 5.20: PD mechanical support analysis: Rail deflection for the APA in the horizontal (left) and vertical (right) orientations.

5.4.9 Photosensor Modules

Depending on the photon collector technology selected, the SiPM analog signal will be ganged in groups of 6-48 in close proximity to the sensors inside the LAr volume; both *passive* and *active* ganging schemes are under consideration. Passive ganging (sensors in parallel) implemented with traces on the SiPM mounting board (module) and has been implemented for ProtoDUNE-SP. The SiPMs are mounted using a pick-and-place machine and standard surface mount device soldering procedures. The ganged analog signals are then brought out via long cables (approximately 25 m) for digitization outside the cryostat. ProtoDUNE-SP will provide essential operational experience with a passive ganging board and signal transport provided by Teflon ethernet CAT6 cables. It is already apparent that R&D is needed to optimize the connectors used to couple the cable to the board; it is a priority to understand the mechanical stresses involved in the SiPM-PCB-Connector system (with different CTEs) as it is cooled (or cycled) to cryogenic temperatures.

A basic level of active ganging locates summing circuitry on the board carrying the photosensors or on a separate PCB also mounted on the PD module. A more complex scheme is being considered that would include cold amplifiers and ADCs. This solution would provide more flexibility in the level of photosensor ganging and also obviate the need for carrying analog signals of long cables. Production of the board would follow standards practices but the complexity introduces concerns with reliability and long-term stability issues related to cold electronics. Basic active ganging prototypes are under study with high priority but the design is not yet at a mature stage.

5.4.10 Electronics

Extensive experience of manufacturing processes was gained during the development of the SSPs under current use on ProtoDUNE-SP, a general description of the readout system of ProtoDUNE-SP can be seen in the section 5.3.6. Compatibility between elements designed by different institutions is guaranteed when standard procedures are followed so the circuit design must be done in accordance with mutually agreed-upon specification documents. A sufficient number of units needs to be produced to allow local testing and for testing in the central facility – for example, in ProtoDUNE-SP 5 12-channel SSPs were produced and delivered to CERN for integration testing prior. Twenty-four were fabricated for ProtoDUNE-SP operation.

The readout electronics of the photon detection system will be designed and produced with similar tools and protocols used for ProtoDUNE-SP. For example: printed circuit board (PCB) layout is performed in accordance with IPC²¹ specifications. Bare PCB manufacturing requirements are embedded within the Gerber file fabrication documents (e.g., layers, spacing, impedance, finish, testing, etc.). Components are assembled on to circuit boards using either trained PD consortium technical staff or by external assembly vendors, based upon volume, in accordance with per-design assembly specification documents. Testing occurs at labs and universities within the collaboration in accordance with a per-design test procedure that typically includes a mix of manual, semi-automatic and automated testing in an engineering test bench followed by overall characterization in a system- or subsystem-test stand. Other considerations and practices relevant to readout electronics production and assembly are itemized here:

- Components: Schematic capture is done using appropriate tools (such as OrCAD 16.6.²² or similar toolset) available within design facility. Design is hierarchical with common front-end page referenced multiple times to ensure that all input channels are identical. The schematic contains complete bill-of-materials (BOM) including all mechanical parts. Subversion repository is typically used for version control and backup. Multiple internal design reviews held before schematic is released to layout. The bill of materials is stored directly within schematic, extracted to spreadsheet when ordering parts. Every part is specified by both manufacturer and distributor information. Distributor information may be overridden by a technician at order time due to price or availability. Standard search engines such as Octopart²³, ECIA²⁴ and PartMiner²⁵ are used to check price or availability across all standard distributors. A parts availability check review is performed prior to handoff from schematic to layout; as required obsolete or long lead time parts were removed from design and replaced. BOM information will include dielectric, tolerance, temperature coefficient, voltage rating and size (footprint) to ensure all parts are fully described.
- Boards: There are standard tools (such as the Allegro²⁶ toolset) available for the printed-circuit-board (PCB) layout. Conventional PCBs are realized as multi-layer, controlled impedance board with many sets of delay-matched nets. In usual practice the complete impedance and

²¹IPCTM, Association Connecting Electronics Industries, <http://www.ipc.org/>.

²²OrCADTM schematic design tool for PCB design <http://www.orcad.com>

²³Octopart <https://octopart.com/>

²⁴ ECIA <https://www.eciaauthorized.com>

²⁵PartMiner <https://www.part-miner.com/>

²⁶Cadence Allegro[®]PCB design solution <https://www.cadence.com>

delay characteristics are calculated within layout tool and crosschecked by PCB vendor prior to manufacture. In usual practice, a competitive bid between multiple previously qualified vendors is used, with a full electrical and impedance testing required. Multiple internal design reviews are held prior to release of the design.

- Cable plant: Cabling will be designed taking into consideration the APA space and in close collaboration with the TPC electronics group to avoid cross-talk effects. A final decision on cable procurement will be taken based on the possibility of cable manufacturing in an institution belonging to the photon detection consortium and the cost of a commercial solution.
- Manufacturer list: In addition to the general laboratory procedures for quality assurance, the general practice will be to use only printed circuit board manufacturers and external assembly vendors whose workmanship and facilities have been personally inspected by experienced production team members. All external assemblers are required to quote in accordance with an assembly specifications document describing the IPC class and specific solder chemistry requirements of the design. The bill of materials document will show selected and alternate suppliers for every component of the front-end boards.
- FRONT-END (FE) electronics firmware: This will be specified and updated iteratively in collaboration with other systems. The electronics working group will be responsible for responding to requests for additional firmware development, including for example, modifications to timing interface, modifications to trigger interface, and implemented sensitivity to in-spill vs. not-in-spill conditions. Documents describing firmware architecture for each major change will be written and distributed to PD and DAQ working groups before implementation. FE electronics user's manual containing all details of new firmware will be distributed with production units when manufactured.
- Mechanical assembly: With the mechanical assembly of electronics readout boards it is common practice to use AutoCAD²⁷ with Allegro (as PCB layout tool). All relevant dimensions of the PC board including connector and indicator placement is extracted from Allegro as base DXF file from which overall exploded mechanical diagram of chassis and other mechanical parts is made. Mechanical items such as shield plates will be provided as well. It is assumed that the front-end chassis will be made by external vendors (one for chassis, one for front/back panels) from AutoCAD drawings provided by the consortium.

5.5 System Interfaces

This section describes the interface between the SP module PDS and several other consortia, task forces (TF) and subsystems listed below:

- APA,
- feedthroughs,

²⁷AutoDESK AutoCAD@computer aided design software application <https://www.autodesk.com/>

- TPC CE,
- CPA / HV System – if the coated-reflector foils option is implemented,
- DAQ,
- Calibration and monitoring.

The contents of the section are focused on what is needed to complete the design, fabrication, installation of the related subsystems, and are organized by the elements of the scope of each subsystem at the interface between them.

5.5.1 Anode Plane Assembly

The PD is integrated in the APA frame to form a single unit for the detection of both ionization charge and scintillation light. The hardware interface between APA and PDS is both mechanical and electrical:

- Mechanical: (1) supports for the PDS detectors; (2) access slots for installation of the detectors; (3) access slots for the cabling of the PD detectors; d) routing of the PDS cables inside the side beams of the APA frame.
- Electrical: grounding scheme and electrical insulation, to be defined together with the CE consortium, given the CE strict requirements on noise.

5.5.2 Feedthroughs

Several PD SiPM signals are summed together into a single readout channel. A long multi-conductor cable with four twisted pairs read out the PD module. Analog signals from the SiPMs are transmitted directly by cables to the appropriate flanges to outside the cryostat. All cold cables originating from the inside the cryostat connect to the outside warm electronics through PCB board feedthroughs installed in the signal flanges that are distributed along the cryostat roof.

All technical specifications for the feedthroughs should be provided by the photon detector group.

5.5.3 TPC Cold Electronics

The hardware interfaces between the CE and PD occur in the feedthroughs and the racks mounted on the top of the cryostat which house low and high voltage power supplies for PD, low and bias voltage power supplies for CE, as well as equipment for the cryogenic instrumentation and slow controls (CISC), and possibly DAQ consortia. There should be no electrical contact between the

PDS and CE components except for sharing a common reference voltage point (ground) at the feedthroughs. An additional indirect hardware interface takes place inside the cryostat where the CE and PD components are both installed on the APA (responsibility of the single phase far detector APA consortium, APA in the following), with cables for CE and PD that may be physically located in the same space in the APA frame, and where the cables and fibers for CE and PD may share the same trays on the top of the cryostat. These trays are the responsibility of the facility and the installation of cables and fibers will follow procedures to be agreed upon in consultation with the underground installation team, underground installation team (UIT) in the following.

In the current design CE and PD use separate flanges for the cold-to-warm transition and each consortium is responsible for the design, procurement, testing, and installation, of their flange on the feedthrough, together with LBNF, who is responsible for the design of the cryostat. The installation of the racks on top of the cryostat is a responsibility of the facility, but the exact arrangement of the various crates inside the racks will be reached after common agreement between the CE, PD, CISC, and possibly DAQ consortia. The PD and CE consortia will retain all responsibilities for the selection, procurement, testing, and installation of their respective racks, unless for space and cost considerations an agreement is reached where common crates are used to house low voltage or high/bias voltage modules for both PDS and CE. Even if both CE and PD plan to use floating power supplies, the consequences of such a choice on possible cross-talk between the systems needs to be studied.

Various test stands and integration facilities will be developed. In all cases the CE and PD consortia will be responsible for the procurement, installation, and initial commissioning of their respective hardware in these common test stands. The main purpose of these test stands is study the possibility that one system may induce noise on the other, and the measures to be taken to minimize this cross-talk. For these purposes, it is desirable to repeat noise measurements whenever new, modified detector components are available for one or the other consortium. This requires that the CE and PD consortia agree on a common set of tests to be performed and that the CE consortium can operate the PDS detectors within a pre-determined range of operating parameters, and vice versa, without the need of providing personnel from the PDS consortium when the CE consortium is performing tests or vice versa. Procedures should be set in place to decide the time allocation to tests of the components of one or the other consortium.

5.5.4 Cathode Plane Assembly and High Voltage System

The PD and the HV systems interact in the case that the former includes wavelength-shifting reflector foils mounted on the cathode plane array (CPA). An additional interface is addressed in Section 5.5.6.

The purpose of installing the wavelength-shifting (wavelength shifting (WLS)) foils is to allow enhanced detection of light from events near to the cathode plane of the detector. The WLS foils consist of a wavelength shifting material (such as TPB) coated on a reflective backing material. The foils would be mounted on the surface of the CPA in order to enhance light collection from events occurring nearer to the CPA, and thus greatly enhancing the spatial uniformity of the light

collection system as detected at the APA mounted light sensors. The foils may be laminated on top of the resistive Kapton surface of the CPA frames, with the option of using metal fasteners or tacks that would also serve to define the field lines.

Production of the FR4+resistive Kapton CPA frames are the responsibility of the HV consortium. Production and TPB coating of the WLS foils will be the responsibility of the Photon Detection consortium. The fixing procedure for applying the WLS foils onto the CPA frames and any required hardware will be the responsibility of the Photon Detection consortium, with the understanding that all designs and procedures will be pre-approved by the HV consortium.

This new detector component is not being tested in ProtoDUNE-SP, however its integration in the present SP module HV system could imply performance and stability degradation (due for example to ion accumulation at the CPA surface); the assembly procedure of the CPA/FC module could become more complex due to the presence of delicate WLS foils. Intense R&D will be required before deciding on its implementation.

An integration test stand will likely be employed to verify the proper operation of the CPA panels with the addition of WLS foils under high voltage conditions. Light performance (wavelength conversion and reflectivity efficiency) will also be verified. The HV consortium will be responsible for HV aspects of the test stand and the PD consortium will be responsible for the light performance aspects.

5.5.5 Data Acquisition

The main system interfaces include:

Data Physical Links: Data are passed from the PD to the DAQ on optical links conforming to an IEEE Ethernet standard. The links run from the PD readout system on the cryostat to the DAQ system in the Central Utilities Cavern (central utility cavern (CUC)).

Data Format: Data are encoded using a data format based on UDP/IP. The data format is derived from the one used by the Dual Phase TPC readout. Details will be finalized by the time of the DAQ TDR.

Data Timing: The data must contain enough information to identify the time at which it was taken.

Trigger Information: The PD may provide summary information useful for data selection. If present, this will be passed to the DAQ on the same physical links as the remaining data.

Timing and Synchronization: Clock and synchronization messages will be propagated from the DAQ to the PD using a backwards compatible development of the ProtoDUNE-SP Timing System protocol (DUNE docdb-1651). There will be at least one timing fiber available for each data links coming from the PDS. Power-on initialization and Start of Run setup: The PDS may require initialization and setup on power-on and start of run. Power on initialization should not

require communication with the DAQ. Start run/stop run and synchronization signals such as accelerator spill information will be passed by the timing system interface.

Interaction with other groups: Related interface documents describe the interface between the CE and LBNF, DAQ and LBNF, DAQ and Photon and both DAQ and CE with Technical Coordination. The cryostat penetrations including through-pipes, flanges, warm interface crates and feedthroughs and associated power and cooling are described in the LBNF/PDS interface document. The rack, computers, space in the CUC and associated power and cooling are described in the LBNF/DAQ interface document. Any cables associated with photon system data or communications are described in the DAQ/Photon interface document. Any cable trays or conduits to hold the DAQ/CE cables are described in the LBNF/Technical Coordination interface documents and currently assumed to be the responsibility of Technical Coordination.

Integration: Various integration facilities are likely to be employed, including vertical slice tests stands, PDS test stands, DAQ test stands and system integration/assembly sites. The DAQ consortia will provide hardware and software for a vertical slice test. The PD consortium will provide PD emulators and PD readout hardware for DAQ test stands. (The PD emulator and PD readout hardware may be the same physical object with different configuration). Responsibility for supply and installation of DAQ/PD cables in these tests will be defined by the time of the DAQ TDR.

5.5.6 Calibration and Monitoring

This subsection defines the internal calibration system for the SP PDS. It may be interfaced to a calibration consortium later.

It is proposed that the SP PDS gain and timing calibration system, a pulsed UV-light system, also be used for PD monitoring purposes during both commissioning and experimental operation. The hardware consists of warm and cold components.

By placing light sources and diffusers on the cathode planes designed to illuminate the anode planes, the PDs embedded in the anode plane assemblies can be illuminated. Cold components (diffusers and fibers) interface with HV and are described in a separate interface document. Warm components include controlled pulsed-UV source and warm optics. These warm components interface calibration and monitoring with the CISC and DAQ subsystems, and are described in corresponding documents. Optical feedthrough is a cryostat interface.

Hardware components will be designed and fabricated by SP-PDS. Other aspects of hardware interfaces are described in the following. The CTF and PDS groups might share rack spaces that needs to be coordinated between both groups. There will not be dedicated ports for all calibration devices. Therefore, multi-purpose ports are planned to be shared between various groups. CTF and SP-PD will define ports for deployment. It is possible that SP-PD might use Detector Support Structure (DSS) ports or TPC signal ports for routing fibers. The CTF in coordination with other groups will provide a scheme for interlock mechanism of operating various calibration devices (e.g. laser, radioactive sources) that will not be damaging to the PD.

5.6 Installation, Integration and Commissioning

5.6.1 Transport and Handling

Following assembly and testing of the PD modules they will be packaged and shipped to the FD site for checkout and any final testing prior to installation into the cryostat. Handling and shipping procedures will depend on the environmental requirements determined for the photon detectors, and will be specified prior to the TDR.

A testing plan will be developed to determine environmental requirements for photon detector handling and shipping. The environmental conditions apply for both surface and underground transport, storage and handling. Requirements for light (UV filtered areas), temperature, and humidity exposure will also be developed.

Handling procedures that ensure environmental requirements are met will be developed. This will include handling at all stages of component and system production and assembly, testing, shipping, and storage. It is likely that PD modules and components will be stored for periods of time during production and prior to installation into the FD cryostats. Appropriate storage facilities need to be constructed at locations where storage will take place. Shipping and storage containers need to be designed and produced. Given the large number of photon detector modules to be installed in the FD, it will be cost effective to take advantage of reusable shipping containers.

Documentation and tracking of all components and PD modules will be required during the full production and installation schedule. Well defined procedures will be in place to ensure that all components/modules are tested and examined prior to, and after, shipping. Information coming from such testing and examinations will be stored in a hardware database.

An Integration and Test Facility (ITF) will be constructed at a location to be decided by the collaboration/project for the integration of the PDs into anode plane assemblies. Transportation to and from ITF should be carefully planned. The PDS units will be shipped from the production area in quantities compatible with the APA transport rates.

Operations: The PDS deliveries will be stored in temperature and humidity controlled storage area. Their mechanical status will be inspected.

Transportation to SURF: The delivery to SURF will be such that the storage time before integration will be at most two weeks.

5.6.2 Integration with APA and Installation

PD modules integration into the APA frame will happen at the Integration facility. Experts from both groups will work with the installation team. An electrical test with APA/PDS/CE will be performed at the integration facility in a cold box, after the integration of PDS and CE on the

APA frame has been completed.

The APA consortium will be responsible for the transportation of the integrated APA frames from the integration facility to the LBNF/SURF facility. The UIT team, under supervision of the APA group, will be responsible to move the equipment into the clean room. Work on the 2-APA connection and inspection underground, prior to installation in the cryostat, is performed by the APA group. Work on cabling during this assembly process is performed by PDS and CE groups under supervision of the APA group. Once the anode plane assemblies will be moved inside the cryostat, the PDS and CE consortia will be responsible for the routing of the cables in the trays hanging from the top of the cryostat.

5.6.3 Installation into the Cryostat and Cabling

The PD modules are installed into the anode plane assemblies. There are ten PD's per APA, inserted into alternating sides of the APA frame, five from each direction. Once a PD is inserted, it is attached mechanically to the APA frame and cabled up with a single power/readout cable. Following PD installation cold electronics (CE) units are installed at the top of the APA frame.

After the APA has been integrated with the PDS and CE, it will be moved via the rails in the clean room to the integrated cold test stand for testing and be moved into the cryostat. The two anode planes of the TPC will be assembled inside the cryostat, each of the fully tested anode plane assemblies mechanically linked together. Signal cables from the TPC readout and the PD modules are routed up to the feedthrough flanges on the cryostat top side. The cables from each of the CE and PD's on the APA are then routed and connected to the final flanges on the cryostat.

5.6.4 Calibration and Monitoring

Commissioning of the SP module PDS will rely heavily on the readout electronics, DAQ, and calibration and monitoring system. Deployment and testing of the readout electronics separately from the in situ installation of photon detector modules in the APA is important to establish their proper functioning before connection to the photon detectors or their flanges. Careful checking at each step of the integration process will help to find unexpected problems early enough to be corrected before individual units are mounted into the larger systems (first in the APA then after installation in the cryostat).

Once the electronics are read out via the DAQ system, it will be appropriate to add the PD modules and continue commissioning of the installed system. In order to be properly tested the PD modules will have to be in the dark. Making sure it is possible to make this check frequently enough to catch problems early is critical. This will have to be balanced with the needs of installation, as work progresses.

Once the basic operation of the readout system is established, the calibration and monitoring system will be of great use during the commissioning. While the background signals from the

warm photon detectors may make calibration difficult, the monitoring system will be able to flash UV light to excite the PD modules. These light signals can be used to determine that cabling is connected, and connected properly by looking at light from different UV emitters. Once the detector is beginning to cool down, the operation of the calibration and monitoring system will become even more important as the monitoring of the individual channels should be a good indication of their proper operation, and again, the proper cabling and interface.

5.7 Quality Assurance and Quality Control

5.7.1 Design Quality Assurance

PD design quality assurance (QA) focuses on ensuring that the detector modules meet the following goals:

- Physics goals as specified in the DUNE requirements document,
- Interfaces with other detector subsystems as specified by the subsystem interface documents,
- Materials selection and testing to ensure non-contamination of the LAr volume.

The PDS consortium will perform the design and fabrication of the components in accordance with the applicable requirements of the LBNF/DUNE Quality Assurance Plan. If the institute (working under the supervision of the consortium) performing the work has a documented QA program the work may be performed in accordance with their own program.

Upon completion of the PDS design and QA/quality control (QC) plan there will be a preliminary design review process, with the reviewers charged to ensure that the design demonstrates compliance with the goals above.

5.7.2 Production and Assembly Quality Assurance

The photon detector system will undergo a QA review for all components prior to completion of the design and development phase of the project. The ProtoDUNE-SP test will represent the most significant test of near-final PD components in a near-DUNE configuration, but additional tests will also be performed. The QA plan will include, but not be limited to, the following areas:

- Materials certification (in the FNAL materials test stand and other facilities) to ensure materials compliance with cleanliness requirements
- Cryogenic testing of all materials to be immersed in LAr, to ensure satisfactory performance through repeated and long-term exposure to LAr. Special attention will be paid to cryogenic

behavior of plastic materials (such as radiators and light guides), SiPMs, cables and connectors. Testing will be conducted both on small-scale test assemblies (such as the small test cryostat at CSU) and full-scale prototypes (such as the full-scale CDDF cryostat at CSU).

- Mechanical interface testing, beginning with simple mechanical go-nogo gauge tests, followed by installation into the ProtoDUNE-SP system, and finally full-scale interface testing of the PDS into the final pre-production TPC system models
- Full-system readout tests of the PD readout electronics, including trigger generation and timing, including tests for electrical interference between the TPC and PD signals.

Prior to the release of the TDR the PDS will undergo a final design review, where these and other QA tests will be reviewed and the system declared ready to move to the pre-production phase.

5.7.3 Production and Assembly Quality Control

Prior to the start of fabrication, a manufacturing and QC plan will be developed detailing the key manufacturing, inspection and test steps. The fabrication, inspection and testing of the components will be performed in accordance with documented procedures. This work will be documented on travelers and applicable test or inspection reports. Records of the fabrication, inspection and testing will be maintained. When a component has been identified as being in noncompliance to the design, the nonconforming condition shall be documented, evaluated and dispositioned as use-as-is (does not meet design but can meet functionality as is), rework (bring into compliance with design), repair (will be brought into meeting functionality but will not meet design) and scrap. For products with a disposition of accept as is or repair, the nonconformance documentation shall be submitted to the design authority for approval.

All QC data (from assembly and pre- and post-installation into the APA) will be directly stored to the DUNE database for ready access of all QC data. Monthly summaries of key performance metrics (TBD) will be generated and inspected to check for quality trends.

Based on the ProtoDUNE-SP model, we expect to conduct the following production testing:

- Dimensional checks of critical components and completed assemblies to insure satisfactory system interfaces.
- Post-assembly cryogenic checkouts of SiPM mounting PCBs (prior to assembly into PD modules).
- Cryogenic testing of completed modules (in CSU CDDF or similar facility) to provide a final pre-shipping module test.
- Warm scan of complete module using motor-driven LED scanner (Or UV LED array).
- Complete visual inspection of module against a standard set of inspection points, with pho-

tographic records kept for each module.

- End-to-end cable continuity and short circuit tests of assembled cables.
- FE electronics functionality check.

5.7.4 Installation Quality Control

PDS pre-installation testing will follow the model established for ProtoDUNE-SP. Prior to installation in the APA, the PD modules will undergo a warm scan in a scanner identical to the one at the PD module assembly facility and the results compared. In addition, the module will undergo a complete visual inspection for defects and a set of photographs of all optical surfaces taken and entered into the QC record database. Following installation into the APA and cabling an immediate check for electrical continuity to the SiPMs will be conducted.

It is expected that following the mounting of the TPC cold electronics and the photon detectors the entire APA will undergo a cold system test in a gaseous argon cold box, similar to that performed during ProtoDUNE-SP. During this test, the PDS system will undergo a final integrated system check prior to installation, checking dark and LED-stimulated SiPM performance for all channels, checking for electrical interference with the cold electronics, and confirming compliance with the detector grounding scheme.

5.8 Safety

Safety management practices will be critical for all phases of the photon system assembly and testing. Planning for safety in all phases of the project, including fabrication, testing and installation will be part of the design process. The initial safety planning for all phases will be reviewed and approved by safety experts as part of the initial design review. All component cleaning, assembly, testing and installation procedure documentation will include a section on safety concerns relevant to that procedure, and will be reviewed during the appropriate pre-production reviews.

Areas of particular importance to the PDS include:

- Hazardous chemicals (particularly WLS chemicals such as TPB used in radiator bar dipping and spraying) and cleaning compounds: All chemicals used will be documented at the consortium management level, with MSDS and approved handling and disposal plans in place.
- Liquid and gaseous cryogenics used in module testing: Full hazard analysis plans will be in place at the consortium management level for all module or module component testing involving cryogenic hazards, and these safety plans will be reviewed in the appropriate pre-production and production reviews

- High voltage safety: Some of the candidate SiPMs require bias voltages above 50 VDC, which may be a regulated voltage as determined by specific labs and institutions. Fabrication and testing plans will demonstrate compliance with local HV safety requirements at the particular institution or lab where the testing or operation is performed, and this compliance will be reviewed as part of the standard review process.
- UV and VUV light exposure: Some QA and QC procedures used for module testing and qualification may require use of UV and/or VUV light sources, which can be hazardous to unprotected operators. Full safety plans must be in place and reviewed by consortium management prior to beginning such testing.
- Working at heights, underground: Some aspects of PDS module fabrication, testing and installation may require working at heights, or deep underground. Safety considerations will be taken into consideration during design and planning for these operations, all procedures will be reviewed prior to implementation, and all applicable safety requirements at the relevant institutions will be observed at all times.

5.9 Organization

5.9.1 Consortium Organization

The SP PDS consortium follows the typical organizational structure of DUNE consortia:

- A consortium lead provides overall leadership for the effort, and attends meetings of the DUNE Executive and Technical Boards.
- A technical lead provides technical support to the consortium lead, attends the Technical Board and other project meetings, oversees the project schedule and work breakdown structure (WBS), and oversees the operation of the project working groups. In the case of the PDS, the technical lead is supported by a deputy technical lead.

Below the leadership, the consortium is divided up into five working groups, each led by two or three working group conveners as shown in Figure 5.21. Each working group is charged with one primary area of responsibility within the consortium, and the conveners report directly to the technical lead regarding those responsibilities. As the consortium advances to a more detailed WBS and project schedule, it is envisioned that each working group will be responsible for one section of those documents.

The working group conveners are appointed by the PDS project lead and technical lead, and the structure may evolve as the consortium matures and additional needs are identified.

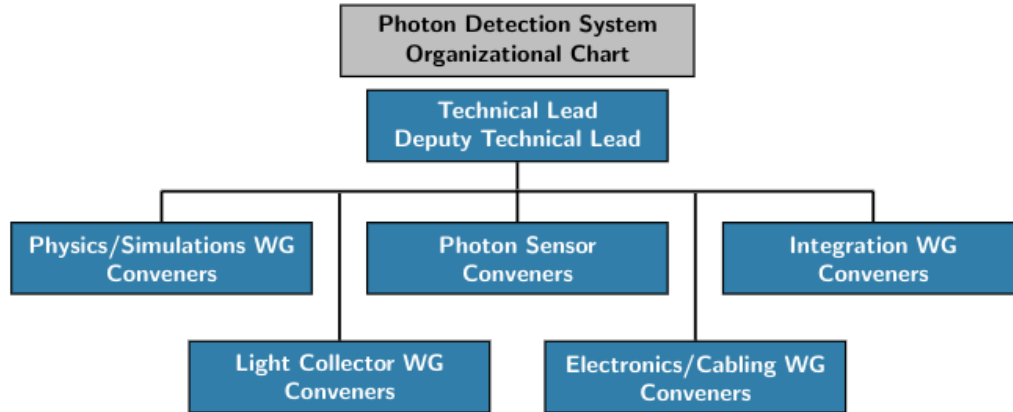


Figure 5.21: PDS consortium organization chart.

5.9.2 Planning Assumptions

Plans for the PDS consortium are based on the overall schedule for the DUNE FD. In particular, the APA schedule defines the time window for the completion of the final development program for the light collectors: A final down-select to a baseline light collector option, photosensors, and FE electronics must be made by late February 2019. Due to the early stage of development for the ARAPUCA light collector system, we may maintain an alternate light collector option up to the pre-production review in September of 2020, but all other systems must be defined prior to the TDR.

For planning purposes, we assume that the PDS modules will undergo final assembly and testing at one or more PDS assembly facilities, with an initial assembly rate of approximately twenty modules per week, accelerating to forty modules per week in the second half of module fabrication.

We further assume that the modules will be shipped from the fabrication facilities to a detector integration facility, at a site to be determined later, to be integrated along with the CE into the APA frames and cold tested in a cryogenic test facility. We plan for an initial rate of two anode plane assemblies per week, with the possibility of accelerating to four anode plane assemblies per week as production lessons are learned. PDS personnel will be present at the integration facility to oversee the installation and testing.

Meeting this timeline requires that the development of the ARAPUCA system be aggressively pursued throughout 2018, with a goal of testing near-final prototypes in the late fall of 2018 and allowing technology comparisons between the ARAPUCA and the light guide technologies in winter of 2019.

Additional development efforts prior to the TDR will focus on:

- Identifying and selecting reliable cryogenic photosensor (SiPM) candidates,

- Reducing cost and optimizing performance of FE electronics,
- Solidifying PDS performance requirements from additional physics simulation efforts.

We assume that apart from these items, where rapid development is still required, most of the detector components to be delivered by the PD consortium will require only minor changes relative to the ProtoDUNE-SP components. For this reason, modifications of these other detector components will be delayed until 2019, which will also help with the funding profile. Exceptions will be made for further development in test stands with regard to cabling studies, and for the interface engineering required to ensure satisfactory integration of the PD with the APA and CE systems.

5.9.3 High-Level Schedule

Table 5.6: Pre-TDR key milestones.

Milestone	Date
Preliminary PD technology selection criteria determined	03/21/18
Results from final prototype light collector studies available	02/21/19
Final PD technology selection criteria available	02/21/19
Down-select to primary (and potential alternate) light collector technology	02/22/19
Submit initial TDR draft for internal review	03/29/19

High-level post-TDR milestones are listed in Table 5.7.

Table 5.7: Post-TDR key milestones.

Milestone	Date
PD pre-production review(s) complete	03/2020
Initial PD module fabrication begins	09/2020
Final PD production review based on initial production QA	02/2021
First PD modules delivered for installation	05/2021
Installation into anode plane assemblies begins	06/2021
PD fabrication complete (first SP module)	07/2023

Chapter 6

Data Acquisition System

6.1 Data Acquisition (DAQ) System Overview

6.1.1 Introduction

The DUNE far detector (FD) data acquisition (DAQ) system must enable the readout, triggering, processing and distribution to permanent storage of data from all detector modules, which includes both their electrical time projection chamber (TPC) and optical photon detection system (PDS) signals. The final output data must retain, with very high efficiency and low bias, a record of all activity in the detector that pertains to the recognized physics goals of the DUNE experiment. The practical constraints of managing this output requires that the DAQ achieve these goals while reducing the input data volume by almost four orders of magnitude.

The current generation of liquid argon time-projection chamber (LArTPC) DAQs, such as used in ProtoDUNE and MicroBooNE, produce data spanning a fixed window of time that is chosen based on the acceptance of an external trigger. The DUNE DAQ faces several major challenges beyond those of the current generation. Foremost, it must accept data from about two orders of magnitude more channels and from that data it must form its own triggers. This self-triggering functionality requires immediate processing of the full-stream data from a large portion of all TPC channels with a throughput of approximately one terabyte per second per detector module. From this data stream, triggers must be raised based on two very different patterns of activity. The first is activity localized in a small region of one detector module, such as due to beam neutrino interactions or the passage of relatively rare cosmic-ray muons. This activity tends to correspond to a relatively large deposition of energy, around 100 MeV or more. The second pattern that must lead to a trigger is lower energy activity dispersed in both time and spatial extent of the detector module, such as due to a supernova neutrino burst (SNB).

The DAQ must also contend with a higher order of complexity compared to the current generation. The FD is not monolithic but ultimately will consist of four detector modules each of 10 kt fiducial

mass. Each module will implement somewhat different technologies and the inevitable asymmetries in the details of how data are read out from each must be absorbed by the unified DAQ at its front end. Further, each detector module is not monolithic but has at least one layer of divisions, here generically named detector units. For example, the single-phase (SP) detector module has anode plane assemblies (APAs) each providing data from a number of warm interface boards (WIBs) and the dual-phase (DP) detector module has charge readout (CRO) and light readout (LRO) units associated with specific electronics crates. In each detector module, there are on the order of 100 detector units (150 for SP and 245 for DP) and each unit has a channel count that is of the same order as that of an entire LArTPC detector of the current generation. The DUNE DAQ, composed of a cohesive collection of DAQ instances called DAQ partitions, must run on a subset of all possible detector units for each given detector module. Each instance effectively runs independently of all the others, however some instances indirectly communicate through the exchange of high-level trigger information. This allows, for example, each detector module to take data in isolation. It also allows for all detector modules to contribute to forming and accepting global SNB triggers, and to simultaneously run small portions – consisting of a few detector units – separately in order to debug problems, run calibrations or perform other activities while not interfering with nominal data taking in order to maintain high uptime.

Substantial computing hardware is required to provide the processing capability needed to identify such activity while keeping up with the rate of data. The nature of various technical, financial and physical constraints leads to the need for much of the computing hardware required for this processing to reside underground, near the detector modules. In such an environment, power, cooling, space, and access is far more costly than in typical data centers.

Past LArTPC and long-baseline (LBL) neutrino detectors have successfully demonstrated external triggering using information related to their beam. The DUNE FD DAQ will accept external information on recent times of Main Injector beam spills from Fermilab. This will assure triggering with high efficiency to capture activity pertaining to interactions from the produced neutrinos.

However, even if the DUNE experiment were interested only in neutrinos from beam spills, an external beam trigger alone would not be sufficient. Absent any other information, such a trigger must inevitably call for the readout of all possible data from the FD over at least one LArTPC drift time. This would lead to an annual data volume approaching an exabyte (10^{18} bytes), the vast majority of which would consist of just noise. This entire data volume would have to be saved to permanent storage and then processed offline in order to get to the signals.

DUNE's physics goals of course extend beyond beam-related interactions, including cosmic-ray muons, which provide an important source of detector calibration, and atmospheric neutrino interactions, which give a secondary source from which to measure neutrino properties. Taken together, recording their activity will dominate the data rate. The DAQ must also record data with sensitivity to rare interactions (both known and hypothetical) such as nucleon decay, other baryon number violating processes (such as neutron-antineutron oscillation), and interactions from the products of SNBs as well as possibly being able to observe isolated low-energy interactions from solar neutrinos and diffuse supernova neutrinos.

Some of these events, while rare in themselves, produce patterns of activity that can be mimicked by other higher-rate backgrounds, particularly in the case of SNBs. While the exact processes involved

in SNBs are not fully understood, it is expected that a prolonged period of activity of many tens of seconds will occur over which their neutrino interactions may be observed. Individually, these interactions will be of low energy (relative to that of beam neutrino interactions, for example), and will be spread over time and over the bulk of the detector modules. Because of their signature and their importance, special attention is required to first ascertain that a SNB may be occurring and to save as much data as possible over its duration.

Thus the DAQ must greatly reduce the full-stream of its input data while using the data itself to do so. It must do this efficiently both in terms of recording essentially all activity important to the physics goals of DUNE and in terms of a rate of data output that is manageable. To perform these primary duties the DAQ provides run control, configuration management, monitoring of both its processes and the general health of the data, and a user interface for these activities.

6.1.2 Design Considerations

The different detector modules vary in terms of their readout technology and schemes, timing systems, channel counts and data throughput and format. These aspects determine the nature of the digital data input to the DAQ. The design of the DAQ strives to contain the unique layers that adapt to the variation in the detector modules toward its front end in order to allow as many of its back end components to remain as identical across the detector modules as possible. In particular, the DAQ must present a unified interface to the ultimate consumer of its data, DUNE offline computing. It must also accept and process the data from a variety of other sources including the accelerator, various calibration systems (including laser, cold electronics (CE), photon detectors (PDs), and potentially others) as well as trigger sources external to DUNE. The modular nature of the DUNE FD implies that the DAQ instances running on each module must also exchange trigger information. In particular, exchanging module-local SNB trigger information will allow higher efficiency for this important physics. The DAQ must be optimized for the above while also retaining the flexibility to scale to handle risks such as excess noise, changes in high voltage (HV), cut network connectivity and other issues that could arise.

Currently, two major variations for the DUNE DAQ are under consideration. The eventual goal is to reduce this to a single high-level design which will service both SP and DP detector modules and be reasonably expected to support the third and fourth modules to come. The first design, designated in this proposal as *nominal*, is illustrated in a high-level way in terms of its data and trigger flow in Figure 6.1. The second design, designated as the alternate, is similarly illustrated in Figure 6.2. The two variants differ largely at their FEs in terms of the order in which they buffer the data received from the detector module electronics and use it to form trigger primitives. They also differ in how they treat triggering and data flow due to a potential SNB. As their FEs are also sensitive to differences between the detector module electronics, this further variation for each general design is described below in Sections 6.2.2 and 6.2.3 for the detector module specific to this volume.

At this general high level, the two designs are outlined. For both, the diagrams are centered on one DAQ front-end fragment FE, which is a portion of the entire DAQ partition servicing a detector module that has one front-end computer (FEC) accepting about 10 to 20 Gbit/s of data

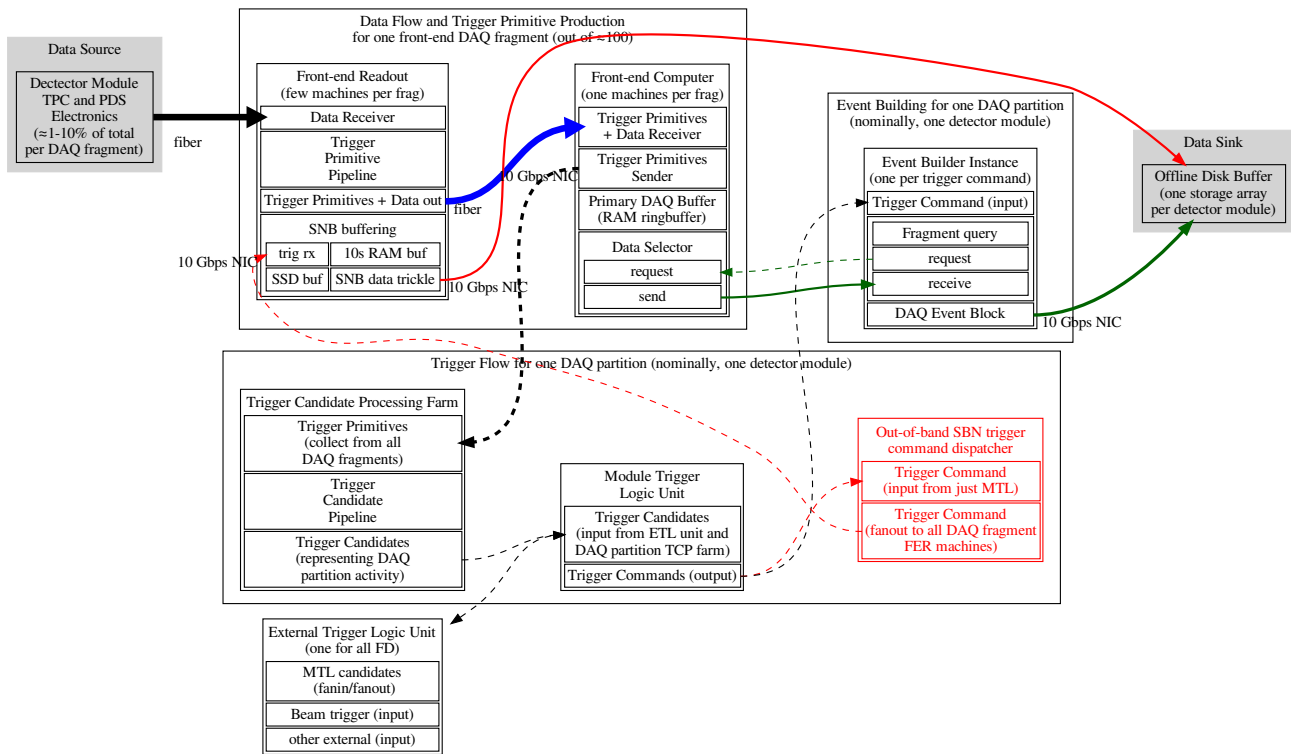


Figure 6.1: The high-level, *nominal* design for the DUNE FD DAQ in terms of data (solid) and trigger (dashed) flows between one DAQ front-end fragment FE and the trigger processing and event building back end for one DAQ partition. Line thickness indicates relative bandwidth requirements. Blue indicates where the full data flow for the DAQ front-end fragment is concentrated to one endpoint. Green indicates final output of normally triggered (non-SNB) data. Red indicates special handling of potential SNB. Each detector module has specialized implementation of some of these high level components, particularly toward the upstream FE as described in the text. The grayed boxes are not in the DAQ scope.

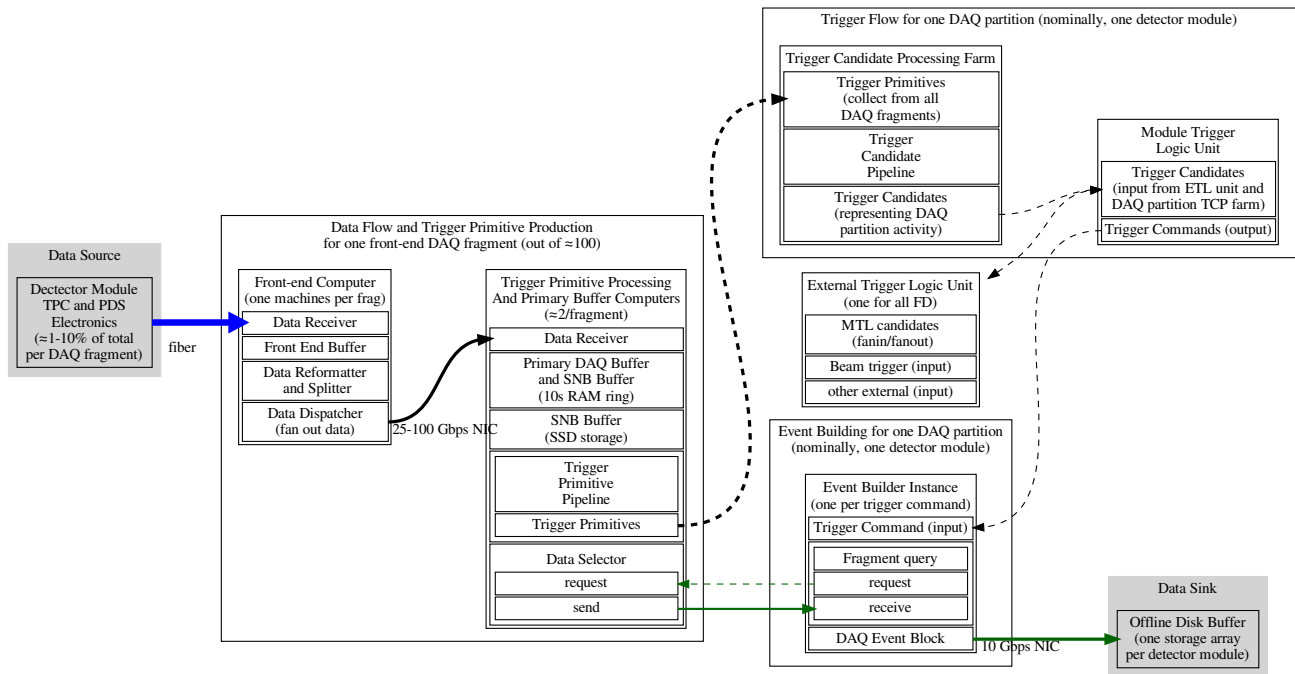


Figure 6.2: The high-level, alternate design for the DUNE FDFD DAQ in terms of data (solid) and trigger (dashed) flows between one DAQ front-end fragment FE and the trigger processing and event building back end for one DAQ partition. Line thickness indicates relative bandwidth requirements. Blue indicates where the full data flow for the DAQ front-end fragment is concentrated to one endpoint. Green indicates final output. Note, except for a longer readout, SNB is handled symmetric to normal data. Each detector module has specialized implementation of some of these high level components, particularly toward the upstream front-end as described in the text. The grayed boxes are not in the DAQ scope.

(uncompressed rate) from some integral number of detector units. Each of the participating DAQ front-end fragments do the following:

- Accept TPC and PDS data from the detector units associated with the DAQ front-end fragment.
- Produce and emit a stream of per-channel trigger primitives.
- Buffer the full data stream long enough for the trigger decision to complete (at least 10 s as driven by SNB requirements).
- Accept data selection requests and return corresponding data fragments.

All participating DAQ front-end fragments in the particular DAQ partition (i.e., the DAQ instance) servicing a portion of one detector module communicate with one trigger processing and event building system. The trigger processing system must:

- Receive the stream of per-channel trigger primitives from all DAQ front-end fragments.
- Correlate the primitives in time and spatially (across channels), and otherwise use them to form higher-level trigger candidates.
- Exchange trigger candidates with the external trigger logic (ETL).
- From them form trigger commands, each of which describes a portion of the data in time and a channel to be read out, such that no two trigger commands overlap.
- Dispatch these commands as required (in general to the event builder (EB)).

The event building system is responsible for performing the following actions:

- Accept a trigger command and allocate one EB instance to dispatch it.
- Interpret and execute the command by making data selection requests to referenced DAQ front-end fragments.
- Accept the returned data fragment from each DAQ front-end fragment and combine them into a DAQ event block.
- Write the result to the secondary DAQ buffer, which is the boundary shared with DUNE offline computing.

The nominal and the alternate DAQ designs differ largely in where the trigger primitive and SNB buffering exist. The *nominal* design places these functions in machines comprising a DAQ front-end readout (FER), which is upstream of the FEC. This then requires the SNB data and trigger handling to be different than that for normal (non-SNB) data. When a SNB trigger command is raised it is forwarded to the out-of-band trigger command dispatcher (OOB dispatcher) which sends

it down to the FERs. After the SNB data is dumped to solid-state disks (SSDs) it is “trickled” out via a path separate from the normal data to the secondary DAQ buffer. The *alternate* design, on the other hand, places these functions downstream of the FEC in trigger processing and data buffering nodes. The RAM of these nodes is used to provide the primary DAQ buffer for normal triggering as well as the deeper buffers needed for SNB. This design handles the SNB data somewhat symmetrically with normal data. When an EB makes a request for SNB data, it differs only in its duration, spanning tens of seconds of instead just a few milliseconds. The FE buffering nodes, instead of directly attempting to return the full SBN data immediately, streams it to local SSD storage. From that storage, the data is sent to the EB as low priority (i.e., also trickled out). Since the module trigger logic (MTL) ensures no overlapping commands, the buffer nodes may service subsequent requests from post-dump data that is in the RAM buffer. Since each trigger command is handled by an individual EB instance, the trickle proceeds asynchronously with respect to any subsequent trigger command handled by another EB instances.

Further description of these designs is given in Section 6.2.

The most critical requirements for the DUNE FD DAQ are summarized in Table 6.1.

Table 6.1: Important requirements on the DAQ system design

Requirement	Description
Scalability	The DUNE FD DAQ shall be capable of receiving and buffering the full raw data from all four detector modules
Zero deadtime	The DUNE FD DAQ shall operate without deadtime under <i>normal</i> operating conditions
Triggering	The DUNE FD DAQ shall provide full-detector triggering functionality as well as self-triggering functionality; the data selection shall maintain high efficiency to physics events while operating within a total bandwidth of 30 PB/year for all operating detector modules
Synchronization	The DUNE FD DAQ shall provide synchronization of different detector modules to within $1\ \mu\text{s}$, and of different subsystems within a module to within 10 ns

The input bandwidth and processing needs of the DAQ are expected to be dominated by the rate of data produced by the TPC system of each detector module. These rates vary between the modules and their estimations are summarized in Table 6.2.

The ultimate limit on the output data rate of the DUNE FD DAQ is expected to be provided by the available bandwidth to the tape, disk and processing capacity of Fermilab. An ample guideline has been established that places this limit at about 30 PB/year or 8 Gbit/s. Extrapolating to four detector modules, this requires a DAQ data reduction factor of almost four orders of magnitude. This is achieved through a simple self-triggered readout strategy.

An overestimate of the annual triggered but uncompressed data volume for one 10 kt detector module is summarized in Table 6.3. It assumes a very generous and simple trigger scheme whereby the data from the entire detector module is saved for a period longer than two drift times around

Table 6.2: The parameters governing the pre-trigger data rate from units of each detector module TPC CEs and the aggregate throughput into the FECs of the DAQ DAQ front-end fragments. Compression is an estimate and will be reduced if excess noise is introduced.

Parameter	single-phase	dual-phase
TPC unit	APA	CRO crate
Unit multiplicity	150	240
Channels per unit	2560 (800 collection)	640 (all collection)
ADC sampling	2 MHz	2.5 MHz
ADC resolution	12 bit	12 bit
Aggregate from CE	1440 GB/s	576 GB/s
Aggregate with compression	288 GB/s (5×)	58 GB/s (10×)

the trigger time. This essentially removes any selection bias at the cost of recording a substantial amount of data that will simply contain noise. Detailed trigger efficiency studies still remain to be performed. Initial understanding indicates that trigger efficiency should be near 100% for localized energy depositions of at least 10 MeV. Sub-MeV signals can be ascertained from noise in existing LArTPCs so the effective trigger threshold may be even lower with high efficiency. Of course, data rates rise quickly when the threshold drops into the range of an MeV. Additional simulation and use of early data will be used to better optimize this threshold.

The data volume estimates also assume that any excess noise beyond what is expected due to intrinsic electronics noise will not lead to an increase in trigger rates. If, for example, excess noise occurs such that it frequently mimics more than about 10 MeV of localized ionization, this would lead to an increase in various types of triggers and subsequently more data. However, at the same time, these estimates do not take into account that some amount of lossless compression of the TPC data will be achieved. In the absence of excess noise it is expected that a compression factor of at least 5× can be achieved with the SP data and up to 10× may be achieved with the DP data, although the actual factor achieved will ultimately depend on the level of excess noise experienced in each detector module. Studies using data from the DUNE 35 ton prototype and early MicroBooNE running have shown that a compression factor of at least 4× can be expected even in the case of rather high levels of excess noise.

One category that will be particularly sensitive to excess noise is the trigger primitives. As discussed further in Section 6.2.3, their primary intended use is as transient objects produced and consumed locally and directly by the DAQ in the trigger decision process. However, as their production is expected to be dominated by ^{39}Ar decays (absent excess noise) they may carry information that proves very useful for calibration purposes. Future studies with simulation and with early data will determine the most feasible methods to exploit this data. These may include committing all or a portion to permanent storage or potentially developing processes that can summarize their data while still retaining information salient to calibration.

Finally, it is important to note that early data will be used to evaluate other selection criteria. It is expected that efficient and bias-free selections can be developed and validated that save a subset of the entire detector module for any given trigger type. For example, a cosmic-muon trigger command for a SP module will indicate which anode plane assemblies contributed to its

Table 6.3: Anticipated annual, uncompressed data rates for a single SP module. The rates for normal (non-SNB triggers) assume a readout window of 5.4 ms. For planning purposes these rates are assumed to apply to a DP module as well, which has a longer readout time but fewer channels. In reality, application of lossless compression is expected to provide as much as a $5\times$ reduction in data volume for the SP module and as much as $10\times$ for the DP module.

Event Type	Data Volume PB/year	Assumptions
Beam interactions	0.03	800 beam and 800 dirt muons; 10 MeV threshold in coincidence with beam time; include cosmics
Cosmics and atmospherics	10	10 MeV threshold, anti-coincident with beam time
Front-end calibration	0.2	Four calibration runs per year, 100 measurements per point
Radioactive source calibration	0.1	Source rate ≤ 10 Hz; single fragment readout; lossless readout
Laser calibration	0.2	1×10^6 total laser pulses, lossy readout
Supernova candidates	0.5	30 seconds full readout, average once per month
Random triggers	0.06	45 per day
Trigger primitives	≤ 6	All three wire planes; 12 bits per primitive word; 4 primitive quantities; ^{39}Ar -dominated

formation (i.e., which ones had local ionization activity). This command can then direct reading out these anode plane assemblies, possibly also including their neighbors, while discarding the data from all other anode plane assemblies. This may reduce the estimated 10 PB/year for cosmics and atmospheric by an order of magnitude. A similar advanced scheme can be applied to the DP module by retaining data for the given readout window from only the subset of CRO crates (and again, potentially their nearest neighbors) that contributed to the formation of the given trigger.

6.1.3 Scope

The nominal scope of the DAQ system is illustrated in Figure 6.1 by the white boxes. It includes the continued procurement of materials for, and the fabrication, testing, delivery and installation of the following systems:

- FE readout (nominal design) or trigger farm (alternate design) hardware and firmware or software development for trigger primitive generation.
- FE computing for hosting of DAQ data receiver (DDR), DAQ primary buffer (primary buffer) and data selector.
- Back-end computing for hosting MTL, EB and the OOB dispatcher processes.
- External trigger logic and its host computing.
- Algorithms to generate trigger commands that perform data selection.
- Timing distribution system.
- DAQ data handling software including that for receiving and building events.
- The online monitoring (OM) of DAQ performance and data content.
- Run control software, configuration database, and user interface
- Rack infrastructure in the central utility cavern (CUC) for readout electronics, FE computing, timing distribution, and data selection.
- Rack infrastructure on surface at SURF for back-end computing.

6.2 DAQ Design

6.2.1 Overview

The design for the DAQ has been driven by finding a cost-effective solution that satisfies the requirements. Several design choices have been made and two major variations remain to be studied. From a hardware perspective, the DAQ design follows a standard HEP experiment design, with customized hardware at the upstream, feeding and funnelling (merging) and moving the data into computers. Once the data and triggering information are in computers, a considerable degree of flexibility is available; the processing proceeds with a pipelined sequence of software operations, involving both parallel processing on multi-core computers and switched networks. The flexibility allows the procurement of computers and networking to be done late in the delivery cycle of the DUNE detector modules, to benefit from increased capability of commercial devices and falling prices.

Since DUNE will operate over a number of decades, the DAQ has been designed with upgradability in mind. With the fall in cost of serial links, a guiding principle is to include enough output bandwidth to allow all the data to be passed downstream of the custom hardware. This allows the possibility for a future very-fast farm of computing elements to accommodate new ideas in how to collect the DUNE data. The high output bandwidth also gives a risk mitigation path in case the noise levels in a part of the detector are higher than specified and higher than tolerable by the baseline trigger decision mechanism; it will allow additional data processing infrastructure to be added (at additional cost).

Digital data will be collected from the TPC and PD readout electronics of the SP and DP detector modules. These categories of data sources are viewed as essentially four types of subdetectors within the DAQ and follow the same overall data collection scheme as shown for the nominal design in Figure 6.1 and for the alternate design in Figure 6.2. The readout is arranged to allow making a trigger decision in a hierarchical manner. Initial inputs are formed at the channel level, then combined at the detector unit level and again combined at the detector module level. In addition, the trigger decision process combines information at this level that may come from the other detector modules as well as information from sources external to the DAQ. This hierarchical structure in forming and consuming triggers allows safeguards to be developed so that any problems in one cavern or in one detector unit of one detector module need not overwhelm the entire DAQ. It also allows a SNB to be recorded in all operational parts of the detector while others may be down for calibration or maintenance.

Generally speaking, the DAQ consists of data flow and trigger flow. The trigger flow involved in self-triggering originates from processing a portion of the data flow. The trigger flow is then consumed back by the DAQ in order to govern what portion of the data flow is finally written out to permanent storage. The nominal and alternate designs differ in where in the data flow the trigger flow originates.

In both designs, a single DAQ front-end fragment associates an integral number of detector units with one front-end computer (FEC). This fragment forms one conceptual unit of the FE DAQ. The

processing on a FEC is kept minimal such that each has a throughput limited by I/O bandwidth. The recently released PCIe v4 doubles the bandwidth from the prior version and thus we assume that ≈ 20 GB/s throughput (out of a theoretical 32 GB/s max) can be achieved based on tests using PCIe v3. In principle then, this allows one FEC to accept the data from: two (if uncompressed) or ten (if $5\times$ compressed) of the 150 SP anode plane assemblies, ten of the 240 DP CRO crates given their nominal $10\times$ compression or the uncompressed data from all five DP LRO crates.

In the nominal design, the data enters the DAQ via the fragment's DAQ front-end readout (FER) component. In the SP the FER consists of eight reconfigurable computing elements (RCEs) and in the DP it consists of a number of Bump On Wire (BOW) computers, (see Section 6.2.2 in each respective detector module volume). The FER is responsible for accepting that data and from it producing channel level trigger primitives. It is also responsible for forwarding compressed data and the primitives to the DAQ data receiver (DDR) in the corresponding FEC. The FER is also responsible for supplying transient memory (RAM) and non-volatile buffer in the form of SSD sufficient for SNB triggering and readout. The DDR accepts the full data stream and transfers it to the DAQ primary buffer of its DAQ front-end fragment. There it is held awaiting a query from the event builder (EB). When the EB receives a trigger command it uses the included information to query all appropriate data selectors and from their returned data fragments an DAQ event block is built and written to file on the secondary DAQ buffer. From there the data becomes responsibility of the offline group to transfer to Fermilab for permanent storage and further processing.

In the alternate design, the data is accepted directly by the DAQ data receiver (DDR) in a FEC from the detector electronics for the particular detector module. The data then flows into the primary buffer and the portion required for forming trigger primitives is dispatched to the trigger computers of the fragment for the production of trigger primitives. Current SSD technology may allow SSD to be directly mounted to the FEC to provide for the SNB dump buffer. Another solution, which puts less pressure on write throughput, is to distribute the SSD for the SNB dumps to the trigger computers. In order to supply enough CPU for trigger primitive pipelines it is expected that at least two hosts per FEC will be needed. While their CPUs are busy finding trigger primitives, their I/O bandwidth will be relatively unused and thus they provide synergistic, cost-effective hosting for the SSDs.

Regardless of where the trigger primitives are produced in either the nominal or alternate design, they are further processed at the DAQ front-end fragment level to produce trigger candidates. At this level, they represent possible activity localized in time and by channel to a portion of the overall detector module. The trigger candidates emitted by all DAQ front-end fragments are sent to the module trigger logic (MTL) associated with the DAQ partition. There, they are time ordered and otherwise processed to form trigger commands. At this level they represent activity localized across the detector module and over some period of time.

The DAQ partition (or DAQ instance) just introduced is the cohesive collection of DAQ parts. One DAQ partition operates essentially independently from any other, and there is typically one per detector module. In some cases multiple DAQ partitions may operate simultaneously in a detector module, such as when some fraction of detector units are undergoing isolated testing or calibration.

Each trigger command is consumed by a single EB instance in order to query back to the DAQ

front-end fragments of its DAQ partition as described above. In addition, the MTL of one module is exchanging messages in the form of trigger candidates with the others. For example, one module may raise a local SNB trigger candidate and forward it to all other modules. Each module is also emitting candidates to sinks and accepting them from sources of external trigger information.

The exact implementation of some of these high-level functions, particularly those near the FE, depends on the particular detector module. The required specialization and in general, more implementation-level details are described in the following sections. Subsequent description proceeds toward the DAQ back end including processes handling dataflow, triggering, event building and data selection.

6.2.2 Front-end Readout and Buffering

Figure 6.3 illustrates the SP-specific DAQ front-end fragment specializing from the generic, nominal design illustrated in Figure 6.1. Starting from the left, it shows the fiber optic connectivity pattern between the four connectors of five SP WIBs associated with each APA and the elements of one SP DAQ front-end readout (FER). In total, the FER is associated with two anode plane assemblies, each of which is serviced by one ATCA Cluster On Board (COB) hosting four compute units called reconfigurable computing element (RCE). Each RCE provides field programmable gate array (FPGA), RAM and SSD resources. Its primary functions include:

- Receive data from WIBs,
- Produce trigger primitives from collection channels (see Section 6.2.3),
- Compress the data,
- Forward data and trigger primitives to the FEC,
- Buffer data in RAM,
- Stream data from RAM to SSDs on receipt of a *dump* trigger command (such as is raised by an SNB candidate),

The data and trigger primitives from the eight RCEs are aggregated to a single Front-End Link eXchange (FELIX) PCIe board residing in the FEC. This is done via 16 10 Gbit/s optical fibers. With no data compression performed in the RCEs the bandwidth of these fibers will be close to saturated. If excess noise is not greater than experienced by MicroBooNE, then a lossless compression factor of at least five may be expected. If achieved, the total throughput into FELIX from the two anode plane assemblies is expected to be about 4 GB/s

The firmware running on the FELIX FPGA transfers the data and trigger streams to the host system RAM. This type of transfer has been demonstrated by ATLAS with a PCIe v3 FELIX board at a throughput up to 10 GB/s. The next generation of FELIX based on PCIe v4 is expected to obtain about a factor of two improvement. The trigger primitives are combined across channels

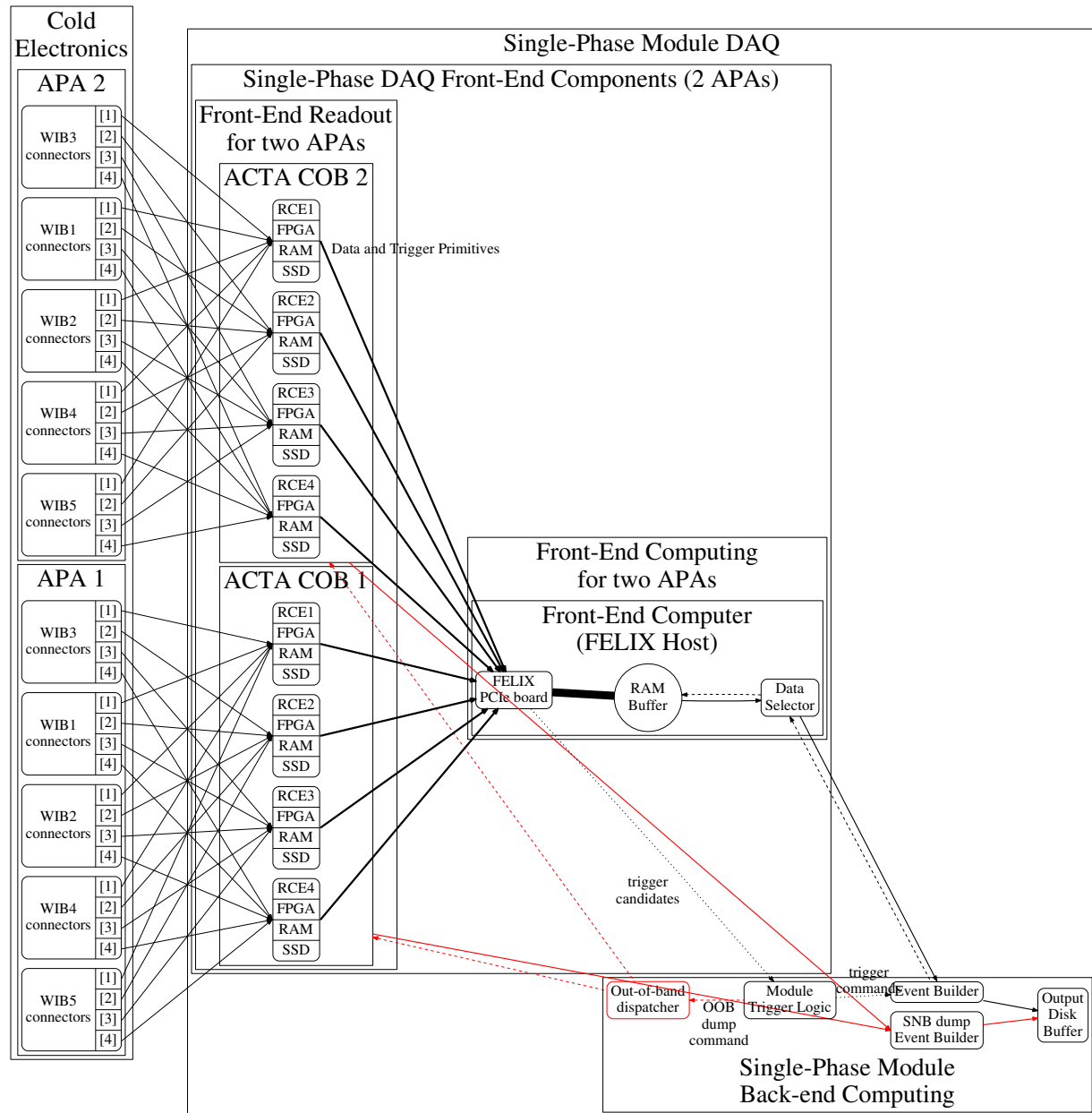


Figure 6.3: Illustration of data (solid arrows) and trigger (dashed) flow for one SP DAQ fragment (two APAs) in the nominal design. Black arrows indicate normal data and trigger flow and red indicate special flow for handling of a potential SNB.

to form trigger candidates that will be sent to the MTL. Meanwhile, the data stream streams into a primary buffer. This buffer will be sized sufficient to retain the full data stream for the period of time needed for a trigger decision to be made. As described above, that decision culminates in a trigger command that is sent to an EB. Based on its information, the EB makes a request to the data selector representing the DAQ front-end fragment, and the data selector replies with a data fragment build from the data available in the primary buffer.

An SNB trigger command is formed via the usual trigger hierarchy, as described in Section 6.2.3, and is consumed by the out-of-band trigger command dispatcher component. This component simply dispatches the command back down to the 600 RCEs in order to relieve the duty from the MTL, thus avoiding a source of trigger latency. This means an SNB trigger command is serviced differently than are all the other types of trigger commands. The RAM on board the RCEs is used to store the full data stream long enough for an SNB trigger command to be formed and distributed. It has been estimated that the rise time to detect an SNB in the SP detector module is about 1 s, so the RAM must be sized to buffer at least this much data. SNB models differ on the total duration over which significant neutrino interactions may be expected, as well as to their possible time profiles. Some allow for SNB neutrino interactions to occur for some time but at a rate not sufficient to rise above a trigger threshold determined by SNB backgrounds. It is assumed that an SNB dump should start about 10 s before the SNB trigger and should span a total 30 s. During the dump, all data is sent to both the SSD storage distributed among the RCEs. Data also continues to flow to the associated FER as during nominal running, which ensures that no dead time is suffered for all other non-SNB triggers. The multiplicities of RCEs and SSDs are such that uncompressed throughput of the SNB dump will just saturate current technology. Given a lossless compression factor of five the throughput to each SSD is expected to be 500 MB/s.

Given the infrequency of detectable SNBs the average SNB trigger rate is effectively governed only by a chosen threshold and by the rate of background from radiological decays, neutrons from cosmic-ray muons and fluctuations of noise, especially any coherent excess noise. The threshold must be tuned to maintain high efficiency for a broad class of SNB models while also not flooding the DAQ and potentially offline computing. This needs further study, but for the purposes of illustration a nominal false positive rate of one SNB dump per month is assumed. Uncompressed, this results in 540 TB/year. Each dump will take up 75 GB on an SSD, each of which is expected to provide 500 GB of storage; this is enough for at least six dumps. Again, lossless compression is expected to achieve a factor of five.

The SNB dumps are expected to remain on the SSD storage for some time in order to perform checks on the data to either rule out and delete the data or accept the candidate and migrate its data to permanent storage. This data migration is done out-of-band of the connection to the FELIX board using a local network connection to the ATCA crate. With the assumed average of one dump per month, if all were saved uncompressed it would require an average bandwidth aggregated over the entire SP module of just over 100 Mbit/s.

In the alternate SP DAQ design (not diagrammed), which corresponds to the generic Figure 6.2, the ten WIBs shown in Figure 6.3 are directly connected to one FELIX board via 10 Gbit/s fiber optic. The readout and buffering then follow the generic design.

6.2.3 Front-end Trigger Primitive Generation

Trigger primitives are generated inside the FE readout hardware associated with each APA from TPC data on a per-channel basis. They are sent along with the waveform data to the FE DAQ computing. In the alternate design, the data is directly sent from the anode plane assemblies to the FECs and the data are sent to the trigger processing computers. In both designs, the primitives from one DAQ front-end fragment are further processed to produce trigger candidates. As such they represent a localization of activity on the corresponding anode plane assemblies for a given period of time. These candidates are emitted to the MTL, which may consider candidates from other detector modules or external sources before generating trigger commands. Section 6.2.5 describes the selections involved in this triggering.

Only the 480 collection channels associated with each APA face are used for forming trigger primitives. Reasons for this limitation include the fact that collection channels:

- have higher signal to noise ratios compared to induction channels;
- are fully and independently sensitive to activity on their APA face;
- have unipolar signals that give direct approximate measures of ionization charge without the costly computation that would be needed to deconvolve the field response functions required for the the induction channels;
- can be easily divided into smaller, independent groups in order to better exploit parallel processing.

Figure 6.3 illustrates the connectivity between the four connectors on each of the five WIBs and the FE readout hardware. The data is received via eighty 1 Gbps fiber optical links by four RCEs in the Advanced Telecommunications Computing Architecture (ATCA) Cluster On Board (COB) system.

Due to the pattern of connectivity between WIBs and RCEs, each RCE receives the data from the collection channels that cover one contiguous half of one APA face. Each RCE has two primary functions. The first is transmission of all data as described in Section 6.2.4. The second is to produce trigger primitives from its portion of the collection channel data. The algorithms to produce the trigger primitives still require development but can be broadly described, as follows.

1. On a per channel basis, calculate a rolling baseline and spread level that characterizes recent noise behavior such that the result is effectively free of influence from actual ionization signals.
2. Locate contiguous runs of analog-to-digital converter (ADC) samples that are above a threshold defined in terms of the baseline and noise spread.
3. Emit their time bounds and total charge as a trigger primitive.

Each trigger primitive represents ionization activity localized (relatively) along the drift direction

by the times at which the signal crosses threshold and by two planes parallel to the collection wire and located midway between the wire and each of its neighboring wires. Depending on the threshold set, these trigger primitives may be numerous due to ^{39}Ar decays and noise fluctuations. If their rate cannot be sustained, the threshold may be raised or further processing may be done, still at the APA level, that considers more global information. This may be performed either in the RCEs or later in the FE computing hosts. In either case, the results are in the form of trigger candidates, which are sent to the MTL.

Sources of radio frequency (RF) emission inside the cryostat are minimized by design. Any residual RF is expected to be picked up coherently across some group of channels. Depending on its intensity, additional processing of the collection waveforms must be employed to mitigate this coherent noise and this must occur before the data is sent for trigger primitive production. If the required mitigation algorithms outgrow the nominally specified RCE FPGA it is possible to double the number of COBs per APA, which would require a redistribution of fibers. Alternatively, or in addition, the higher number of trigger primitives produced as a result of excess noise can be passed along for further processing in the FE computing. This would require reprocessing the raw waveform data.

6.2.4 Dataflow, Trigger and Event Builder

In the general data and trigger flow diagrams for the nominal (Figure 6.1) and alternate (Figure 6.2) designs, the dataflow, trigger and event builder functions take as input data from the detector module electronics and culminate in files deposited to the secondary DAQ buffer for transfer to permanent storage by offline computing processes. The continuous, uncompressed data rate of the input from one detector module is on the order of 1 TB/s. The final output data rate, for all detector modules operating at any given time is approximately limited to 1 GB/s.

To accept this high data-inflow rate and to apply the substantial processing needed to achieve the required reduction factor, which is on the order of 1000, the DAQ follows a distributed design. The units of distribution for the front end of the DAQ must match up with natural units of the detector module providing the data. This unit is called the DAQ front-end fragment and each accepts input at a rate of about 10 to 20 GB/s. The exact choice maps to some integral number of physical detector module units (e.g., SP anode plane assemblies or DP CROs and LROs).

As described in the previous sections, the nominal and alternate designs differ essentially in the order and manner in which the SNB buffering occurs and the trigger primitives are formed. The overall data flow, higher level triggering and building of *event* data blocks for final writing are conceptually very similar. This processing begins with the data being received by the FELIX PCIe board hosted in the FEC. The FELIX board performs a DMA transfer of the data into the primary buffer for the DAQ front-end fragment, which resides in the FEC host system RAM. This buffer is sized to hold ten seconds of data assuming the maximum uncompressed input rate associated with the fragment. While data is being written to the buffer, a delayed portion is also being read in order to dispatch it for various purposes. Any and all requests to further dispatch a subset of this data from the primary buffer must arrive within this buffer time. In the nominal design, the only dispatching will be from a request made by an EB (described more below) upon

receipt of a trigger command. In the alternate design, a suitable fraction of the data is also dispatched via high bandwidth (at least 25 to 50 Gbit/s simplex, less if data is compressed at this stage) network connections to a trigger farm so that trigger primitives may be formed. Whether the primitives are formed in this manner or extracted from the stream sent by the FER (as in the nominal design) these trigger primitives from one DAQ front-end fragment are collectively sent for further processing in order to be combined across channels and to then produce trigger candidates. These are finally combined for one detector module in the MTL. It is in the MTL where trigger candidates from additional sources are also considered, as described in section 6.2.5.

In both the nominal and alternate designs the dispatch of data initiated by normal (non-SNB) trigger commands is identical. This dispatch, commonly termed *event building* involves collection of data spanning an identical and continuous period of time from multiple primary buffers across the DAQ. As introduced above, each trigger command is consumed by an EB process. It uses fragment address information in the trigger command to query the data selector process representing each referenced DAQ front-end fragment and accepts the returned a data fragment. In the exceptional case that the delay of this request is so large that the primary buffer no longer contains the data, then an error return is supplied and recorded by the EB in place of the lost data. Such failures lead to indicators displayed by the detector operation monitoring system. The EB finally assembles all responses into a DAQ event block and writes it to file on the secondary DAQ buffer where it becomes the responsibility of DUNE offline computing.

The data selector and EB services are implemented using the general-purpose Fermilab data acquisition framework *artDAQ* for distributed data combination and processing. It is designed to exploit the parallelism that is possible with modern multi-core and networked computers, and has been used in ProtoDUNE and other experiments. The *artDAQ* framework is the principal architecture that will be used for the DUNE DAQ back-end computing. The authors of *artDAQ* have accommodated DUNE-specific requests for feature additions. Also, a number of libraries have been developed based on existing parts of *artDAQ* used to handle incoming data from data sources. It is likely that future DUNE extensions will be made by one of these two routes.

Unlike the dispatch of data initiated by a normal trigger commands, a command formed to indicate the possibility of a SNB is handled differently between the nominal and alternate designs. Such a command is interpreted to save all data from all channels for a rather extended time of 30s starting from 10s before the time associated with the trigger command. As no data selection is being performed, given the required bandwidth, special buffering to nonvolatile storage, in the form of SSD, is required. Today's technology supplies individual SSD in the M.2 expansion card form factor, which supports individual write speeds up to 2.5 GB/s. The two designs differ as to the location of and data source for these buffers.

In the nominal design, these SSDs reside in the FER as described in Section 6.2.2. In that location, due to larger granularity of computing units, the data rate into any one SSD is within the quoted write bandwidth. However, and as shown in Figure 6.1, the data and trigger flow for SNB in the nominal case takes a special path. Instead of an EB consuming the trigger command as described above, it is sent to the out-of-band trigger command dispatcher (OOB dispatcher), which dispatches it to each FER unit hosting an SSD. This component is used to immediately free up the MTL to continue to process normal triggers. When the command is received, each host must begin to stream data from its local RAM, supplying at least 10s of buffer to the SSD, and

continue until the full 30 s has elapsed. While it is performing this dump it must continue to form trigger primitives and pass them and the full data stream to the connected FEC.

In the alternate design the same primary buffer provides the 10 s of pre-trigger SNB buffering. As in the nominal case, it must rely on fast, local SSD storage to sink the dump. Current SSD technology allows four M.2 SSD devices to be hosted on a PCIe board. Initial benchmarks of this technology show that such a combination can achieve 7.5 GB/s write bandwidth, which is short of linear scaling. To support the maximum of 20 GB/s, three such boards would be required. The alternate design presents a synergy between the need to dump high-rate data and the need to provide CPU to form the trigger primitives. With current commodity computing hardware it is expected that each FEC will need to be augmented with about two computers in the trigger farm. These trigger processors will need to accept the entire DP and three-eighths of the SP data stream from their DAQ front-end fragment. If they instead accept the entire stream, they can also provide RAM buffering and split up the data rate, which must be sunk to SSD buffers.

In both designs, the data dumped to SSD may contain precious information about a potential SNB. It must be extracted from the buffer, processed and either discarded or saved to permanent storage. The requirements on these processes are not easy to determine. The average period between actual SNBs to which DUNE is sensitive is measured in decades. However, to maintain high efficiency for capturing such important physics, the thresholds will be placed as low as feasible, limited only by the ability to acquire, validate and (if validated) write out the data to permanent storage. Notwithstanding, the (largely false positive) SNB trigger rate is expected to be minuscule relative to normal triggers. Understanding the exact rate requires more study, including using early data, but for planning purposes it is simply assumed that one whole-detector data dump will occur per month on average. Using the SP module as an example, and choosing the nominal time span for the dump to be 30 s, about 45 PB of uncompressed data would result. In the nominal SP DAQ design, this dump would be spread over 600 SSD units leading to 75 GB per SSD per dump. Thus, typical SSDs offer storage to allow any given dump to be held for at least one half year before it must be purged to assure storage is available for subsequent dumps. If every dump were to be sent to permanent storage, it would represent a sustained 0.14 Gbit/s (per detector module), which is a small perturbation on the bandwidth supplied throughout the DAQ network. Saved to permanent storage this rate integrates to 0.5 PB/year, which while substantial, is a minor fraction of the total data budget. The size of each dump is still larger than is convenient to place into a single file, so the SNB event-building will likely differ from that for normal triggers in that the entire dump is not held in a single DAQ event block. Finally, it is important to qualify that these rates assume uncompressed data. At the cost of additional processing elements, lossless compression can be expected to reduce this data rate by 5 to $10\times$ or alternatively allow lower thresholds that lead to the same factor of more dumps. Additional study is required to optimize the costs against the expected increase in sensitivity.

6.2.5 Data Selection Algorithms

Data selection follows a hierarchical design. It begins with forming detector unit-level trigger candidates inside the DAQ front-end fragment FE computing using channel-level trigger primitives. These are then used to form detector module trigger commands in the MTL. When executed,

they lead to readout of a small subset of the total data. In addition, trigger candidates are provided to the MTL from external sources such as the ETL in order to indicate external events such as beam spills, or SNB candidates detected by the other detector modules. In addition to supplying triggers to SuperNova Early Warning System (SNEWS), triggers from SNEWS or other cosmological detector sources such as LIGO and VIRGO can be accepted in order to possibly record low-energy or dispersed activity that would not pass the self-triggering. The latency of arrival for these sources must be less than the nominal 10 s buffers used to capture low-level early SNB activity. A high-level trigger (HLT) may also be active within the MTL. The hierarchical approach is natural from a design standpoint and it allows for vertical slice testing and running multiple DAQ partitions simultaneously during commissioning of the system or when debugging of individual detector units is required.

As discussed in Sections 6.2.2 and 6.2.3, trigger primitives are generated in either in FERs (in the nominal design) or in trigger processing computers (in the alternate design). In both designs, and for both SP and DP detector modules, only data from TPC collection channels (three-eighths of SP and all of DP channels) feed the self-triggering, as their waveforms directly supply a measure of ionization activity without computationally costly signal processing. The trigger primitive contains summary information for each channel, such as the time of any threshold-crossing pulse, its integral charge, and time over threshold. A channel with an associated trigger primitive is said to be *hit* for the time spanned by the primitive. Trigger primitives from one detector unit are then further processed to produce a trigger candidate. The candidate represents a cluster of hits across time and channel, localized to the detector unit. The candidates from all DAQ front-end fragments are passed to the MTL.

The MTL arbitrates between various trigger types, determines trigger priority and ultimately the time range and detector coverage for a trigger command, which it emits back to the FECs. The MTL assures that no trigger commands are issued that overlap in time or in detector channel space. It also may employ a HLT to reduce or aggregate triggers into fewer trigger commands so as to optimize the subsequent readout. For example, aggregating many small readouts into fewer but larger ones may allow for more efficient processing. This can be particularly important during periods of high-rate activity due to e.g., various backgrounds or instrumental effects.

When activity leads to the formation of a trigger command this command is sent down to the FECs instructing which slice of time of its buffered data should be saved. The trigger command information is saved along with this data. At the start of DUNE data taking, it is anticipated that for any given single-interaction trigger (a cosmic-ray track, for example), waveforms from all channels in the detector module will be recorded over a one readout window (nominally, 5.4 ms for SP and 16.4 ms for DP, chosen to be two drift times plus an extra 20%).

Such an approach is clearly very generous in terms of the amount of data saved, but it ensures that associated low-energy physics (such as captures of neutrons produced by neutrino interactions or cosmic rays) are recorded without any need to fine-tune detector unit-level triggering, and does not depend on the noise environment across detector units. In addition, the wide readout window ensures that the data of all associated activity is recorded. As generous as it is, it is estimated that this readout window will not produce an unmanageable volume of data. As shown in Table 6.3, the uncompressed selected data from the SP module will fill about half of the nominal annual data budget. The longer DP drift and its fewer channels will give approximately the same data

rate. However, once a modest amount of lossless compression is applied, the nominal data budget can be met. Early running will allow experience to be gained and more advanced data selection algorithms to be validated allowing the DAQ to discard the many data fragments in each trigger consistent with just electronics noise. This has the potential for a reduction of at least another factor of ten.

Other trigger streams – calibrations, random triggers, and prescales of various trigger thresholds – are also generated at the detector module level, and filtering and compression can be applied based upon the trigger stream. For example, a large fraction of random triggers may have zero-suppression (ZS) applied to their waveforms, reducing the data volume substantially, as the dominant data source for these will be ^{39}Ar events. Additional signal-processing can also be done on particular trigger streams if needed and if the processing is available, such as fast analyses of calibration data.

At the detector module level, a decision can also be made on whether a series of interactions is consistent with an SNB. If the number of detector unit-level, low-energy trigger candidates exceeds a threshold for the number of such events in a given time, a trigger command is sent from the MTL back to the FERs, which store up to 10s of full waveform data. That data is then streamed to non-volatile storage to allow for subsequent analysis by the SNB working group, perhaps as an automated process. If not rejected, it is sent out of the DAQ to permanent offline storage.

In addition, the MTL passes trigger candidates up to a detector-wide ETL, which among other functions, can decide whether, integrated across all modules, enough detector units have detected interactions to qualify as an SNB, even if within a particular module the threshold is not exceeded. Trigger candidates from the ETL are passed to the MTL for dispatch to the FECs (or FERs in the case of SNB dump commands in the nominal design). That is, to the MTL, an external trigger candidate looks like just one more *external* trigger input.

Detector unit level trigger candidates are generated within the context of one DAQ front-end fragment, specifically in each FEC. The trigger decision is based on the number of nearby channels hit in a given fragment within a time window (roughly 100 μs), the total charge collected in these adjacent channels, and possibly the union of time-over-threshold for the trigger primitives in the collection plane. Studies show that even for low-energy events (roughly 10 MeV to 20 MeV) the reduction in radiological backgrounds is extremely high with such criteria. The highest-rate background, ^{39}Ar , which has an overall rate of 10 MBq within a 10 kt volume of argon, has an endpoint of 500 keV and requires significant pileup in both space and time to get near a 10 MeV threshold. One important background source is ^{42}Ar , which has a 3.5 MeV endpoint and an overall rate of 1 kBq. ^{222}Rn decays via a 5.5 MeV kinetic energy α and is also an important source of background. The radon decays to ^{218}Po , which within a few minutes leads to a 6 MeV kinetic energy α , and ultimately to a ^{214}Bi daughter (many minutes later), which has a β decay with its endpoint near 3.5 MeV kinetic energy. The α ranges are short, resulting in charge being collected on one or two anode wires at most, but the charge deposit can be large, and therefore the charge threshold must be well above the α deposits plus any pileup from ^{39}Ar and noise.

At the level of one detector unit, two kinds of local trigger candidates can be generated. One is a high-energy trigger that indicates local ionization activity corresponding to more than than 10 MeV. The per-channel thresholds on total charge and time-over-threshold will be optimized to

achieve at least 50 % efficiency at this energy threshold, with efficiency increasing to 100 % via a turn-on curve that ensures at least 90 % efficiency at 20 MeV. The second type of trigger candidate generated is for low-energy events between 5 MeV and 10 MeV. In isolation, these candidates do not lead to formation of a trigger command. Rather, at the detector module level they are combined, time ordered and their aggregate rate compared against a threshold based on fluctuations due to noise and backgrounds in order to form an SNB trigger command.

The MTL takes as input trigger candidates (both low-energy and high-energy) from the participating DAQ front-end fragments, as well as external trigger candidate sources, such as the ETL, which includes global, detector-wide triggers, external trigger sources such as SNEWS, and information about the time of a Fermilab beam spill. The MTL also generates trigger commands for internal consumption, such as random triggers and calibration triggers (for example, telling a laser system to fire at a prescribed time). The MTL can also generate trigger commands from a prescaled fraction of trigger types that otherwise do not generate such commands on their own. For example, a prescaled fraction of single, low-energy trigger commands could be allowed to generate a trigger command, even though those candidates normally only result in a trigger command when aggregated (i.e., as they would be for an SNB).

The MTL is also responsible for checking candidate triggers against the current run control (RC) trigger mask: in some runs, for example, we may decide that only random triggers are accepted, or that certain trigger candidates streams should not be considered because their DAQ front-end fragments have been producing unreasonably large rates in the recent past (such as may be due to noise spikes, flaky hardware or buggy software). In addition, the MTL counts low-energy trigger candidates, and based upon their number and distribution over a long time interval (e.g., 10 s), decides to generate an SNB trigger command. The trigger logic will be optimized to record the data due to at least 90 % of all Milky Way supernovae, and studies of simple low-energy trigger criteria show that a much higher efficiency can likely be achieved.

The HLT can also be applied at this level, particularly if there are unexpectedly higher rates from instrumental or low-energy backgrounds that require some level of reconstruction or pattern recognition. An HLT might also allow for efficiently triggering on lower-energy single interactions, or allow for better sensitivity for supernovae originating outside the Milky Way galaxy, by employing a weighting scheme to individual trigger candidates – higher-energy trigger candidates receiving higher weights. Thus, for example, two trigger candidates consistent with 10 MeV interactions in 10 s might be enough to create a SNB candidate trigger, while a hundred 5 MeV trigger candidates in 10 s might not. Lastly, the HLT can allow for dynamic thresholding; for example, if a trigger appears to be due to a cosmic-ray muon, the threshold for single interactions can be lowered (and possibly prescaled) for a short time after that to identify spallation products. In addition, the HLT could allow for a dynamic threshold after a SNB, to extend sensitivity beyond the 10 s SNB readout window, while not increasing the data volume associated with SNB candidates linearly.

All low-energy trigger candidates are also passed upwards to the ETL so that they may be integrated across all 10 kt detector modules in order to determine that a SNB may be occurring. This approach increases the sensitivity to trigger on SNBs by a factor of four (for 40 kt), thus extending the burst sensitivity to a distance twice as far as for a single 10 kt detector module.

The MTL is also responsible for including in the trigger command a global timestamp built from

its input trigger candidates, and information on what type of trigger was created. Information on trigger candidates is also kept, whether or not they contribute to the formation of a trigger command. As described above, the readout window for nominal trigger commands (those other than for SNB candidates) is somewhat more than two times the maximum drift time. Further, a nominal readout spans all channels in a detector module. The MTL is also responsible for sending the trigger commands that tell the FERs to stream all data from the past 10s and for a total of 30s in hopes to catch SNBs. This command may be produced based on trigger candidates from inside the MTL itself or it may be produced based on an external SNB trigger candidate passed to the MTL by the ETL.

6.2.6 Timing and Synchronization

All components of the SP module are synchronized to a common clock. In order to make full use of the information from the PDS, the common clock must be aligned within a single detector unit with an accuracy of O 1ns. In order to form a common trigger for SNB between detector modules, the timing between them must be aligned with an accuracy of O 1ms. However, a tighter constraint is the need to calibrate the common clock to universal time (derived from GPS) in order to adjust the data selection algorithm inside an accelerator spill, which requires an absolute accuracy of O 1 μ s.

SP and DP detector modules use different timing systems, driven by the different technical requirements and development history of the two technologies. A SP module has many more timing end points than a DP module and many of the end points are simpler than the end points in the DP, for example a WIB versus Micro Telecommunications Computing Architecture (μ TCA) crate. Both systems have been successfully prototyped.

The DUNE SP module uses a development of the ProtoDUNE-SP timing system. Synchronization messages are transmitted over a serial data stream with the clock embedded in the data. The format is described in DUNE DocDB-1651 [29]. Figure 6.4 shows the overall arrangement of components within the SP Timing System (SPTS). A stable master clock, disciplined with a 10 MHz reference is used in the SPTS. A one-pulse-per-second signal (1PPS signal) is also received by the system and is time-stamped onto a counter clocked by the SPTS master clock, however the periodic synchronization messages distributed to the SP detector module are an exact number of clock cycles apart even if there is jitter in the 1PPS signal.

The GPS signal is encoded onto optical fiber and transmitted to the CUC, where it is converted back to an RF signal on coaxial cable and used as the input to a GPS disciplined oscillator. The oscillator module also houses a IEEE 1588 (PTP) grandmaster and an NTP server. The PTP grandmaster provides a timing signal for the DP White Rabbit (WR) timing network. The NTP server provides an absolute time for the 1PPS signal. The SPTS relates its time counter onto GPS time by timestamping the 1PPS signal onto the SPTS time counter and reading the time in software from the NTP server.

The latency from the GPS antenna on the surface to the GPS receiver in the CUC will be measured by optical time domain reflectometry at installation. Given the modest absolute time accuracy

required (sufficient to select data within an accelerator spill) dynamic monitoring of this delay is not required.

The WR synchronization signals from the DP detector module are time-stamped onto the SPTS clock domain and the SPTS synchronization signals are time stamped onto the DP clock domain. This allows the timing in the SP and DP detector modules to be aligned. A similar scheme is used to relate the ProtoDUNE-SP timing domain to the beam instrumentation WR time domain.

In order to provide redundancy, and also the ability to easily detect issues with the timing path, two independent GPS systems are used. One with an antenna at the head of the Yates Shaft, the other with an antenna at the head of the Ross Shaft. The two independent timing paths are brought together in the same rack in the CUC. Using 1:2 fiber splitters one SPTS unit can be left as a hot spare while the other is active. This also allows testing of new firmware and software during commissioning without the risk of losing the SPTS if a bug is introduced.

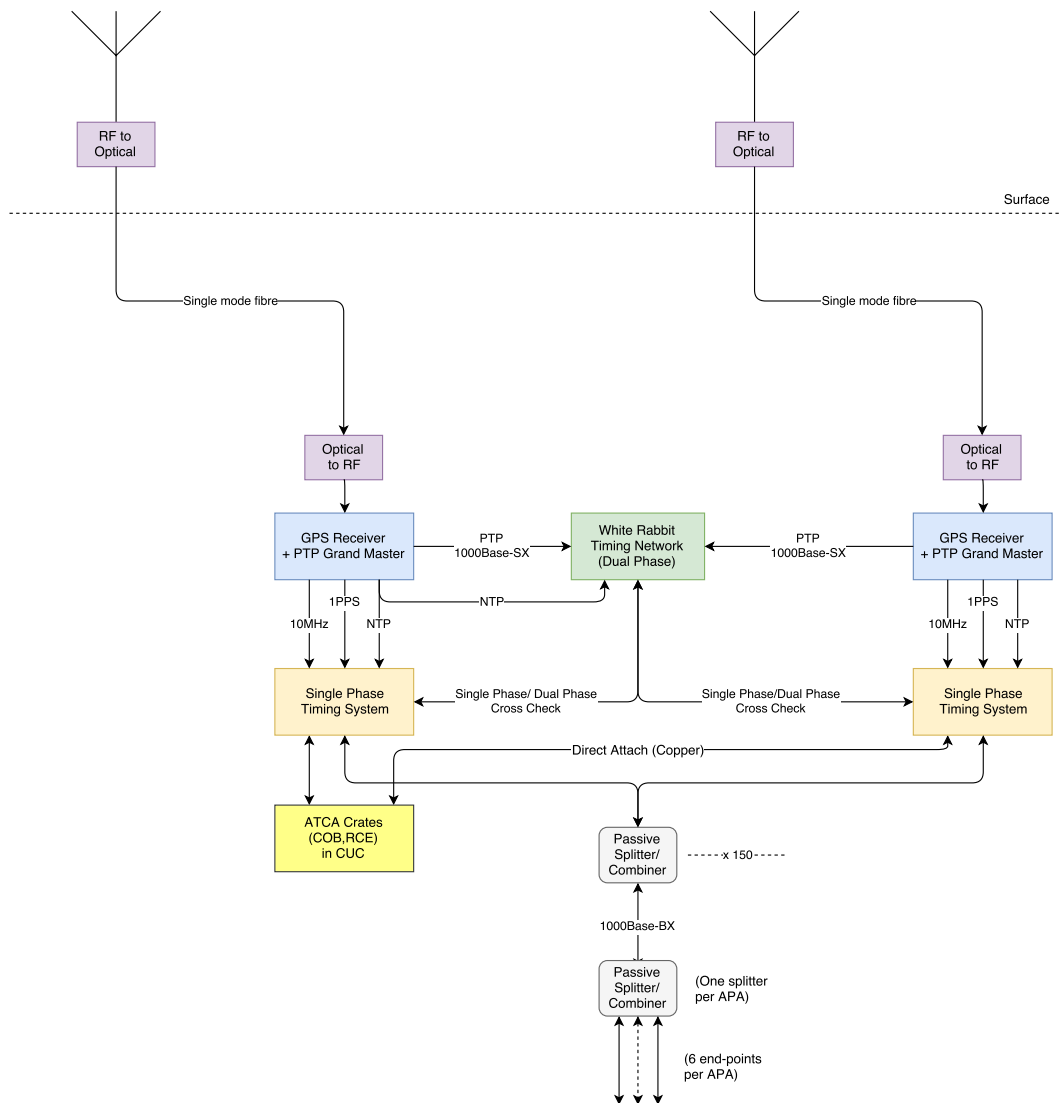


Figure 6.4: Illustration of the components in the DUNE timing system.

All the custom electronic components for the SPTS are contained in two μ TCA shelves. At any

one time one is active and the other is a hot spare. The 10 MHz reference clock and the 1PPS signal are received by a single width advanced mezzanine card (AMC) at the center of the μ TCA shelf. This master timing AMC produces the SPTS signals and encodes them onto a serial data stream. This serial datastream is distributed over a standard star-point backplane to the fanout AMCs, which each drive the signal onto up to 13 SFP cages. The SFP cages are either occupied by 1000Base-BX SFPs, each of which connects to a fiber running to an APA, or to a Direct Attach cable which connects to systems elsewhere in the CUC, i.e., the RCE crates and the data selection system. This arrangement is shown in Figure 6.5

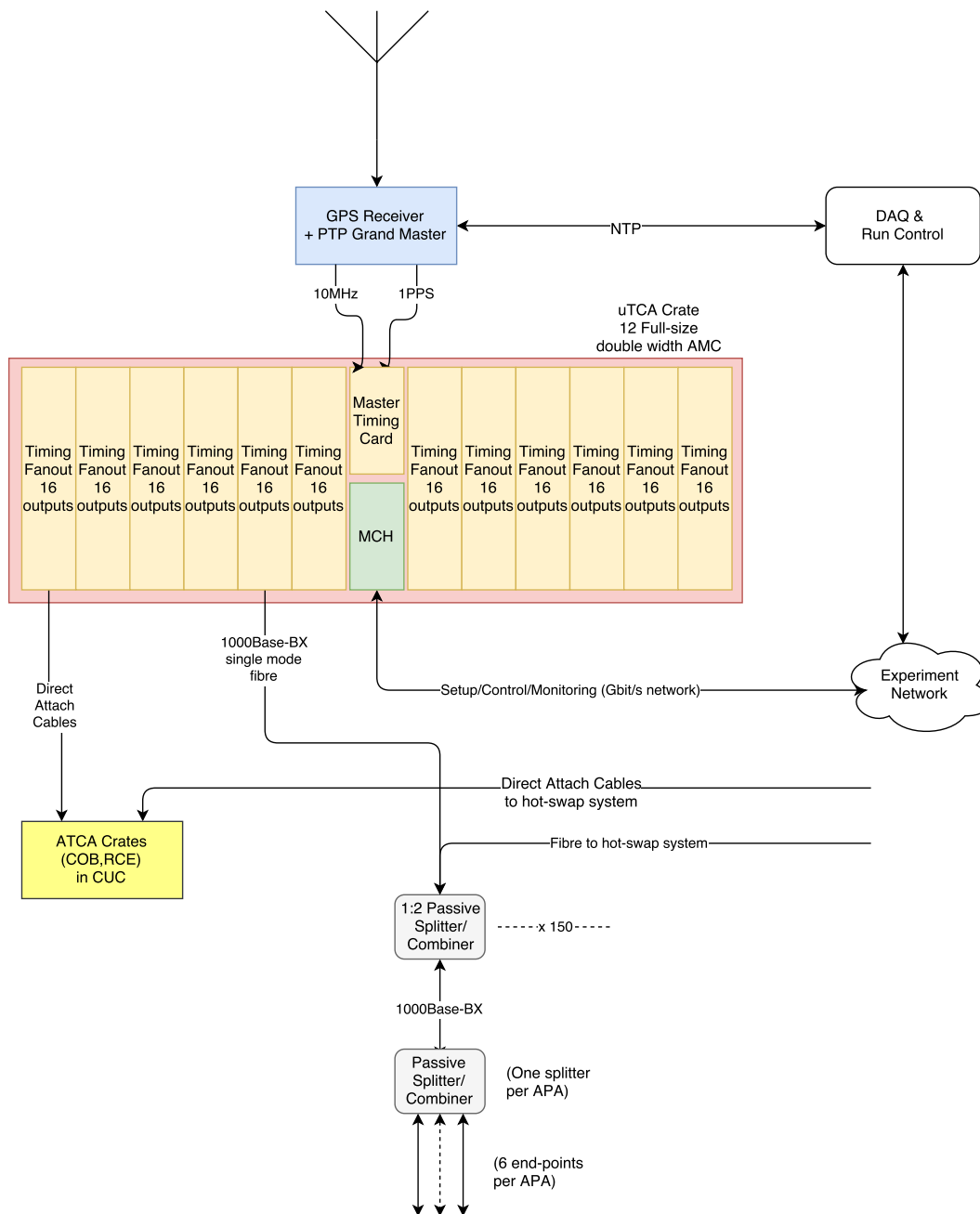


Figure 6.5: Illustration of the components in the SP timing system.

6.2.6.1 Beam timing

The neutrino beam is produced at the Fermilab accelerator complex in spills of 10 μ s duration. A spill location system (SLS) at the Far Detector site will locate the time periods in the data when beam could be present, based on network packets received from Fermilab containing predictions of the GPS-time of spills soon to occur or absolute time stamps of recent spills. Experience from MINOS and NO ν A shows that this can provide beam triggering with high reliability with some small fraction of late or dropped packets. To improve reliability further, the system outlined here contains an extra layer of redundancy in the prediction process. Several stages of prediction based on recent spill behavior will be applied, aiming for an accuracy of better than 10% of a readout time (sub-ms) in time for the data to be selected from the DAQ buffers. Ultimately, an offline database will match the actual time of the spill with the data, thus removing any reliance on real-time network transfer for this crucial stage of the oscillation measurements. The network transfer of spill-timing information is simply to ensure that a correctly located and sufficiently wide window of data is considered as beam data. This system is not required, and is not designed to provide signals accurate enough to measure neutrino time-of-flight.

The precision to which the spill time can be predicted at Fermilab improves as the acceleration process of the protons producing the spill in question advances. The spills currently occur at intervals of 1.3 s; the system will be designed to work with any interval, and to be adaptable in case the sequence described here changes. For redundancy, three packets will be sent to the far detector for each spill. The first is approximately 1.6 s before the spill-time, which is at the point where a 15 Hz booster cycle is selected; from this point on, there will be a fixed number of booster cycles until the neutrinos and the time is subject to a few ms of jitter. The second is about 0.7 s before the spill, at the point where the main injector acceleration is no longer coupled to the booster timing; this is governed by a crystal oscillator and so has a few μ s of jitter. The third will be at the so called ‘\$74’ signal generated before the beamline kicker magnet fires to direct the protons at the LBNF target; this doesn’t improve the timing at the Far Detector much, but serves as a cross check for missing packets. This system is enhanced compared to that of MINOS-NO ν A, which only use a third of the above timing signals. The reason for the larger uncertainty in the time interval from 1.6 s to 0.7 s is that the booster cycle time is synchronized to the electricity supply company’s 60 Hz, which has a variation of about 1%.

Arrival-time monitoring information from a year of MINOS data-taking was analyzed, and it was found that 97% of packets arrived within 100 ms of being sent and 99.88% within 300 ms.

The SLS will therefore have estimators of the GPS-times of future spills, and recent spills with associated data contained in the primary buffers. These estimators will improve in precision as more packets arrive. The DAQ will use data in a wider window than usual, if, at the time the trigger decision has to be made, the precision is lower due to missing or late packets. From the MINOS monitoring analysis, this expected to be very rare.

6.2.7 Computing and Network Infrastructure

The computing and network infrastructure that will be used in each of the four detector modules is similar, if not identical. It supports the buffering, data selection, event building, and data flow functionality described above, and it includes computing elements that consist of servers that:

- buffer the data until a trigger decision is received;
- host the software processes that build the data fragments from the relevant parts of the detector into complete events;
- host the processes that make the trigger decision;
- host the data logging processes and the disk buffer where the data is written;
- host the real-time data quality monitoring processing;
- host the control and monitoring processes.

The network infrastructure that connects these computers has the following components:

- subnets for transferring triggered data from the buffer nodes to the event builder nodes; these need to connect underground and above-ground computers;
- a control and monitoring subnet that connects all computers in the DAQ system and all FE electronics that support Ethernet communication; this sub-network must connect to underground and above-ground computers;
- a subnet for transferring complete events from the event builder servers to the storage servers; this subnet is completely above-ground.

6.2.8 Run Control and Monitoring

The online software constitutes the backbone of the DUNE DAQ system and provides control, configuration and monitoring of the data taking in a uniform way. It can be subdivided logically into four subsystems: the run control, the management of the DAQ and detector module electronics configuration, the monitoring, and the non-physics data archival. Each of these subsystems has a distinct function, but their implementation will share underlying technologies and tools.

In contrast to experiments in which data taking sessions, i.e., runs, are naturally subdivided into time slots by external conditions (e.g., a collider fill, a beam extraction period), the DUNE experiment aims to take data continuously. Therefore, a classic run control with a coherent state machine and a predefined and concurrently configured number of active detector and DAQ elements does not seem adequate.

The DUNE online software is thus structured according to the architecture principle of loose coupling: each component has as little knowledge as possible of other components. While the granularity of the back-end DAQ components may match the individual software processes, for the front-end DAQ a minimum granularity must be defined, balancing fault tolerance and recovery capability against the requirement of data consistency. The smallest independent component is called a DAQ front-end fragment, which is made up of the detector units associated with a single front-end computer. In the nominal design, this corresponds to two SP anode plane assemblies and about ten DP CRO crates.

The concept of a *run* represents a period of time in which the same FE elements are active or the same data selection criteria are in effect (possibly with maximum lengths for offline processing reasons). More than just orchestrating data taking, the run control provides the mechanisms allowing DAQ applications to publish their availability, subscribe to information, and exchange messages. In addition, the online software provides a configuration service for DAQ elements to store their settings and a conditions archive, keeping track of varying detector electronics settings and status.

Another important aspect of the online software is the monitoring service. Monitoring can be subdivided into two main domains: the monitoring of the data taking operations (rates, number of data fragments in flight, error flags, application logs, network bandwidth, computing and network infrastructure) and the monitoring of the physics data. Both are essential to the success of the experiment and must be designed and integrated into the DAQ system from the start. In particular, for such a large and distributed system, the information sharing and archival system is very important, as are scalable and easily accessible data visualization tools, which will evolve during the lifetime of the experiment. The online software provides the glue that holds the DAQ applications together and enables data taking. Its architecture guides the approach to DAQ application design and also shapes the view that the operators will have of the experiment.

6.3 Interfaces

6.3.1 TPC Electronics

Details about the interfaces between the DAQ and the TPC electronics are documented for the SP detector modules in [30].

In the case of the SP module, data from the CE front-end mother boards (FEMBs) are 8b10 encoded and sent to the WIBs on copper cables at a bit rate of 1.28 Gbit/s. There are two options being considered for the WIBs. In one, the data are simply converted to optical signals and transmitted to the DAQ in the CUC on 1.28 Gbit/s optical links with a total of 80 fibres per APA. In the second option, the WIBs aggregate the data onto links running at ≈ 10 Gbit/s before transmission to the DAQ, with a total of ten fibres per APA. In both cases the data are received on rear transition modules connected to the COB ATCA boards (see Section 6.2.2).

6.3.2 PD Electronics

Details about the interfaces between the DAQ and SP photon detection system are documented in [31].

For the SP PDS the S/N ratio of the silicon photomultiplier (SiPM) signals is high enough to allow zero-suppression to be safely applied to the data. This reduces the data flow so that a bandwidth of 8 Gbit/s per APA is sufficient to transfer it to the DAQ, with an order of magnitude safety factor. The link from the SP cryostat to the CUC will be implemented as either eight 1000Base-SX links or a single 10GBase-LR link per APA. The data on the links will be encoded using UDP/IP.

6.3.3 Offline Computing

The interface between the DAQ and offline computing is described in [32]. The DAQ team is responsible for reducing the data volume to the level that is agreed upon by all interested parties, and the raw data files are transferred from SURF to Fermilab using a dedicated network connection. A disk buffer is provided by the DAQ on or near the SURF site to hold several days worth of data so that the operation of the experiment is not affected if there happens to be a network disruption between SURF and Fermilab.

During stable running, the data volume produced by the DAQ systems of all four detector modules will be no larger than 30 PB/year. The maximum data rate is expected to be independent of the number of detector modules that are operational. During the construction of the second, third, and fourth detector modules, the extra rate per detector module will be used to gather data to aid in the refinement of the data selection algorithms. During commissioning, the data rate is expected to be higher than nominal running and it is anticipated that a data volume corresponding to (order) one year will be necessary to commission a detector module.

The disk buffer at SURF is planned to be 300 TB in size. The data link from SURF to Fermilab will support 100 Gbit/s (30 PB/year corresponds to about 8 Gbit/s). The offline computing team is responsible for developing the software to manage the transfer of files from SURF to Fermilab. The DAQ team is responsible for producing a reference implementation of the software that is used to access and decode the raw electronics data. The offline group is also responsible for providing the framework for real-time data quality monitoring (DQM). This monitoring is distinct from the online monitoring (OM). Developing the payload jobs that run various algorithms to summarize the data is the joint responsibility of the DAQ, offline, reconstruction and other groups. The DQM system includes a visualization system that can be accessed from the Internet and shows specifically where operation shifts are performed.

6.3.4 Slow Control

The cryogenic instrumentation and slow controls (CISC) systems monitor detector hardware and conditions not directly involved in taking the data described above. That data is stored both locally (in CISC database servers in the CUC) and offline (the databases will be replicated back to Fermilab) in a relational database indexed by timestamp. This allows bi-directional communications between the DAQ and CISC by reading or inserting data into the database as needed for non time-critical information.

For prompt, time sensitive status information such as *run is in progress* or *camera is on*, a low-latency software status register is available on the local network to both systems.

There is no hardware interface. However, several racks of CISC servers are in the counting room of the CUC, and rack monitors in DAQ racks are read out into the CISC data stream.

Note that life and hardware safety-critical items will be hardware interlocked according to Fermilab standards, and fall outside the scope of this interface.

6.3.5 External Systems

The DAQ is required to save data based on external triggers, e.g., when a pulse of beam neutrinos arrives at the FD; or upon notice of an interesting astrophysical event by SNEWS [33] or LIGO. This could involve going back to save data that has already been buffered (see Section 6.2.2), or changing the trigger or zero suppression criteria for data taken during the interesting time period.

6.3.5.1 Beam Trigger

The method for predicting and receiving the time of the beam spill is described in Section 6.2.6.1. Once that time is known to the DAQ, a high-level trigger can be issued to ensure that the necessary full data can be saved from the buffer and saved as an event.

6.3.5.2 Astrophysical Triggers

SuperNova Early Warning System (SNEWS) is a coincidence network of neutrino experiments that are individually sensitive to an SNB observed from a core-collapse supernova somewhere in our galaxy. While DUNE must be sensitive to such a burst on its own, and is expected to be able to contribute to the coincidence network (Section 6.2.5) via a TCP/IP socket, the capability to save data based on other observations provides an additional opportunity to ensure capture of this rare and valuable data. A SNEWS alert is formed when two or more neutrino experiments report a potential SNB signal within 10s. A script running on the SNEWS server at BNL, provided by a given experiment that wishes to receive an alert, sends out a message with the earliest time in the

coincidence. The latency from the neutrino burst is set by the response time of the second fastest detector to report to SNEWS. This could be as short as seconds, but could be tens of seconds. At latencies larger than 10 s, full data might not be available, but selected data is expected to be manageable.

Other astrophysical triggers are available to which DUNE alone is unlikely to have sensitivity, except in rare cases, or if the triggers are taken as an ensemble. Among these are gravitational wave triggers (the details are being worked out during the current LIGO shutdown), and high-energy photon transients, most notably gamma ray bursts. In fact, the use of network sockets on the timescale of seconds enabled cooperation between LIGO, VIRGO, the Gamma Ray Coordinates Network (GCN) ¹, and a number of automated telescopes to make the discovery that *short/hard* gamma ray bursts are caused by colliding neutron stars [34].

6.4 Production and Assembly

6.4.1 DAQ Components

The FD DAQ system comprises the classes of components listed below. In each case, we outline the production, procurement, quality assurance (QA), and quality control (QC) strategies.

6.4.1.1 Custom Electronic Modules

Custom electronic modules, specified and designed by the DAQ consortium, are used for two functional components in the DAQ FE. The first is to interface the detector module electronics to the DAQ FEC systems, which are likely to be based on the FELIX PCIe board. The other is for real-time data processing (particularly for the SP module), which will likely be based on the COB ATCA blade. ProtoDUNE-SP currently implements both designs, and new designs optimized according to DUNE requirements will be developed. It is possible that we will make use of commercially-designed hardware in one or other of these roles. DAQ consortium institutes have significant experience in the design and production of high-performance digital electronics for previous experiments. Our strategy is therefore to carry out design in-house, manufacturing and QA steps in industry, and testing and QC procedures at a number of specialized centers within the DUNE collaboration. Where technically and economically feasible, modules will be split into subassemblies (e.g., carrier board plus processing daughter cards), allowing production tasks to be spread over more consortium institutes.

DUNE electronic hardware will be of relatively high performance by commercial standards, and will contain high-value subassemblies such as large FPGAs. Achieving a high yield will require significant effort in design verification, prototyping and pre-production tests, as well as in tendering and vendor selection. The production schedule is largely driven by these stages and the need for

¹Described in detail at https://gcn.gsfc.nasa.gov/gcn_describe.html

thorough testing and integration with firmware and software before installation, rather than by the time for series hardware manufacture. This is somewhat different from the majority of other DUNE FD components.

6.4.1.2 Commercial Computing

The majority of procured items will be standard commercial computing equipment, in the form of compute and storage servers. Here, the emphasis is on correct definition of the detailed specification, and the tracking of technology development, in order to obtain the best value during the tendering process. Computing hardware will be procured in several batches, as the need for DAQ throughput increases during the construction period.

6.4.1.3 Networking and data links

The data movement system is a combination of custom optical links (for data transmission from the cryostats to the CUC) and commercial networking equipment. The latter items will be procured in the same way as other computing components. The favored approach to procurement of custom optics is purchase of pre-manufactured assemblies ready for installation, rather than on-site fiber preparation and termination. Since transmission distances and latencies in the underground area are not critical, the fiber run lengths do not need to be of more than a few variants. It is assumed that fibers will not be easily accessible for servicing or replacement during the lifetime of the experiment, meaning that procurement and installation of spare *dark* fibers (including, if necessary, riser fibers up the SURF hoist shafts) is necessary.

6.4.1.4 Infrastructure

All DAQ components will be designed for installation in 48.3 cm (standard 19 in) rack infrastructure, either in the CUC or above ground. Standard commercial server racks with local air-water heat exchangers are likely to be used. These items will be specified and procured within the consortium, but will be pre-installed (along with the necessary electrical, cooling and safety infrastructure) under the control of technical coordination (TC) before DAQ beneficial occupancy.

6.4.1.5 Software and firmware

The majority of the DAQ construction effort will be invested in the production of custom software and firmware. Based on previous experiments, these projects are likely to use tens to hundreds of staff-years of effort, and will be significant projects even by commercial standards, mainly due to the specialized skills required for real-time software and firmware. A major project management effort is required to guide the specification, design, implementation and testing of the necessary

components, especially as developers will be distributed around the world. Use of common components and frameworks across all areas of the DAQ is mandatory. Effective DAQ software and firmware development has been a demonstrated weakness of several previous experiments, and substantial work is required in the next two years to put in place the necessary project management regime.

6.4.2 Quality Assurance and Quality Control

High availability is a basic requirement for the DAQ, and this rests upon three key principles:

- A rigorous QA and QC regime for components (including software and firmware);
- Redundancy in system design, to avoid single points of failure;
- Ease of component replacement or upgrade with minimal downtime.

The lifetime of most electronic assemblies or commercial computing components will not match the 20 year lifespan of the DUNE experiment. It is to be expected that essentially all components will therefore be replaced during this time. Careful system design will allow this to take place without changes to interfaces. However, it is intended that the system run for at least the first three to four years without substantial replacements, and QA and QC, as well as spares production, will be steered by this goal. Of particular importance is adequate burn-in of all components before installation underground, and careful record-keeping of both module and subcomponent provenance, in order to identify systematic lifetime issues during running.

6.4.3 Integration testing

Since the DAQ will use subcomponents produced by many different teams, integration testing is a key tool in ensuring compatibility and conformance to specification. This is particularly important in the prototyping phase before the design of final hardware. Once pre-production hardware is in hand, an extended integration phase will be necessary in order to perform final debugging and performance tuning of firmware and software. In order to facilitate ongoing optimization in parallel with operations, and compatibility testing of new hardware or software, we envisage the construction of one or more permanent integration test stands at DAQ institutions. These will be in locations convenient to the majority of consortium members, i.e., at major labs in Europe and the USA. A temporary DAQ integration and testing facility near SURF will also be required as part of the installation procedure.

6.5 Installation, Integration and Commissioning

6.5.1 Installation

The majority of DAQ components will be installed in a dedicated and partitioned area of the CUC as shown in Figure 6.6, starting as soon as the consortium has beneficial occupancy of this space. The conventional facilities (CF) is responsible for running fiber from the SP module's WIBs to the DAQ, and from the DAQ to the surface. This is currently projected to take place eighteen months before anode plane assemblies are installed in the SP module, allowing time for final component acceptance testing in the underground environment, and to prepare the DAQ for detector testing and commissioning. Some DAQ components (event builder, storage cluster and WAN routers, plus any post-event-builder processing) will be installed above ground.

A total of 500 kVA of power and cooling will be available to run the computers in the counting room. Twelve 48.3 cm (standard 19 in) server racks (of up to 58U height) per module have initially been allocated for each detector module, with two more each for facilities and CISC. An optimized layout, including the necessary space for hardware installation and maintenance, plus on-site spares, will be developed once the DAQ design is finalized. The racks will be water cooled with local air-to-water heat exchangers. To allow expanded headroom for initial testing, development, and commissioning throughput, the full complement of rack infrastructure and network equipment for four detector modules will be installed from the start.

The counting room is similar to a server room at a university or national lab in terms of the need for cleanliness, ventilation, fire protection, drop flooring, and access control. Networking infrastructure and fiber breakout will take up some of the rack space, but very little of the power budget. Power to individual machines and crates must to be controlled remotely via power distribution units, since it is desirable to minimize DAQ workers' presence underground if there is work that can be done from the surface or remotely. Some uninterruptible power supply (UPS) capacity is needed to allow for an orderly shutdown of computers, but only networking equipment requires longer-duration backup power, this is to enable remote recovery from short-term power failures.

6.5.2 Integration with Detector Electronics

Basic technical integration with detector electronics will take place before installation, during a number of integration exercises in the preceding years. We anticipate that the consortium will supply and support small-scale instances of the DAQ system for testing of readout hardware at the production sites, based on prototype or pre-production hardware. Full-scale DAQ testing will have been completed with artificial data sources during internal integration. The work to be done during installation is therefore essentially channel-by-channel verification of the final system as it is installed, on a schedule allowing for any rectifying work to be carried out on the detector immediately (i.e., the DAQ must gather and present data in effectively real time). This implies the presence of a minimal but sufficient functional DAQ system before detector installation commences, along with the timing and fast control system, and the capability to permanently record data for

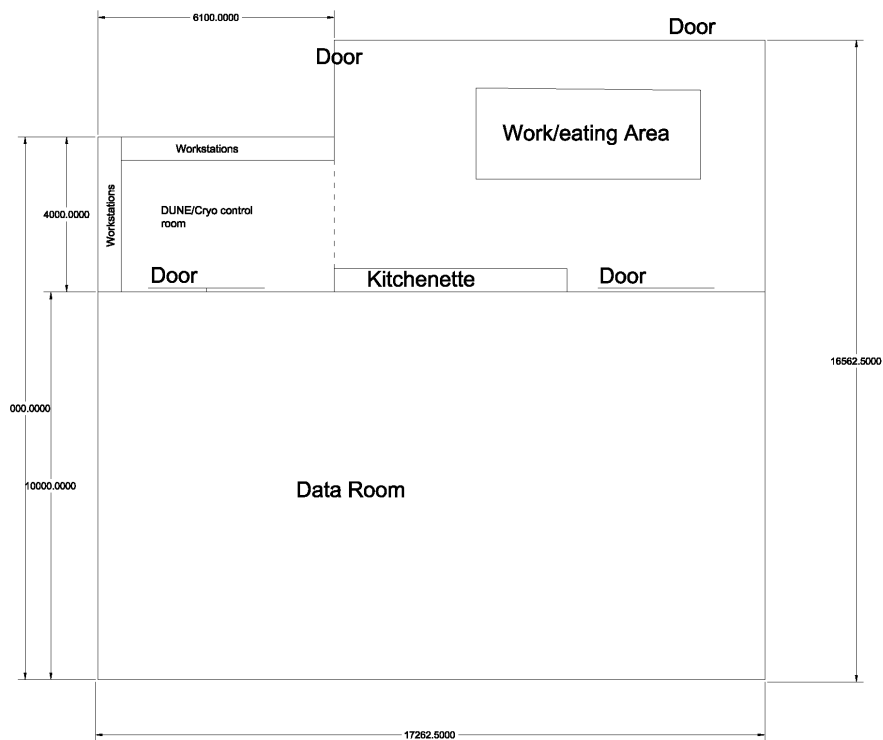


Figure 6.6: Floor plan for the DAQ and control room space in the CUC. The DAQ Room has space for at least 52 racks of servers and routers. Fiber from the WIBs in the detector caverns enter in the upper right of this room, terminate in a breakout panel, and are distributed to the RCEs in these racks, then to FELIX servers (also in this room) as outlined in Figure 6.3. Fibers to the surface enter this room from the lower left.

offline analysis. However, it does not require triggering, substantial event building or data transfer capacity. The DAQ installation schedule is essentially driven by this requirement.

In addition, the data pipeline from event builder, via the storage buffer and WAN, to the offline computing facilities, must be developed and tested. We anticipate this work largely happening at Fermilab in parallel with detector installation, and the full-scale instances of these components being installed at SURF in preparation for start of data-taking.

6.5.3 Commissioning

System commissioning for the DAQ comprises the following steps:

- Integration with detector subsystems of successive detector modules;
- Final integration and functional testing of all DAQ components;
- Establishment of the necessary tools and procedures to achieve high-efficiency operation;
- Selection, optimization and testing of trigger criteria;
- Ongoing and continuous self-test of the system to identify actual or imminent failures, and to assess performance.

Each of these steps will have been carried out at the integration test stands before being used on the final system. The final steps are to some extent continuous activities over the experiment lifetime, but which require knowledge of realistic detector working conditions before final validation of the system can take place. We anticipate that these steps will be carried out during the cryostat filling period, and form the major focus of the DAQ consortium effort during this time.

6.6 Safety

Two overall safety plans will be followed by the FD DAQ. General work underground will comply with all safety procedures in place for working in the detector caverns and CUC underground at SURF. DAQ-specific procedures for working with racks full of electronics or computers, as defined at Fermilab, will be followed, especially with respect to electrical safety and the fire suppression system chosen for the counting room. For example, a glass wall between the server room space and the other areas in Figure 6.6 will be necessary to prevent workers in the server room from being unseen if they are in distress, and an adequate hearing protection regime must be put in place.

There are no other special safety items for the DAQ system not already covered by the more general safety plans referenced above. The long-term emphasis is on remote operations capability from around the world, limiting the need for physical presence at SURF, and with underground

access required only for urgent interventions or hardware replacement.

6.7 Organization and Management

At the time of writing, the DAQ consortium comprises 30 institutions, including universities and national labs, from five countries. Since its conception, the DAQ consortium has met on roughly a weekly basis, and has so far held two international workshops dedicated to advancing the FD DAQ design. The current DAQ consortium leader is from U. Bristol, UK.

Several key technical and architectural decisions have been made in the last months, that have formed an agreed basis for the DAQ design and implementation presented in this document.

6.7.1 DAQ Consortium Organization

The DUNE DAQ consortium is currently organized in the form of five active Working Groups (WG) and WG leaders:

- Architecture, current WG leaders are from: U. Oxford and CERN;
- Hardware, current WG leaders are from: U. Bristol and SLAC;
- Data selection, current WG leader is from: U. Penn.;
- Back-end, current WG leader is from: Fermilab;
- Integration and Infrastructure, current WG leader is from: U. Minnesota Duluth.

During the ongoing early stages of the design, the architecture and hardware WGs have been holding additional meetings focused on aspects of the design related to architecture solutions and costing. In parallel, the DAQ Simulation Task Force effort, which was in place at the time of the consortium inception, has been adopted under the data selection WG, and simulation studies have continued to inform design considerations. This working structure is expected to remain in place through at least the completion of the interim design report (IDR). During the construction phase of the project we anticipate a new organization, built around major subsystem construction and commissioning responsibilities, and drawing also upon expertise build up during the ProtoDUNE projects.

6.7.2 Planning Assumptions

The DAQ planning is based the assumption of a SP module first, followed by a DP module. The schedule is sensitive to this assumption, as the DAQ requirements for the two module types are quite different. Five partially overlapping phases of activity are planned (see Figure 6.7):

- A further period of R&D activity, beginning at the time of writing, and culminating in a documented system design in the technical design report (TDR) around July 2019;
- Production and testing of a full prototype DAQ slice of realistic design, culminating in an engineering design review;
- Preparation and fit out of the CUC counting room with a minimal DAQ slice, in support of the first module installation;
- Production and delivery of final hardware, computing, software and firmware for the first module;
- Production and delivery of final hardware, computing, software and firmware for the second module.

This schedule assumes beneficial occupancy of the CUC counting room by end of the first quarter of 2022, and the availability of facilities to support an extended large-scale integration test in 2020 (e.g., CERN or Fermilab). We assume the availability of resources for installation and commissioning of final DAQ hardware (e.g., surface control room and server room facilities) from around the first quarter of 2023, and the integration and test facility (ITF) from the second quarter of 2022. The majority of capital resources for DAQ construction will be required from the second quarter of 2022, with a first portion of funds for the minimal DAQ slice from the first quarter of 2021.

6.7.3 High-level Cost and Schedule

The high-level DAQ schedule, which is based upon the current DUNE FD top-level schedule, is shown in Figure 6.7.

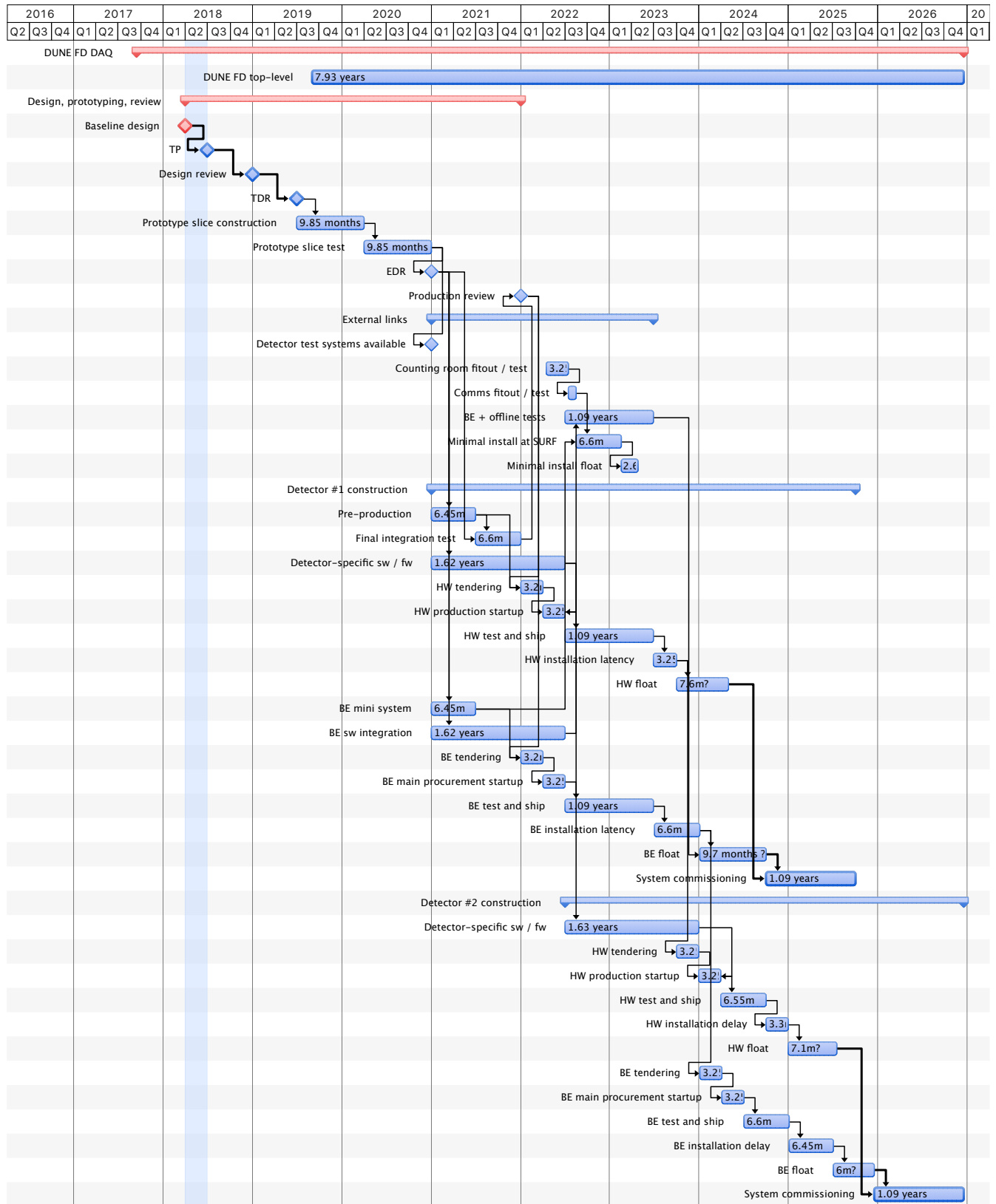


Figure 6.7: DAQ high-level schedule

Chapter 7

Slow Controls and Cryogenics Instrumentation

7.1 Slow Controls and Cryogenics Instrumentation Overview

7.1.1 Introduction

The cryogenic instrumentation and slow controls (CISC) system provides comprehensive monitoring for all detector module components as well as for the LAr quality and behavior, both being crucial to guarantee high-quality data. Beyond passive monitoring, CISC also provides a control system for some of the detector components. The structure of the CISC consortium is quite complex. A subsystem chart for the CISC system is shown in Figure 7.1.

Two main branches can be distinguished: cryogenics instrumentation and slow controls. The former includes a set of devices to monitor the quality and behavior of the LAr volume in the cryostat interior, ensuring the correct functioning of the full cryogenics system and the suitability of the LAr for good quality physics data. Those devices are purity monitors, temperature monitors, gas analyzers, LAr level monitors, cameras with their associated light emitting system.

Cryogenics instrumentation also requires significant physics and simulation work such as E field simulations and cryogenics modeling studies using computational fluid dynamics (CFD). E field simulations are required to identify desirable locations for instrumentation devices in the cryostat so that they are not in regions of high E field and that their presence does not induce large field distortions. CFD simulations are needed to understand the expected temperature, impurity and velocity flow distributions and guide the placement and distribution of instrumentation devices inside the cryostat.

From the organizational point of view cryogenics instrumentation has been divided into three main parts: (1) cryogenics systems, which includes all components directly related to the external cryo-

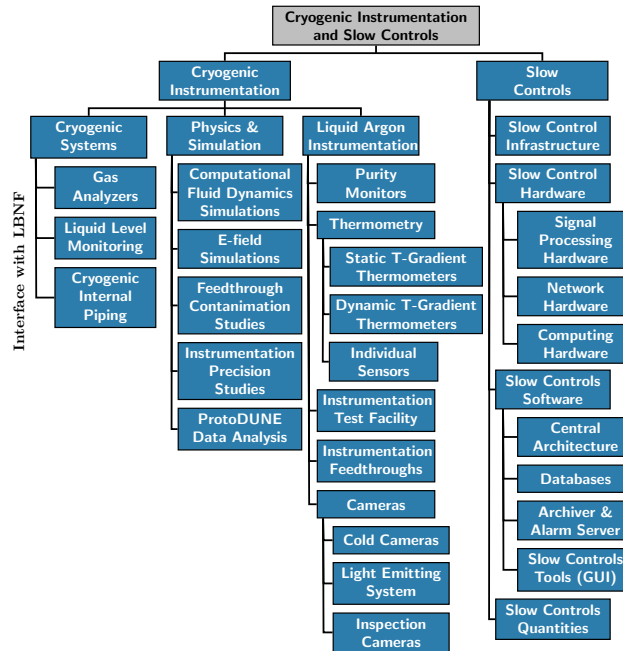


Figure 7.1: CISC subsystem chart

genic system as liquid level monitoring, gas analysers and internal cryogenics piping, all having substantial interfaces with LBNF; (2) LAr instrumentation, which includes all other instrumentation devices, and (3) physics and simulation.

The second branch of CISC is the slow controls (SC) system, in charge of monitoring and controlling most detector elements, as power supplies, electronics, racks, instrumentation devices, calibration devices, etc. It includes four main components: hardware, infrastructure, software, and firmware. The slow controls hardware and infrastructure consists of networking hardware, signal processing hardware, computing hardware, and relevant rack infrastructure. The slow controls software and firmware is needed for signal processing, alarms, archiving, and control room displays.

Two other systems have been included by the DUNE management as part of the CISC consortium, a test facility for the instrumentation devices and the cryogenics piping inside the cryostat. Those are included inside the cryogenics instrumentation branch.

7.1.2 Design Considerations

For all LAr instrumentation devices, ProtoDUNE-SP designs are considered as the baseline, and requirements for most design parameters are extrapolated from ProtoDUNE-SP. Hence a critical step for the CISC consortium is to analyze data from ProtoDUNE-SP when available to validate the instrumentation designs and understand their performance. For example, a crucial design parameter, which should be evaluated in ProtoDUNE-SP, is the maximum noise level induced by instrumentation devices on the readout electronics that can be tolerated to avoid confusing event

reconstruction.

Some of the common design considerations for instrumentation devices include stability, reliability and longevity such that the devices can survive for a period of at least 20 year. Since it is uncommon for any device to have such a long lifetime, provisions are made in the overall design to allow replacement of devices where possible.

As for any other element inside the cryostat, the E field on the instrumentation devices is required to be less than 30 kV/cm, so that the risk of dielectric breakdown in LAr is minimized. This requirement imposes stringent constraints on the location and mechanical design of some devices. Electrostatic simulations will be performed to compute the expected field on the boundaries of instrumentation devices and to design the appropriate E field shielding in the case the E field approaches the limit.

Another common consideration for all instrumentation devices is their support structure design, which is expected to be substantially different from the one used in ProtoDUNE-SP.

For slow controls, the system is designed to be robust enough to support a large number of monitored variables and a broad range of monitoring and archiving rates and has to interface with a large number of systems to establish two-way communication for control and monitoring. Table 7.1 shows some of the important CISC system design requirements.

7.1.3 Scope

As described above, and shown schematically in Figure 7.1, the scope of the CISC system spans a broad range of activities. In the case of cryogenics systems (gas analyzers, liquid level monitors and cryogenic internal piping), LBNF provides the needed expertise and is responsible for the design, installation, and commissioning activities while the CISC consortium provides the resources and supplements the labor as needed. In the case of LAr Instrumentation devices (purity monitors, thermometers, cameras and light-emitting system; and their associated feedthroughs) and instrumentation test facility, CISC is responsible from design to commissioning in the far detectors (FDs).

From the slow controls side, CISC provides control and monitoring of all detector elements that provide data on the health of the detector module or conditions important to the experiment. The scope of systems that slow controls includes is listed below:

- **Slow Controls Base Software and Databases:** provides the central tools needed to develop control and monitoring for various detector systems and interfaces.
 - Base input/output software,
 - Alarms; archiving; display panels; operator interface tools,
 - Slow controls system documentation and operations guidelines.

Table 7.1: Important design requirements on the single phase CISC system design

Design Parameter	Requirement	Motivation	Comment
Electron lifetime measurement precision	< 1.4 % at 3 ms	Per DUNE-FD Task Force [35], needed to keep the bias on the charge readout in the TPC to be low 0.5 % at 3 ms	Purity monitors do not directly sample TPC: see sec. 7.2.2
Thermometer precision	< 5 mK	Driven by CFD simulation validation; based on ProtoDUNE-SP-SP design	Expected ProtoDUNE-SP performance 2 mK
Thermometer density	> 2/m (vert.), ~ 0.2/m (horiz.)	Driven by CFD simulation	Achieved by design
Liquid level meters precision (SP)	0.1 % over 14 m	Standard sensitivity; two level meters for redundancy	ProtoDUNE-SP design
Cameras	— multiple requirements imposed by interfaces: see Table 7.3 —		
Cryogenic Instrumentation Test Facility cryostat volumes	0.5 to 3 m ³	Based on filling costs and turn around times	Under design
Max. E field on instrumentation devices	< 30 kV/cm	The mechanical design of the system should be such that E field is below this value, to minimize the risk of dielectric breakdown in LAr	ProtoDUNE-SP designs based on electrostatic simulations
Noise introduced into readout electronics	Below significant levels	Keep readout electronics free from external noise, which confuses event reconstruction	To be evaluated at ProtoDUNE-SP
Total no. of variables	50k to 100k	Expected number based on scaling past experiments; requires robust base software model that can handle large no. of variables.	Achievable in existing control systems; DUNE choice in progress.
Max. archiving rate per channel	1 Hz (burst), 1 min ⁻¹ (avg.)	Based on expected rapidity of interesting changes; impacts the base software choice; depends on data storage capabilities	Achievable in existing control system software; DUNE choice in progress.

- **Slow Controls for External Systems:** export data from systems external to the detector and provide status to operators and archiving.
 - Beam status; cryogenics status; data acquisition (DAQ) status; facilities systems status,
 - For the systems above, import other interesting monitoring data as needed (e.g., pumps data from cryogenics system, heaters data from facility systems, etc.),
 - Building controls; detector hall monitoring; ground impedance monitoring,
 - Interlock status bit monitoring (but not the actual interlock mechanism).
- **Slow Controls for Detector Hardware Systems:** develop software interfaces for detector hardware devices
 - Monitoring and control of all power supplies,
 - Full rack monitoring (rack fans, thermometers and rack protection system),
 - Instrumentation and calibration device monitoring (and control to the extent needed),
 - Power distribution units monitoring; computer hardware monitoring,
 - High voltage system monitoring through cold cameras,
 - Detector components inspection through warm cameras.

In terms of slow controls hardware, CISC will develop, install and commission any hardware related to rack monitoring and control. While most power supplies might only need a cable from the device to an Ethernet switch, some power supplies might need special cables (e.g., GPIB or RS232) for communication. The CISC consortium is responsible for providing such control cables.

In addition to the listed activities, CISC also has activities that span outside the scope of the consortium and require interfacing with other groups. This is discussed in Sec. 7.4.

7.2 Cryogenics Instrumentation

Instrumentation inside the cryostat must ensure that the condition of the liquid argon (LAr) is adequate for operation of the TPC. This instrumentation includes devices to monitor the impurity level of the argon, e.g., the purity monitors, which provide high-precision electron lifetime measurements, and gas analyzers to ensure that the levels of atmospheric contamination drop below certain limits during the cryostat purging, cooling and filling. The cryogenics system operation is monitored by temperature sensors deployed in vertical arrays and at the top and bottom of the detector, providing a detailed 3D temperature map that can help to predict the LAr purity

across the entire cryostat. The cryogenics instrumentation also includes LAr level monitors and a system of internal cameras to help in locating sparks in the cryostat and for overall monitoring of the cryostat interior. As mentioned in the introduction, cryogenics instrumentation requires simulation work to identify the proper location for these devices inside the cryostat and for the coherent analysis of the instrumentation data.

Figure 7.2 shows the current map of cryostat ports for the SP module, highlighting the ones assigned to instrumentation devices, as well as the preliminary location for some of these devices. Vertical temperature profilers are located behind the anode plane assemblies (APAs) (T_S) and behind the east end wall (T_D). They are complemented by a coarser 2D grid of sensors at the top and bottom of the cryostat (not shown in the figure). Purity monitors and level meters are planned in each detector side, behind the two front end walls. Inspection cameras will use some of the multipurpose instrumentation ports, but their exact locations are yet to be decided.

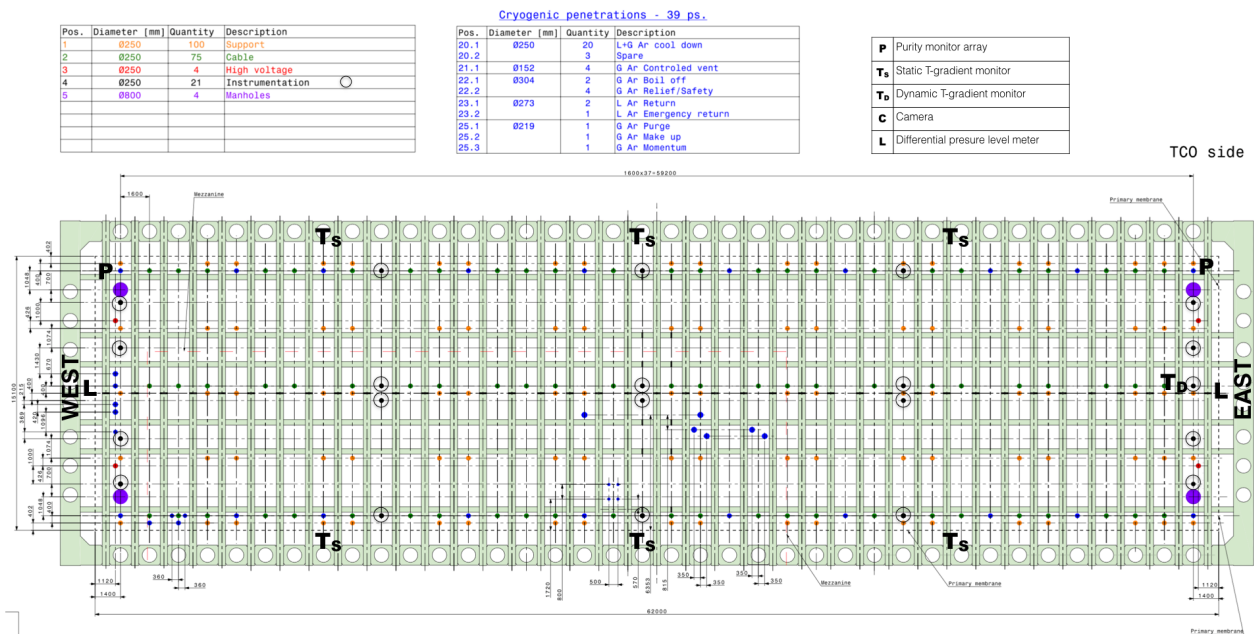


Figure 7.2: Cryostat ports and preliminary location of some instrumentation devices.

7.2.1 Fluid Dynamics Simulations

Proper placement of purity monitors, thermometers, and liquid level monitors within the detector module requires knowledge of how LAr behaves within the cryostat in terms of its fluid dynamics, heat and mass transfer, and distribution of impurity concentrations. Fluid motion within the cryostat is driven primarily by small changes in density from thermal gradients, although pump flow rates and inlet and outlet locations also contribute. Heat sources include exterior heat from the surroundings, interior heat from the electronics, and heat flow through the pump inlet.

The fluid flow behavior can be determined through simulation of LAr flow within the detector

using ANSYS CFX¹, a commercially available computational fluid dynamics (CFD) code. Such a model must include proper definition of the fluid characteristics, solid bodies and fluid-solid interfaces, and a means for measuring contamination, while still maintaining reasonable computation times. Although simulation of the detector module presents challenges, there exist acceptable simplifications for accurately representing the fluid, the interfacing solid bodies, and variations of contaminant concentrations. Because of the magnitude of thermal variation within the cryostat, modeling of the LAr is simplified through use of constant thermophysical properties, calculation of buoyant force through use of the Boussinesq Model (using constant a density for the fluid with application of a temperature dependent buoyant force), and a standard shear stress transport turbulence model. Solid bodies that contact the LAr include the cryostat wall, the cathode planes, the anode planes, the ground plane, and the field cage (FC). As in previous CFD models of the DUNE 35 ton prototype and ProtoDUNE by South Dakota State University (SDSU)[36], the FC planes, anode planes, and ground plane (GP) can be represented by porous bodies. Since impurity concentration and electron lifetime do not impact the fluid flow, these variables can be simulated as passive scalars, as is commonly done for smoke releases [37] in air or dyes released in liquids.

Significant discrepancies between real data and simulations can have potential impacts on detector performance, as simulation results contribute to decisions about where to locate sensors and monitors, as well as definitions of various calibration quantities. However, methods of mitigating such risks include well established convergence criteria, sensitivity studies, and comparison to results of previous CFD simulation work by SDSU and Fermilab. Additionally, the simulation will be improved with input from temperature measurements and validation tests.

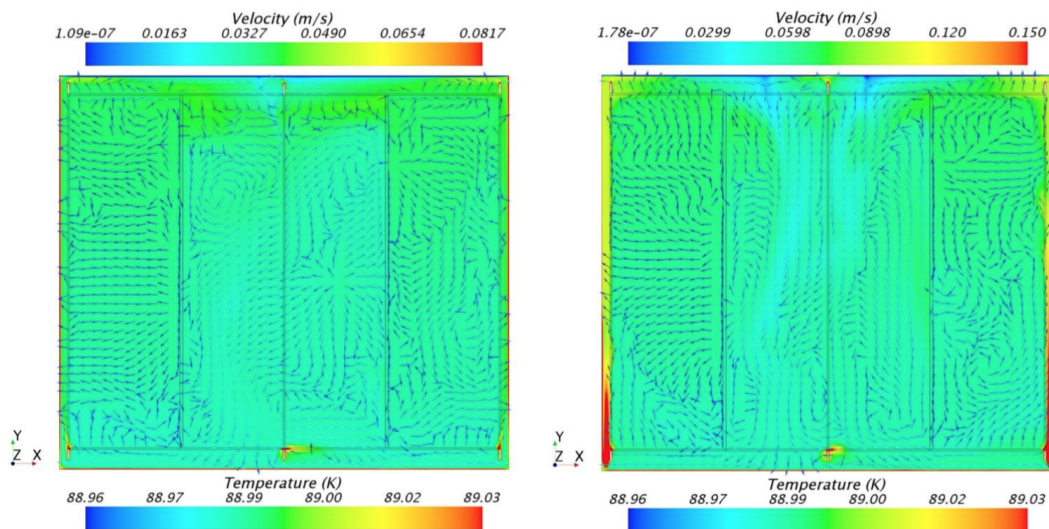


Figure 7.3: Distribution of temperature on a plane intersecting an inlet (right) and halfway between an inlet and an outlet (left), as predicted by SDSU CFD simulations [36]. (See Figure 7.4 for geometry.)

Figure 7.3 shows an example of the temperature distribution on a plane intersecting a LAr inlet and at a plane halfway between an inlet and an outlet; the geometry used for this simulation is shown in Figure 7.4. Note the plume of higher temperature LAr between the walls and the outer APA on the inlet plane. The current locations of instrumentation in the cryostat as shown in

¹ANSYS™, <https://www.ansys.com/products/fluids/ansys-cfx>.

Figure 7.2 were determined using the temperature and impurity distributions from these previous simulations.

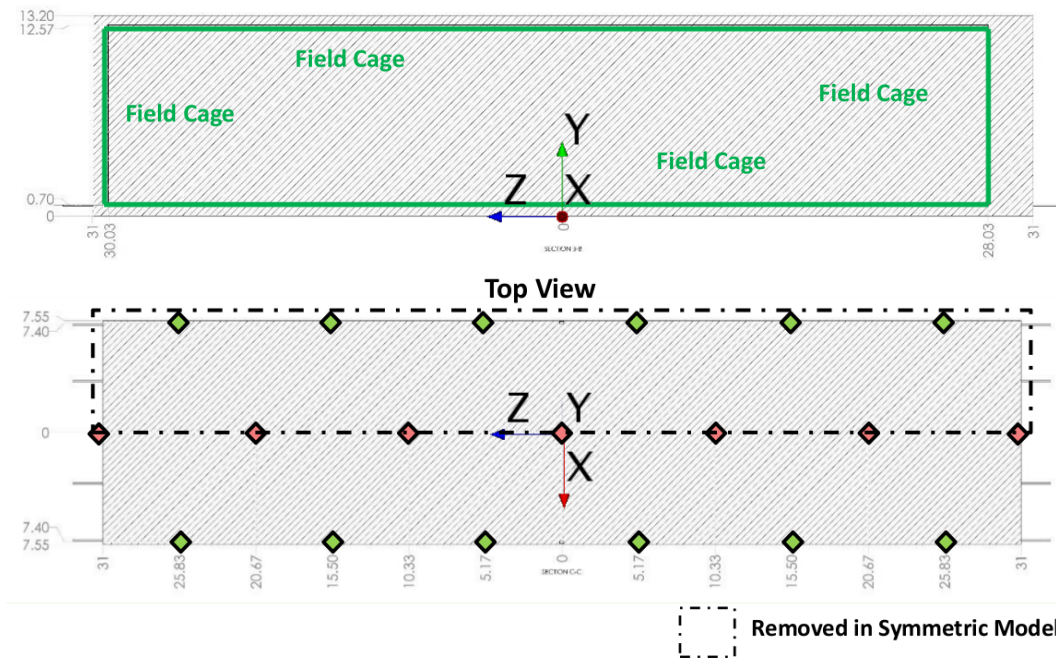


Figure 7.4: Layout of the TPC within the cryostat (top) and positions of LAr inlets and outlets (bottom) as modeled in the SDSU CFD simulations [36]. The Y axis is vertical and the X axis is parallel to the TPC drift direction. Inlets are shown in green and outlets are shown in red.

The initial strategy for the future computational fluid dynamics (CFD) simulation effort is to understand the performance of ProtoDUNE cryogenics system and model the FDs to derive requirements for instrumentation devices. The following is a prioritized set of studies planned to help drive the requirements for other systems:

1. Review the DUNE FD cryogenics system design and verify the current implementation in simulation; this is important to ensure that the model represents what will be built.
2. Model the ProtoDUNE-DP liquid and gas regions with the same precision as the FD. Presently only the liquid model exists. The liquid model is needed to interpret the thermometer data, and the gas model is needed to understand how to place thermometers in the ullage and verify the design of the gaseous argon purge system.
3. Perform a CFD study to determine the feasibility of a wiper for DP; this helps to determine if it can be used to clean the LAr surface before the extraction grid is submerged in the DP module.
4. Verify the SP module SP CFD model in simulation performed by LBNF; this defines the requirements for instrumentation devices (e.g., thermometry).
5. Model the ProtoDUNE-DP liquid and gas regions with the same precision as the FD.

7.2.2 Purity Monitors

A fundamental requirement of a LAr TPC is that ionization electrons drift over long distances in LAr. Part of the charge is inevitably lost due to the presence of electronegative impurities in the liquid. To keep such loss to a minimum, purifying the LAr during operation is essential, as is the monitoring of impurities.

Residual gas analyzers are an obvious choice when analyzing argon gas and can be exploited for the monitoring of the gas in the ullage of the tank. Unfortunately, commercially available and suitable mass spectrometers have a detection limit of ~ 10 parts per billion (ppb), whereas DUNE requires a sensitivity down to the parts per trillion (ppt) level. Instead, specially constructed purity monitors measure LAr purity in all the phases of operations, and enable the position-dependent purity measurements necessary to achieve DUNE's physics goal.

Purity monitors also serve to mitigate LAr contamination risk. The large scale of the detector modules increases the risk of failing to notice a sudden unexpected infusion of contaminated LAr being injected back into the cryostat. If this condition were to persist, it could cause irreversible contamination to the LAr and terminate useful data taking. Strategically placed purity monitors mitigate this risk.

Purity monitors are placed inside the cryostat, but outside of the detector TPC, as well as outside the cryostat within the recirculation system before and after filtration. Continuous monitoring of the LAr supply lines to the detector module provides a strong line of defense against contaminated LAr. Gas analyzers (described in Section 7.2.5) provide a first line of defense against contaminated gas. Purity monitors inside the detector module provide a strong defense against all sources of contamination in the LAr volume and contamination from recirculated LAr. Furthermore, multiple purity monitors measuring lifetime with high precision at carefully chosen points can provide key inputs to CFD models of the detector, such as vertical gradients in impurity concentrations.

Purity monitors have been deployed in the ICARUS and MicroBooNE detectors and in the 35 ton prototype detector at Fermilab. In particular during the first run of the 35 ton prototype, two out of four purity monitors stopped working during the cooldown, and a third was intermittent. It was later found out that this was due to poor electrical contacts of the resistor chain on the purity monitor. A new design was then implemented and successfully tested in the second run. The ProtoDUNE-SP and ProtoDUNE-DP employ purity monitors based on the same design principles. ProtoDUNE-SP utilizes a string of purity monitors similar to that of the 35 ton prototype, enabling measurement of the electron drift lifetime as a function of height. A similar system design is exploited in the DUNE FD, with modifications made to accommodate the instrumentation port placement relative to the purity monitor system and the requirements and constraints coming from the different geometric relations between the TPC and cryostat.

7.2.2.1 Physics and Simulation

A purity monitor is a small ionization chamber that can be used to independently infer the effective free electron lifetime in the LArTPC. The operational principle of the purity monitor consists of generating a known electron current via illumination of a cathode with UV light, followed by collecting at an anode the current that survives after drifting a known distance. The attenuation of the current can be related to the electron lifetime. The electron loss can be parameterized as $N(t) = N(0)e^{-t/\tau}$, where $N(0)$ is the number of electrons generated by ionization, $N(t)$ is the number of electrons after drift time t , and τ is the electron lifetime.

For the SP module, the drift distance is 3.53 m and the E field is 500 V cm^{-1} . Given the drift velocity at this field of approximately $1.5 \text{ mm } \mu\text{s}^{-1}$, the time to go from cathode to anode is around $\sim 2.4 \text{ ms}$ [38]. The LAr TPC signal attenuation, $[N(0) - N(t)]/N(0)$, is to be kept less than 20% over the entire drift distance [35]. The corresponding electron lifetime is $2.4/[-\ln(0.8)] \simeq 11 \text{ ms}$.

For the DP module, the maximum drift distance is 12 m, therefore the requirement on the electron lifetime is much higher.

The 35 ton prototype at Fermilab was instrumented with four purity monitors. The data taken with them during the first part of the second phase is shown in Figure 7.5 and clearly shows the ability to measure the electron lifetime between 100 μs and 3.5 ms.

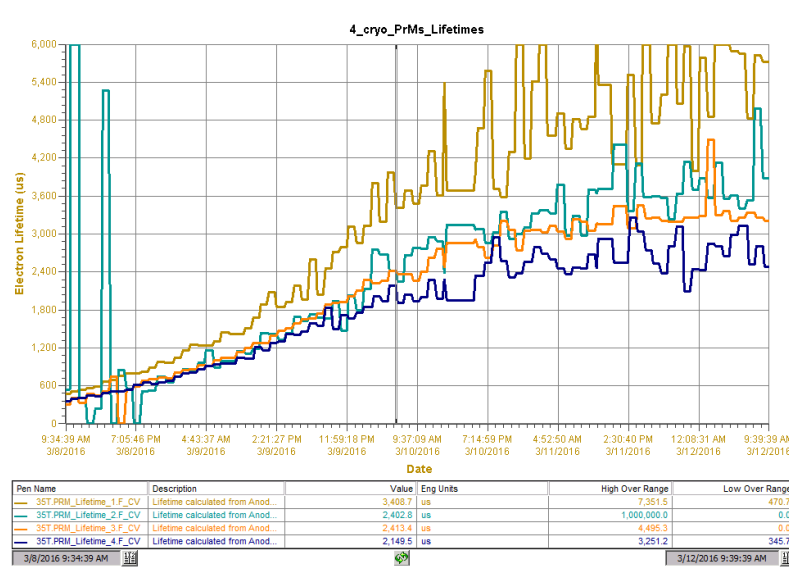


Figure 7.5: The measured electron lifetimes in the four purity monitors as a function of time at Fermilab 35 ton prototype.

7.2.2.2 Purity Monitor Design

The basic design of a purity monitor is based on those used by the ICARUS experiment (Figure 7.6)[39]. It is a double-gridded ion chamber immersed in the LAr volume. The purity monitor

consists of four parallel, circular electrodes: a disk holding a photocathode, two grid rings (anode and cathode), and an anode disk. The cathode grid is held at ground potential. The cathode, anode grid, and anode are electrically accessible via modified vacuum grade high-voltage feedthroughs and separate bias voltages held at each one. The anode grid and the field shaping rings are connected to the cathode grid by an internal chain of 50 M Ω resistors to ensure the uniformity of the E fields in the drift regions. A stainless mesh cylinder is used as a Faraday cage to isolate the purity monitor from external electrostatic backgrounds.

The purity monitor measures the electron drift lifetime between its anode and cathode. The electrons are generated by the purity monitor’s UV-illuminated gold photocathode via the photoelectric effect. As the electron lifetime in LAr is inversely proportional to the electronegative impurity concentration, the fraction of electrons generated at the cathode that arrive at the anode (Q_A/Q_C) after the electron drift time t gives a measure of the electron lifetime τ : $Q_A/Q_C \sim e^{-t/\tau}$.

It is clear from this formula that the purity monitor reaches its sensitivity limit once the electron lifetime becomes much larger than the drift time t . For $\tau \gg t$ the anode to cathode charge ratio becomes ~ 1 . But, as the drift time is inversely proportional to the E field, by lowering the drift field one can in principle measure any lifetime no matter the length of the purity monitor (the lower the field, the lower the drift velocity, i.e., the longer the drift time). In practice, at very low fields it is hard to drift the electrons all the way up to the anode. Currently, specific sensitivity limits for purity monitors with a drift distance of the order of ~ 20 cm are still to be determined in a series of tests. If the required sensitivity is not achieved by these “short” purity monitors, longer ones may be developed.

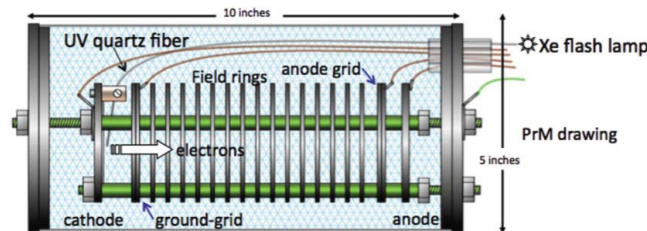


Figure 7.6: Schematic diagram of the basic purity monitor design [39].

The photocathode that produces the photoelectrons is an aluminum plate coated with 50 Å of titanium and 1000 Å of gold and attached to the cathode disk. A xenon flash lamp is used as the light source in the baseline design, although this could potentially be replaced by a more reliable and possibly submersible light source in the future, perhaps LED driven. The UV output of the lamp is quite good around $\lambda = 225$ nm, which is close to the work function of gold (4.9 eV to 5.1 eV). Several UV quartz fibers are used to carry the xenon UV light into the cryostat to illuminate the gold photocathode. Another quartz fiber is used to deliver the light into a properly biased photodiode outside of the cryostat to provide the trigger signal for when the lamp flashes.

7.2.2.3 Electronics, DAQ and Slow Controls Interfacing

The purity monitor electronics and DAQ system consist of front-end (FE) electronics, waveform digitizers, and a DAQ PC. The block diagram of the system is shown in Figure 7.7.

The baseline design of the FE electronics is the one used for the purity monitors at the 35 ton prototype, LAPD, and MicroBooNE. The cathode and anode signals are fed into two charge amplifiers contained within the purity monitor electronics module. The amplified outputs of the anode and cathode are recorded with a waveform digitizer that interfaces with a DAQ PC.

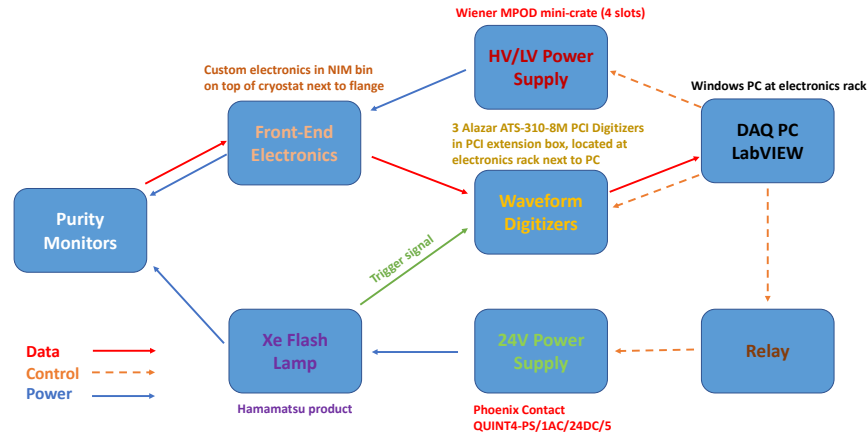


Figure 7.7: Block diagram of the purity monitor system.

A custom LabVIEW application running on the DAQ PC is developed and executes two functions: it controls the waveform digitizers and the power supplies, and it monitors the signals and key parameters. The application configures the digitizers to set the sampling rate, the number of waveforms to be stored in the memory, pre-trigger data, and a trigger mode. A signal from a photodiode triggered by the xenon flash lamp is directly fed into the digitizer as an external trigger to initiate data acquisition. The LabVIEW application automatically turns on the xenon flash lamp by powering a relay at the start of data taking and then turns it off when finished. The application continuously displays the waveforms and important parameters, such as measured electron lifetime, peak voltages, and drift time of electrons in the purity monitors, and shows these parameters over time.

The xenon flash lamp and the FE electronics are installed close to the purity monitor flange, to reduce light loss through the optical fiber and prevent signal loss. Other pieces of equipment are mounted in a rack separate from the cryostat. They distribute power to the xenon flash lamp and the FE electronics, as well as collect data from the electronics. The slow control system communicates with the purity monitor DAQ software and has control of the high voltage (HV) and LV power supplies of the purity monitor system. As the optical fiber has to be very close to the photocathode (less than 0.5 mm) for efficient photoelectron extraction, no interference with the photon detection system (PDS) is expected. Nevertheless light interference will be evaluated more precisely at ProtoDUNE.

Conversely the electronics of purity monitors may induce noise in the TPC electronics, largely coming from the current surge in the discharging process of the main capacitor of the purity monitor xenon light source when producing a flash. This source of noise can be controlled by placing the xenon flash lamp inside its own Faraday cage, allowing for proper grounding and shielding; the extent of mitigation will be evaluated at ProtoDUNE. If an unavoidable interference

problem is found to exist, then software can be implemented to allow the DAQ to know if and when the purity monitors are running and to veto purity monitor measurements in the event of a supernova neutrino burst (SNB) alert or trigger.

7.2.2.4 Production and Assembly

Production of the individual purity monitors and their assembly into the string that gets placed into the detector module cryostat follows the same methodology that is being developed for Pro-toDUNE. Each of the individual monitors is fabricated, assembled and then tested in a smaller test stand. After confirming that each of the individual purity monitors operates at the required performance, they are assembled together via the support tubes used to mount the system to the inside of the cryostat such that three purity monitors are grouped together to form one string, as shown in Figure 7.8. Each monitor is assembled as the string is built from the top down, and in the end three individual purity monitors hang from a single string. The assembly of the string concludes once the purity monitors are each in place, but with the Faraday cages removed and the HV cables and optical fibers yet to be run. This full string assembly is then shipped to the FD site for installation into the cryostat.



Figure 7.8: Design of the purity monitor string that will contain three purity monitors.

7.2.3 Thermometers

A detailed 3D temperature map is important to monitor the correct functioning of the cryogenics system and the LAr uniformity. Given the complexity and size of purity monitors, those can only be installed on the cryostat sides to provide a local measurement of the LAr purity. While a direct measurement of the LAr purity across the entire cryostat is not viable, a sufficiently detailed 3D temperature map can be used to predict the LAr purity using CFD simulations. Measuring the vertical temperature profile is especially important since this is closely related to the LAr recirculation and uniformity.

High-precision temperature sensors are distributed near the TPC walls in two ways: (1) in high-density (> 2 sensors/m) vertical arrays (the T-gradient monitors), and (2) in coarser (~ 1 sensor/5 m) 2D arrays at the top and bottom of the detector, which are the most sensitive regions (the individual sensors).

Since temperature variations inside the cryostat are expected to be very small (0.02 K, see Figure 7.3), to properly measure the 3D temperature map sensors must be cross-calibrated to better than 0.005 K. Most sensors are calibrated in the laboratory, prior to installation, as described in Section 7.2.3.1. This is in fact the only viable method for sensors in areas where the available space is restricted: on the long sides of the detector (behind the anode plane assemblies for SP, and behind the lateral endwall field cage (endwall FC) for DP) and top/bottom of the detector.

Given the precision required and the unknown longevity of the sensors (which could require a new calibration after some time), a complementary method is used for T-gradient monitors behind the front endwalls, at least for the SP module. In those areas there is sufficient space for a movable system that can be used to cross-calibrate in situ the temperature sensors.

In the baseline design for all three systems mentioned above, three elements are common: sensors, cables and readout system. Platinum sensors with $100\ \Omega$ resistance, PT100 series, produced by Lakeshore², are adequate for the temperature range of interest, 83 K to 92 K, since in this range those sensors have ~ 5 mK reproducibility and absolute temperature accuracy of 100 mK. In addition, using four-wire readout greatly reduces the issues related to the lead resistance, any parasitic resistances, connections through the flange, and general electromagnetic noise pick-up. The Lakeshore PT102 sensors have been previously used in the 35 ton prototype and ProtoDUNE-SP detector, giving excellent results. For the inner readout cables a custom cable made by Axon³ is the baseline. It consists of four AWG28 teflon-jacketed copper wires forming two twisted pairs, with a metallic external shield and an outer teflon jacket. The readout system is described below in Section 7.2.3.5.

Another set of lower-precision sensors is used to monitor the filling of the cryostat in its initial stage. Those sensors are epoxied into the cryostat bottom membrane with a density to be determined, not to exceed one sensor every 5 m. Finally, the inner walls and roof of the cryostat are instrumented with the same type of sensors in order to monitor their temperature during cooldown and filling. The baseline distribution has three vertical arrays of sensors epoxied to the membrane: one behind each of the two front endwall FCs and the third one in the middle of the cryostat (behind the anode plane assemblies for SP and behind the lateral endwall FCs for DP).

7.2.3.1 Static T-gradient Monitors

Several vertical arrays of high-precision temperature sensors cross-calibrated in the laboratory are installed near the lateral walls (behind the anode plane assemblies for SP and behind the lateral endwall FCs for DP). For the SP module, since the electric potential is zero behind the anode plane assemblies, no E field shielding is required, simplifying enormously the mechanical design. This does not apply for the DP module, for which the proper shielding must be provided.

Sensors are cross-calibrated in the lab using a well controlled environment and a high-precision readout system, described below in Section 7.2.3.5. Although the calibration procedure will certainly improve, the one currently used for ProtoDUNE-SP is described here. Four sensors are placed as close as possible (such that identical temperature can be assumed for all of them) inside a small cylindrical aluminum capsule, which protects the sensors from thermal shocks and helps in minimizing convection. One of the sensors acts as reference while the other three are calibrated. Five independent calibrations are performed for each set of three sensors, such that the reproducibility of each sensor can be computed. For each calibration the capsule is introduced in a 3D printed polylactic acid (PLA) box of size $9.5 \times 9.5 \times 19$ cm³, with two concentric independent volumes of LAr and surrounded by a polystyrene box with 15 cm thick walls. A small quantity of

²Lakeshore™, <https://www.lakeshore.com/Pages/Home.aspx>.

³Axon™, http://www.axon-cable.com/en/00_home/00_start/00/index.aspx

LAr is used to slowly cool down the capsule to ~ 90 K, avoiding thermal shocks that could damage the sensors. Then the capsule is immersed in LAr such that it penetrates inside, fully covering the sensors. Once the temperature stabilizes to the 1-2 mK level (after 5-15 minutes) measurements are taken. Then the capsule is taken out from LAr and exposed to room temperature until it reaches 200 K. As mentioned above, this procedure is repeated five times, before going to the next set of three sensors. As shown in Figure 7.10 a reproducibility (RMS of the mean offset in the flat region) of ~ 2 mK has been achieved in the ProtoDUNE-SP design.

The baseline design for the mechanics of the SP system consists of two stainless strings anchored at top and bottom corners of the cryostat using the available M10 bolts (see Figure 7.9). One of the strings is used to route the cables while the other, separated by 340 mm, serves as support for temperature sensors. Given the height of the cryostat, the need of intermediate anchoring points is under discussion. For the DP module no baseline design exists yet, since additional complications due to the required E field shielding must be taken into account. Figure 7.9 shows the baseline design of the PCB support for temperature sensors, with an IDC-4 male connector. It has a size of 52×15 mm². Each four-wire cable from the sensor to the flange has an IDC-4 female connector on the sensor side; on the other side, it is directly soldered into the inner pins of male SUBD-25 connectors on the flanges. The CF63 side ports on the detector support system (DSS)/cryogenic ports are used to extract the cables.

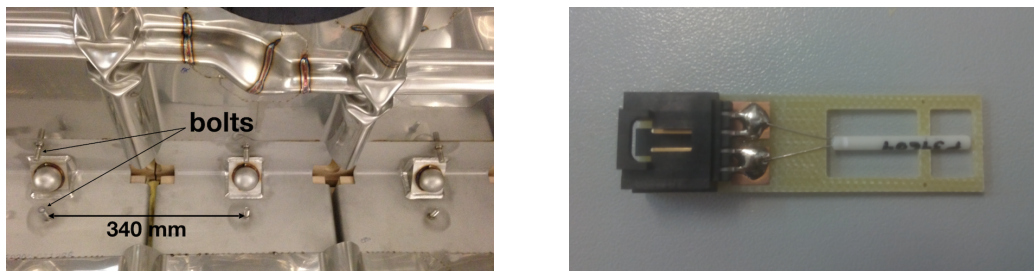


Figure 7.9: Left: bolts at the bottom corner of the cryostat. Right: Lakeshore PT102 sensor mounted on a PCB with an IDC-4 connector.

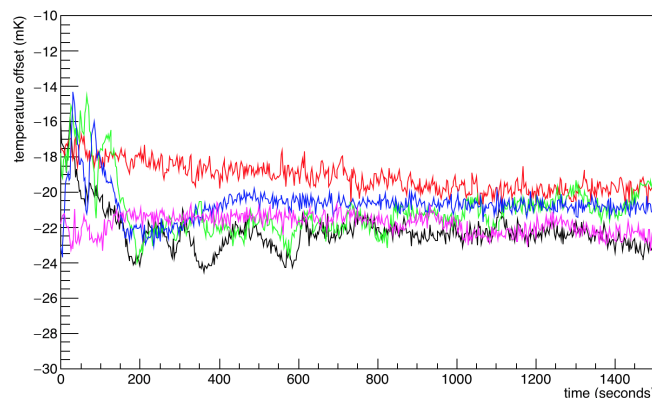


Figure 7.10: Temperature offset between two sensors as a function of time for five independent immersions in LAr. The reproducibility of those sensors, defined as the RMS of the mean offset in the flat region, is ~ 2 mK. The resolution for individual measurements, defined as the RMS of one of the offsets in the flat region, is better than 1 mK.

7.2.3.2 Dynamic T-gradient Monitors

The dynamic temperature monitor is a vertical array of high precision temperature sensors with the goal of measuring vertical temperature gradient with precision of few mK. The design of the system is driven by two factors:

- A few-mK uncertainty in the measured vertical temperature profile over the entire detector height is required in order to monitor LAr purity and provide useful feedback of efficiency of cryogenic recirculation and purification.
- Simulations of the cryogenic recirculation predict very slow change in temperature at meter scale except at the bottom and top of the cryostat. Thus, sensors are placed every 50 cm along the detector module height with increased frequency in the first 50 cm, closest to the bottom of the cryostat and the last 50 cm, closest to the top of the cryostat, where spacing between sensors is reduced to 10 cm.

In order to address concerns related to possible differences in the sensor readings prior to and after installation in a detector module, a dynamic temperature monitor allows cross-calibration of sensors in situ. Namely, this T-gradient monitor can move vertically while installed in the detector module, which allows for precise cross-calibration between the sensors in situ at predefined locations, as well as in between them. The procedure for cross-calibrations is the following: the temperature reading is taken at the lowest position with all sensors. The stepper motor then moves the carrier rod up 50 cm, putting all sensors in the previous location of their neighbor that was 50 cm above them. Then the second reading is taken. In this manner, except for the lowest position we have temperature measurement at each location with two adjacent sensors, and by linking the temperature offsets between the two readings at each location, temperature readings from all sensors are cross-calibrated in situ, cancelling all offsets due to electromagnetic noise or any parasitic resistances that may have prevailed despite the four point connection to the sensors that should cancel most of the offsets. These measurements are taken with very stable current source, which ensures high precision of repeated temperature measurements over time. The motion of the dynamic T-monitor is stepper motor operated, delivering measurements with high spatial resolution.

7.2.3.3 Dynamic T-gradient Monitor Design

A dynamic T-gradient monitor consists of three distinct parts: a carrier rod on which sensors are mounted, an enclosure above the cryostat housing the space that allows vertical motion of the carrier rod 1.5 m above its lowest location, and the motion mechanism. The motion mechanism consists of a stepper motor connected to a gear and pinion through a ferrofluidic dynamic seal. The sensors have two pins that are soldered to a printed circuit board (PCB). Two wires are soldered to the common soldering pad for each pin, individually. There is a cutout in the PCB around the sensor that allows free flow of argon for more accurate temperature reading. Stepper motors typically have very fine steps allowing high-precision positioning of the sensors. Figure 7.11 shows the overall design of the dynamic T-gradient monitor with the sensor carrier rod, enclosure above

the cryostat and the stepper motor mounted on the side of the enclosure. The enclosure consists of two parts connected by a six-way cross flange. One side of this cross flange is used to for the signal wires, another side is used as a viewing window, while the two other ports are spares. Figure 7.12 (left) shows the mounting of the PCB board on the carrier rod and mounting on the sensor on the PCB along with the four point connection to the signal readout wires. Finally, Figure 7.12 (right) shows the stepper motor mounted on the side of the rod enclosure. The motor is kept outside, at room temperature, and its power and control cables are also kept outside.

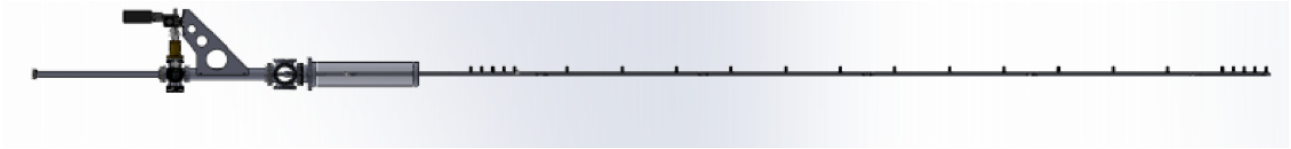


Figure 7.11: An overview of the dynamic T-gradient monitor.

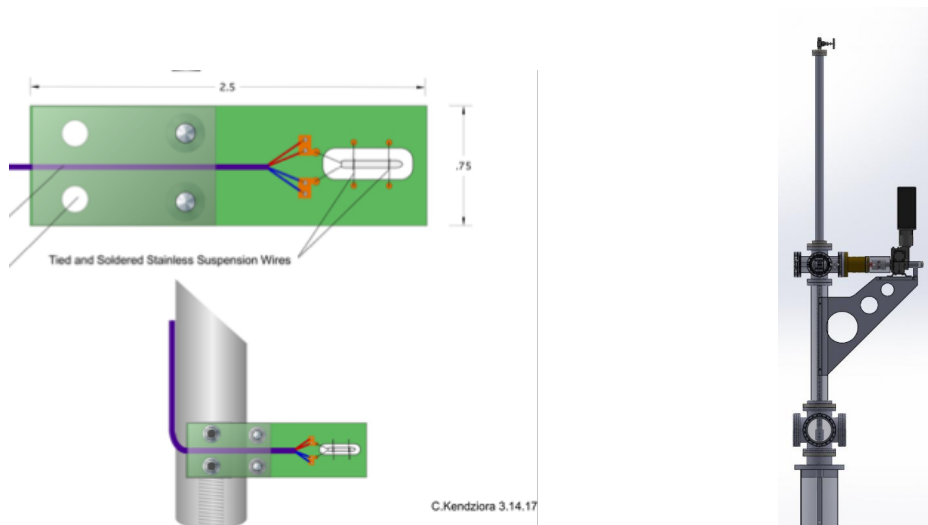


Figure 7.12: Left: Sensor mounted on a PCB board and PCB board mounted on the rod. Right: The driving mechanism of the dynamic T-gradient monitor. It consists of a stepper motor driving the pinion and gear linear motion mechanism.

7.2.3.4 Individual Temperature Sensors

T-Gradient monitors provide a vertical temperature profiling outside the TPCs. They are complemented by a coarser 2D array at the top and bottom of the detector. Sensors, cables and readout system are the same as for the T-gradient monitors.

In principle, a similar distribution of sensors is used at top and bottom. Following the ProtoDUNE-SP design, bottom sensors use the cryogenic pipes as a support structure, while top sensors are anchored to the GPs. Teflon pieces (see Figure 7.13) are used to route cables from the sensors to the CF63 side ports on DSS-cryogenics ports, which are used to extract the cables. The PCB sensor's support, cables and connection to the flanges are the same as for the static T-gradient monitors.

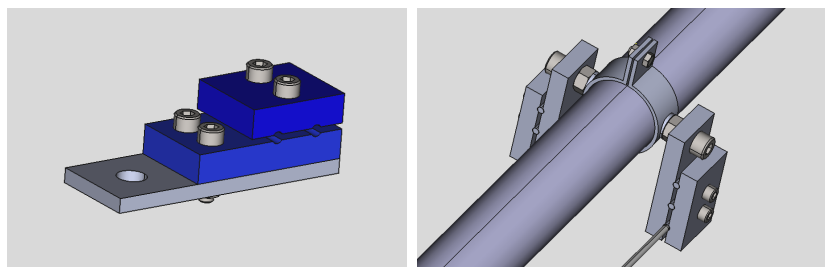


Figure 7.13: Left: support for two cables on ground planes. Right: Supports for three cables mounted on cryogenics pipes using split clamps

7.2.3.5 Readout System for Thermometers

A high precision and very stable system is required to achieved the design precision of < 5 mK. The proposed readout system is the one used in ProtoDUNE-SP, which is based on a variant of an existing mass PT100 temperature readout system developed at CERN for one of the LHC experiments. The system consists of three parts:

- An accurate current source for the excitation of the temperature sensors, implemented by a compact electronic circuit using a high-precision voltage reference from Texas Instruments ⁴;
- A multiplexing circuit based on an Analog Devices ADG707⁵ multiplexer electronic device;
- A high-resolution and accuracy voltage signal readout module based on National Instruments ⁶ NI9238, which has 24 bit resolution over a 1 V range. This module is inserted in a National Instruments compact RIO device that distributes the temperature values to the main slow control software through the standard OPC UA protocol. The Ethernet DAQ also includes the multiplexing logic.

The current mode of operation averages over 2000 samples taken every second for each sensor. As inferred from Figure 7.10 the system has a resolution better than 1 mK, the RMS of one of the offsets in the stable region.

7.2.4 Liquid Level Monitoring

The goals for the level monitoring system are basic level sensing when filling, and precise level sensing during static operations.

For filling the detector module the differential pressure between the top of the detector and known points below it can be converted to depth using the known density of LAr. The temperatures of

⁴Texas Instruments™, <http://www.ti.com/>.

⁵Analog Devices™, http://www.analog.com/media/en/technical-documentation/data-sheets/ADG706_707.pdf.

⁶National Instruments™, <http://www.ni.com/en-us.html/>.

RTDs at known heights may also be used to determine when the cold liquid reaches each RTD.

During operation, the purpose of liquid level monitoring is twofold: the cryogenics system uses it to tune the LAr flow, and the SP module uses it to guarantee that the top GPs are always submerged (otherwise the risk of dielectric breakdown is high). Two differential pressure level meters are installed as part of the cryogenics system, one on each side of the detector module. They have a precision of 0.1%, which corresponds to 14 mm at the nominal LAr surface. This precision is sufficient for the SP module, since the plan is to keep the LAr surface at least 20 cm above the GPs (this is the value used for the HV interlock in ProtoDUNE-SP); thus, no additional level meters are required for the SP. However, in the DP LAr system the surface level should be controlled at the millimeter level, which can be accomplished with capacitive monitors. Using the same capacitive monitor system in each detector module reduces design differences and provides a redundant system for the SP. Either system could be used for the HV interlock.

Table 7.2 summarizes the requirements for the liquid level monitor system.

Table 7.2: Liquid level monitor requirements

Requirement	Physics Requirement Driver
Measurement accuracy (filling) ~ 14 mm	Understand status of detector during filling
Measurement accuracy (operation, DP) ~ 1 mm	Maintain correct depth of gas phase. (Exceeds SP requirements)
Provide interlock with HV	Prevent damage to detector module from HV discharge in gas

Cryogenic pressure sensors will be purchased from commercial sources. Installation methods and positions will be determined as part of the cryogenics internal piping plan. Sufficient redundancy will be designed in to ensure that no single point of failure compromises the level measurement.

Multiple capacitive level sensors are deployed along the top of the fluid to be used during stable operation and checked against each other.

During operations of the WA105 DP demonstrator, the cryogenic programmable logic controller (PLC) continuously checked the measurements from one level meter on the charge readout plane (charge-readout plane (CRP)) in order to regulate the flow from the liquid recirculation to maintain a constant liquid level inside the cryostat. Continuous measurements from the level meters around the drift cage and the CRP demonstrated the stability of the liquid level within the 100 μm intrinsic precision of the instruments. The observation of the level was complemented by live feeds from the custom built cryogenic cameras, thereby providing qualitative feedback on the position and flatness of the surface.

In addition to the installed level meters, the liquid height in the extraction region of the CRP could be inferred by measuring the capacitance between the grid and the bottom electrode of each large electron multiplier (LEM). Averaging over all 12 LEMs the measured values of this capacitance typically ranged from 150 pF with the liquid below the grid to around 350 pF when the LEMs are submerged. This method offers the potential advantage of monitoring the liquid level in the CRP extraction region with a $50 \times 50 \text{ cm}^2$ granularity and could be used for the CRP level adjustment

in a DUNE DP module where, due to the space constraints, placement of the level meters along the CRP perimeter is not possible.

7.2.5 Gas Analyzers

Gas analyzers are commercially produced modules that measure trace quantities of specific gases contained within a stream of carrier gas. The carrier gas for DUNE is argon, and the trace gases of interest are oxygen (O_2), water (H_2O), and nitrogen (N_2). Oxygen and water impact the electron lifetime in LAr, while N_2 impacts the efficiency of scintillation light production. In the LAr environment, these trace gases represent contaminants that need to be kept at levels below 0.1 ppb. The argon is sampled from either the argon vapor in the ullage or from the LAr by the use of small diameter tubing run from the sampling point to the gas analyzer. Typically the tubing runs from the sampling points are connected to a switchyard valve that is used to route the sample points to the desired gas analyzers. Figure 7.14 is a photo of such a switchyard.

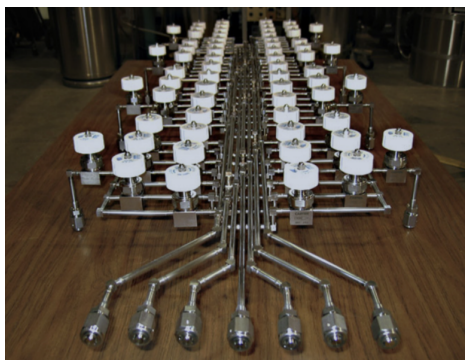


Figure 7.14: A Gas Analyzer switchyard that routes sample points to the different gas analyzers.

Gas analyzers can be used to:

1. Eliminate the air atmosphere from the cryostat after detector installation to levels low enough to begin cooldown is an argon piston purge followed by a recirculation of the remaining argon gas through the filtration system. This process is described more fully in Section 7.5. Figure 7.15 shows the evolution of the N_2 , O_2 , and H_2O levels from gas analyzer data taken during the purge and recirculation stages of the DUNE 35 ton prototype phase 1 run.
2. Track trace O_2 and H_2O contaminants from the tens of ppb to the hundreds of ppt. This is useful when other means of monitoring the impurity level (e.g., purity monitors, or TPC tracks) are not yet sensitive. Figure 7.16 shows an example plot of the O_2 level at the beginning of LAr purification from one of the later 35t HV runs.
3. Monitor the tanker LAr deliveries purity during the cryostat-filling period. This allows tracking the impurity load on the filtration system and rejecting any deliveries that are out of specifications. Likely specifications for the delivered LAr are in the 10 ppm range per contaminant.

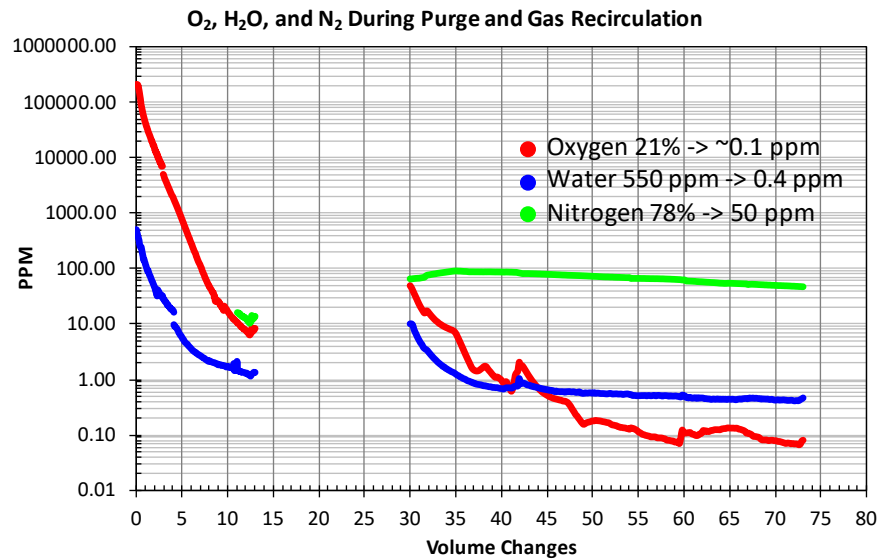


Figure 7.15: Plot of the O₂, H₂O, and N₂ levels during the piston purge and gas recirculation stages of the 35t phase 1 run.

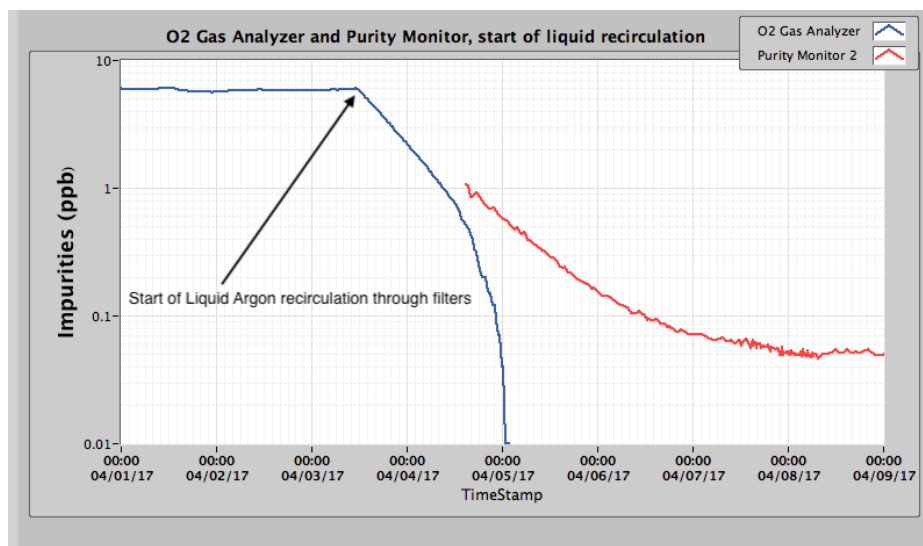


Figure 7.16: O₂ as measured by a precision O₂ analyzer just after the 35 ton prototype was filled with LAr, continuing with the LAr pump start and beginning of LAr recirculation through the filtration system. As the gas analyzer loses sensitivity, the purity monitor is able to pick up the impurity measurement. Note that the purity monitor is sensitive to both O₂ and H₂O impurities giving rise to its higher level of impurity.

As any one gas analyzer covers only one contaminant species and 3 to 4 orders of magnitude of range, multiple units are needed both for the three contaminant gases and to cover the ranges that are seen between the cryostat closure to the beginning of TPC operations: 20% to \lesssim 100 ppt for O_2 , 80% to \lesssim 1 ppm for N_2 , and \sim 1% to \lesssim 1 ppb for H_2O . Since the total cost of these analyzers exceeds \$100k, it is useful to be able to sample more than a single location or cryostat with the same gas analyzers. At the same time, the tubing run lengths from the sample point should be as short as possible in order to keep the response of the gas analyzer timely. This puts some constraints on the sharing of devices since, for example, the argon deliveries are at the surface, perhaps necessitating a separate surface gas analyzer.

7.2.6 Cameras

Cameras provide direct visual information about the state of the detector module during critical operations and when damage or unusual conditions are suspected. Cameras in the WA105 DP demonstrator allowed spray from cool-down nozzles to be seen and the level and state of the LAr to be observed as it covered the CRP [40]. A camera was used in the Liquid Argon Purity Demonstrator cryostat[39] to study HV discharges in LAr, and in EXO-100 during operation of a TPC [41]. Warm cameras viewing LAr from a distance have been used to observe HV discharges in LAr in fine detail [42]. Cameras are commonly used during calibration source deployment in many experiments (e.g., the KamLAND ultra-clean system [43]).

In DUNE, cameras are used to verify the stability, straightness, and alignment of the hanging TPC structures during cool-down and filling; to ensure that there is no bubbling near the GPs (SP) or CRPs (DP); to inspect the state of movable parts in the detector module (calibration devices, dynamic thermometers) as needed; and to closely inspect parts of the TPC as necessary following any seismic activity or other unanticipated occurrence. These functions are performed using a set of fixed *cold* cameras permanently mounted at fixed points in the cryostat for use during filling and commissioning, and a movable, replaceable *warm* inspection camera that can be deployed through any free instrumentation flange at any time throughout the life of the experiment. Table 7.3 summarizes the requirements for the camera system.

The following sections describe the design considerations for the cold and warm cameras and the associated lighting system. The same basic design may be used for both the single and dual phase detectors.

7.2.6.1 Cryogenic Cameras (Cold)

The fixed cameras monitor the following items during filling:

- Positions of corners of APA or CRP, cathode plane assembly (CPA) or cathode, FCs, GPs (1 mm resolution);
- Relative straightness and alignment of APA/CRP, CPA/cathode, and FC ($<\sim$ 1 mm);

Table 7.3: Camera system requirements

Requirement	Physics Requirement Driver
General	
No component may contaminate the LAr.	High LAr purity is required for TPC operation.
No component may produce bubbles in the liquid argon if the HV is on.	Bubbles increase risk of HV discharge.
No point in the camera system shall have a field greater than 15 kV/cm when the drift field is at nominal voltage.	Fields must be well below 30 kV/cm to avoid risk of HV discharge.
The camera system shall not produce measurable noise in any detector system.	Low noise is required for TPC operation.
Cameras provide the viewing functionality as agreed upon with the other subsystems for viewing, as documented in the ICDs with the individual systems.	
Cold cameras	
Minimize heat dissipation when camera not in operation.	Do not generate bubbles when HV is on.
Longevity must exceed 18 months.	Cameras must function throughout cryostat filling and detector commissioning.
Frame rate ≥ 10 /s.	Observe bubbling, waves, detritus, etc.
Inspection cameras	
Keep heat transfer to LAr low when in operation.	Do not generate bubbles, some use cases may require operation when HV is on.
Deploy without exposing LAr to air.	Keep LAr free of N ₂ and other electronegative contaminants.
Camera enclosure must be replaceable.	Replace broken camera, or upgrade, throughout life of experiment.
Light emitting system	
No emission of wavelengths shorter than 400 nm	Avoid damaging tetra-phenyl butadiene (TPB) waveshifter.
Longevity must exceed 18 months.	Lighting for fixed cameras must function throughout cryostat filling and detector commissioning.

- Relative position of profiles and endcaps (0.5 mm resolution);
- State of LAr surface: e.g., the presence of bubbling or debris.

There are published articles and unpublished presentations describing completely or partially successful operation of low-cost, off-the-shelf CMOS cameras in custom enclosures immersed in cryogenics. (e.g., EXO-100: [41]; DUNE 35 ton prototype test [44]; WA105 DP demonstrator: [40].) Generally it is reported that such cameras show poor performance and ultimately fail to function below some temperature of order 150 K to 200 K, but some report that their cameras recover fully after being stored (not operated) at temperatures as low as 77 K and then brought up to minimum operating temperature.

However, as with photon sensors, experience has also shown that it is non-trivial to ensure reliable and reproducible mechanical and electrical integrity of such cameras in the cryogenic environment (e.g., [44] and [45]). Off-the-shelf cameras and camera components are generally only specified by the vendors and original manufacturers for operation down to -40°C or -50°C . In addition, many low-cost cameras use digital interfaces not intended for long distance deployment, such as USB (2 ~ 5 m) or CSI (circuit board scale), leading to signal degradation and noise problems.

The design for the DUNE fixed cameras uses an enclosure based on the successful EXO-100 design[41], which was also used successfully in LAPD (see Figure 7.17). The enclosure is connected to a stainless steel gas line to allow it to be flushed with argon gas at low enough pressure to prevent liquification, using the same design as the gas line for the beam plug tested in the 35 ton prototype HV test and in ProtoDUNE. A thermocouple in the enclosure allows temperature monitoring, and a heating element provides temperature control. The camera transmits its video signal using either a composite video signal over shielded coax or Ethernet over optical fiber. Most importantly, the DUNE CISC consortium must work with vendors to design camera circuit boards that are robust and reliable in the cryogenic environment.

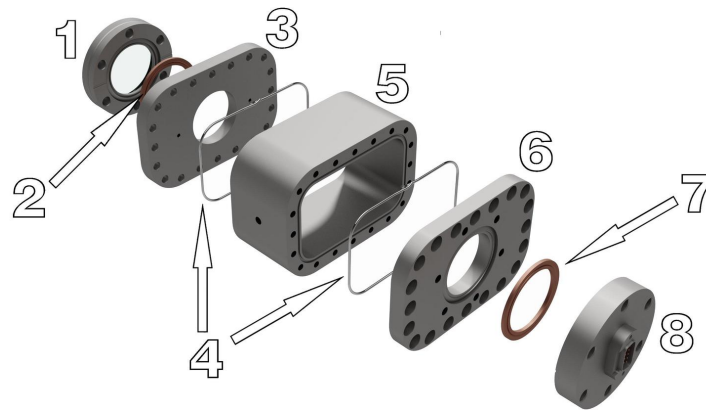


Figure 7.17: CAD exploded view of vacuum-tight camera enclosure suited for cryogenic applications from [41]. (1) quartz window, (2 and 7) copper gasket, (3 and 6) flanges, (4) indium wires, (5) body piece, (8) signal feedthrough.

7.2.6.2 Inspection Cameras (Warm)

The inspection cameras are intended to be as versatile as possible. However, the following locations have been identified as likely to be of interest:

- Status of HV feedthrough and cup;
- Status of FC profiles, endcaps (0.5 mm resolution);
- y -axis deployment of calibration sources;
- Status of thermometers, especially dynamic thermometers;
- HV discharge, corona, or streamers on HV feedthrough, cup, or FC;
- Relative straightness and alignment of APA/CRP, CPA/cathode, and FC (1 mm resolution);
- Gaps between CPA frames (1 mm resolution);
- Relative position of profiles and endcaps (0.5 mm resolution);
- Sense wires at top of outer wire planes in SP APA (0.5 mm resolution).

Unlike the fixed cameras, the inspection cameras need operate only as long as inspection lasts, as the camera can be replaced in case of failure. It is also more practical to keep the cameras continuously *warm* (above -150°C) during deployment; this offers more options for commercial cameras, e.g., the same model camera used successfully to observe discharges in LAr from 120 cm away [42].

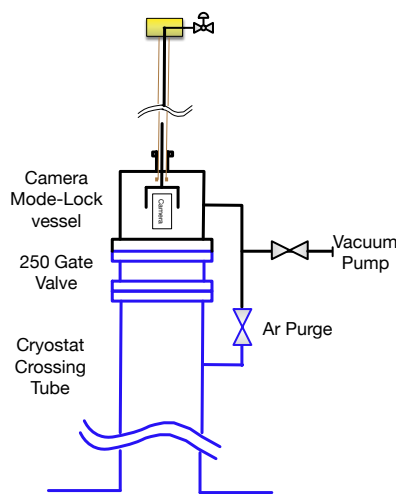


Figure 7.18: An overview of the inspection camera design.

The design for the inspection camera system employs the same basic enclosure design as for cold cameras, but mounted on an insertable fork using a design similar to the dynamic temperature

probes. See Figure 7.18 and Figure 7.12. The entire system is sealed to avoid contamination with air. In order to avoid contamination, the camera can only be deployed through a feedthrough equipped with a gate valve and a purging system, similar to that used for the vertical axis calibration system at KamLAND [43]. The entire system is purged with pure argon gas before the gate valve is opened.

Motors above the flange allow rotation and vertical movement of the fork. A chain drive system, with motor mounted on the end of the fork, allows tilting of the camera assembly, creating a point-tilt mount with vertical motion capability. Taking into account the room above the cryostat flanges and the thickness of the cryostat insulation, a vertical range of motion of 1 m inside the cryostat is achievable. The motors for rotation and vertical motion are located outside the sealed volume, coupled mechanically using ferrofluidic seals, thus reducing contamination risks and allowing for manual rotation of the vertical drive in the event of a motor failure. A significant prototyping and testing effort is needed to finalize and validate this design.

7.2.6.3 Light-emitting system

The light-emitting system is based on LEDs with the capability of illuminating the interior with selected wavelengths (IR and visible) that are suitable for detection by the cameras. Performance criteria for the light-emission system are based on the efficiency of detection with the cameras, in conjunction with adding minimal heat to the cryostat. The use of very high-efficiency LEDs helps reduce heat generation; as an example, one 750 nm LED has a specification of 32 % conversion of electrical input power to light.

While data on the performance of LEDs at cryogenic temperatures is sparse, some studies related to NASA projects [46] indicate that LED efficiency increases with reduced temperature, and that the emitted wavelengths may change, particularly for blue LEDs. The wavelength changes cited would have no impact on illumination, however, since in order to avoid degradation of wavelength-shifting materials in the PDS, such short wavelength LEDs would not be used.

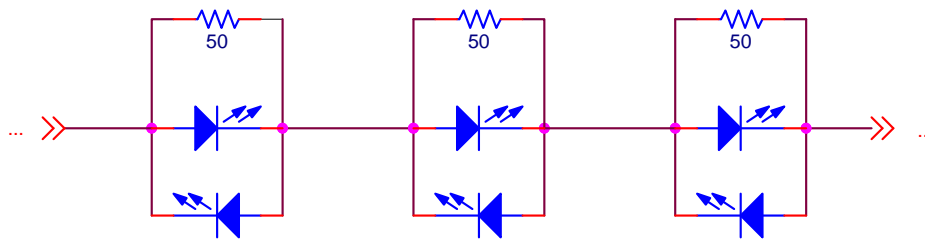


Figure 7.19: Suggested LED chain for lighting inside the cryostat, with dual-wavelength and failure-tolerant operation.

A *chain* of LEDs should be connected in series and driven with a constant-current circuit. It would be advantageous to pair each LED in parallel with an opposite polarity LED and a resistor (see Figure 7.19). This allows two different wavelengths of illumination with a single installed chain (by changing the direction of the drive current) and continued use of an LED chain even if individual LEDs fail.

The LEDs should be placed as a *ring light* around the outside of each camera lens, pointing in the same direction as the lens, to illuminate the part of the detector module within the field of view of the camera. Commercially available LEDs can be obtained with a range of angular spreads, and can be matched to the needs of the cameras without additional optics.

7.2.7 Cryogenics Test Facility

The cryogenics test facility is intended to provide the access to a small (< 1 ton) to intermediate (~ 4 tons) volumes of purified TPC-grade LAr. Hardware that needs liquid of purity this high include any device intending to drift electrons for millisecond time periods. Not all devices require purity this high, but some may need a relatively large volume to provide the needed prototyping environment. Of importance is a relatively fast turn-around time of approximately a week for short prototyping runs.

Figure 7.20 shows the Blanche test stand cryostat at Fermilab.



Figure 7.20: Blanche Cryostat at Fermilab. This cryostat holds ~ 0.75 tons of LAr.

7.2.8 Cryogenic Internal Piping

The cryogenic internal piping comprises several manifolds to distribute the liquid and gaseous argon inside the cryostat during all phases (e.g., gaseous purge, liquid distribution, cool down)

and various pipe stands to return argon to the outside (e.g., boil-off gaseous argon). Vacuum-insulated pipe stands are needed to transition from inside to outside in a way that does not affect the purity and does not introduce a significant heat load.

LBNF has the expertise for engineering design and installation of the detector internal piping, while the CISC consortium has the expertise on the physics requirements, the relevant risk registries, and the interfaces with other detector systems. Ultimate responsibility for costing the internal cryogenic piping system also lies with the CISC consortium. It is important for these two groups to interact closely to ensure that the system enables achievement of the physics, avoids interference with other detector systems, and mitigates risks.

DUNE has formed a cryogenics systems working group with conveners from both the CISC consortium and LBNF. This group has both LBNF and CISC members and provides an official forum where we interface and establish the final design.

The initial design for the cryogenic internal piping calls for some 750 m of pipe per cryostat for purging and filling, laid out as shown in Figure 7.21-Left, and 20 flange-pipes assemblies, as the one shown on the right panel of Figure 7.21, with a CF DN250 flange penetrated by two ~ 2.2 m long pipes.

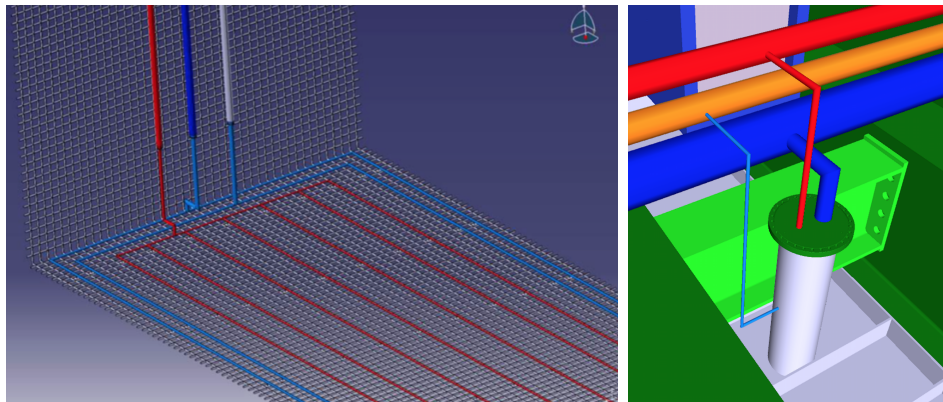


Figure 7.21: Left: Cryogenic internal piping for purging (red) and filling (blue). Right: Cool-down pipes, LAr in blue (vacuum jacketed) and gaseous argon in red.

7.3 Slow Controls

The slow controls system collects, archives, and displays data from a broad variety of sources, and provides real time alarms and warnings for detector operators. Data is acquired via network interfaces. Figure 7.22 shows the connections between major parts of the slow controls system and other systems.

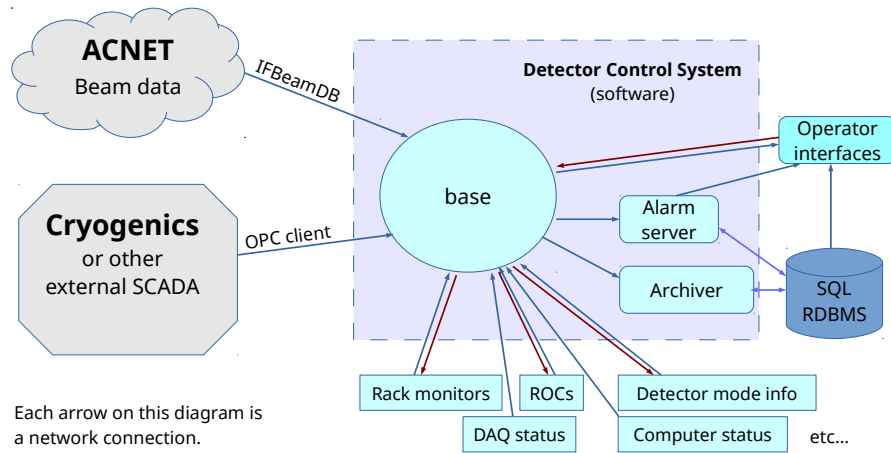


Figure 7.22: Typical Slow Controls system connections and data flow

7.3.1 Slow Controls Hardware

The slow controls will always require a small amount of dedicated network and computing hardware as described below. It also relies on common infrastructure, as described in Section 7.3.2.

7.3.1.1 Slow Controls Network Hardware

The slow controls data originates from the cryogenic instrumentation discussed in Section 7.2 and from other systems, and is collected by software running on servers (Section 7.3.1.2) housed in the underground data room in the central utility cavern, where data is archived in a central CISC database. The instrumentation data is transported over conventional network hardware from any sensors located in the cryogenic plant. However, the readouts that are located in the racks on top the cryostats must take care with grounding and noise. Therefore, each rack on the cryostat has a small network switch that sends any network traffic from that rack to the CUC via a fiber transponder. This is the only network hardware specific to slow controls; network infrastructure requirements are described in Section 7.3.2.

7.3.1.2 Slow Controls Computing Hardware

Two servers (a primary server and a replicated backup) suitable for the needed relational database discussed in Section 7.3.3 are located in the CUC data room, with an additional two servers to perform FE monitoring interface services: for example, assembling dynamic CISC monitoring web pages from the adjacent databases. Any special purpose software, such as iFix or EPICS, would also run here. It is expected that one or two more servers will accommodate these programs. Replicating this setup on a per-module basis would allow for easier commissioning and independent operation, accommodate different module design (and the resulting differences in database tables),

and ensure sufficient capacity. Including four sets of networking hardware, this would fit tightly into one rack or very comfortably into two.

7.3.2 Slow Controls Infrastructure

The total number of slow controls quantities and the update rate are low enough that the data rate will be in the tens of kilobytes per second range (Section 7.3.4), placing minimal requirements on the local network infrastructure. Network traffic out of SURF to Fermilab will be primarily database calls to the central CISC database: either from monitoring applications, or from database replication to the offline version of the CISC database. This traffic is of a low enough bandwidth that the proposed general purpose links both out of the mine and back to Fermilab can accommodate it.

Up to two racks of space and appropriate power and cooling are available in the CUC's DAQ server room for CISC usage. Somewhat less space than that is currently envisioned, as described in 7.3.1.2.

7.3.3 Slow Controls Software

The slow controls software includes the following components in order to provide complete monitoring and control of detector subsystems:

- Control systems base that performs input and output operations and defines processing logic, scan conditions, alarm conditions, archiving rate, etc.;
- Alarm server that monitors all channels and sends alarm messages to operators;
- Data archiver that performs automatic sampling and storage of values for history tracking;
- Integrated operator interface that provides display panels for controls and monitoring.

An additional requirement for the software is the ability to indirectly interface with external systems (e.g., cryogenics control system) and databases (e.g., beam database) to export data into slow controls process variables (or channels) for archiving and status displays. This allows integrating displays and warnings into one system for the experiment operators, and provides integrated archiving for sampled data in the archived database. In this case, one can imagine an input output controller (IOC) running on a central DAQ server provides soft channels for these data. Figure 7.22 shows a typical workflow of a slow controls system.

In terms of key features of the software, a highly evolved software is needed that is designed for managing real-time data exchange, scalable to large number of channels and high bandwidth if needed. The software should be well documented, supported, and known to be reliable. The base software should also allow easy access of any channel by name. The archiver software should allow

data storage in an SQL database with adjustable rates and thresholds such that one can easily retrieve data for any channel by using channel name and time range. Among the key features, the alarm server software should remember state, support arbitrary number of clients, and provide logic for delayed alarms and acknowledging alarms. As part of the software, a standard naming convention for channels is followed to aid dealing with large number of channels and subsystems.

7.3.4 Slow Controls Quantities

The final set of quantities to monitor will ultimately be determined by the needs of the subsystems being monitored, as documented in appropriate interface control documents (ICDs), and continually revised based on operational experience. The total number of quantities to monitor has been very roughly estimated by taking the total number of quantities monitored in MicroBooNE and scaling by the detector length and the number of planes, giving a number in the range of 50 to 100 thousand. Quantities are expected to update on average no faster than once per minute. The subsystems to be monitored include the cryogenic instrumentation described in this chapter, the other detector systems, and relevant infrastructure and external devices. Table 7.4 lists the kind of quantities expected from each system.

7.3.5 Local Integration

The local integration for the slow controls consists entirely of software and network interfaces with systems outside of the scope of the detector module. This includes the following:

- readings from the LBNF-managed external cryogenics systems, for status of pumps, flow rates, inlet and return temperature and pressure, which are implemented via OPC or a similar SCADA interfaces;
- beam status, such as protons on target, rate, target steering, beam pulse timing, which are retrieved via IFBeamDB;
- near detector status, which can be retrieved from a common slow controls database.

This integration occurs after both the slow controls and non-detector systems are in place. The LBNF-CISC interface is managed by the cryogenics systems working group described in Section 7.2.8. IFBeamDB is already well established. An internal near-detector–FD working group may be established to coordinate detector status exchange between near and far sites interfacing.

Table 7.4: Slow controls quantities

System	Quantities
Detector Cryogenic Instrumentation	
Purity monitors	Anode and cathode charge, bias voltage and current, flash lamp status, calculated electron lifetime
Thermometers	Temperature, position of dynamic thermometers
Liquid level	Liquid level
Gas analyzers	Purity level readings
Cameras	Camera voltage and current draw, temperature, heater current and voltage, lighting current and voltage
Cryogenic internal piping	feedthrough gas purge flow and temperature
Other Detector Systems	
HV systems	Drift HV voltage, current; end-of-field cage current, bias; ground plane currents
TPC electronics	Voltage and current to electronics
photon detector (PD)	Bias, current, electronics
DAQ	Warm electronics currents and voltages; run status; DAQ buffer sizes, trigger rates, data rates, GPS status, etc.; computer and disk health status; other health metrics as defined by DAQ group
CRP / APA	Bias voltages and currents
Infrastructure and external systems	
Cryogenics (external)	Status of pumps, flow rates, inlet and return temperature and pressure (via OPC or similar SCADA interface)
Beam status	Protons on target, rate, target steering, beam pulse timing (via IFBeamDB)
Near detector	Near detector run status (through common slow controls database)
Racks power and status	PDU current and voltage, air temperature, fan status if applicable, interlock status (fire, moisture, etc.)

7.4 Interfaces

The CISC consortium interfaces with all other consortia, task forces (calibration), working groups (physics, software/computing) and technical coordination. This section provides a brief summary; further details can be found in references [47]-[48].

There are obvious interfaces with detector consortia since CISC provides full rack monitoring (rack fans, thermometers and rack protection system), interlock status bit monitoring (not the actual interlock mechanism) and monitoring and control for all power supplies. The CISC consortium must maintain close contacts with all other consortia to ensure that specific hardware choices have acceptable slow controls (SC) solutions. Also, installation of instrumentation devices interferes with other devices and must be coordinated with the respective consortia. On the software side CISC must define, in coordination with other consortia, the quantities to be monitored and controlled by slow controls and the corresponding alarms, archiving and GUIs.

A major interface is the one with the cryogenics system. As mentioned in Section 7.2.2 purity monitors and gas analyzers are essential to mitigate the liquid argon contamination risk. The appropriate interlock mechanism to prevent the cryogenics system from irreversible contamination must be designed and implemented.

Another important interface is the one with the HV system [49] since several aspects related with safety must be taken into account. For all instrumentation devices inside the cryostat, electric field simulations are needed to guaranty proper shielding is in place. Although this is a CISC responsibility, input from HV is crucial. During the deployment of inspection cameras, generation of bubbles must be avoided when HV is on, as it can lead to discharges.

There are also interfaces with the PDS [50]. Purity monitors and the light-emitting system for cameras both emit light that might damage PDs. Although this should be understood and quantified, CISC and the SP PDS may have to define the necessary hardware interlocks that avoid turning on any other light source accidentally when PDs are on.

The DAQ-CISC interface [51] is described in Section 6.3.4. CISC data is stored both locally (in CISC database servers in the central utility cavern (CUC)) and offline (the databases are replicated back to Fermilab) in a relational database indexed by timestamp. This allows bidirectional communications between DAQ and CISC by reading or inserting data into the database as needed for non-time-critical information.

CISC also interfaces with the beam and cryogenics group since at least the status of these systems must be monitored.

Assuming that the scope of software & computing SWC group includes scientific computing support to project activities, there are substantial interfaces with that group [52]. The hardware interfaces responsibility of the SWC include networking installation and maintenance, maintenance of SC servers and any additional computing hardware needed by instrumentation devices. CISC provides the needed monitoring for power distribution units (PDUs). Regarding software interfaces the

SWC group provides: (1) SC database maintenance, (2) API for accessing the SC database offline, (3) UPS packages, local installation and maintenance of software needed by CISC, and (4) SWC creating and maintaining computer accounts on production clusters. Additionally CISC provides the required monitoring and control of SWC quantities including alarms, archiving, and GUIs, where applicable.

The CISC consortium may have additional hardware interfaces with the not-as-yet formed calibration consortium [53]. Indeed, since the shared ports are multi-purpose to enable deploying various devices, both CISC and calibration must interact in terms of flange design and sharing space around the ports. Also, CISC might use calibration ports to extract cables from CISC devices. At the software level, CISC is responsible for calibration device monitoring (and control to the extent needed) and monitors the interlock bit status for laser and radioactive sources.

CISC indirectly interfaces to physics through the shared devices. One specific need for physics is to extract instrumentation or slow controls data to correlate high-level quantities to low-level or calibration data. This requires tools to extract data from the slow controls database (see CISC-SWC interface document [52]). A brief list of what CISC data is needed by physics is given in the CISC-Physics interface document [54].

Interfaces between CISC and technical coordination are detailed in the corresponding interface documents for the facility [55], installation [48] and integration facility [56].

7.5 Installation, Integration and Commissioning

7.5.1 Cryogenics Internal Piping

The installation of internal cryogenic pipes occurs soon after the cryostat is completed or towards the end of the cryostat completion, depending on how the cryostat work proceeds. A concrete installation plan will be developed by the company designing the internal cryogenics. It depends on how they address the thermal contraction of the long horizontal and vertical runs. We are investigating several options, which each have different installation sequences. All involve delivery and welding together of prefabricated spool pieces inside the cryostat, and vacuum insulation of the vertical lines. The horizontal lines are bare pipes.

The cool-down assemblies are installed in dedicated cool-down feedthroughs at the top, arranged in two rows of ten each in the long direction of the cryostat. Each one features a LAr line connected to a gaseous argon line via a mixing nozzle and a gaseous argon line with spraying nozzles. The mixing nozzles generate droplets of liquid that are circulated uniformly inside the cryostat by the spraying nozzles. They are prefabricated at the vendor's site and delivered as full pieces, then mounted over the feedthroughs.

The current 3D model of the internal cryogenics is developed and archived at CERN as part of the full cryostat model. CERN is currently responsible for the integration of the detector cavern:

cryostat, detector, and proximity cryogenics in the detector cavern, including cryogenics on the mezzanine and main LAr circulation pumps.

The prefabricated spool pieces and the cool down nozzles undergo testing at the vendor before delivery. The installed pieces are helium leak-checked before commissioning, but no other integrated testing or commissioning is possible after the installation, because the pipes are open to the cryostat volume. The internal cryogenics are commissioned once the cryostat is closed.

7.5.2 Purity Monitors

The purity monitor system is built in a modular way, such that it can be assembled outside of detector module cryostat. The assembly of the purity monitors themselves occurs outside of the cryostat and includes everything described in the previous section. The installation of the purity monitor system can then be carried out with the least number of steps inside the cryostat. The assembly itself is transported into the cryostat with the three individual purity monitors mounted to the support tubes but before installation of HV cables and optical fibers. The support tube at the top and bottom of the assembly is then mounted to the brackets inside the cryostat that could be attached to the cables trays or the detector support structure. In parallel to this work, the FE electronics and light source can be installed on the top of the cryostat, along with the installation of the electronics and power supplies into the electronics rack.

Integration begins by running the HV cables and optical fibers to the purity monitors, coming from the top of the cryostat. The HV cables are attached to the HV feedthroughs with enough length to reach each of the respective purity monitors. The cables are run through the port reserved for the purity monitor system, along cable trays inside the cryostat until they reach the purity monitor system, and are terminated through the support tube down to each of the purity monitors. Each purity monitor has three HV cables that connect it to the feedthrough, and then along to the FE electronics. The optical fibers are run through the special optical fiber feedthrough, into the cryostat, and guided to the purity monitor system either using the cables trays or guide tubes. Whichever solution is adopted for running the optical fibers from the feedthrough to the purity monitor system, it must protect the fibers from accidental breakage during the remainder of the detector and instrumentation installation process. The optical fibers are then run inside of the purity monitor support tube and to the respective purity monitors, terminating at the photocathode of each.

Integration continues with the connection of the HV cables between the feedthrough and the system FE electronics, and then the optical fibers to the light source. The cables connecting the FE electronics and the light source to the electronics rack are also run and connected at this point. This allows for the system to turn on and the software to begin testing the various components and connections. Once it is confirmed that all connections are successfully made, the integration to the slow controls system is made, first by establishing communications between the two systems and then transferring data between them to ensure successful exchange of important system parameters and measurements.

The purity monitor system is formally commissioned once the cryostat is purged and a gaseous

argon atmosphere is present. At this point the HV for the purity monitors is ramped up without the risk of discharge through the air, and the light source is turned on. Although the drift electron lifetime in the gaseous argon is very large and therefore not measurable with the purity monitors themselves, comparing the signal strength at the cathode and anode gives a good indication of how well the light source is generating drift electrons from the photocathode and whether they drift successfully to the anode.

7.5.3 Thermometers

Individual temperature sensors on pipes and cryostat membrane are installed prior to any detector component, right after the installation of the pipes. First, all cable supports are anchored to pipes. Then each cable is routed individually starting from the sensor end (with IDC-4 female connector but no sensor) towards the corresponding cryostat port. Once a port's cables are routed, they are cut to the same length such that they can be properly soldered to the pins of the SUBD-25 connectors on the flange. To avoid damage, the sensors are installed at a later stage, just before unfolding the bottom GPs.

Static T-gradient monitors are installed before the outer anode plane assemblies, after the installation of the pipes and before the installation of individual sensors. This proceeds in several steps: (1) installation of the two stainless steel strings to the bottom and top corners of the cryostat, (2) tension and verticality checks, (3) installation of cable supports in one of the strings, (4) installation of sensor supports in the other string, (5) cable routing starting from the sensor end towards the corresponding cryostat port, (6) cutting all cables at the same point in that port, and (7) soldering cable wires to the pins of the SUBD-25 connectors on the flange. Then, at a later stage, just before moving corresponding APA into its final position, (8) the sensors are plugged into IDC-4 connectors.

For the SP, individual sensors on the top GP must be integrated with the GPs. For each CPA (with its corresponding four GP modules) going inside the cryostat, cable and sensor supports are anchored to the GP threaded rods as soon as possible. Once the CPA is moved into its final position and its top FC is ready to be unfolded, sensors on those GPs are installed. Once unfolded, cables exceeding the GP limits can be routed to the corresponding cryostat port either using neighboring GPs or DSS I-beams.

Dynamic T-gradient monitors are installed after the completion of the detector. The monitor comes in several segments with sensors and cabling already in place. Additional slack is provided at segment joints to ease the installation process. Segments are fed into the flange one at a time. The segments being fed into the detector module are held at the top with a pin that prevents the segment from sliding in all the way. Then the next segment is connected. The pin is removed, and the segment is pushed down until the next segment top is held with the pin at the flange. Then this next segment is installed. The process continues until the entire monitor is in its place inside the cryostat. Use of a crane is foreseen to facilitate the process. Extra cable slack at the top is provided again in order to ease the connection to the D-Sub standard connector flange and to allow vertical movement of the entire system. Then, a four-way cross flange with electric feedthroughs on one side and a window on the other side. The wires are connected to the D-sub connector

on the electric flange feedthrough on the side. On the top of the cross, a moving mechanism is then installed with a crane. The pinion is connected to the top segment. The moving mechanism will come reassembled with motor on the side in place and pinion and gear motion mechanism in place as well. The moving mechanism enclosure is then connected to top part of the cross and this completes the installation process of the dynamic T-gradient monitor.

Commissioning of all thermometers proceeds in several steps. Since in the first stage only cables are installed, the readout performance and the noise level inside the cryostat are tested with precision resistors. Once sensors are installed the entire chain is checked again at room temperature. The final commissioning phase occurs during and after cryostat filling.

7.5.4 Gas Analyzers

Prior to the piston purge and gas recirculation phases of the cryostat commissioning, the gas analyzers are installed near the tubing switchyard. This minimizes tubing runs and is convenient for switching the sampling points and gas analyzers. Since each is a standalone module, a single rack with shelves, should be adequate to house the modules.

Concerning the integration, the gas analyzers typically have an analog output (4 to 20 mA or 0 to 10V) that maps to the input range of the analyzers. They also usually have a number of relays that indicate the scale they are currently running. These outputs can be connected to the slow controls for readout. However, using a digital readout is preferred since this directly gives the analyzer reading at any scale. Currently there are a number of digital output connections, ranging from RS-232, RS-485, USB, and Ethernet. At the time of purchase, one can choose the preferred option, since the protocol is likely to evolve. The readout usually responds to a simple set of text commands. Due to the natural time scales of the gas analyzers, and lags in the gas delivery times (depending on the length of the tubing runs), sampling on timescales of a minute most likely is adequate.

Before the beginning of the gas phase of the cryostat commissioning, the analyzers must be brought online and calibrated. Calibration varies for the different modules, but often requires using argon gas with both zero contaminants (usually removed with a local inline filter) for the zero of the analyzer, and argon with a known level of the contaminant to check the scale. Since the start of the gas phase begins with normal air, the more sensitive analyzers are valved off at the switchyard to prevent overloading their inputs and potentially saturating their detectors. As the argon purge and gas recirculation progress, the various analyzers are valved back in when the contaminant levels reach the upper limits of the analyzer ranges.

7.5.5 Liquid Level Monitoring

Multiple differential pressure level monitors are installed in the cryostat, connected both to the side penetration of the cryostat at the bottom and to dedicated instrumentation ports at the top.

The capacitance level sensors are installed at the top of the cryostat in coordination with the TPC installation. Their placement relative to the upper ground plane (single phase) or CRP (dual phase) is important as these sensors will be used for a hardware interlock on the HV, and, in the case of the DP module, to measure the LAr level at the millimeter level as required for DP operation. Post installation in situ testing of the capacitive level sensors can be accomplished with a small dewar of liquid.

7.5.6 Cameras and Light-Emitting System

Fixed camera installation is in principle simple, but involves a considerable number of interfaces. Each camera enclosure has threaded holes to allow bolting it to a bracket. A mechanical interface is required with the cryostat wall, cryogenic internal piping, or DSS. Each enclosure is attached to a gas line for maintaining appropriate underpressure in the fill gas; this is an interface with cryogenic internal piping. Each camera has a cable for the video signal (coax or optical), and a multiconductor cable for power and control, to be run through cable trays to flanges on assigned instrumentation feedthroughs.

The inspection camera is designed to be inserted and removed on any instrumentation feedthrough equipped with a gate valve at any time during operation. Installation of the gate valves and purge system for instrumentation feedthroughs falls under cryogenic internal piping.

Installation of fixed lighting sources separate from the cameras would require similar interfaces as fixed cameras. However, the current design has lights integrated with the cameras, which do not require separate installation.

7.5.7 Slow Controls Hardware

Slow controls hardware installation includes multiple servers, network cables, any specialized cables needed for device communication, and possibly some custom-built rack monitoring hardware. The installation sequence is interfaced and planned with the facilities group and other consortia. The network cables and rack monitoring hardware are common across many racks and are installed first as part of the basic rack installation, led by the facilities group. The installation of specialized cables needed for slow controls and servers is done after the common rack hardware is installed, and will be coordinated with other consortia and the DAQ group respectively.

7.5.8 Transport, Handling and Storage

Most instrumentation devices are shipped to SURF in pieces and mounted in situ. Instrumentation devices are in general small except the support structures for purity monitors and T-gradient monitors, which will cover the entire height of the cryostat. Since the load on those structures is relatively small (< 100 kg) they can be fabricated in parts of less than 3 m, which can be

easily transported to SURF. These parts are also easy to transport down the shaft and through the tunnels. All instrumentation devices except the dynamic T-gradient monitors, which are introduced into the cryostat through a dedicated cryostat port, can be moved into the cryostat without the crane.

Cryogenic internal piping needs special treatment given the number of pipes and their lengths. Purging and filling pipes will be most likely pre-assembled by the manufacturer as much as possible, using the largest size that can be shipped and transported down the shaft. Assuming 6 m long sections, pipes could be grouped in bunches of 10 to 15 pipes and stored in five pallets or boxes of about 6.2 m \times 0.8 m \times 0.5 m. These would be delivered to the site, stored, transported down to the detector cavern, and stored again before they are used. Depending on when they are installed, they could be stored inside the cryostat itself or in one of the drifts. Cool-down pipes are easier to handle. They could be transported in 20 boxes of 2.2 m \times 0.6 m \times 0.6 m, although there is room for saving some space using a different packaging scheme. Once in the cavern they could be stored on top of the cryostat.

7.6 Quality Control

A series of tests should be done by the manufacturer and the institute in charge of the device assembly. The purpose of quality control (QC) is to ensure that the equipment is capable of performing its intended function. The QC includes post-fabrication tests and also tests to run after shipping and installation. In case of a complex system, the whole system performance will be tested before shipping. Additional QC procedures can be performed at the integration and test facility (ITF) and underground after installation if possible. The planned tests for each subsystem are described below.

7.6.1 Purity Monitors

The purity monitor system undergoes a series of tests to ensure the performance of the system. This starts with testing the individual purity monitors in vacuum after each one is fabricated and assembled. This test looks at the amplitude of the signal generated by the drift electrons at the cathode and the anode. This ensures that the photocathode is able to provide a sufficient number of photoelectrons for the measurement with the required precision, and that the field gradient resistors are all working properly to maintain the drift field and hence transport the drift electrons to the anode. A follow-up test in LAr is then performed for each individual purity monitor, ensuring that the performance expected in LAr is met.

The next step is to assemble the entire system and make checks of the connections along the way. Ensuring that the connections are all proper during this time reduces the risk of having issues once the system is finally assembled and ready for the final test. The assembled system is placed into the shipping tube, which serves as a vacuum chamber, and tested. If an adequately sized LAr test facility is available, a full system test can be performed at LAr temperature prior to installation.

7.6.2 Thermometers

7.6.2.1 Static T-Gradient Thermometers

Three type of tests are carried out at the production site prior to installation. First, the mechanical rigidity of the system is tested such that swinging is minimized (< 5 cm) to reduce the risk of touching the anode plane assemblies. This is done with a 15 m stainless steel string, strung horizontal anchored to two points; its tension is controlled and measured. Second, all sensors are calibrated in the lab, as explained in Section 7.2.3. The main concern is the reproducibility of the results since sensors could potentially change their resistance (and hence their temperature scale) when undergoing successive immersions in LAr. In this case the QC is given by the calibration procedure itself since five independent measurements are planned for each set of sensors. Sensors with reproducibility (based on the RMS of those five measurements) beyond the requirements (2 mK for ProtoDUNE-SP) are discarded. The calibration serves as QC for the readout system (similar to the final one) and of the PCB-sensor-connector assembly. Finally, the cable-connector assemblies are tested: sensors must measure the expected values with no additional noise introduced by the cable or connector.

If the available LAr test facility has sufficient height or length to test a good portion of the system, an integrated system test is conducted there ensuring that the system operates in LAr and achieves the required performance. Ideally, the laboratory sensor calibration will be compared with the in situ calibration of the dynamic T-gradient monitors by operating both dynamic and static T-gradient monitors simultaneously.

The last phase of QC takes place after installation. The verticality of each array is checked and the tensions in the horizontal strings are adjusted as necessary. Before soldering the wires to the flange, the entire readout chain is tested with temporary SUBD-25 connectors. This allows testing the sensor-connector assembly, the cable-connector assembly and the noise level inside the cryostat. If any of the sensors gives a problem, it is replaced. If the problem persists, the cable is checked and replaced if needed.

7.6.2.2 Dynamic T-Gradient Thermometers

The dynamic T-gradient monitor consists of an array of high-precision temperature sensors mounted on a vertical rod. The rod can move vertically in order to perform cross-calibration of the temperature sensors in situ. Several tests are foreseen to ensure that the dynamic T-gradient monitor delivers vertical temperature gradient measurements with precision at the level of a few mK.

- Before installation, temperature sensors are tested in LN to verify correct operation and to set the baseline calibration for each sensor with respect to the absolutely calibrated reference sensor.
- Warm and cold temperature readings are taken with each sensor after mounting on the PCB board and soldering the readout cables.

- The sensor readout is taken for all sensors after the cold cables are connected to electric feedthroughs on the flange and the warm cables outside of the cryostat are connected to the temperature readout system.
- The stepper motor is tested before and after connecting to the gear and pinion system.
- The fully assembled rod is connected to the pinion and gear, and moved with the stepper motor on a high platform many times to verify repeatability, possible offsets and uncertainty in the positioning. Finally, by repeating the test a large number of times, the sturdiness of the system will be verified.
- The full system is tested after installation in the cryostat: both motion and sensor operation are tested by checking sensor readout and vertical motion of the system.

7.6.2.3 Individual Sensors

The method to address the quality of individual precision sensors is the same as for the static T-gradient monitors. The QC of the sensors is part of the laboratory calibration. After mounting six sensors with their corresponding cables, a temporary SUBD-25 connector will be added and the six sensors tested at room temperature. All sensors should work and give values within specifications. If any of the sensors gives problems, it is replaced. If the problem persists the cable is checked and replaced if needed.

7.6.3 Gas Analyzers

The gas analyzers will be guaranteed by the manufacturer. However, once received, the gas analyzer modules are checked for both *zero* and the *span* values using a gas-mixing instrument. This is done using two gas cylinders with both a zero level of the gas analyzer contaminant species and a cylinder with a known percentage of the contaminant gas. This should verify the proper operation of the gas analyzers. When eventually installed at SURF, this process is repeated before the commissioning of the cryostat. It is also important to repeat the calibrations at the manufacturer-recommended periods over the gas analyzer lifetime.

7.6.4 Liquid Level Monitoring

The differential pressure level meters will require QC by the manufacturer. While the capacitive sensors can be tested with a modest sample of LAr in the lab, the differential pressure level meters require testing over a greater range. While they do not require testing over the whole range, lab tests in LAr done over a meter or two can ensure operation at cryogenic temperatures. Depth tests can be accomplished using a pressurization chamber with water.

7.6.5 Cameras

Before transport to SURF, each cryogenic camera unit (comprising the enclosure, camera, and internal thermal control and monitoring) is checked for correct operation of all operating features, for recovery from 87 K non-operating mode, for no leakage, and for physical defects. Lighting systems are similarly checked for operation. Operations tests will include verification of correct current draw, image quality, and temperature readback and control. The movable inspection camera apparatus is inspected for physical defects, and checked for proper mechanical operation before shipping. A checklist is completed for each unit, filed electronically in the DUNE logbook, and a hard copy sent with each unit.

Before installation, each fixed cryogenic camera unit is inspected for physical damage or defects and checked in the cryogenics test facility for correct operation of all operating features, for recovery from 87 K non-operating mode, and for no contamination of the LAr. Lighting systems are similarly checked for operation. Operations tests include correct current draw, image quality, and temperature readback and control. After installation and connection of wiring, fixed cameras and lighting are again checked for operation. The movable inspection camera apparatus is inspected for physical defects and, after integration with a camera unit, tested in facility for proper mechanical and electronic operation and cleanliness, before installation or storage. A checklist is completed for each QC check and filed electronically in the DUNE logbook.

7.6.6 Light-emitting System

The complete system is checked before installation to ensure the functionality of the light emission. Initial testing of the light-emitting system (see Figure 7.19) is done by first measuring the current when a low voltage (1 V) is applied, to check that the resistive LED failover path is correct. Next, measurement of the forward voltage is done with the nominal forward current applied, to check that it is within 10 % of the nominal forward voltage drop of the LEDs, that all of the LEDs are illuminated, and that each of the LEDs is visible over the nominal angular range. If the LEDs are infrared, a video camera with IR filter removed is used for the visual check. This procedure is then duplicated with the current reversed for the LEDs oriented in the opposite direction.

These tests are duplicated during installation to make sure that the system has not been damaged in transportation or installation. However, once the LEDs are in the cryostat a visual check could be difficult or impossible.

7.6.7 Slow Controls Hardware

Networking and computing systems will be purchased commercially, requiring quality assurance (QA). However, the new servers are tested after delivery to confirm no damage during shipping. The new system is allowed to *burn in* overnight or for a few days, running a diagnostics suite on a loop. This should turn up anything that escaped the manufacturer's QA process.

The system can be shipped directly to the underground, where an on-site expert performs the initial booting of systems and basic configuration. Then the specific configuration information is pulled over the network, after which others may log in remotely to do the final setup, minimizing the number of people underground.

7.7 Safety

Several aspects related to safety must be taken into account for the different phases of the CISC project, including R&D, laboratory calibration and testing, mounting tests and installation. The initial safety planning for all phases is reviewed and approved by safety experts as part of the initial design review, and always prior to implementation. All component cleaning, assembly, testing and installation procedure documentation includes a section on safety concerns relevant to that procedure, and is reviewed during the appropriate pre-production reviews.

Areas of particular importance to CISC include:

- Hazardous chemicals (e.g., epoxy compounds used to attach sensors to cryostat inner membrane) and cleaning compounds: All chemicals used are documented at the consortium management level, with an MSDS (Material safety data sheet) and approved handling and disposal plans in place.
- Liquid and gaseous cryogenics used in calibration and testing: LN and LAr are used for calibration and testing of most of the instrumentation devices. Full hazard analysis plans will be in place at the consortium management level for all module or module component testing involving cryogenic hazards, and these safety plans will be reviewed in the appropriate pre-production and production reviews
- HV safety: Purity monitors operate at ~ 2000 V. Fabrication and testing plans will demonstrate compliance with local HV safety requirements at the particular institution or lab where the testing or operation is performed, and this compliance will be reviewed as part of the standard review process.
- Working at heights: Some aspects of the fabrication, testing and installation of CISC devices require working at heights. This is the case of T-gradient monitors and purity monitors, which are quite long. Temperature sensors installed near the top cryostat membrane and cable routing for all instrumentation devices require working at heights as well. The appropriate safety procedures including lift and harness training will be designed and reviewed.
- Falling objects: all work at height comes with associated risks of falling objects. The corresponding safety procedures, including the proper helmet usage and the observation of well delimited safety areas, will be included in the safety plan.

7.8 Organization and Management

7.8.1 Slow Controls and Cryogenics Instrumentation Consortium Organization

The organization of the CISC consortium is shown in Figure 7.23. The CISC consortium board is currently formed from institutional representatives from 17 institutes. The consortium leader acts as the spokesperson for the consortium and is responsible for the overall scientific program and management of the group. The technical leader of the consortium is responsible for the project management for the group. Currently five working groups are envisioned in the consortium (leaders to be appointed):

Cryogenics Systems gas analyzers, liquid level monitors and cryogenic internal piping; CFD simulations.

LAr Instrumentation purity monitors, thermometers, cameras and lightemitting system, and instrumentation test facility; feedthroughs; E field simulations; instrumentation precision studies; ProtoDUNE data analysis coordination efforts.

Slow Controls Base Software and Databases Base software, alarms and archiving databases, and monitoring tools; variable naming convention and slow controls quantities.

Slow Controls Detector System Interfaces Signal processing software and hardware interfaces (e.g., power supplies); firmware; rack hardware and infrastructure.

Slow Controls External Interfaces Interfaces with external detector systems (e.g., cryogenics system, beam, facilities, DAQ).

Additionally, since the CISC consortium broadly interfaces with other groups, liaisons have been identified for various roles as listed in Figure 7.23. A short-term focus group was recently formed to understand the needs for cryogenics modeling for the consortium. Currently members from new institutes are added to the consortium based on consensus from the consortium board members.

7.8.2 Planning Assumptions

The slow controls and cryogenic instrumentation is a joint effort for SP and DP. A single slow controls system will be implemented to serve both SP and DP.

Design and installation of cryogenics systems (gas analyzers, liquid level monitoring, internal piping) is coordinated with LBNF, with the consortium providing resources, and effort and expertise provided by LBNF. ProtoDUNE designs for LAr instrumentation (purity monitors, thermometers, cameras, test facility) provide the basis for DUNE designs. Design validation, testing, calibration, and performance will be evaluated through ProtoDUNE data.

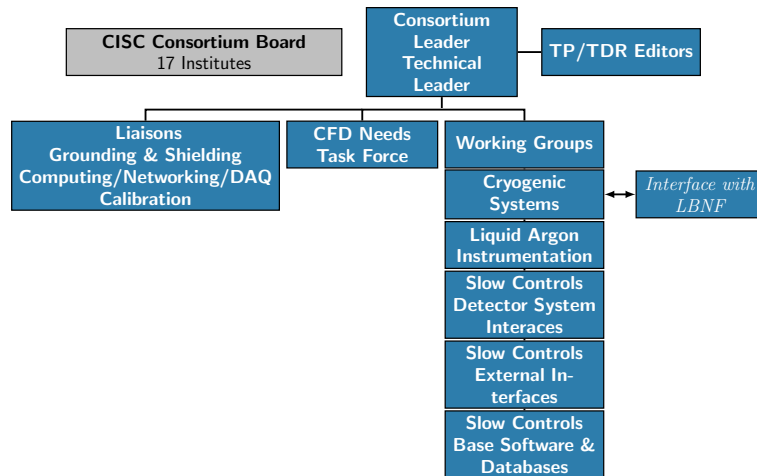


Figure 7.23: CISC consortium organizational chart

7.8.3 High-level Schedule

Table 7.5 shows key milestones on the path to commissioning of the first two DUNE detector modules.

Table 7.5: Key CISC milestones leading towards commissioning of the first two DUNE detector modules.

Date	Milestone
Aug. 2018	Validate instrumentation designs using data from ProtoDUNE
Jan. 2019	Complete architectural design for slow controls ready
Feb. 2019	Full final designs of all cryogenic instrumentation devices ready
Feb. 2023	Installation of Cryogenic Internal Piping for Cryostat 1
Apr. 2023	Installation of support structure for all instrumentation devices for Cryostat 1
Oct. 2023	All Instrumentation devices installed in Cryostat 1
Feb. 2024	All Slow Controls hardware and infrastructure installed for Cryostat 1
May 2024	Installation of Cryogenic Internal Piping for Cryostat 2
July 2024	Installation of support structure for all instrumentation devices for Cryostat 2
Jan. 2025	All Instrumentation devices installed in Cryostat 2
Apr. 2025	All Slow Controls hardware and infrastructure installed for Cryostat 2
July 2025	Full Slow controls systems commissioned and integrated into remote operations

Chapter 8

Technical Coordination

The technical coordination (TC) team is responsible for detector integration and installation support. The DUNE collaboration consists of a large number of institutions distributed throughout the world. They are supported by a large number of funding sources and collaborate with a large number of commercial partners. Groups of institutes within DUNE form consortia that take complete responsibility for construction of their system. DUNE has empowered several consortia (currently nine) with the responsibility to secure funding and design, fabricate, assemble, install, commission and operate their components of the DUNE far detector (FD). There are three consortia focusing exclusively on the SP module: anode plane assembly (APA), SP cold electronics (CE) and SP photon detection system (PDS). There are three focusing exclusively on the DP module: charge-readout plane (CRP), DP CE and DP PDS. There are three joint consortia: high voltage (HV), data acquisition (DAQ) and cryogenic instrumentation and slow controls (CISC). Other consortia may be formed over time as concepts more fully emerge, such as a FD calibration system and various aspects of the near detector (ND). DUNE TC, under the direction of the Technical Coordinator, has responsibility to monitor the technical aspects of the detector construction, to integrate and install the detector modules and to deliver the common projects. The DUNE TC organization is shown in Figure 8.1.

The TC organization staffing will grow over time as the project advances. TC will provide staffing for teams underground at SURF, at integration facilities, and at the near site at Fermilab, in addition to the core team distributed among collaborating institutions.

The DUNE Project consists of a FD and a ND. The ND is at a pre-conceptual state; as the conceptual design and organization emerges, it will become part of the DUNE Project. Currently the DUNE Project consists of the DUNE FD consortia and TC. The DUNE Project is moving towards a technical design report (TDR) for the FD, both SP and DP options, in 2019. It is expected that a Conceptual Design Report for the ND will be prepared at the same time.

The FD components will be shipped from the consortia construction sites to the integration and test facility (ITF). TC will evaluate and accept consortia components either at integration facilities or the installation site and oversee the integration of components as appropriate. The scope of the FD integration and installation effort is shown graphically in Figure 8.2.

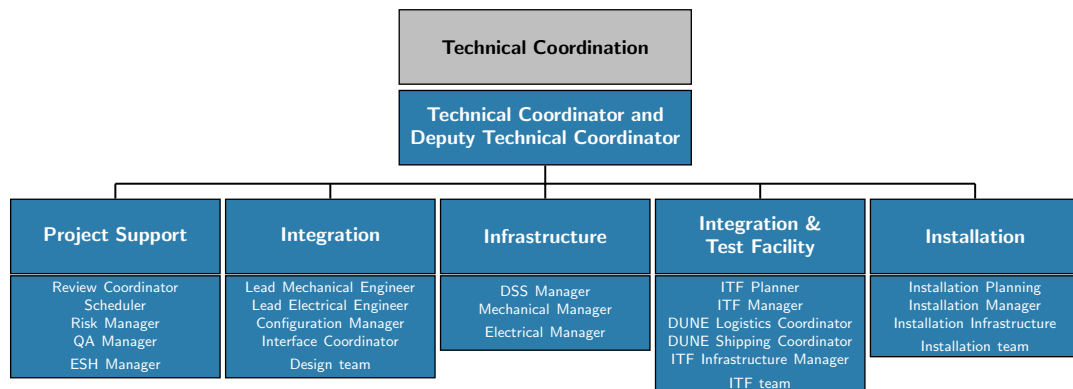


Figure 8.1: Organization of TC. This organization oversees the construction of the FD, both SP and DP, and the ND.

TC interacts with the consortia via three main areas: project coordination, integration, and installation. Construction of the DUNE FD requires careful technical coordination due to its complexity. Given the horizontal nature of the consortia structure and the extensive interdependencies between the systems, a significant engineering organization is required to deliver DUNE on schedule and within specifications and funding constraints.

The responsibilities of TC include:

- management and delivery of all common projects;
- development and monitoring of the consortia interfaces;
- configuration control of all interface documents, drawings and envelopes;
- installation of detectors at the near and far sites;
- logistics for detector integration and installation at the near and far sites;
- survey of the detector;
- primary interface to Long-Baseline Neutrino Facility (LBNF) for conventional facilities, cryostat and cryogenics;
- primary interface to the host laboratory for infrastructure and operations support;

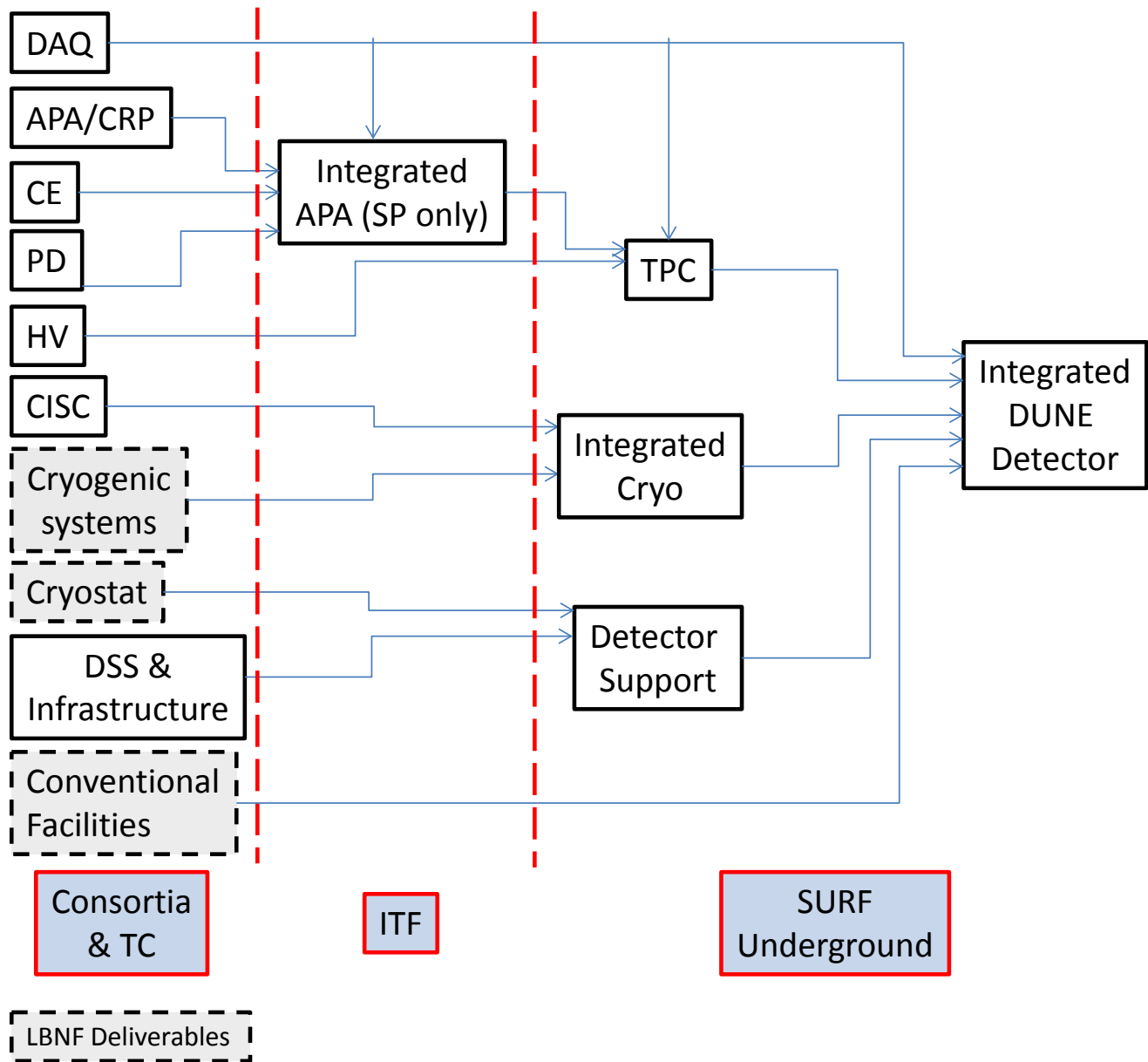


Figure 8.2: Flow of components from the consortia to the FD.

- development and tracking of project schedule and milestones;
- review of all aspects of the project;
- recording and approving all project engineering information, including: documents, drawings and models;
- project work breakdown schedules;
- project risk register;
- DUNE engineering and safety standards, including grounding and shielding;
- monitoring of all consortia design and construction progress;
- quality assurance (QA) and all QA related studies and documents;
- ES&H organization and all safety related studies and documents.

DUNE TC interacts with LBNF primarily through the LBNF/DUNE systems engineering organization. TC provides the points of contact between the consortia and LBNF. TC will work with the LBNF/DUNE Systems Engineer to implement the LBNF/DUNE Configuration Management Plan to assure that all aspects of the overall LBNF/DUNE project are well integrated. TC will work with LBNF and the host laboratory to ensure that adequate infrastructure and operations support are provided during construction, integration, installation, commissioning and operation of the detectors. The LBNF/DUNE systems engineering organization is shown in Figure 8.3.

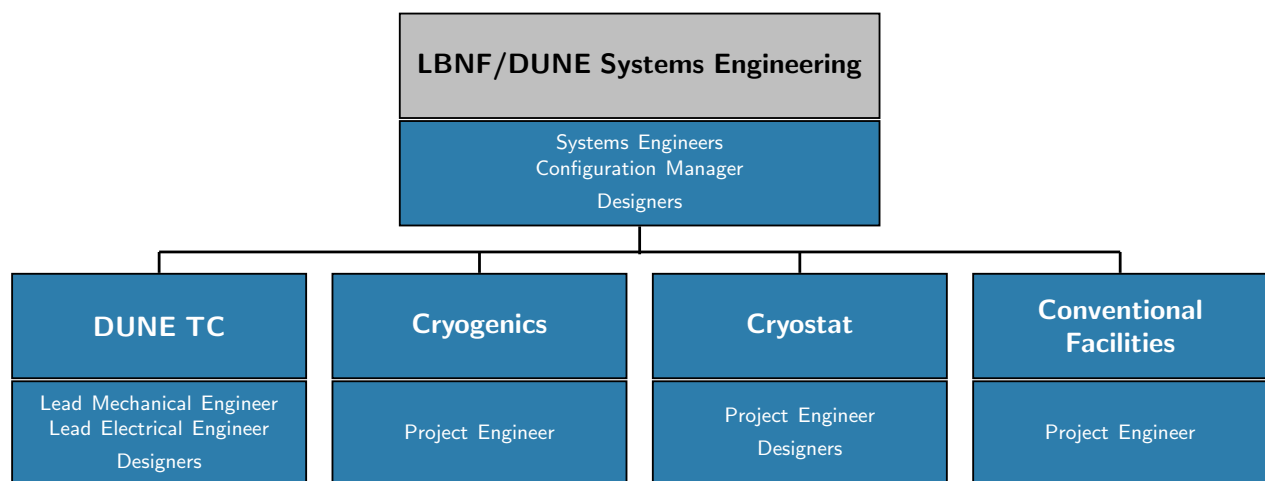


Figure 8.3: LBNF/DUNE systems engineering organizational structure.

Proper integration of the FDs within the supporting facilities and infrastructure at SURF is a major engineering task. The LBNF/DUNE Systems Engineer is responsible for the interfaces between the major LBNF and DUNE systems (conventional facilities, cryostats, cryogenics systems and

detector modules). The LBNF/DUNE systems engineering team includes several engineers and designers with responsibility for maintaining computer aided design (CAD) models. DUNE TC supports an engineering team that works directly with the LBNF/DUNE systems engineering team to ensure that the detector is properly integrated into the overall system.

TC has been working with the LBNF/DUNE systems engineering team to define requirements from DUNE for the conventional facilities final design for the detector chambers, central utility cavern (CUC), drifts and utilities. TC is representing the interests of the DUNE detector in the conventional facilities (CF) design. This includes refining the detector installation plan to understand how much space is needed in front of the temporary construction openings (TCOs) of the cryostats and therefore of the size of the chambers. TC continues to refine the detector needs for utilities in the detector caverns and the CUC where the DAQ will be housed.

Physics requirements on TC include cleanliness in the cryostats, survey and alignment tolerances, and grounding and shielding requirements. The cleanliness requirement is for ISO 8 (class 100,000), which will keep rates from dust radioactivity below those of the inherent ^{39}Ar background. The alignment tolerances are driven by physics requirements on reconstructing tracks. Grounding and shielding are critical to enable this very sensitive, low-noise detector to achieve the required S/N. The physics requirements for LBNF and DUNE are maintained in DocDB-112.

8.1 Project Support

As defined in the DUNE Management Plan (DMP), the DUNE Technical Board (TB) generates and recommends technical decisions to the collaboration executive board (EB) (see Figure 8.4).

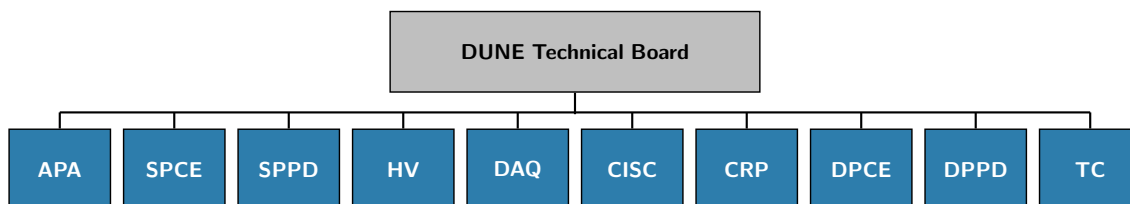


Figure 8.4: DUNE Technical Board.

It consists of all consortia scientific and technical leads. It meets on a regular basis (approximately monthly) to review and resolve any technical issues associated with the detector construction. It reports through the EB to collaboration management. The DUNE TB is chaired by the technical coordinator. DUNE collaboration management, including the EB, is shown in Figure 8.5. The TC engineering team also meets on a regular basis (approximately monthly) to discuss more detailed

technical issues. TC does not have responsibility for financial issues; that will instead be referred to the EB and Resource Coordinator (RC).

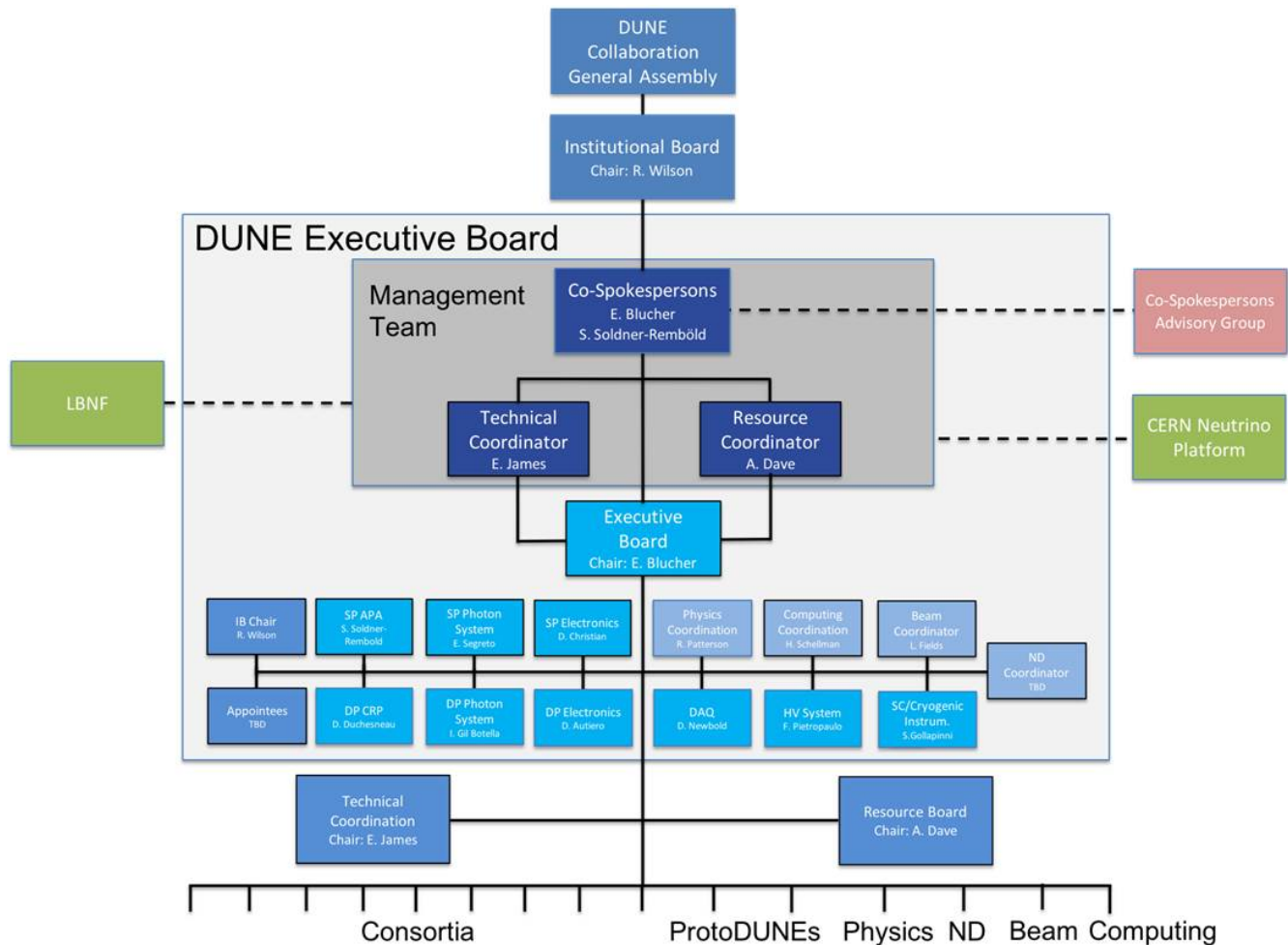


Figure 8.5: DUNE management organizational structure.

TC has several major project support tasks that need to be accomplished:

- Assure that each consortium has a well defined and complete scope, that the interfaces between the consortia are sufficiently well defined and that any remaining scope can be covered by TC through common fund or flagged as missing scope to the EB and RC. In other words, assure that the full detector scope is identified. Monitor the interfaces and consortia progress in delivering their scope.
- Develop an overall project integrated master schedule that includes reasonable production schedules, testing plans and a well developed installation schedule from each consortium. Monitor the integrated master schedule (IMS) as well as the individual consortium schedules.
- Ensure that appropriate engineering and safety standards are developed and agreed to by all key stakeholders and that these standards are conveyed to and understood by each consortium. Monitor the design and engineering work.

- Ensure that all DUNE requirements on LBNF for conventional facilities, cryostat and cryogenics have been clearly defined and understood by each consortium. Negotiate scope boundaries with LBNF. Monitor LBNF progress on final conventional facility design, cryostat design and cryogenics design.
- Ensure that all technical issues associated with scaling from ProtoDUNE have sufficient resources to converge on decisions that enable the detector to be fully integrated and installed.
- Ensure that the integration and quality control (QC) processes for each consortium are fully developed and reviewed and that the requirements on an ITF are well defined.

TC is responsible for technical quality and schedule and is not responsible for consortia funding or budgets. TC will try to help resolve any issue that it can, but will likely have to push all financial issues to the TB, EB and RC for resolution.

TC maintains a web page¹ with links to project documents. TC maintains repositories of project documents and drawings. These include the work breakdown structure (WBS), schedule, risk register, requirements, milestones, strategy, detector models and drawings that define the DUNE detector.

8.1.1 Schedule

A series of tiered milestones are being developed for the DUNE project. The Tier-0 milestones are held by the spokespersons and host laboratory director. Three have been defined and the current milestones and target dates are:

- | | |
|--|------|
| 1. Start main cavern excavation | 2019 |
| 2. Start detector module 1 installation | 2022 |
| 3. Start operations of detector module 1–2 with beam | 2026 |

These dates will be revisited at the time of the TDR review. Tier-1 milestones will be held by the technical coordinator and LBNF Project Manager and will be defined in advance of the TDR review. Tier-2 milestones will be held by the consortia.

A high level version of the DUNE milestones from the IMS can be seen in Table 8.1.

TC will maintain the IMS that links all consortium schedules and contains appropriate milestones to monitor progress. The IMS is envisioned to be maintained in MS-Project² as it is expected that many consortia will use this tool. It is currently envisioned as three levels of control and notification milestones in addition to the detailed consortium schedules. The highest level contains external milestones, with the second level containing the key milestones for TC to monitor deliverables and

¹https://web.fnal.gov/collaboration/DUNE/DUNE%20Project/_layouts/15/start.aspx#/.

²Microsoft™ Project.

Table 8.1: Overall DUNE Project Tier-1 milestones.

Milestone	Date
RRB Approval of Technical Design Review	09/02/2019
Beneficial Occupancy of Integration Test Facility	09/01/2021
Construction of steel frame for Cryostat #1 complete	12/17/2021
Construction of Mezzanine for Cryostat #1 complete	01/17/2022
Begin integration/testing of Detector #1 components at ITF	02/01/2022
Beneficial Occupancy of Central Utility Cavern Counting room	04/16/2022
Construction of steel frame for Cryostat #2 complete	07/01/2022
Construction of Mezzanine for Cryostat #2 complete	08/01/2022
Beneficial occupancy of Cryostat #1	12/23/2022
Cryostat #1 ready for TPC installation	05/01/2023
Begin integration/testing of Detector #2 components at ITF	11/01/2023
Beneficial occupancy of Cryostat #2	03/01/2024
Begin closing Temporary Construction Opening for Cryostat #1	05/01/2024
Cryostat #2 ready for TPC installation	08/01/2024
Cryostat #1 ready for filling	10/01/2024
Begin closing Temporary Construction Opening for Cryostat #2	07/18/2025
Detector #1 ready for operations	10/01/2025
Cryostat #2 ready for filling	12/05/2025
Detector #2 ready for operations	12/18/2026

installation progress, and the third level containing the inter-consortium links. The schedules will go under change control after agreement with each consortium on the notification milestone dates and the TDR is approved.

In addition to the overall IMS for construction and installation, a schedule of key consortia activity in the period 2018–19 leading up to the TDR has been developed.

To ensure that the DUNE detector remains on schedule, TC will monitor schedule status from each consortium, will organize reviews of schedules and risks as appropriate. As schedule problems arise TC will work with the affected consortium to resolve the problems. If problems cannot be solved, TC will take the issue to the TB and EB.

A monthly report with input from all consortia will be published by TC. This will include updates on consortium technical progress and updates from TC itself.

8.1.2 Risk

The successful operation of ProtoDUNE will retire a great many potential risks to DUNE. This includes most risks associated with the technical design, production processes, QA, integration and installation. Residual risks remain relating to design and production modifications associated with scaling to DUNE, mitigations to known installation and performance issues in ProtoDUNE, underground installation at SURF and organizational growth.

The highest technical risks include: development of a system to deliver 600 kV to the DP cathode; general delivery of the required HV; cathode and field cage (FC) discharge to the cryostat membrane; noise levels, particularly for the CE; number of dead channels; lifetime of components surpassing 20 year; QC of all components; verification of improved large electron multiplier (LEM) performance; verification of new cold analog-to-digital converter (ADC) and COLDATA performance; argon purity; electron drift lifetime; photoelectron light yield; incomplete calibration plan; and incomplete connection of design to physics. Other major risks include insufficient funding, optimistic production schedules, incomplete integration, testing and installation plans.

Key risks for TC to manage include the following:

1. Too much scope is unaccounted for by the consortia and falls to TC and common fund.
2. Insufficient organizational systems are put into place to ensure that this complex international mega-science project, including TC, Fermilab as host laboratory, SURF, DOE and all international partners continue to successfully work together to ensure appropriate rules and services are provided to enable success of the project.
3. Inability of TC to obtain sufficient personnel resources so as to ensure that TC can oversee and coordinate all of its project tasks. While the USA has a special responsibility towards TC as host country, it is expected that personnel resources will be directed to TC from each collaborating country. Related to this risk is the fact that consortium deliverables are not

really stand-alone subsystems; they are all parts of a single detector module. This elevates the requirements on coordination between consortia.

The consortia have provided preliminary versions of risk analyses that have been collected on the TC webpage. These are being developed into an overall risk register that will be monitored and maintained by TC in coordination with the consortia.

8.1.3 Reviews

TC is responsible for reviewing all stages of detector development and works with each consortium to arrange reviews of the design (preliminary design review (PDR) and final design review (FDR)), production (production readiness review (PRR) and production progress review (PPR)) and operational readiness review (ORR) of their system. These reviews provide input for the TB to evaluate technical decisions. Review reports are tracked by TC and provide guidance as to key issues that will require engineering oversight by the TC engineering team. TC will maintain a calendar of DUNE reviews.

TC works with consortia leaders to review all detector designs, with an expectation for a PDR, followed by a FDR. All major technology decisions will be reviewed prior to down-select. TC may form task forces as necessary for specific issues that need more in-depth review.

Start of production of detector elements can commence only after successful PRRs. Regular production progress reviews will be held once production has commenced. The PRRs will typically include review of the production of *Module 0*, the first such module produced at the facility. TC will work with consortium leaders for all production reviews.

TC is responsible to coordinate technical documents for the LBNC Technical Design Review.

8.1.4 Quality Assurance

The LBNF/DUNE QAP outlines the QA requirements for all DUNE consortia and describes how the requirements shall be met. The consortia will be responsible for implementing a quality plan that meet the requirements of the LBNF/DUNE QAP. The consortia implement the plan through the development of individual quality plans, procedures, guides, QC inspection and test requirements and travelers³ and test reports. In lieu of a consortium-specific quality plan, the consortia may work under the LBNF/DUNE QAP and develop manufacturing and QC plans, procedures and documentation specific to their work scope. The technical coordinator and consortia leaders are responsible for providing the resources needed to conduct the Project successfully, including those required to manage, perform and verify work that affects quality. The DUNE consortia leaders are responsible for identifying adequate resources to complete the work scope and to ensure that their team members are adequately trained and qualified to perform their assigned work.

³The traveler is a document that details the fabrication and inspection steps and ensures that all steps have been satisfactorily completed.

The consortia work will be documented on travelers and applicable test or inspection reports. Records of the fabrication, inspection and testing will be maintained. When a component has been identified as being in noncompliance to the design, the nonconforming condition shall be documented, evaluated and dispositioned as one of the following: use-as-is (does not meet design but can meet functionality as is), rework (bring into compliance with design), repair (will be brought into meeting functionality but will not meet design) or scrap. For nonconforming equipment or material that is dispositioned as use-as-is or repair, a technical justification shall be provided allowing for the use of the material or equipment and approved by the design authority.

The LBNF/DUNE QAM reports to the LBNF Project Manager and DUNE Technical Coordinator and provides oversight and support to the consortium leaders to ensure a consistent quality program.

1. The QAM will plan reviews as independent assessments to assist the technical coordinator in identifying opportunities for quality and performance-based improvement and to ensure compliance with specified requirements.
2. The QAM is responsible to work with the consortia in developing their QA and QC Plans.
3. The QAM will review consortia QA and QC activity, including production site visits.
4. The QAM will participate in consortia design reviews, conduct PRRs prior to the start of production, conduct PRRs on a regular basis (as described in Section 8.1.3), and perform follow-up visits to consortium facilities prior to shipment of components to ensure all components and documentation are satisfactory.
5. The QAM is responsible for performing assessments at the ITF, the Far Site and the Near Site to ensure the activities performed at these locations are in accordance with the LBNF/DUNE QA Program and applicable procedures, specifications and drawings.

8.1.4.1 Document Control

TC maintains repositories of project documents and drawings in two document management systems. DUNE Project documents will be stored in the DUNE DocDB ⁴. DUNE drawings will be stored in electronic document management system (EDMS) ⁵. TC will maintain approved versions of QA, QC and testing plans, installation plans, engineering and safety standards in the DUNE DocDB.

Consortia have developed initial interface, risk, schedule and WBS documents that will be put under change control and managed by the TC engineering team along with the consortia involved. These are currently in DocDB and will likely go under change control later in 2018, although they will continue to be developed through the TDR.

⁴<https://docs.dunescience.org>

⁵<https://edms.cern.ch/ui/#!master/navigator/project?P:1637280201:1637280201:subDocs>.

Thresholds for change control are described in the LBNF/DUNE CMP. The control process is further described in Section 8.2.1.

8.1.5 ESH

The DUNE ES&H program is described in the LBNF/DUNE IESHP. This plan is maintained by the LBNF/DUNE ES&H Manager, who reports to the LBNF Project Manager and the technical coordinator. The ES&H manager is responsible to work with the consortia in reviewing their hazards and their ES&H plans. The ES&H Manager is responsible to review ES&H at production sites, integration sites and at SURF. It is expected that the ES&H reviews will be conducted as part of the PRR and PPR process described in Section 8.1.3.

A strong ES&H program is essential to successful completion of the LBNF/DUNE Project at Fermilab, collaborating laboratories and universities, the ITF, and SURF. DUNE is committed to ensuring a safe work environment for collaborators at all institutions and to protecting the public from hazards associated with construction and operation of LBNF/DUNE. In addition, all work will be performed in a manner that preserves the quality of the environment and prevents property damage. Accidents and injuries are preventable and it is important that we work together to establish an injury-free workplace.

To achieve the culture and safety performance required for this project, it is essential that DUNE ensure that procedures are established to support the following ES&H policy statements:

- Line managers are responsible for environmental stewardship and personal safety at the DUNE work sites.
- Line managers, supported by the LBNF/DUNE, Fermilab, other collaborating laboratories, and SURF ES&H organizations, will provide consistent guidance and enforcement of the ES&H program that governs the activities of workers at each site where work is being performed.
- Incidents, whether they involve personal injuries or other losses, can be prevented through proper planning. All LBNF/DUNE work is planned.
- Workers are involved in the work planning process and continuous improvement, including the identification of hazards and controls.
- Working safely and in compliance with requirements is vital to a safe work environment. Line managers will enforce disciplinary policies for violations of safety rules.
- Each of us is responsible for our own safety and for that of our co-workers. Together we create a safe work environment.
- A strong program of independent audits, self-assessments and surveillance will be employed to periodically evaluate the effectiveness of the ES&H program.

- Any incidents that result or could have resulted in personal injury or illness, significant damage to buildings or equipment, or impact of the environment, will be investigated to determine corrective actions and lessons that can be applied to prevent recurrence. LBNF/DUNE encourages open reporting of errors and events.

To achieve the culture and safety performance required for this project, it is essential that ES&H be fully integrated into the project and be managed as tightly as quality, cost, and schedule.

8.2 Integration Engineering

The major aspects of detector integration focus on the mechanical and electrical connections between each of the detector systems. This includes verification that subassemblies and their interfaces are correct (e.g., APA and SP PDS). A second major area is in the support of the detector modules and their interfaces to the cryostat and cryogenics. A third major area is in assuring that the detector modules can be installed — that the integrated components can be moved into their final configuration. A fourth major area is in the integration of the detector modules with the necessary services provided by the conventional facilities.

8.2.1 Configuration Management

The TC engineering team will maintain configuration data in the appropriate format for the management of the detector configuration. The consortia are responsible for providing engineering data for their subsystems to TC. The TC engineering team will work with the LBNF project team to integrate the full detector data into the global LBNF configuration files. Appropriate thresholds for tracking and for change control will be established.

For mechanical design aspects, the TC engineering team will maintain full 3D CAD models of the detector modules. Appropriate level of detail will be specified for each type of model. Each consortium will be responsible for providing CAD models of their detector components to be integrated into overall models. The TC engineering team will work with the LBNF project team to integrate the full detector module models into a global LBNF CAD model which will include cryostats, cryogenics systems, and the conventional facilities. These will include models using varying software packages. The TC engineering team will work directly with the consortium technical leads and their supporting engineering teams to resolve any detector component interference or interface issues with other detector systems, detector infrastructure, and facility infrastructure.

For electrical design aspects, the TC engineering team will maintain high-level interface documents that describe all aspects of required electrical infrastructure and electrical connections. All consortia must document power requirements and rack space requirements. Consortia are responsible for defining any cabling that bridges the design efforts of two or more consortia. This agreed-upon and signed-off interface documentation shall include cable specification, connector specification, connector pinout and any data format, signal levels and timing. All cables, connectors, printed

circuit board components, physical layout and construction will be subject to project review. This is especially true of elements which will be inaccessible during the project lifetime. Consortia shall provide details on LAr temperature acceptance testing and lifetime of components, boards, cables and connectors.

At the time of the release of the TDR, the TC engineering team will work with the consortia to produce formal engineering drawings for all detector components. These drawings are expected to be signed by the consortia technical leads, project engineers, and Technical Coordinator. Starting from that point, the detector modules models and drawings will sit under formal change control as discussed in Section 8.1.4. It is anticipated that designs will undergo further revisions prior to the start of detector construction, but any changes made after the release of the TDR will need to be agreed to by all of the drawing signers and an updated, signed drawing produced. The major areas of configuration management include:

1. 3D model,
2. Interface definitions,
3. Envelope drawings for installation,
4. Drawing management.

TC will put into place processes for configuration management. Configuration management will provide TC and engineering staff the ability to define and control the actual build of the detector at any point in time and to track any changes which may occur over duration of the build as well as the lifetime of the project as described in Section 8.1.4.

For detector elements within a cryostat, configuration management will be frozen once the elements are permanently sealed within the cryostat. However, during the integration and installation process of building the detector modules within the cryostat, changes may need to occur. For detector elements outside the cryostat and accessible, all repairs, replacements, hardware upgrades, system grounding changes, firmware and software changes must be tracked.

Any change will require revision control, configuration identification, change management and release management.

Revision Control

Consortia will be responsible for providing accurate and well documented revision control. Revision control will provide a method of tracking and maintaining the history of changes to a detector element. Each detector element must be clearly identified with a document which includes a revision number and revision history. For mechanical elements, this will be reflected by a drawing number with revision information. For electrical elements, schematics will be used to track revisions. Consortia will be responsible for identifying the revision status of each installed detector element. Revisions are further controlled through maintenance of the documents in DocDB and EDMS.

Configuration Identification

Consortia are responsible for providing unique identifiers or part numbers for each detector element. Plans will be developed on how inventories will be maintained and tracked during the build. Plans will clearly identify any dynamic configuration modes which may be unique to a specific detector element. For example, a printed circuit board may have firmware that affects its performance.

Change Management

TC will provide guidelines for formal change management. During the beginning phase of the project, drawings and interface documents are expected to be signed by the consortium technical leads, project engineers, and technical coordinator. Once this initial design phase is complete, the detector models, drawings, schematics and interface documents will be under formal change control. It is anticipated that designs will undergo further revisions prior to the start of detector construction, but any changes made after the release of the TDR will need to be agreed to by all drawing signers and an updated signed drawing produced.

Release Management

Release management focuses on the delivery of the more dynamic aspects of the project such as firmware and software. Consortia with deliverables that have the potential to affect performance of the detector by changing firmware or software must provide plans on how these revisions will be tracked, tested and released. The modification of any software or firmware after the initial release, must be formally controlled, agreed upon and tracked.

8.2.2 Engineering Process and Support

The TC organization will work with the consortia through its TC engineering team to ensure the proper integration of all detector components. The TC engineering team will document requirements on engineering standards and documentation that the consortia will need to adhere to in the design process for the detector components under their responsibility. Similarly, the project QA and ES&H managers will document QC and safety criteria that the consortia will be required to follow during the construction, installation, and commissioning of their detector components, as discussed in sections 8.1.4 and 8.1.5.

Consortia interfaces with the conventional facilities, cryostats, and cryogenics are managed through the TC organization. The TC engineering team will work with the consortia to understand their interfaces to the facilities and then communicate these globally to the LBNF Project team. For conventional facilities the types of interfaces to be considered are requirements for bringing needed detector components down the shaft and through the underground tunnels to the appropriate detector cavern, overall requirements for power and cooling in the detector caverns, and the requirements on cable connections from the underground area to the surface. Interfaces to the cryostat include the number and sizes of the penetrations on top of the cryostat, required mechanical structures attaching to the cryostat walls for supporting cables and instrumentation, and requirements on the global positioning of the detector modules within the cryostat. Cryogenics system interfaces include requirements on the location of inlet and output ports, requirements on the monitoring of the LAr both inside and outside the cryostat, and grounding and shielding requirements on piping attached to the cryostat.

LBNF will be responsible for the design and construction of the cryostats used to house the detector modules. The consortia are required to provide input on the location and sizes of the needed penetrations at the top of the cryostats. The consortia also need to specify any mechanical structures to be attached to the cryostat walls for supporting cables or instrumentation. The TC engineering team will work with the LBNF cryostat engineering team to understand what attached fixturing is possible and iterate with the consortia as necessary. The consortia will also work with the TC engineering team through the development of the 3D CAD model to understand the overall position of the detector modules within the cryostat and any issues associated with the resulting locations of their detector components.

LBNF will be responsible for the cryogenics systems used to purge, cool, and fill the cryostats. It will also be responsible for the system that continually re-circulates LAr through filtering systems to remove impurities. Any detector requirements on the flow of liquid within the cryostat will be developed by the consortia and transmitted to LBNF through the TC engineering team. Similarly, any requirements on the rate of cool-down or maximum temperature differential across the cryostat during the cool-down process will be specified by the consortia and transmitted to the LBNF team.

The engineering design process is defined by a set of steps taken to fulfill the requirements of the design. By the time of the TDR, all design requirements must be fully defined and proposed designs must be shown to meet these requirements. Based on prior work, some detector elements may be quite advanced in the engineering process, while others may be in earlier stages. Each design process shall closely follow the engineering steps described below.

Development of specifications

Each consortium is responsible for the technical review and approval of the engineering specifications. The documented specifications for all major design elements will include the scope of work, project milestones, relevant codes and standards to be followed, acceptance criteria and specify appropriate internal or external design reviews. Specifications shall be treated as controlled documents and cannot be altered without approval of the TC team. The TC engineering team will participate in and help facilitate all major reviews as described in Section 8.1.3. Special TB reviews will be scheduled for major detector elements.

Engineering Risk Analysis

Each consortium is responsible for identifying and defining the level of risk associated with their deliverables as described in Section 8.1.2. TC will work with the consortia, through its TC engineering team, to document these risks in a risk database and follow them throughout the project until they are realized or can be retired.

Specification Review

The DUNE TC organization and project engineers shall review consortium specifications for overall compliance with the project requirements. Consortia must document all internal reviews and provide that documentation to TC. Additional higher-level reviews may be scheduled by TC as described in Section 8.1.3.

System Design

The system design process includes the production of mechanical drawings, electrical schematics, calculations which verify compliance to engineering standards, firmware, printed circuit board

layout, cabling and connector specification, software plans, and any other aspects that lead to a fully documented functional design. All relevant documentation shall be recorded, with appropriate document number, into the chosen engineering data management system and be available for the review process.

Design Review

The design review process is determined by the complexity and risk associated with the design element. For a simple design element, a consortium may do an internal review. For a more complex or high risk element a formal review will be scheduled. DUNE TC will facilitate the review, bringing in outside experts as needed. In all cases, the result of any reviews must be well documented and captured in the engineering data management system. If recommendations are made, those recommendations will be tracked in a database and the consortia will be expected to provide responses. All results of these engineering reviews will be made available for the subsystem design reviews described in Section 8.1.3.

Procurement

The procurement process will include the documented technical specifications for all procured materials and parts. All procurement technical documents are reviewed for compliance to engineering standards and ES&H concerns. DUNE TC will assist the consortia in working with their procurement staff as needed.

Production and assembly

During the implementation phase of the project, the consortia shall provide the Technical Coordinator with updates on schedule. A test plan will be fully developed which will allow for verification that the initial requirements have been met. This is part of the QA plan that will be documented and followed as described in Section 8.1.4.

Testing and Validation

The testing plan documented in the above step will be followed and results will be well documented in consultation with the QAM. The Technical Coordinator and TC engineering team will be informed as to the results and whether the design meets the specifications. If not, a plan will be formulated to address any shortcomings and presented to the Technical Coordinator.

Final Documentation

Final reports will be generated that describe the as built equipment, lessons learned, safety reports, installation procedures, testing results and operations procedures.

8.3 Detector Infrastructure

TC is responsible for delivering the common infrastructure for the FD. This infrastructure is typically equipment that is used by many groups. This may include: the electronics racks on top of the cryostat with power, cooling, networking and safety systems, cable trays, cryostat crossing tubes, and flanges, detector safety systems and ground monitoring and isolation transformers.

TC is responsible for the systems to support the detectors. For the DP module this may consist of a cable winch system similar to ProtoDUNE-DP. In the case of the SP module the installation group also provides the detector support system (DSS), which supports the detector and is needed to bring equipment into the correct location in the cryostat.

8.3.1 Detector Support System

The DSS provides the structural support for the SP module inside the cryostat. It also provides the necessary infrastructure to move the detector elements into location during assembly. As the DSS is a new design and is quite different from the ProtoDUNE-SP DSS it is described in some detail in this section. The detector elements supported by the DSS include the endwall field cages (endwall FCs), the anode plane assemblies, and the cathode plane assemblies (CPAs) with top and bottom FC panels. The DSS is supported by the cryostat outer steel structure through a series of feedthroughs that cross through the cryostat insulation and are anchored with flanges on the cryostat roof. Inside the cryostat a series of stainless steel I-beams are connected to the feedthroughs and used to support the detector. The DSS defines the location of the detector inside the cryostat and it also defines how the detector elements move and contract as the detector is brought to liquid argon (LAr) temperature. The design of the DSS encompasses the overall structural design of the detector module as only after the elements are mounted to the DSS and are connected together do they make a unified mechanical structure. The requirements of the DSS are as follows:

- Support the weight of the detector.
- Accommodate cryostat roof movement during filling, testing, and operation.
- Accommodate variation in feedthrough locations and variation in the flange angles due to installation tolerances and loading on the warm structure.
- Accommodate shrinkage of the detector and DSS from ambient temperature to LAr temperature.
- Define the position of the detector components relative to each other.
- Provide electrical connection to the cryostat ground and remain electrically isolated from the detector.
- Allow for the support penetrations to be purged with gaseous argon to prevent contaminants from diffusing back into the liquid.
- Ensure that the instrumentation cabling does not interfere with the DSS.
- Consist entirely of components that can be installed through the TCO.
- Meet AISC-360 or appropriate codes required at SURF.
- Meet seismic requirements one mile underground at SURF.
- Consist entirely of materials that are compatible for operation in ultrapure LAr.
- Ensure that beams are completely submerged in LAr.
- Ensure that detector components are not less than 400 mm from the membrane flat surface.
- Ensure that the supports do not interfere with the cryostat I-beam structures.
- Ensure that the detector's lower ground plane (GP) is above the cryogenic piping and the top of the DSS beams are submerged in LAr while leaving a 4% ullage at the top of the cryostat.

- Include the infrastructure necessary to move the APA and CPA-FC assemblies from outside the cryostat through the TCO and to the correct position.

Figure 8.6 (left) shows the DSS structure; there are five rows of supports for the alternating rows of APA-CPA-APA-CPA-APA. The DSS is connected to the warm structure at a flange that is mounted on the outside of the cryostat. Figure 8.6 (right) shows the layout of these structural feedthroughs. The DSS consists of pairs of feedthroughs that support 6.4 m-long S8x18.4 stainless steel I-beam sections. The proposed design of the DSS has 10 I-beam segments per row for a total of 50 I-beam segments. Each I-beam is suspended on both ends by rods from feedthroughs that penetrate the roof. When cold, each beam shrinks, causing gaps to form between anode plane assemblies that are adjacent but supported on separate beams. Anode plane assemblies that are supported on the same beam will not have gaps develop because both the beam and anode plane assemblies are stainless steel so they shrink together. Each beam is supported by a nearly 2 m long rod that allows the beam support to move as the beam contracts.

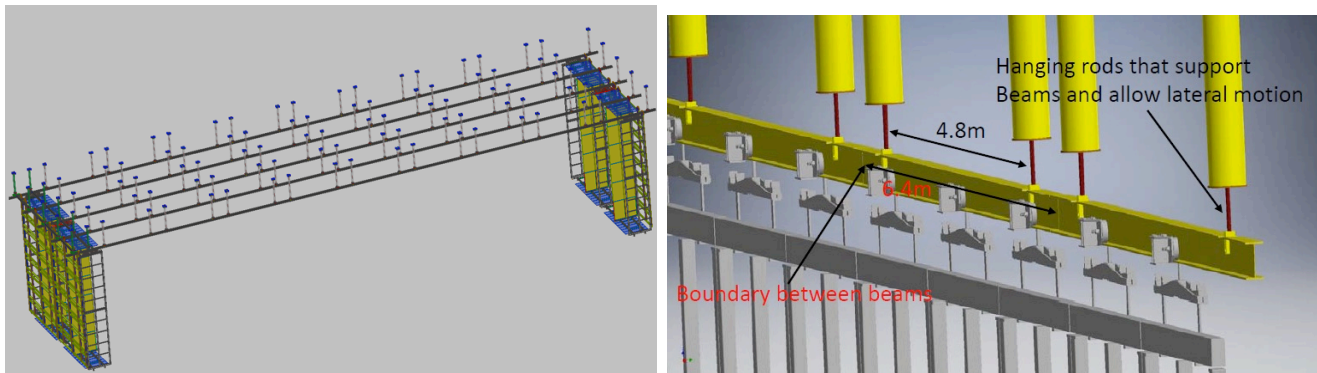


Figure 8.6: 3D model of the DSS showing the entire structure on the left along with one row of APA and CPA-FC at each end. The right panel is a zoomed image showing the connections between the vertical supports and the horizontal I-beams.

Detector components are installed using a shuttle beam system illustrated in Figure 8.7. The last two columns of feedthroughs (eastern-most) support temporary beams that run north-south, perpendicular to the main DSS beams. A shuttle beam has trolleys mounted to it and transverse north-south until aligned with the required row of DSS beam. The last APA or CPA in a row is supported by the shuttle beam which is bolted directly to the feedthroughs once it is in place. As the last CPA or APA in each row is installed, the north-south beams are removed.

A mechanical interlock system prevents trolleys from passing the end of the shuttle beam unless it is aligned with a corresponding DSS beam. The shuttle beam and each detector component are moved using a motorized trolley. A commercially available motorized trolley will be modified as needed to meet the needs of the installation.

The DSS installation begins with the placement and alignment of all the feedthroughs onto the flanges that are mounted to the warm vessel. There are 25 feedthroughs per row and five rows for a total of 125 feedthroughs. A fixture with a tooling ball is attached to the clevis of each feedthrough. The xy position in the horizontal plane and the vertical z position of this tooling ball is defined, then a survey is performed to determine the location of each tooling ball center and xy and z adjustments are made to get the tooling ball centers to within ± 3 mm. The 6.4 m

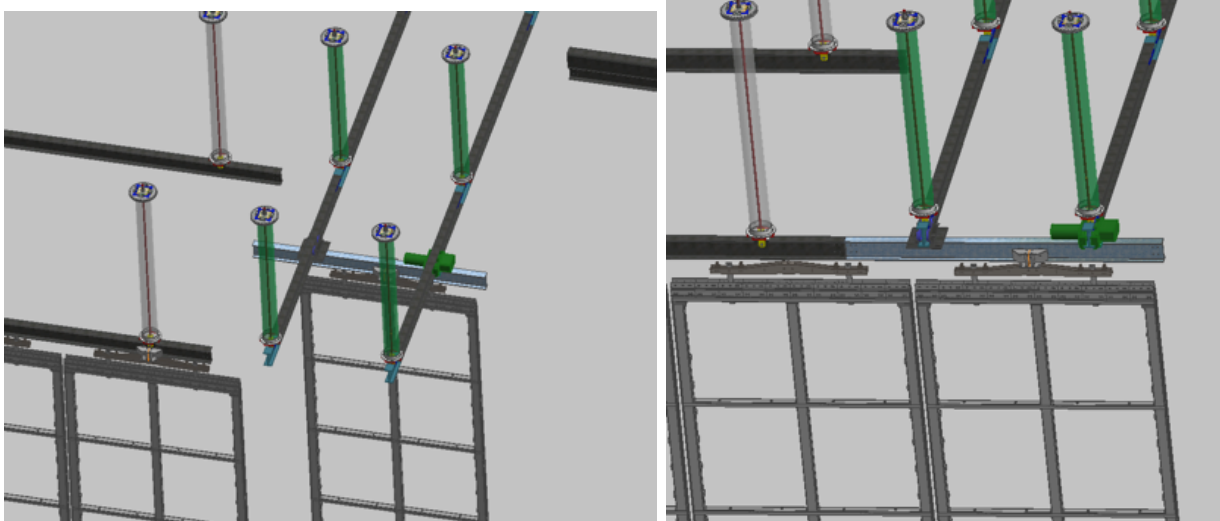


Figure 8.7: 3D models of the shuttle beam end of the DSS. The figures show how an APA is translated into position using the north-south beams until it lines up with the correct row of I-beams

long I-beams are then raised and pinned to the clevis. Each beam weighs roughly 160 kg (350 lbs). A lifting tripod is placed over each of the feedthroughs supporting a beam, and a 0.64 cm 0.25 in cable is fed through the top flange of the feedthrough down the 14 m to the cryostat floor where it is attached to the I-beam. The winches on each tripod raise the beam in unison in order to get it to the correct height to be pinned to the feedthrough clevis. Once the beams are mounted, a final survey of the beams takes place to ensure they are properly located and aligned to each other.

A mock-up of the shuttle system is constructed to test the mechanical interlock and drive systems for the shuttle beam for each detector module. Tests are conducted to evaluate the level of misalignment between beams that can be tolerated and the amount of positional control that can be achieved with the motorized trolley. It is expected this will be finished prior to the TDR. At the time of the TDR a larger prototype installation at Ash River will be under construction. This prototype will use full scale elements and will be used to develop the installation procedures and to test the detector module installation process.

8.4 The Integration and Test Facility

DUNE TC is responsible for interfacing with the LBNF logistics team at SURF to coordinate transport of all detector components into the underground areas. Due to the limited availability of surface areas at SURF for component storage, nearby facilities will be required to receive, store and ship materials to the Ross Shaft on an as-needed basis. A team within the TC organization will develop and execute the plan for receiving detector components at a surface facility and transporting them to the Ross Shaft in coordination with the on-site LBNF logistics team. The surface facility will require warehouse space with an associated inventory system, storage facilities, material transport equipment and access to trucking. Basic functions of this facility will be to receive the detector components arriving from different production sites around the world and

prepare them for transport into the underground areas, incorporating re-packaging and testing as necessary. As a substantial facility will be required, it can also serve as a location where some detector components are integrated and undergo further testing prior to installation.

The logistics associated with integrating and installing the FDs and their associated infrastructure present a number of challenges. These include the size and complexity of the detector itself, the number of sites around the world that will be fabricating detector and infrastructure components, the necessity for protecting components from dust, vibration and shock during their journey to the deep underground laboratory, and the lack of space on the surface near the Ross Shaft. To help mitigate the associated risks, DUNE plans to establish an ITF somewhere in the vicinity of SURF. This facility and its associated staff will need to provide certain functions and services connected to the DUNE FD integration and installation effort and will have other potential roles that are still under consideration. The areas to which the ITF will and could contribute are the following:

- **Transport buffer:** The ITF needs to provide storage capacity for a minimum one-month buffer of detector components required for the detector installation process in the vicinity of SURF and be able to accept packaging materials returned from the underground laboratory.
- **Longer-term storage:** The ITF needs to provide longer-term storage of detector components that need to be produced in advance of when they are to be installed and for which sufficient storage space does not exist at the production sites.
- **Re-packaging** The ITF needs to have the capability to re-package components arriving from the various production sites into boxes that can be safely transported through the shaft into the underground areas.
- **Component fabrication:** It could be convenient to fabricate some components in the vicinity of SURF at the ITF, taking advantage of undergraduate science and engineering students from the South Dakota School of Mines and Technology (SDSMT).
- **Component integration:** Integration of detector components received from different production sites that must be done prior to transport underground, such as the installation of photon detectors (PDs) and electronics on the anode plane assemblies, could be done prior to re-packaging at the ITF.
- **Inspection, testing and repair:** In cases where components are re-packaged for transport to the underground area, ITF support for performing tests on these components to ensure that no damage has occurred during shipping is likely desirable. In addition, components integrated at the ITF would require additional testing prior to being re-packaged. The ITF could provide facilities needed to repair some of the damaged components (others would likely need to be returned to their production sites).
- **Collaborator support:** The host institution of the ITF will need to provide support for a significant number of DUNE collaborators involved in the above activities including services such as housing assistance, office space, computing access, and safety training.
- **Outreach:** The host institution of the ITF would be ideally situated for supporting an

outreach program to build upon the considerable public interest in the experiment that exists within South Dakota.

The facilities project (LBNF) will provide the cryostats that house the detector modules and the cryogenics systems that support them. Additional large surface facilities in the vicinity of SURF will be required to stage the components of these infrastructure pieces prior to their installation in the underground areas. The requirements for these facilities, in contrast to the ITF, are relatively straight-forward and can likely be met by a commercial warehousing vendor, who would provide suitable storage space, loading and unloading facilities, and a commercial inventory management and control system. It is currently envisioned that operation of the LBNF surface facilities and the DUNE ITF will be independent from one another. However, the inventory systems used at the different facilities will need to ensure proper coordination of all deliveries being made to the SURF site.

A reasonable criterion for the locations of these surface staging facilities is to be within roughly an hour's drive of SURF. Population centers in South Dakota within this radius are Lead, Deadwood, Sturgis, Spearfish, and Rapid City. The LBNF surface facilities, which are not expected to have significant auxiliary functionality, would logically be located as near to the SURF site as possible. In the case of the DUNE ITF, however, locating the facility in Rapid City to take advantage of facilities and resources associated with the South Dakota School of Mines & Technologies (SDSMT) has a number of potential advantages. SDSMT and the local business community in Rapid City have expressed interest in incorporating the DUNE ITF into an overall regional development program.

8.4.1 Requirements

The leadership teams associated with the DUNE consortia taking responsibility for the different FD subsystems have provided input to TC on which potential ITF functions and services would be applicable to their subsystems. The consortia have also made preliminary assessments of the facility infrastructure requirements that would be necessary in order for these functions and services to be provided for their subsystems at the ITF. An attempt to capture preliminary, global requirements for the ITF based on the information received from the consortia results in the following:

- Warehousing space on the order of 2800 m² (30,000 square feet); driven by potential need to store hundreds of the larger detector components needed to construct the TPCs. The provided space will need to maintain some minimal cleanliness requirements (e.g.; no insects) and be climate-controlled within reasonable temperature and humidity ranges.
- Crane or forklift coverage throughout the warehousing space to access components as needed for further processing or transport to SURF.
- Docking area to load trucks with detector components being transported to SURF and to receive packaging materials returned from the site.
- Smaller clean room areas within the warehousing space to allow for the re-packaging of

detector components for transport underground. Re-packaging of larger components will require local crane coverage within the appropriate clean room spaces.

- Dedicated space for racks and cabinets available for dry-air storage and testing of electronics components. Racks and cabinets must be properly connected to the building ground to avoid potential damage from electrostatic discharges.
- Climate-controlled dark room space for the handling and testing PD components.
- Dedicated clean room on order of 1000 m² (10,000 square feet) to facilitate integration of electronics and PDs on anode plane assemblies. The integrated anode plane assemblies are tested in cold boxes supported by cryogenics infrastructure. Clean room lighting must be UV-filtered to avoid damaging the PDs. The height of the clean room must accommodate crane coverage needed for movement of the anode plane assemblies in and out of the cold boxes. It will also be necessary to have platforms for installation crews to perform work at heights within different locations in the clean room.
- Access to machine and electronics shops for making simple repairs and fabricating unanticipated tooling.
- Access to shared office space for up to 30 collaborators contributing to the activities taking place at the ITF. Assistance for identifying temporary housing in the vicinity of the ITF for the visiting collaborators.

8.4.2 Management

Overall management of the ITF is envisioned to be responsibility of one or more of the collaborating institutions on DUNE. If the ITF is located in Rapid City, SDSMT would be a natural choice due to its physical proximity, connections to the local community and ability to provide access to resources and facilities that would benefit planned ITF activities. Initial discussions with SDSMT representatives have taken place, in which they have expressed a clear interest for hosting the ITF. Additional discussions will be needed to understand the details of the ITF management structure with in the context of a more finalized set of requirements for the facility.

8.4.3 Inventory System

Effective inventory management will be essential for all aspects of DUNE detector development, construction, installation and operation. While its relevance and importance go beyond the ITF, the ITF is the location at which LBNF, DUNE project management, consortium scientific personnel and SURF operations will interface. We therefore will develop standards and protocols for inventory management as part of the ITF planning. A critical requirement for the project is that the inventory management system for procurement, construction and installation be compatible with future QA, calibration and detector performance database systems. Experience with past large de-

detector projects, notably $\text{NO}\nu\text{A}$, has demonstrated that the capability to track component-specific information is extremely valuable throughout installation, testing, commissioning and routine operation. Compatibility between separate inventory management and physics information systems will be maintained for effective operation and analysis of DUNE data.

8.4.4 ITF Infrastructure

TC is responsible for providing the common support infrastructure at the ITF. This includes the cranes and forklifts to move equipment in the ITF, any cryostats and cryogenics systems to enable cold tests of consortium-provided components, the cleanrooms and cleanroom equipment to enable work on or testing of consortia components, and UV-filtered lighting as needed. This also includes racks and cable trays.

8.5 Installation Coordination and Support

Installation Coordination and Support (also called simply *Installation*) is responsible for coordinating the detector installations, providing detector installation support and providing installation-related infrastructure. The installation group management responsibility is shared by a scientific lead and a technical lead that report to the Technical Coordinator. The group responsible for activities in the underground areas is referred to as the underground installation team (UIT). The ITF group, which delivers equipment to the Ross Shaft, and the UIT, which receives the equipment underground, need to be in close communication and work closely together.

Underground installation is in general responsible for coordinating and supporting the installation of the detector modules and providing necessary infrastructure for installation of the experiment. While the individual consortia are responsible for the installation of their own detector equipment, it is essential that the detector installation be planned as a whole and that a single group coordinates the installation and adapts the plans throughout the installation process. The UIT has responsibility for overall coordination of the installations. In conjunction with each consortium the UIT makes the installation plan that describes how the detector modules are to be installed. The installation plan is used to define the spaces and infrastructure that will be needed to install them. The installation plan will also be used to define the interfaces between the Installation group and the consortium deliverables.

8.5.1 UIT Infrastructure

The installation scope includes the infrastructure needed to install the FD such as the cleanroom, a small machine shop, special cranes, scissor lifts, and access equipment. Additional equipment required for installation includes: rigging equipment, hand tools, diagnostic equipment (including oscilloscopes, network analyzers, and leak detectors), local storage with some critical supplies and

some personal protective equipment (PPE). The UIT will also provide trained personnel to operate the installation infrastructure. The consortia will provide the detector elements and custom tooling and fixtures as required to install their detector components.

8.5.2 Underground Detector Installation

For the detector modules to be installed in safe and efficient manner, the efforts of the individual consortia must be coordinated such that the installation is planned as a coherent process. The interfaces between the individual components must be understood and the spaces required for the installation process planned and documented. The installation planning must take into account the plans and scope of the LBNF effort and the individual plans of the nine consortia. By working with the LBNF team and the members of the consortia responsible for building and installing their components, a joint installation plan and schedule, taking into account all activities and needs of all stakeholders, can be developed. Although the organization of the installation effort is still evolving, an installation coordinator will be the equivalent of a scientific lead for this effort.

One of the primary early responsibilities of the UIT is to develop and maintain the DUNE installation plan and the installation schedule. This installation plan describes the installation process in sufficient detail to demonstrate how all the individual consortium installation plans mesh and it gives an overview of the installation process. The installation plan is used by the UIT to define the underground infrastructure needed for detector installation and the interfaces it has with respect to the consortia. The UIT is responsible for reviewing and approving the consortium installation plans. Approved installation plans, engineering design notes, signed final drawings, and safety documentation and procedures are all prerequisites for the PRR. Approved procedures, safety approval, and proper training are all required before the UIT performs work. During the installation phase the installation leadership coordinates the DUNE installation effort and adapts the schedule as needed. The installation coordinator, together with management, will also resolve issues when problems occur.

The installation infrastructure to be provided by the UIT includes: the underground ISO 8 (or class 100,000) clean room used for the installation; cranes and hoists (if they are not delivered by LBNF); and scissor lifts, aerial lifts, and the common work platforms outside the cryostat. The UIT will have responsibility for operating this equipment and assisting the consortia with activities related to rigging, material transport, and logistics. Each consortium is responsible for the installation of their own equipment, so the responsibility of the installation group is limited, but the material handling scope is substantial. To support the installation process, an installation floor manager will lead a trained crew with the main responsibility of transporting the equipment to the necessary location and operating the cranes, hoists, and other common equipment needed for the installation. It is expected that the installation crew will work with the teams from the various consortia but will mainly act in a supporting function. The UIT floor manager will be responsible for supervising the UIT crew, but the ultimate responsibility for all detector components remains with the consortia even while the underground team is rigging or transporting these components. This will be critical in the case where any parts are damaged during transport or installation, as the consortia need to judge the necessary actions. For this reason, a representative or point of contact (POC) from the consortia must be present when any work is performed on their equipment.

The consortium is responsible for certifying that each installation step is properly performed.

The UIT acts as the primary point of contact with LBNF and SURF from the time the components reach the Ross headframe until the equipment reaches the experimental cavern. If something goes wrong, SURF calls the UIT leader who then contacts the responsible party. The consortia are responsible for delivering to the UIT all approved procedures and specialized tooling required for transport. The UIT leader acts as a point of contact if the LBNF or SURF team has questions or difficulties with the underground transport. The UIT receives the materials from LBNF and SURF at the entrance to the DUNE excavations. The UIT then delivers the equipment to the required underground location.

In an effort to get an early estimate of the equipment required to install the detectors the UIT has developed a preliminary installation plan that outlines the installation process. At present the installation plan consists of a 3D model of the cryostat in the excavations. The SP module elements are inserted in the model and a proposal for how they are transported, assembled, and inserted into the cryostat has been conceptually developed and expressed in a series of images some of which are shown in Figures 8.8 and 8.9. Conceptual designs of the infrastructure needed to support the transport and assembly are also included in the model. See Figures 8.10 and 8.11. With this as a tool, the proposed installation sequence can be iterated with the consortia to converge on a baseline installation plan. A similar process will be followed for the DP module once the base configuration for the single-phase (SP) installation is agreed upon. The UIT has focused initially on the SP module as the SP components are larger and the installation process more complex.

In the current installation plan, DUNE will take ownership of the different underground areas at different times. The surface data room and the underground room in the CUC are available significantly before the collaboration has access to the cryostats; the optical fibers between the surface and underground will be in place even earlier. This will allow a DAQ prototype to be developed and tested early. The installation of the DAQ hardware can also be finished before the start of detector installation if desired, so the DAQ will not be on the critical path. When the collaboration receives access to Cryostat 1 the steel work for Cryostat 2 will be finished and the work on installing the membrane will have started. Excavation will be complete. For planning purposes it is assumed that the first detector module will be SP and the second dual-phase (DP). The first step in the SP installation is to install the cryogenics piping and the DSS. As this piping will require welding and grinding, it is a dirty process and must be complete before the area can be used as a clean room. When this is complete the cryostat can be cleaned and the false floor re-installed. The clean infrastructure for installing the detector module, including the clean room, work platforms, scaffolding, the fixturing to hold the detector elements during assembly, and all the lifts need to be set up. Once the infrastructure is in place and the area is clean, the installation of the main elements can start. The general layout of the installation area showing the necessary space and equipment is shown in Figure 8.8.

The SP module is installed by first installing the west endwall or endwall 1 (see Figure 8.12).

The anode plane assemblies and cathode plane assemblies with top and bottom FC panels are installed next. The plan is to install six anode plane assemblies and four cathode plane assemblies per week, which is enough to complete one of the 25 rows every week. Additional time is built into the schedule to take into account that the installation will be slower at the beginning and some

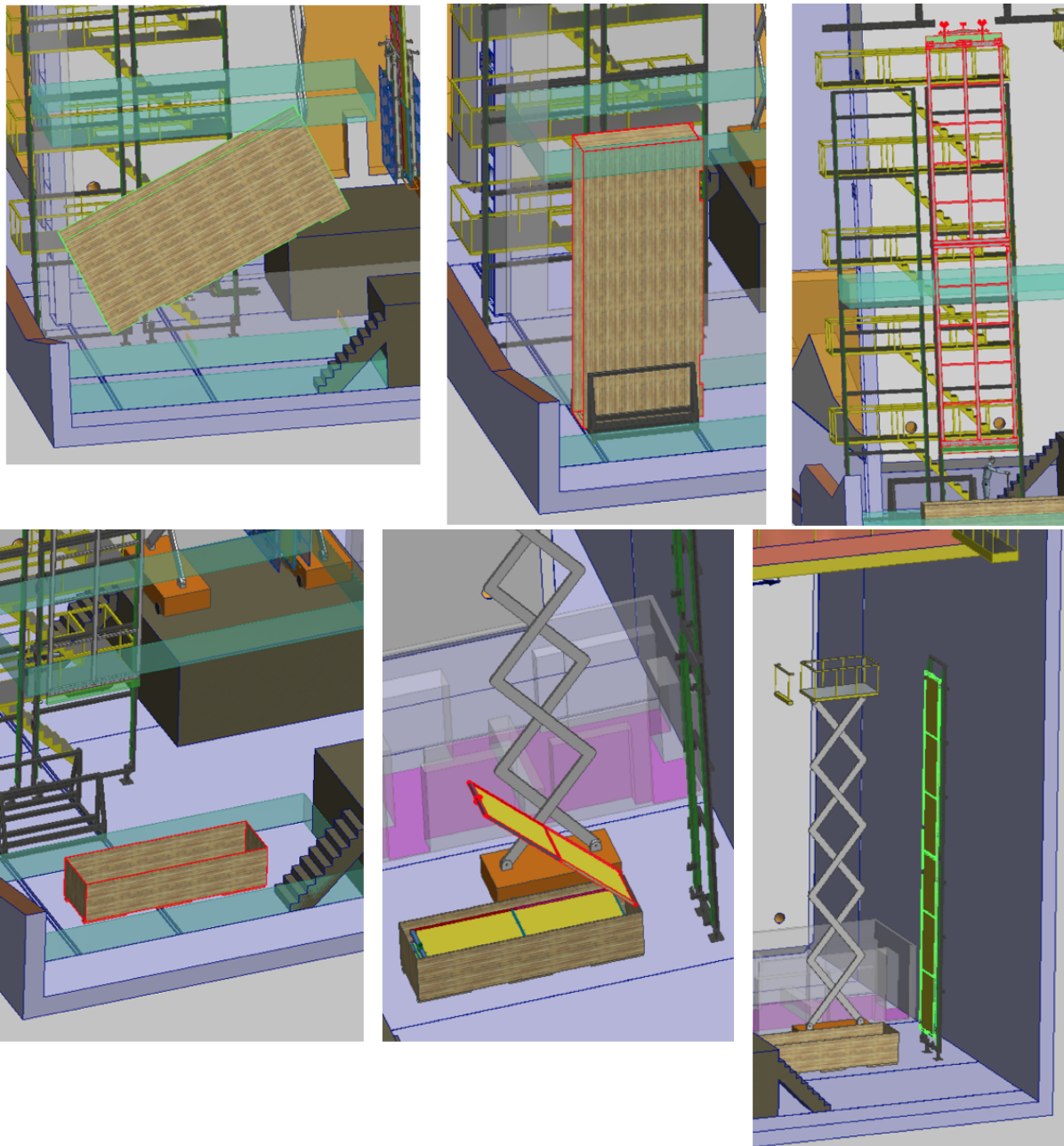


Figure 8.8: Top row from left: crated APA rotating to vertical position; crated vertical APA placed in cart; APA panels moved to fixture using the under-bridge crane. Bottom row: series showing CPA panels uncrated and moved to fixture.

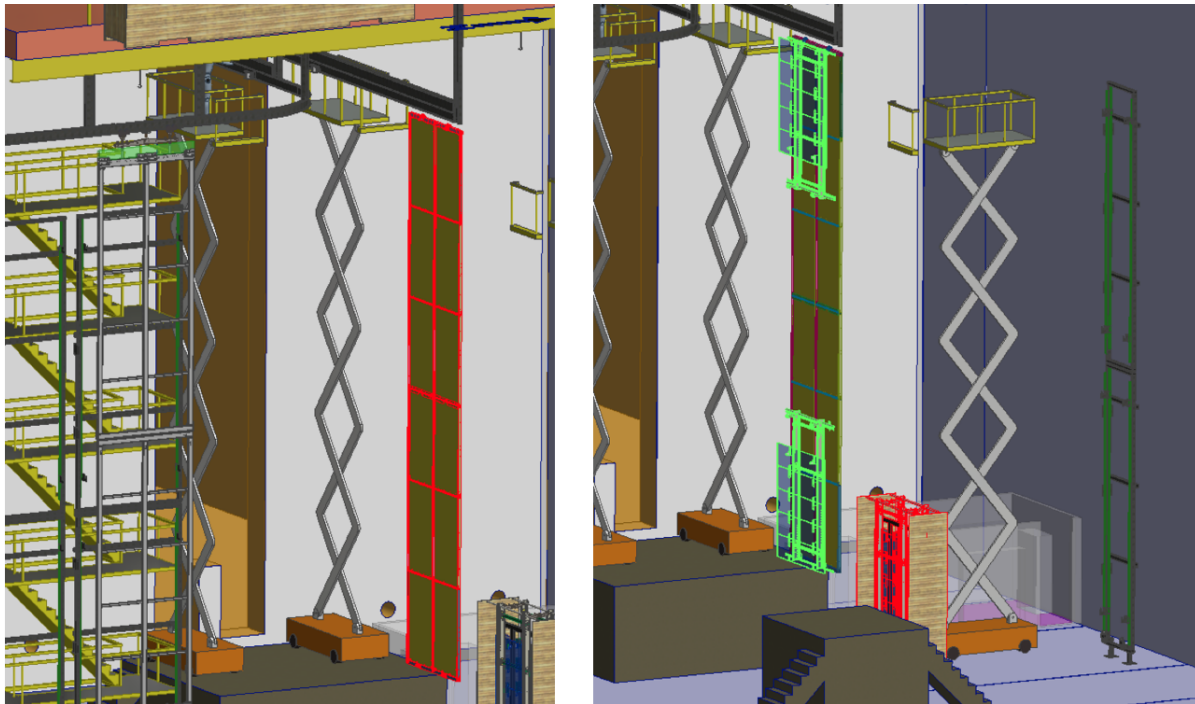


Figure 8.9: On the left, the assembled CPA panel is placed onto the north TCO beam. On the right, the (green) FC panels (already lowered into SAS and moved into the clean room) are installed as the CPA array hangs under the TCO beam.

re-work may be needed. By building west-to-east, complete rows can be finished and tested before moving to the next row. This reduces the risk of finding a fault after final FC deployment and cabling, which would require dismantling part of the detector module. Some of the steps needed to install the APA and CPA modules outside the cryostat are also shown in Figure 8.8. The middle three panels show how the APA needs to be handled in order to rotate it and mount it to the assembly frame. After two anode plane assemblies are mounted on top of each other, the cabling for the lower anode plane assemblies, and the CE and PD cables can be installed. The lower three panels show how the 2m CPA sub-panels are removed from the transport crates and assembled on a holding frame. Once the CPA module is assembled the FC units can be mounted. Finally, once the anode plane assemblies and cathode plane assemblies are installed, the endwall 2 can be installed. A high-level summary of the schedule is shown in Figure 8.13.

As is seen in the installation schedule the second cryostat becomes available four months before the first detector module installation is complete. In this period, installation work for both detector modules proceeds in parallel. Like the SP module, the first step is the installation of the cryogenics piping, followed by a thorough cleaning and installation of the false floor. While this piping is being installed, the DP chimneys for the electronics along with the PDS and CRP instrumentation feedthroughs can also be installed. Since the chimneys are installed into the roof of the cryostat, this work is performed well away from the final installation work on the first detector module so there should be no conflicts. Once the first detector module is installed work on setting up the second detector module's installation infrastructure can begin. This work includes moving the cranes and work platforms along with moving the walls of the clean room so that the second cryostat is clean. The air filtration to the cryostat is also moved to the second cryostat. Since

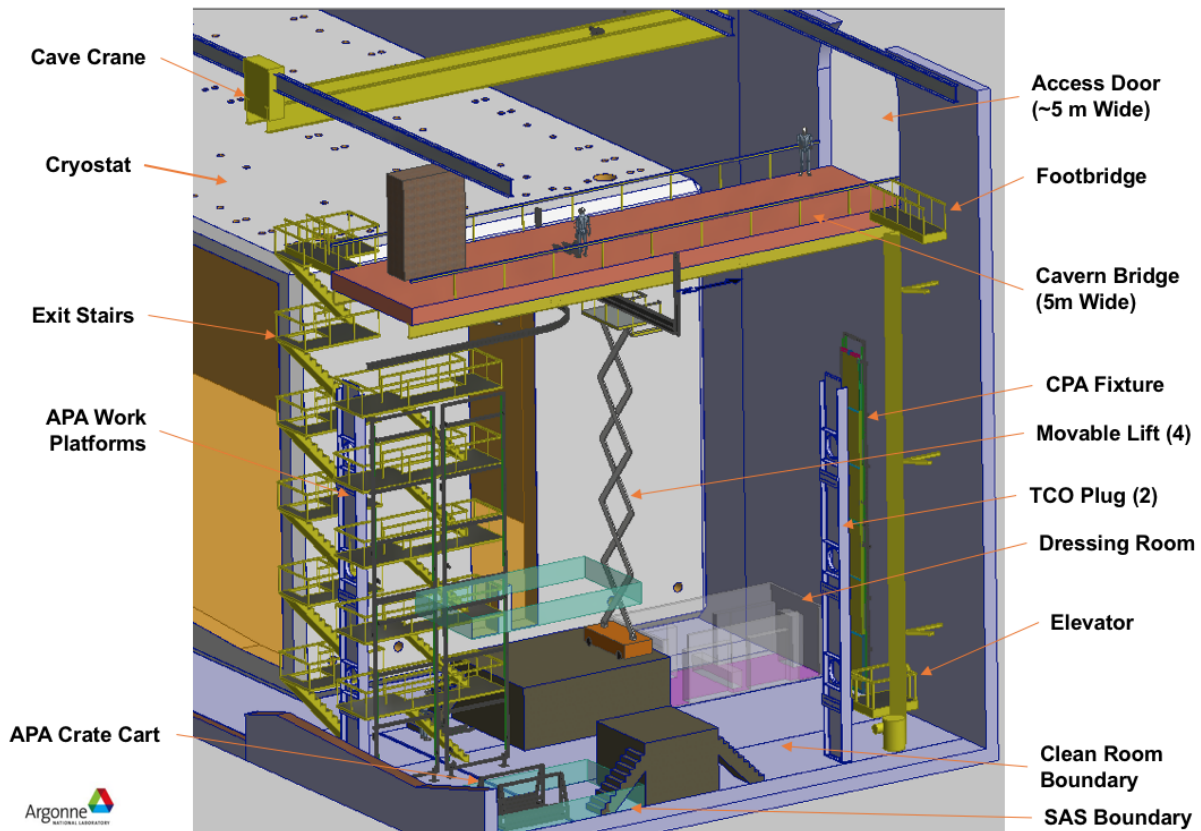


Figure 8.10: 3D model of the underground area showing the infrastructure to install the SP module in cryostat 1. The most significant features are presented including the APA and CPA assembly areas, the region around the TCO for materials entering the cryostat, the changing room, the region for the materials air lock, (SAS), and the means of egress.

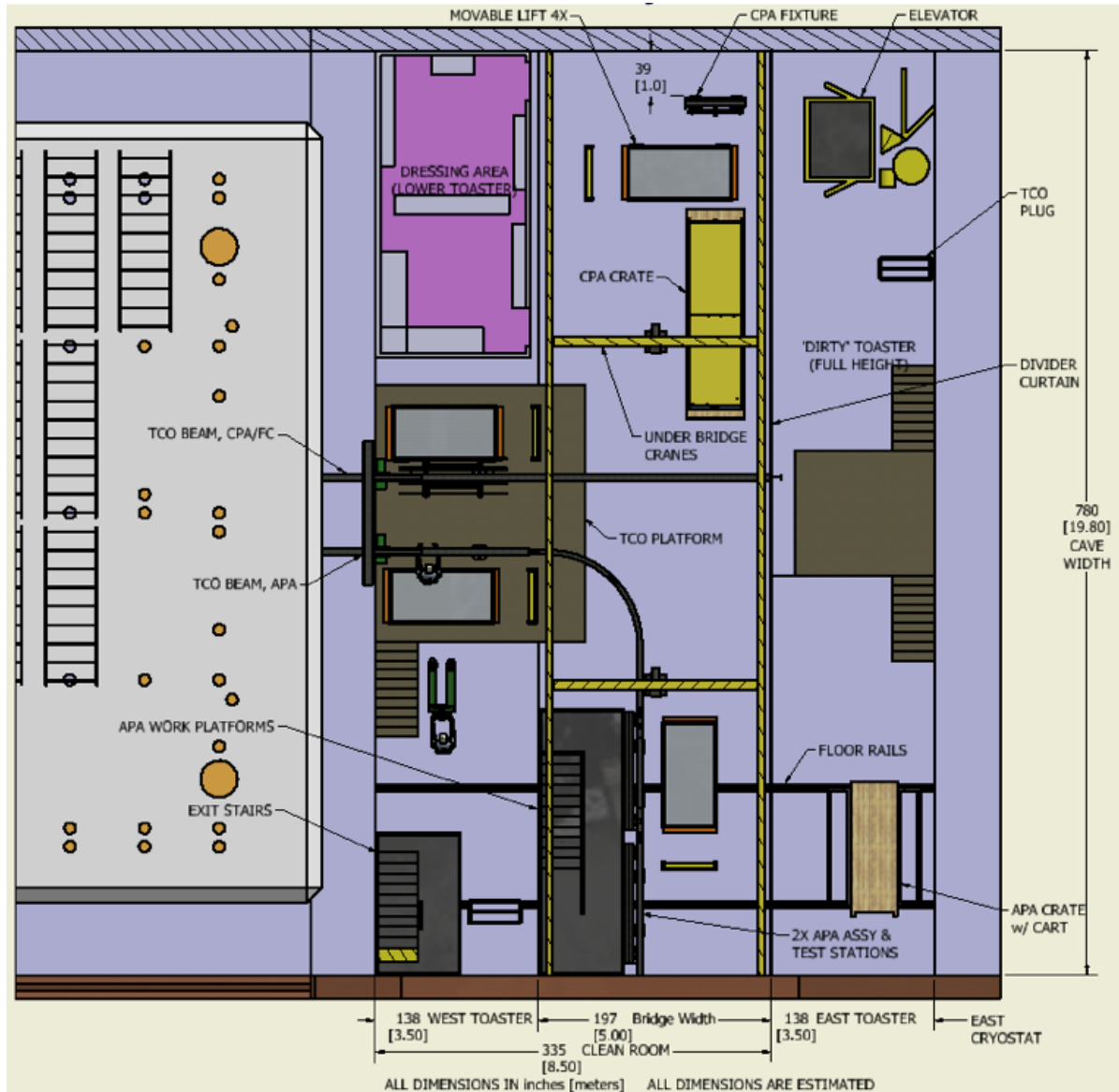


Figure 8.11: Section view of the 3D model showing layout, looking down on the installation area from below the bridge. Areas shown, left to right, are the cryostat and TCO, the platform in front of the TCO, the dressing area, the APA and CPA assembly area (directly under the bridge), and the stairs and elevator. The lower right corner of the region is used as the materials air lock.

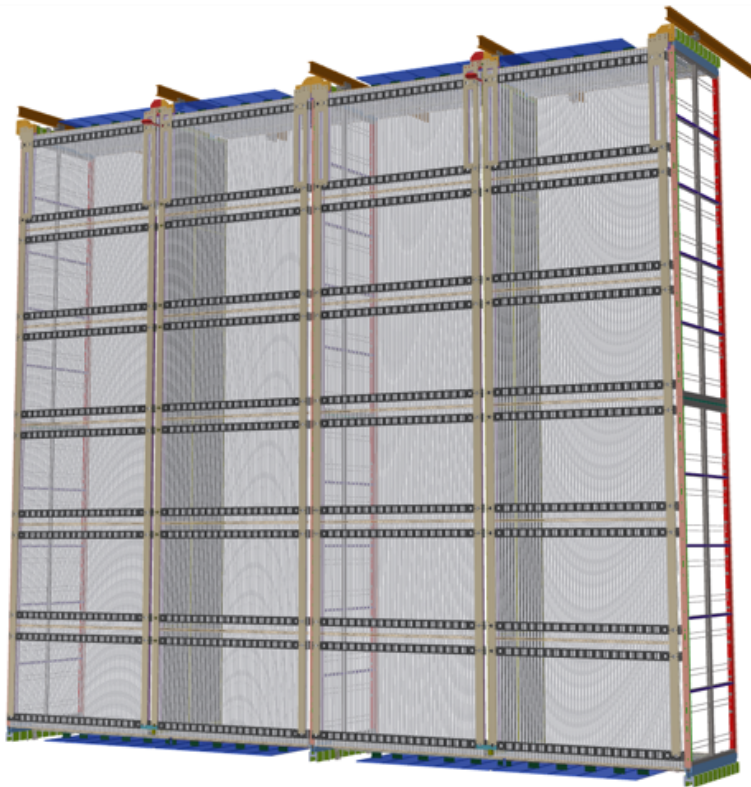


Figure 8.12: End view of SP module with endwall FC in place, with one row of anode plane assemblies and cathode plane assemblies.

much of the work for the DP installation will be performed inside the cryostat, in principle, outside the cryostat a clean room area smaller than that for the SP module would suffice. However, for planning purposes, it will not be completely clear what type of detector module will be installed in the second cryostat until fairly late. Therefore the UIT will plan to provide a sufficiently large area outside the cryostat to accommodate either detector technology. The much smaller clean room for a DP module could be installed just outside the TCO. The installation process inside the DP module will proceed east-to-west. At the start of the TPC installation the first four CRPs – comprising the first row – will be installed. The left panel in Figure 8.14 shows two CRPs being installed near the roof of the cryostat and the right panel shows one of the CRPs in a transport box being moved into the cryostat. Once the first CRP row is installed and tested, the first endwall FC can be installed. In general rows of CRPs will be installed, followed by rows of FC modules, followed by the cathode installation at the bottom of the detector module, followed by PDs under the cathode plane. At the end of the installation, the second endwall FC is installed and a final testing period for the full detector module is foreseen. The DP module installation sequence is shown in green in Figure 8.13.

Prior to the TDR, mutually agreed upon installation plans must be approved. These will set the schedule for the installation and will determine the planning for staffing and budget. Having good estimates for the time needed and having enough experience to ensure that the interfaces are understood and the procedures are complete is important for accurate planning. The experience at ProtoDUNE will be very important as the ProtoDUNE installation establishes the procedures for handling all the detector elements and in many cases gives accurate estimates for the time

needed. However, in the case of the SP module, many of these procedures need to be revised or newly developed. For example, the SP module will be twice as high as ProtoDUNE-SP, so two anode plane assemblies need to be assembled together and a totally different cabling scheme is needed. Testing the cabling must be done prior to the TDR in order to ensure the design is viable. The DP will also need to develop installation procedures as the DP module will have a significantly different FC and cathode plane.

By definition, the installation is on the critical path, making it vital that the work be performed efficiently and in a manner that has low risk. In order to achieve this, a prototype of the installation equipment for the SP module will be constructed at Ash River (the NO ν A neutrino experiment FD site in Ash River, Minnesota, USA), and the installation process tested with dummy detector elements. It is expected that the setup will be available at the time of the TDR, but any lessons learned will need to be implemented and tested after this. In the period just prior to the start of installation, the Ash River setup will be used as a training ground for the UIT.

8.5.3 Preparation for Operations

After the detector modules are installed in the cryostats there remains a lot of work before they can be operated. First the TCO must be closed. This requires bringing back the cryostat manufacturer. First the missing panel with the steel beams and steel panel are installed to complete the cryostat's outer structural hull. Then the remaining foam blocks and membrane panels are installed from the inside using the roof access holes to enter the cryostat.

In parallel, the LAr pumps are installed at the ends of the cryostat and final connections are made to the recirculation plant. Once the pumps are installed, the cryostat is closed, and everything is leak tested, the cryogenics plant can be brought into operation. First the air inside the cryostat is purged by injecting pure argon gas at the bottom at a rate such that the cryostat volume is filled uniformly but faster than the diffusion rate. This produces a column of argon gas that rises through the volume and sweeps out the air. This process is referred to as the *piston purge*. When the piston purge is complete the cool-down of the detector module can begin. Misting nozzles inject a liquid-gas mix into the cryostat that cools the detector components at a controlled rate.

Once the detector is cold the filling process can begin. Gaseous argon stored at the surface at SURF is brought down the shaft and is re-condensed underground. The LAr then flows through filters to remove any H₂O or O₂ and flows into the cryostat. Given the very large volume of the cryostats and the limited cooling power for re-condensing, it is expected to take 12 months to fill the first detector module and 14 months to fill the second. During this time the detector readout electronics will be on monitoring the status of the detector. Once the detector module is full, the drift high voltage can be carefully ramped up and data taking can begin.

Glossary

35 ton prototype The 35 ton prototype cryostat and single-phase (SP) detector built at Fermilab before the ProtoDUNE detectors. 75, 95, 178, 216, 218, 219, 221, 223, 229, 230, 233

analog-to-digital converter (ADC) A sampling of a voltage resulting in a discrete integer count corresponding in some way to the input. 45, 47–49, 51, 53–61, 67, 70–72, 74, 76, 80, 82, 83, 145, 186, 264

as low as reasonably achievable (ALARA) Typically used with regard management of radiation exposure but may be used more generally. It means making every reasonable effort to maintain e.g., exposures, to as far below the limits as practical, consistent with the purpose for that the activity is undertaken. 90

advanced mezzanine card (AMC) Holds digitizing electronics and lives in Micro Telecommunications Computing Architecture (μ TCA) crates. 195

anode plane assembly (APA) A unit of the SP detector module containing the elements sensitive to ionization in the LAr. It contains two faces each of three planes of wires, and interfaces to the cold electronics and photon detection system. 4–51, 53, 54, 57, 58, 60–62, 65, 67–76, 78–88, 91, 92, 98, 99, 101–104, 111, 115, 123–125, 128, 129, 131, 136, 137, 139–142, 147, 153–156, 158–164, 166, 167, 169, 170, 172, 178, 180, 182, 183, 186, 187, 195, 198, 199, 204, 215, 216, 222, 223, 231, 234, 241, 245, 249, 256, 268, 273–276, 278, 281–286, 288, 293

artDAQ A general-purpose Fermilab data acquisition framework for distributed data combination and processing. It is designed to exploit the parallelism that is possible with modern multi-core and networked computers. 188

ASIC application-specific integrated circuit. 45, 47–49, 51, 53–61, 65, 67–71, 74–77, 80, 82–85

Advanced Telecommunications Computing Architecture (ATCA) An advanced computer architecture specification developed for the telecommunications, military, and aerospace industries that incorporates the latest trends high-speed interconnect technologies, next-generation processors, and improved reliability, availability and serviceability. 186, 198

bottom field cage (bottom FC) The horizontal portions of the SP FC on the bottom. 86, 91, 92, 98, 100, 101, 105–107, 111, 112, 114, 115, 118

- Bump On Wire (BOW)** A working name for the front-end readout computing elements used in the nominal DAQ design to interface the DP crates to the DAQ front-end computers. 182
- cold electronics (CE)** Refers to readout electronics that operate at cryogenic temperatures. 17, 20, 21, 25, 26, 44–50, 52, 54, 56–58, 61–63, 65, 67–72, 75–85, 128, 159, 160, 162–164, 169, 170, 173, 178, 198, 256, 264, 283
- computational fluid dynamics (CFD)** High performance computer-assisted modeling of fluid dynamical systems. 210, 216, 217, 222
- conventional facilities (CF)** Pertaining to construction and operation of buildings or caverns and conventional infrastructure. 204
- cryogenic instrumentation and slow controls (CISC)** A DUNE consortium responsible for the cryogenic instrumentation and slow controls components. 7, 68, 78, 159, 160, 162, 200, 204, 210–214, 233, 237–240, 242, 243, 252–256
- CMOS** Complementary metal-oxide-semiconductor. 44, 45, 53, 54, 57, 58, 67, 68, 233
- CMP** configuration management plan. 267
- Cluster On Board (COB)** An ATCA motherboard housing four RCEs. 183, 186, 187, 198, 201, 296
- COLDATA** a 64-channel control and communications ASIC. 47, 51, 54, 56, 57, 62, 65, 68–71, 74, 82, 83, 264
- common fund** The shared resources of the collaboration. 261, 264
- cathode plane assembly (CPA)** The component of the SP detector module that provides the drift HV cathode. 4–6, 9, 40, 78, 79, 86, 87, 89, 91–93, 95–109, 111–119, 137, 140, 141, 159–161, 231, 234, 273, 274, 281–286
- charge-parity symmetry violation (CPV)** Lack of symmetry in a system before and after charge and parity transformations are applied. 2, 13
- charge readout (CRO)** The system for detecting ionization charge distributions in a DP detector module. 172, 178, 180, 182, 187, 198
- charge-readout plane (CRP)** In the DP technology, a collection of electrodes in a planar arrangement placed at a particular voltage relative to some applied E field such that drifting electrons may be collected and their number and time may be measured. 228, 229, 231, 234, 241, 256, 283, 286, 287
- central utility cavern (CUC)** The central underground cavern containing utilities such as central cryogenics and other systems, and the underground data center and control room. 69, 70, 161, 162, 180, 193–195, 198–200, 202, 204–206, 208, 242, 260, 281

- DAQ primary buffer (primary buffer)** The portion of the DAQ front-end fragment that accepts full data stream from the corresponding detector unit and retains it sufficiently long for it to be available to produce a data fragment. 180, 182, 185, 187–189, 196, 291, 293
- DAQ data receiver (DDR)** The portion of the DAQ front-end fragment that accepts data from the DAQ front-end readout (FER), emits trigger candidates produced from the input trigger primitives, and forwards the full data stream to the DAQ primary buffer (primary buffer). 180, 182, 293
- data selector** The portion of the DAQ front-end fragment that accepts trigger commands and returns the corresponding data fragment. 180, 182, 185, 188, 293
- DAQ front-end readout (FER)** The portion of a DAQ front-end fragment that accepts data from the detector electronics and provides it to the front-end computer (FEC). In the nominal design it is also responsible for generating channel level trigger primitives. 176, 177, 182, 183, 185, 188, 190, 191, 193, 291, 293
- DAQ front-end fragment** The portion of one DAQ partition relating to a single FEC and corresponding to an integral number of detector units. See also data fragment. 173–176, 178, 181–183, 185–192, 198, 291
- out-of-band trigger command dispatcher (OOB dispatcher)** This component is responsible for dispatching a supernova neutrino burst (SNB) dump command to all FERs in the detector module. 176, 180, 188
- DAQ partition** A cohesive and coherent collection of DAQ hardware and software working together to trigger and read out some portion of one detector module; it consists of an integral number of DAQ front-end fragments. Multiple DAQ partitions may operate simultaneously, but each instance operates independently. 172–176, 182, 183, 190, 291, 293
- data acquisition (DAQ)** The data acquisition system accepts data from the detector FE electronics, buffers the data, performs a trigger decision, builds events from the selected data and delivers the result to the offline secondary DAQ buffer. 6, 7, 41, 61, 63, 65, 67–70, 74, 79, 83, 123, 159–162, 164, 171–178, 180–189, 191, 196–209, 214, 220–222, 227, 239, 241, 242, 247, 253, 256, 260, 281, 292
- data fragment** A block of data read out from a single DAQ front-end fragment that span a contiguous period of time as requested by a trigger command. 176, 182, 185, 188, 191, 198, 291
- detector module** The entire DUNE far detector is segmented into four modules, each with a nominal 10 kt fiducial mass. 2–4, 7–9, 87, 90, 91, 124, 171–173, 176–178, 181–183, 185–194, 197–199, 201, 204, 206, 210, 212, 215, 216, 218, 222, 225, 227, 228, 231, 236, 240, 244, 245, 256, 260, 262, 265, 268–271, 273, 275, 277, 279–281, 283, 286, 288, 291, 292, 296–298
- detector unit** A subdetector may be partitioned into a number of similar parts. For example the single-phase TPC subdetector is made up of APA units. 172, 176, 181, 182, 189–191, 193,

198, 291, 293, 295, 299

secondary DAQ buffer A secondary DAQ buffer holds a small subset of the full rate as selected by a trigger command. This buffer also marks the interface with the DUNE Offline. 176, 177, 182, 187, 188, 291

DP module dual-phase detector module. 117, 128, 179, 180, 193, 208, 217, 219, 223, 224, 229, 246, 256, 273, 281, 286-288

dual-phase (DP) Distinguishes one of the DUNE far detector technologies by the fact that it operates using argon in both gas and liquid phases. 118, 172, 182, 187, 190, 193, 194, 198, 281, 283, 286-288

data quality monitoring (DQM) Analysis of the raw data to monitor the integrity of the data and the performance of the detectors and their electronics. This type of monitoring may be performed in real time, within the data acquisition (DAQ) system, or in later stages of processing, using disk files as input. 199

DRE dynamic range enhancement. 60, 61

detector support system (DSS) The system used to support the SP detector within the cryostat. 23, 36, 38, 224, 226, 247, 273-275, 281

DUNE Deep Underground Neutrino Experiment. 256, 257, 259, 260, 262-268, 271, 272, 275-281

event builder (EB) A software agent servicing one detector module by executing trigger commands by reading out the requested data. 176, 177, 180, 182, 185, 187, 188

electronic document management system (EDMS) A computerized system used at CERN by which documents are managed. 266, 269

ENC equivalent noise charge. 44, 45, 60, 72, 73, 75, 76

ES&H Environment, Safety and Health. 117, 259, 267, 268, 270, 272

external trigger logic (ETL) Trigger processing that consumes detector module level trigger notification information and other global sources of trigger input and emits trigger command information back to the module trigger logics (MTLs). 176, 190-193, 295, 298

endwall field cage (endwall FC) The vertical portions of the SP FC near the wall. 86, 87, 91, 92, 95, 98-104, 108-111, 113, 115, 116, 118, 119, 222, 223, 273, 286

external trigger candidate Information provided to the MTL about events external to a detector module so that it may be considered in forming trigger commands. 191, 192, 295

field cage (FC) The component of a LArTPC that contains and shapes the applied E field. 4-6, 9, 23, 62, 67, 79, 86-88, 90-92, 95, 98-100, 103-105, 107, 109, 111-119, 216, 231, 234, 245,

264, 273, 274, 281, 283, 286–288

final design review (FDR) A project management device by which a final design is reviewed. 265

far detector (FD) Refers to the 40 kt fiducial mass DUNE detector to be installed at the far site at SURF in Lead, SD, to be composed of four 10 kt modules. 3, 12, 43, 71, 72, 121, 123, 163, 169, 171–175, 177, 200–202, 206–208, 212, 217, 218, 222, 240, 256–259, 272, 276, 277, 279, 288

FEA finite element analysis. 156

front-end computer (FEC) The portion of one DAQ partition that hosts the DAQ data receiver (DDR), primary buffer and data selector. It is connected to the FER via fiber optic. Each detector unit of a certain granularity, such as two SP anode plane assemblies (APAs), has one front-end computer that receives data from the readout hardware, hosts the primary DAQ memory buffer for that data, emits trigger candidates derived from that data, and satisfies requests for producing subsets of that data for egress. 173, 176–178, 181–183, 186, 187, 189–191, 201, 291

Front-End Link eXchange (FELIX) A high-throughput interface between front-end and trigger electronics and the standard PCIe computer bus. 183, 185, 187, 201, 205

front-end mother board (FEMB) Refers a unit of the SP cold electronics that contains the front-end amplifier and ADC ASICs covering 128 channels. 45, 47–53, 56–59, 61–65, 67–72, 74–76, 78–80, 82–85, 198

front-end (FE) The front-end refers a point that is “upstream” of the data flow for a particular subsystem. For example the front-end electronics is where the cold electronics meet the sense wires of the TPC and the front-end DAQ is where the DAQ meets the output of the electronics. 6, 8, 12, 24–26, 36, 47–49, 51, 53, 54, 60, 69, 70, 74, 88, 158, 167, 169, 170, 173–175, 177, 180, 181, 183, 186, 187, 189, 197, 198, 201, 220, 221, 238, 244, 298

FNAL see Fermilab. 128, 137, 148, 165

field programmable gate array (FPGA) An integrated circuit technology that allows the hardware to be reconfigured to execute different algorithms after its manufacture and deployment. 51, 64, 65, 69, 70, 83, 183, 187, 201, 296

FSS field shaping strips. 96, 105, 106, 111

GEometry ANd Tracking, version 4 (Geant4) A software toolkit for the simulation of the passage of particles through matter using Monte Carlo methods. 128

ground plane (GP) An electrode that is held to be electrically neutral relative to Earth ground voltage. 11, 91, 95, 98–101, 107, 111, 112, 216, 226, 228, 231, 245, 273

high-level trigger (HLT) A source of triggering at the module level. 190, 192

- high voltage (HV)** Generally describes a voltage applied to drive the motion of free electrons through some media. 6, 23, 31, 48, 58, 68, 69, 71, 72, 74, 78, 80, 81, 86, 88, 90–96, 98, 103–106, 109, 111–119, 126, 159–162, 173, 221, 222, 228, 229, 231–234, 241, 242, 244, 246, 252, 256, 264
- IESHP** integrated environmental, safety and health plan. 267
- integrated master schedule (IMS)** A project management device consisting of linked tasks and milestones. 261, 262, 264
- integration and test facility (ITF)** A facility where various detector components will be tested prior to installation. 7, 36, 37, 39–41, 208, 248, 256, 262, 266, 267, 276–279
- LArASIC** A 16-channel front-end ASIC that provides signal amplification and pulse shaping. 47, 51, 53–56, 62, 67, 71, 82
- liquid argon time-projection chamber (LArTPC)** A class of detector technology that forms the basis for the DUNE far detector modules. It typically entails observation of ionization activity by electrical signals and of scintillation by optical signals. 86, 171
- liquid argon (LAr)** The liquid phase of argon. 90, 98, 114, 115, 214–219, 229, 230, 273
- long-baseline (LBL)** Refers to the distance between the neutrino source and the far detector. It can also refer to the distance between the near and far detectors. The “long” designation is an approximate and relative distinction. For DUNE, this distance (between Fermilab and SURF) is approximately 1300 km. 172
- Long-Baseline Neutrino Facility (LBNF)** The organizational entity responsible for developing the neutrino beam, the cryostats and cryogenics systems, and the conventional facilities for DUNE. 257, 259, 260, 262, 265–268, 270, 271, 275, 277, 278, 280, 281
- LED** Light-emitting diode. 166, 167, 235, 236, 251
- large electron multiplier (LEM)** A micro-pattern detector suitable for use in ultra-pure argon vapor; LEMs consist of copper-clad PCB boards with sub-millimeter-size holes through which electrons undergo amplification. 228, 264
- light readout (LRO)** The system for detecting scintillation photons in a DP detector module. 172, 182, 187
- LVDS** low-voltage differential signaling. 54, 61
- LV** low voltage. 45, 47, 62–67, 71, 76, 84, 221
- Monte Carlo (MC)** Refers to a method of numerical integration that entails the statistical sampling of the integrand function. Forms the basis for some types of detector and physics simulations. 125–127, 133

- minimum ionizing particle (MIP)** Refers to a momentum traversing some medium such that the particle is losing near the minimum amount of energy per distance traversed. 11–13
- module trigger logic (MTL)** Trigger processing that consumes detector unit level trigger command information and emits trigger commands. It provides the external trigger logic (ETL) with trigger notifications and receives back any external trigger candidates. 177, 180, 182, 183, 185–193, 292, 298
- near detector (ND)** Refers to the detector(s) installed close to the neutrino source at Fermilab. 256, 257
- online monitoring (OM)** Processes that run inside the DAQ on data “in flight,” specifically before landing on the offline disk buffer, and that provide feedback on the operation of the DAQ itself and the general health of the data it is marshalling. 180, 199
- operational readiness review (ORR)** A project management device by which the operational readiness is reviewed. 265
- ProtoDUNE-DP** The DP ProtoDUNE detector. 117, 217, 218, 273
- preliminary design review (PDR)** A project management device by which an early design is reviewed. 265
- ProtoDUNE-SP** The SP ProtoDUNE detector. 9, 11, 15, 16, 18, 19, 21, 23, 25, 27–29, 31, 32, 34, 35, 39, 41–43, 47, 48, 50–54, 58, 60, 63–65, 67, 69–76, 78, 81–83, 88, 93, 94, 96–98, 100, 106, 107, 109, 111–113, 116–118, 124–129, 134, 135, 137–142, 145–153, 156, 157, 161, 165–167, 170, 193, 194, 201, 211–213, 218, 223, 224, 226–228, 249, 273, 288
- photon detection system (PDS)** The detector subsystem sensitive to light produced in the LAr. 4–7, 16, 23, 25, 26, 36, 45, 50, 61, 68, 71, 72, 74, 78, 79, 86, 120–123, 128, 129, 131, 134, 140, 141, 146, 158, 159, 162, 164–166, 168–171, 176, 193, 199, 221, 235, 242, 256, 268, 283
- photon detector (PD)** Refers to the detector elements involved in measurement of number and arrival times of optical photons produced in a detector module. 3, 6, 8, 15, 16, 25, 36, 46, 48, 50, 72, 74, 120, 123, 124, 126–129, 131, 134, 136, 139–142, 144–148, 151–168, 170, 173, 181, 241, 242, 276, 278, 283, 286
- photomultiplier tube (PMT)** A device that makes use of the photoelectric effect to produce an electrical signal from the arrival of optical photons. 127
- parts per billion (ppb)** A number equal to 10^{-9} . 218
- production progress review (PPR)** A project management device by which the progress of production is reviewed. 265–267
- one-pulse-per-second signal (1PPS signal)** An electrical signal with a fast rise time and that arrives in real time with a precise period of one second. 193, 195

- parts per trillion (ppt)** A number equal to 10^{-12} . 3, 218
- ProtoDUNE** Either of the two DUNE prototype detectors constructed at CERN and operated in a CERN test beam (expected fall 2018). One prototype implements SP and the other DP technology. 117, 171, 188, 207, 216, 217, 221, 222, 233, 253, 262, 264, 286, 289
- production readiness review (PRR)** A project management device by which the production readiness is reviewed. 265–267, 280
- power and timing cards (PTC)** Cards that provide further processing and distribution of the signals entering and exiting the SP cryostat. 47, 63–65, 67, 70, 72, 74, 76
- QAM** quality assurance manager. 266, 272
- QAP** quality assurance plan. 265
- quality assurance (QA)** The process by which quality is maintained so as to preserve high availability and precise function. 34, 39, 41, 70, 165, 166, 168, 170, 201, 203, 251, 259, 264–266, 270, 272, 278
- quality control (QC)** A system of maintaining quality through testing products against a specification. 35, 36, 39, 76, 82, 111, 115, 116, 118, 165–168, 201, 203, 248–251, 262, 264–266, 270
- DAQ event block** The unit of data output by the DAQ. It contains trigger and detector data spanning a unique, contiguous time period and a subset of the detector channels.. 176, 182, 188, 189
- reconfigurable computing element (RCE)** Data processor located outside of the cryostat on a Cluster On Board (COB) which contains field programmable gate array (FPGA), RAM and SSD resources, responsible for buffering data, producing trigger primitives, responding to triggered requests for data and sinking SNB dumps. 182, 183, 185–187, 195, 205
- run control (RC)** The system for configuring, starting and terminating the DAQ. 192
- readout window** A fixed, atomic and continuous period of time over which data from a detector module, in whole or in part, is recorded. This period may differ based on the trigger that initiated the readout. 190, 192, 193
- radio frequency (RF)** Electromagnetic emissions that are within the (radio) frequency band of sensitivity of the detector electronics. 187
- RTD** Cryostat level and temperature monitoring devices. 228
- S/N** signal-to-noise (ratio). 90, 127, 199, 260
- SAR** successive approximation register. 60, 61

- SAS** A pass-through chamber used to ensure safe transfer of materials, avoiding contamination in both directions. 283, 284
- SBN** Short-Baseline Neutrino program (at Fermilab). 177
- silicon photomultiplier (SiPM)** A solid-state avalanche photodiode sensitive to single photoelectron signals. 7, 123–127, 129, 131–148, 155, 156, 159, 166–169, 199
- spill location system (SLS)** A system residing at the DUNE far detector site that provides information, possibly predictive, indicating periods of time when neutrinos are being produced by the Fermilab Main Injector beam spills. 196
- supernova neutrino burst (SNB)** A prompt increase in the flux of low-energy neutrinos emitted in the first few seconds of a core-collapse supernova. It can also refer to a trigger command type that may be due to an SNB, or detector conditions that mimic its interaction signature. 7, 120, 121, 126, 128–131, 141, 171–177, 179, 181–185, 187–193, 200, 222, 291, 296
- SuperNova Early Warning System (SNEWS)** A global supernova neutrino burst trigger formed by a coincidence of SNB triggers collected from participating experiments. 190, 192, 200, 201
- SP module** single-phase detector module. 2–6, 8, 9, 12, 13, 16, 23, 27, 28, 42–45, 47, 51, 54, 58, 60–65, 67, 69–72, 77, 78, 81, 83, 84, 87, 91–93, 95, 98, 106, 112, 114, 116–118, 120, 122–124, 127, 131, 136, 137, 139, 140, 147–151, 158, 161, 164, 170, 178, 179, 185, 189, 190, 193, 198, 201, 204, 208, 215, 217, 219, 223, 228, 256, 273, 281, 283, 284, 286, 288
- single-phase (SP)** Distinguishes one of the DUNE far detector technologies by the fact that it operates using argon in its liquid phase only. 116–119, 172, 182, 183, 185, 187, 189, 190, 193, 194, 198, 199, 281, 289, 293
- solid-state disk (SSD)** Any storage device that may provide sufficient write throughput to receive, both collectively and distributed, the sustained full rate of data from a detector module for many seconds. 177, 182, 183, 185, 188, 189
- SSP** SiPM signal processor. 52, 129, 145, 146
- subdetector** A detector unit of granularity less than one detector module such as the TPC of either a SP or DP module. 181, 292
- SWC** Software & Computing. 242, 243
- TalBo** A cylindrical cryostat at Fermilab primarily used for developing scintillation light collection technologies for LArTPC detectors. 131, 134, 137
- temporary construction opening (TCO)** An opening in the side of a cryostat through which detector elements are brought into the cryostat; utilized during construction and installation. 36–38, 40, 79, 80, 85, 260, 273, 274, 283–286, 288

- technical coordination (TC)** A dedicated DUNE project effort responsible for assuring proper interfaces between the collaboration consortia. 202, 256, 257, 259–262, 264–266, 268–273, 275, 277, 279
- technical design report (TDR)** A formal project document that describes the experiment at a technical level. 12, 34, 43, 70, 71, 74, 82, 84, 117, 127, 128, 131, 144, 151, 161–163, 166, 169, 170, 208, 256, 262, 264, 266, 269–271, 275, 286, 288, 298
- top field cage (top FC)** The horizontal portions of the SP FC on the top. 86, 91, 92, 98, 100, 101, 105–108, 111–115, 118
- tetra-phenyl butadiene (TPB)** A type of wavelength shifting material. 123, 125, 127, 131, 133, 134, 136–138, 140, 146, 161, 232
- time projection chamber (TPC)** The portion of each DUNE detector module that records ionization electrons after they drift away from a cathode through the LAr, and also through gaseous argon in a DP module. The activity is recorded by digitizing the waveforms of current induced on the anode as the distribution of ionization charge passes by or is collected on the electrode. 86, 90, 91, 98, 100, 102, 106, 113–115, 171, 217, 246
- interim design report (IDR)** An intermediate milestone on the path to a full technical design report (TDR). 131, 207
- trigger candidate** Summary information derived from the full data stream and representing a contribution toward forming a trigger decision. 176, 182, 183, 185–193, 298
- trigger command** Information derived from one or more trigger candidates that directs elements of the detector module to read out a portion of the data stream. 176, 182, 185, 188–190, 192, 193, 291–293, 295, 298
- trigger decision** The process by which trigger candidates are converted into trigger commands. 176, 178, 181, 185, 197, 291, 298
- trigger notification** Information provided by MTL to ETL about trigger decision its processing. 292, 295
- trigger primitive** Information derived by the DAQ front-end (FE) hardware that describes a region of space (e.g., one or several neighboring channels) and time (e.g., a contiguous set of ADC sample ticks) associated with some activity. 173, 176, 180, 182, 183, 186–191, 291
- underground installation team (UIT)** An organizational unit responsible for installation in the underground area at the SURF site. 160, 164, 279–281, 286, 288
- Micro Telecommunications Computing Architecture (μ TCA)** The computer architecture specification followed by the crates that house charge and light readout electronics in the dual-phase module. 67, 193–195, 289

VUV vacuum ultra-violet. 122–125, 127, 131, 137–141

WA105 DP demonstrator The $3 \times 1 \times 1 \text{ m}^3$ WA105 dual-phase prototype detector at CERN. 228, 231, 233

work breakdown structure (WBS) An organizational project management tool by which the tasks to be performed are partitioned in a hierarchical manner. 83, 84, 168, 262, 266

warm interface board (WIB) Digital electronics situated just outside the SP cryostat that receives digital data from the FEMBs over cold copper connections and sends it to the RCE FE readout hardware. 47, 61–67, 69, 70, 72, 74, 76, 79, 85, 172, 183, 185, 186, 193, 198, 204, 205

warm interface electronics crate (WIEC) Crates mounted on the signal flanges that contain the warm interface boards. 47, 63, 67, 69, 70, 72, 76, 79

wavelength shifting (WLS) A material or process by which incident photons are absorbed by a material and photons are emitted at a different, typically longer, wavelength. 160, 161

White Rabbit (WR) A component of the timing system that forwards clock signal and time-of-day reference data to the master timing unit. 193, 194

zero-suppression (ZS) Used to delete some portion of a data stream that does not significantly deviate from zero or intrinsic noise levels. It may be applied at different granularity from per-channel to per detector unit. 191

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- CaltechNRAO, LIGO Scientific, High Time Resolution Universe Survey, Nordic Optical Telescope, Las Cumbres Observatory Group, TZAC Consortium, LOFAR, IPN, DLT40, Texas Tech University, HAWC, ANTARES, KU, Dark Energy Camera GW-EM, CALET, Euro VLBI Team, ALMA Collaboration, B. P. Abbott *et al.*, “Multi-messenger Observations of a Binary Neutron Star Merger,” *Astrophys. J.* **848** no. 2, (2017) L12, arXiv:1710.05833 [astro-ph.HE].
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