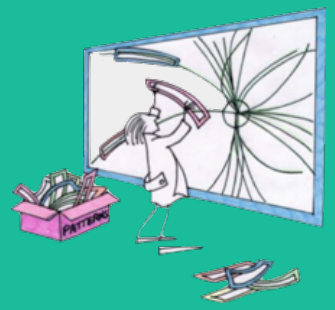

ATLAS Hardware Based Track-Finding: Present and Future

Todd Seiss

On behalf of the ATLAS Collaboration
for Computing in High Energy Physics 2018

Outline

- **Introduction**
  - ATLAS
  - The ATLAS Trigger
  - Tracking in ATLAS
- **Hardware Tracking**
  - Overview
  - Algorithm
- **Current and Future Systems**
  - The Fast TracKer (FTK)
  - Hardware Tracking for the Trigger (HTT)
- **Conclusion & outlook**

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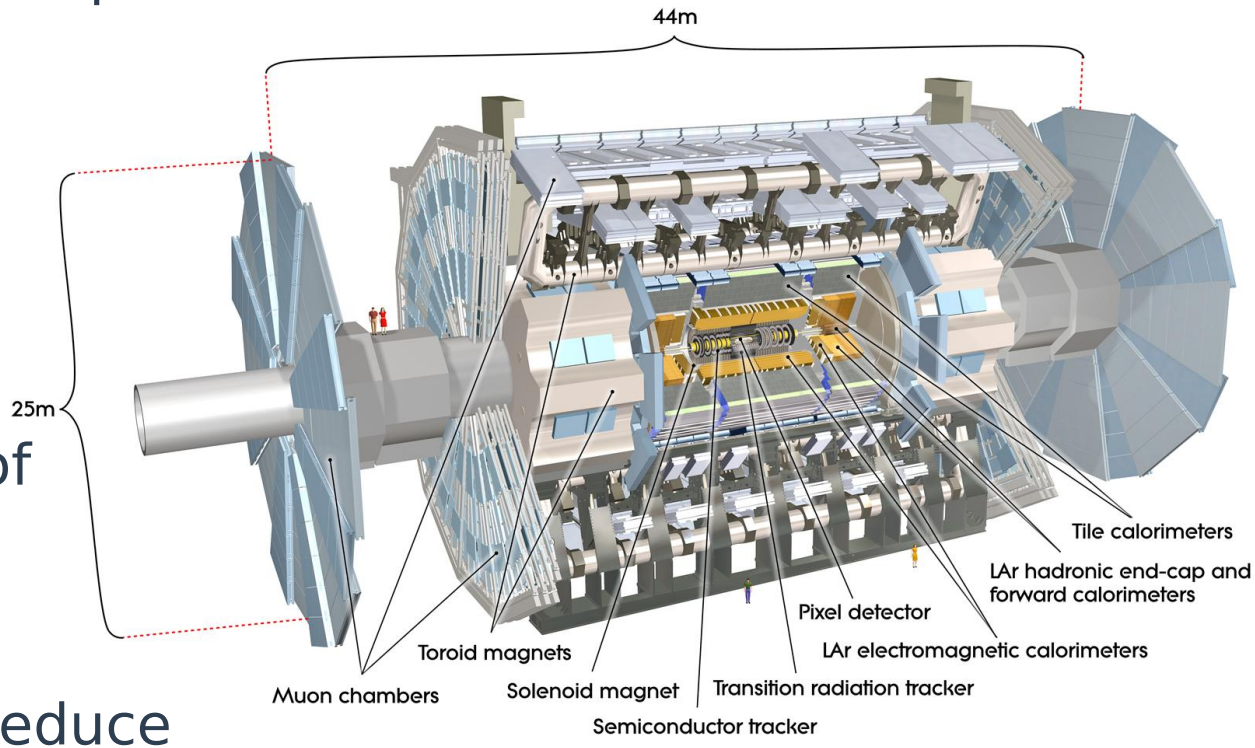
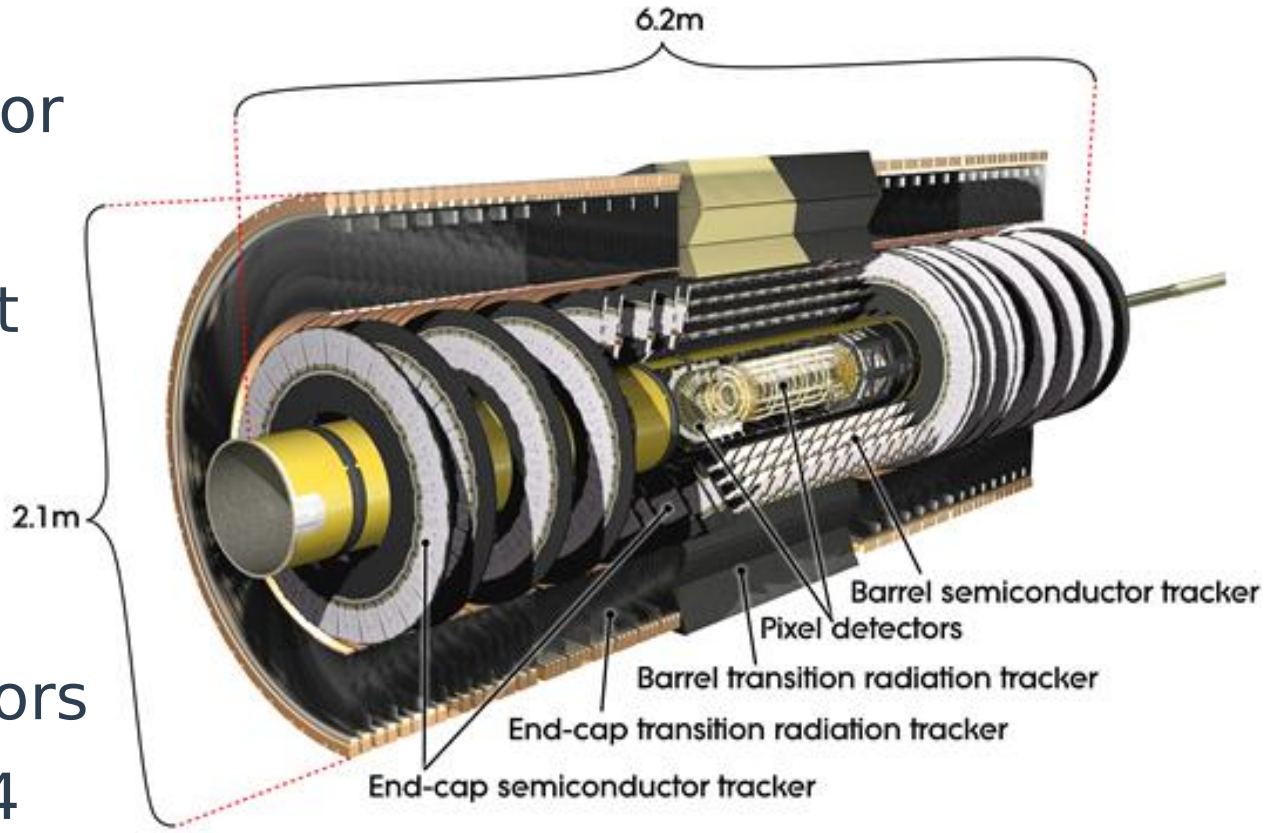
The ATLAS Detector: Key Components

- **ATLAS**
  - General purpose, multi-layer detector to measure tracks and energy depositions from particles in LHC collisions
- **Inner Silicon Detector**
  - The innermost layers of ATLAS, used for tracking
  - Concentric cylinders of silicon detectors
- **Trigger**
  - Multi-level trigger to reduce event rate from 40 MHz to 1.5 kHz



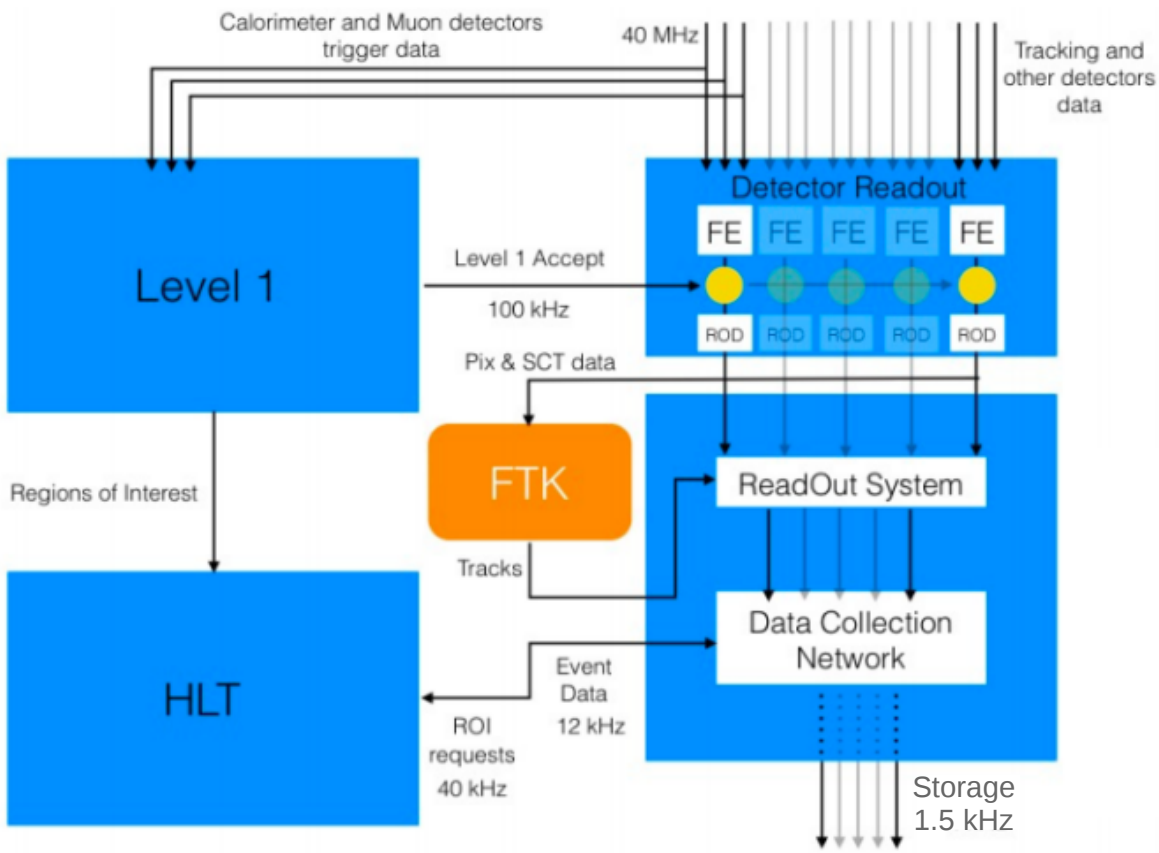
The ATLAS Silicon Layers

- **Pixel**
  - Silicon pixel detector
  - 4 layers in barrel
  - r, phi, z for each hit
- **SCT (Semiconductor Tracker)**
  - Silicon strip detectors
  - 8 layers in barrel (4 stereo layers)
  - r, phi for each layer



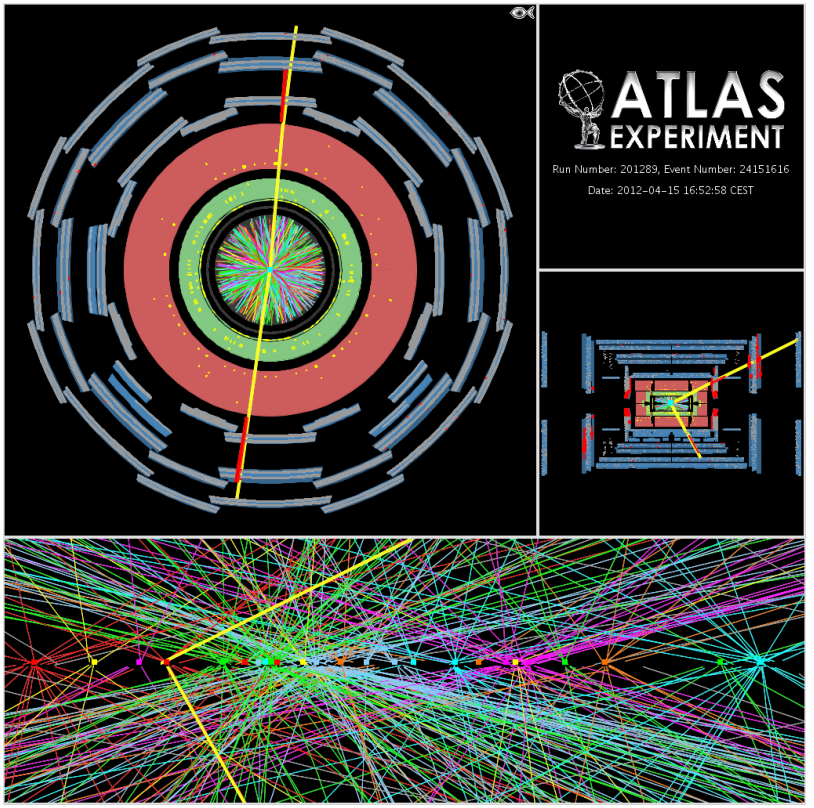
The ATLAS Trigger

- **40 MHz input → 1.5 kHz output**
- **Level 1:**
  - Mostly hardware, simple algorithms, fast decisions
- **High-Level Trigger (HLT)**
  - Mostly software, more complex algorithms, slower decisions



Tracking: Current Status

- **Need to connect-the-dots for the silicon hits**
- **Done in HLT farm, but computationally expensive**
  - 100-1000 hits/layer. Brute force is exponentially complex
  - O(10-100 ms) for just single region-of-interest tracking
  - Cannot do full tracking => Would be O(1 sec/event)
- **Have to make stringent decisions on what to track**
  - Forces high p_T for objects so tracking rate is low enough
  - b-jet tracking is still enormous CPU usage



Pileup 25 Z→μμ in data

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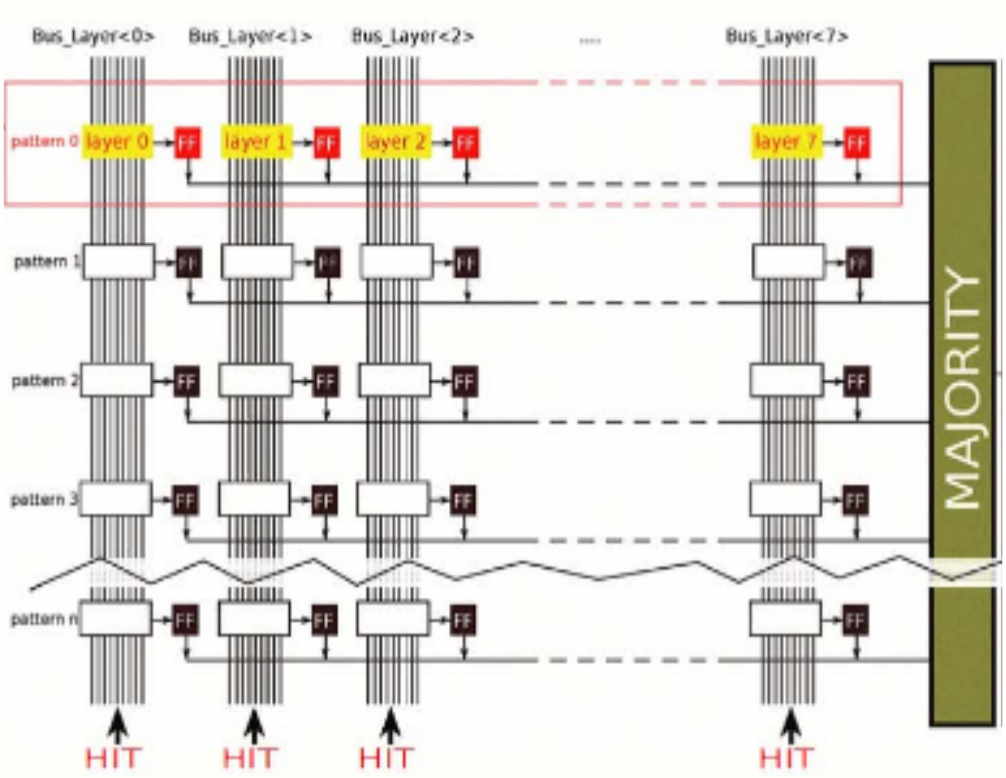
Hardware Based Track Finding

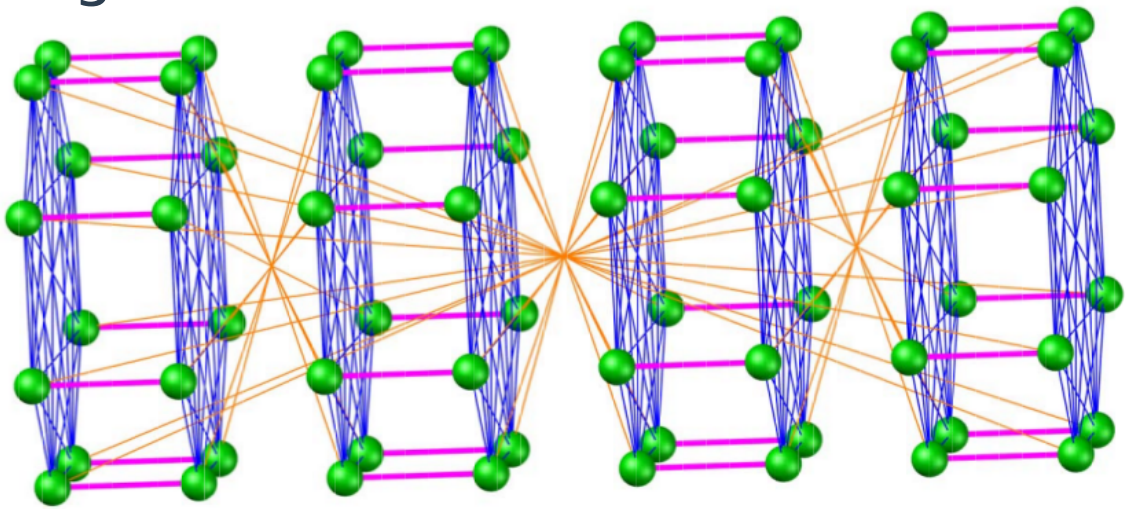
- **Goal: Have tracks for HLT, freeing CPU usage**
- **ASICs**
  - Pattern recognition with Associative Memory
  - Simultaneously compare inputs to all patterns in chip memory
- **FPGAs**
  - Highly parallel tracking based on the patterns
- **O(100 µs) latency for full tracking**
  - 10^4 times faster than CPU!



Associative Memory ASIC

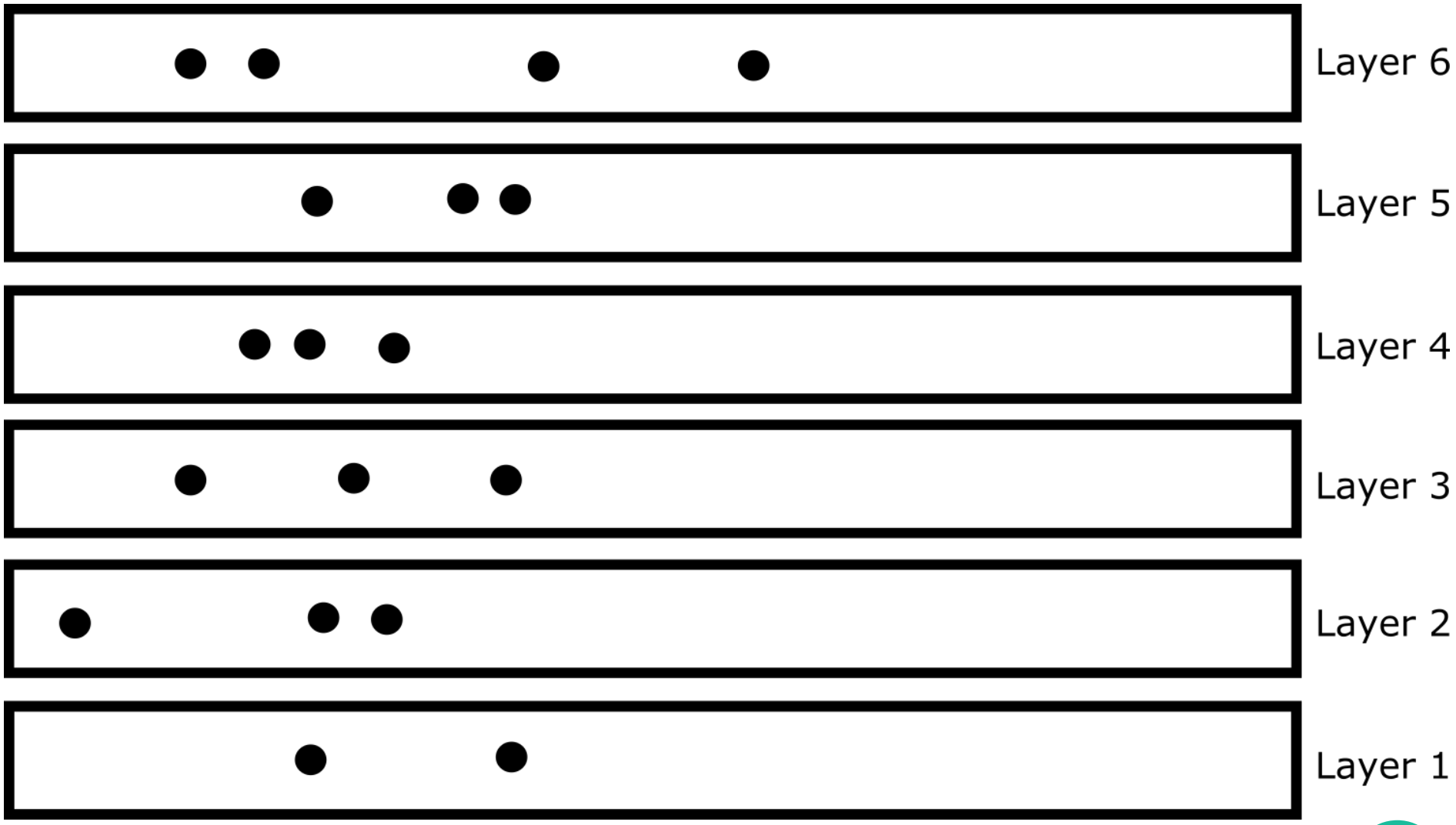
Hardware Tracking: Preprocessing

- **Cluster raw hits**
  - Sliding window clustering
- **Route Clusters into tracking regions**
  - Inner detector is divided into independent parallel tracking regions

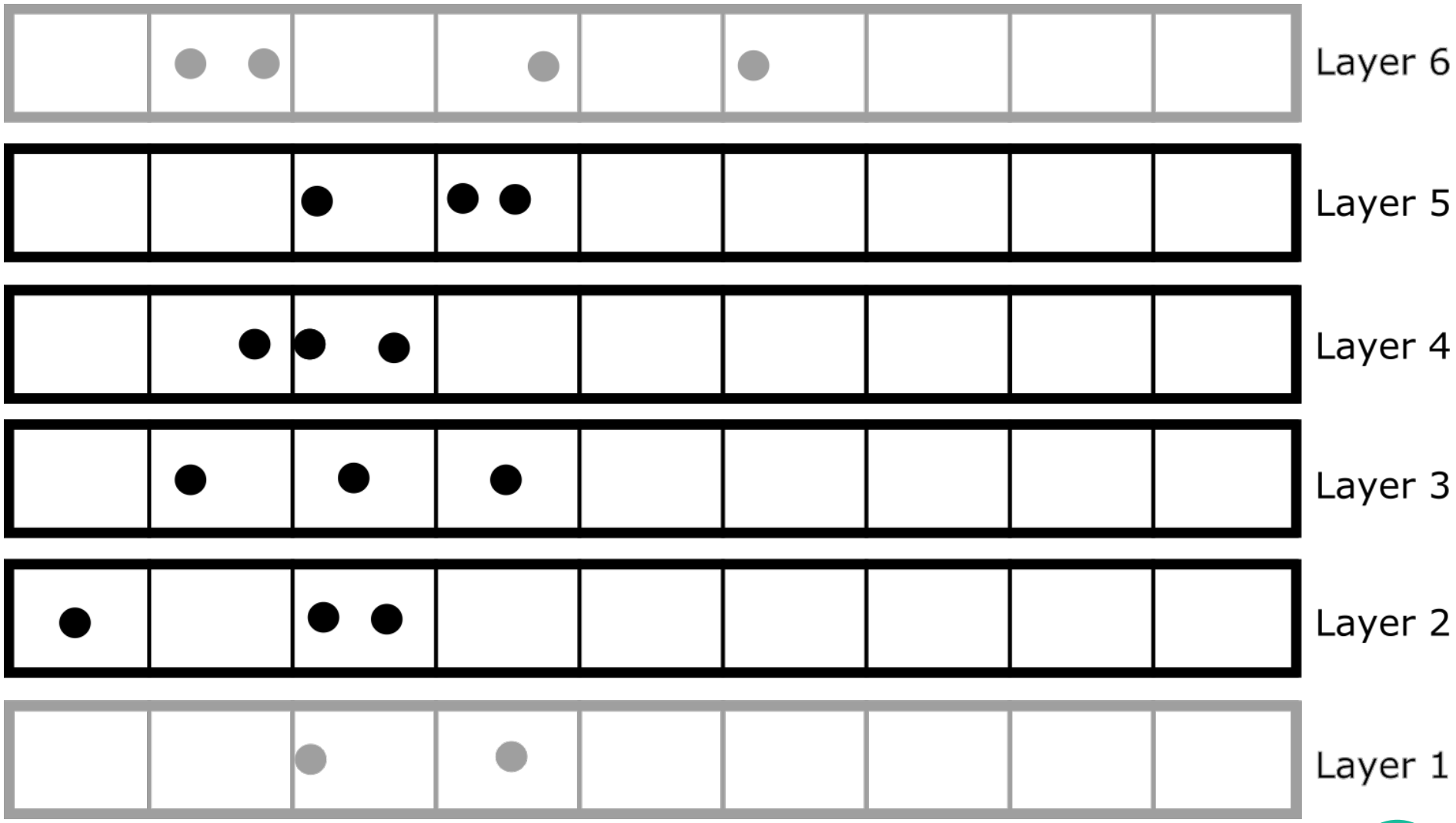


FTK routing network

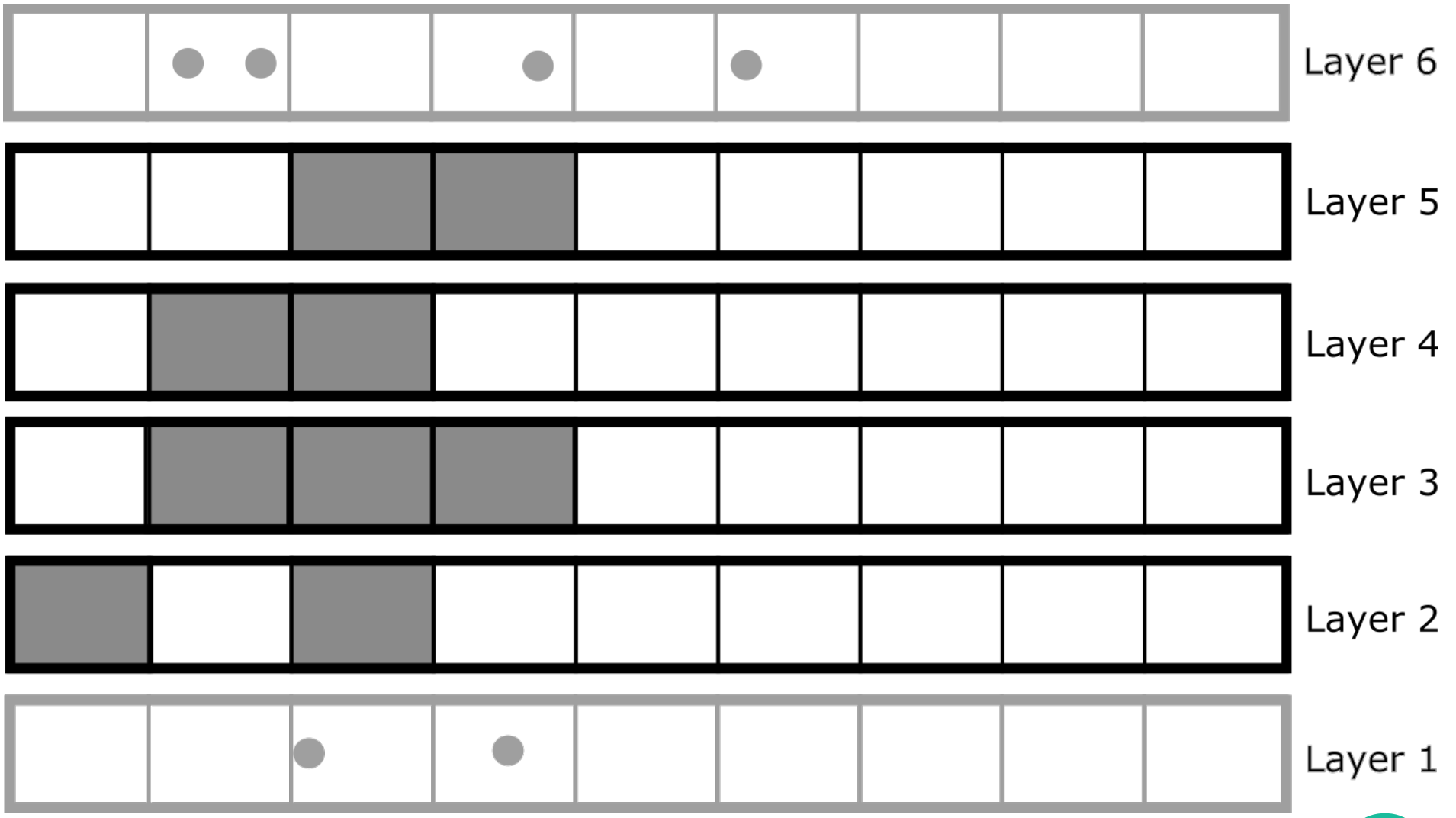
Input Clusters



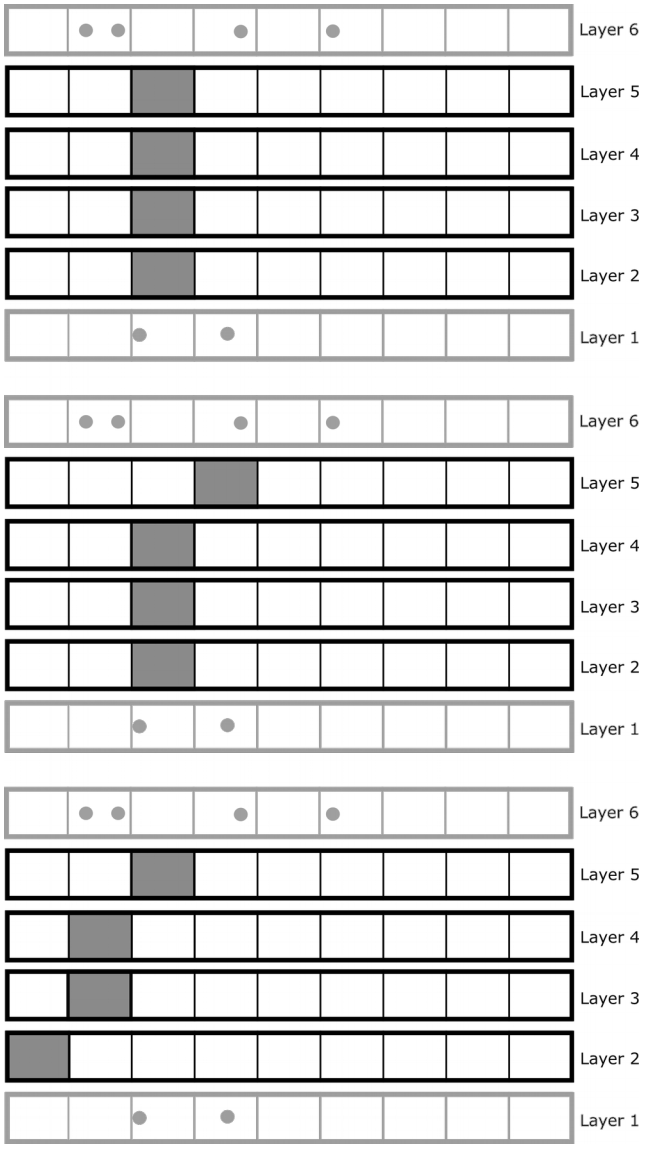
Define superstrips (coarser resolution)



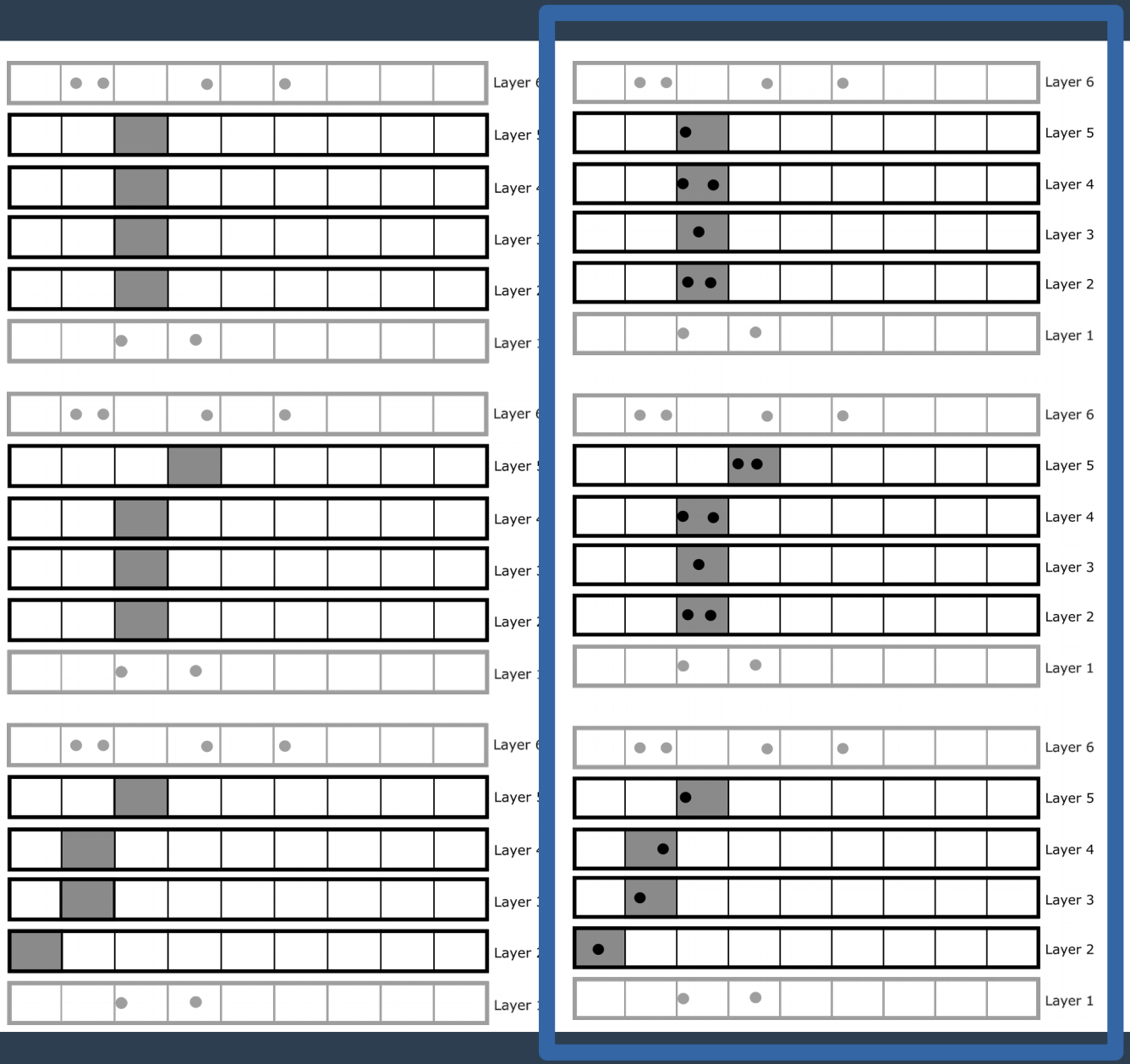
Look up superstrips for each cluster in first-stage layers



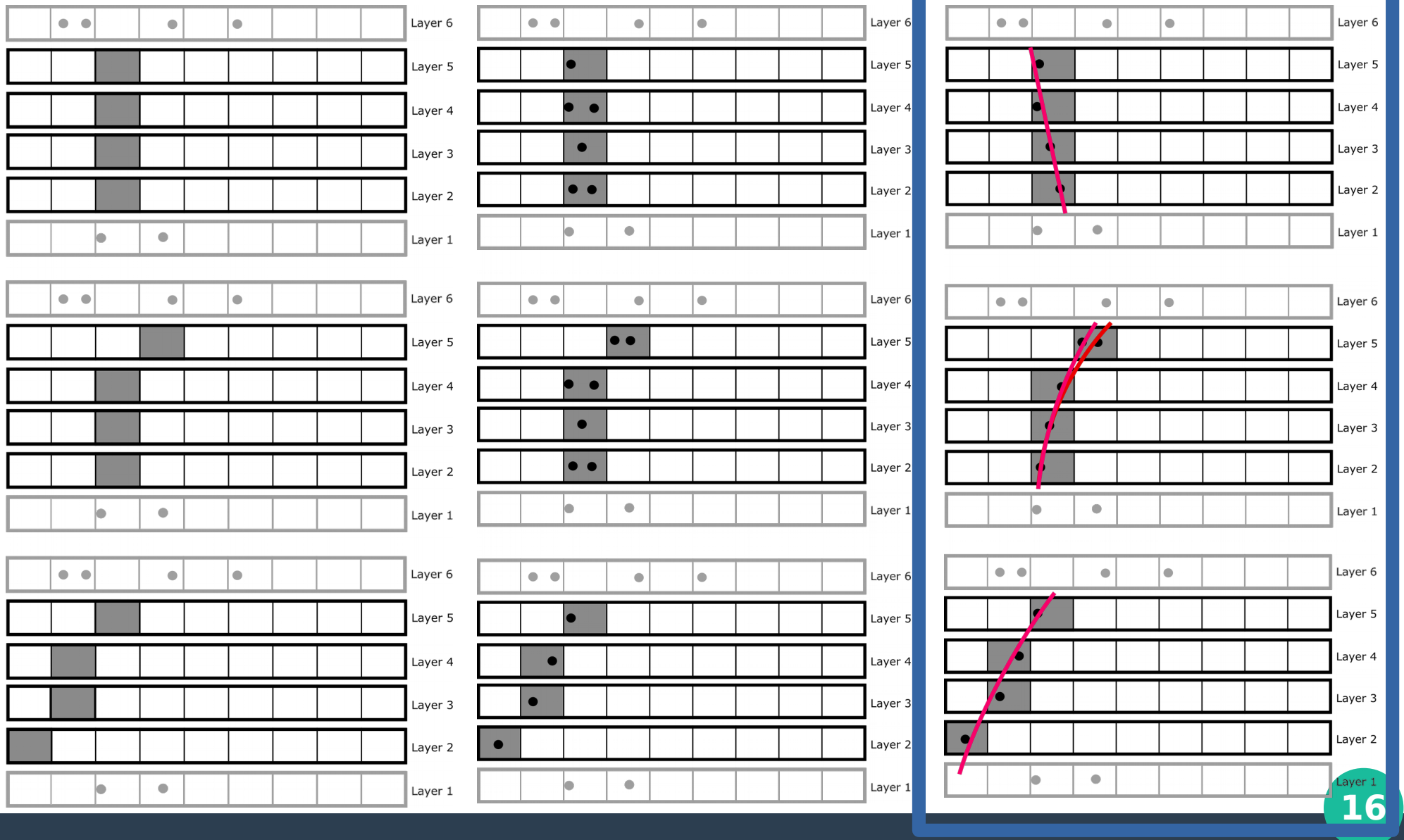
Pattern matching for superstrips



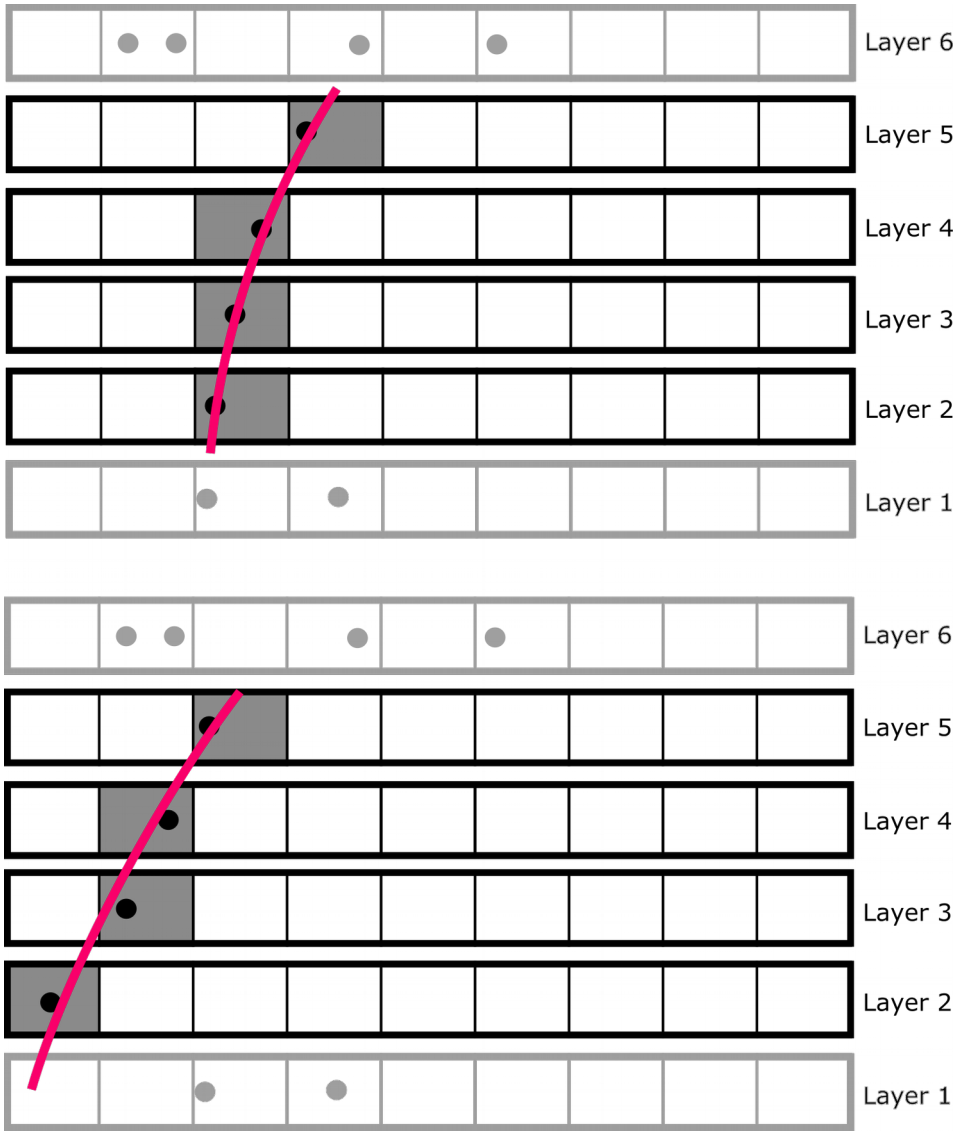
Get full resolution clusters in superstrips



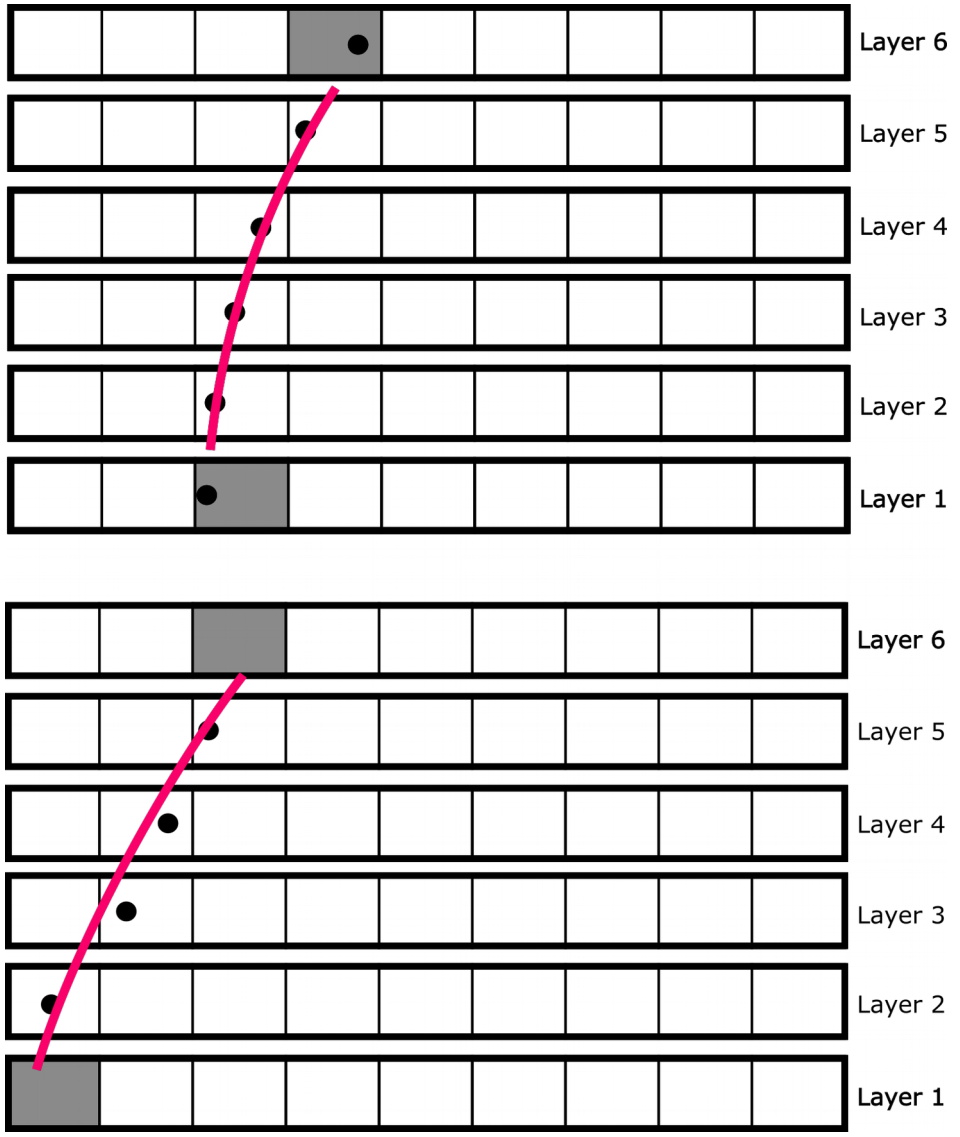
Fit all possible combinations of clusters (i.e., compute χ^2)



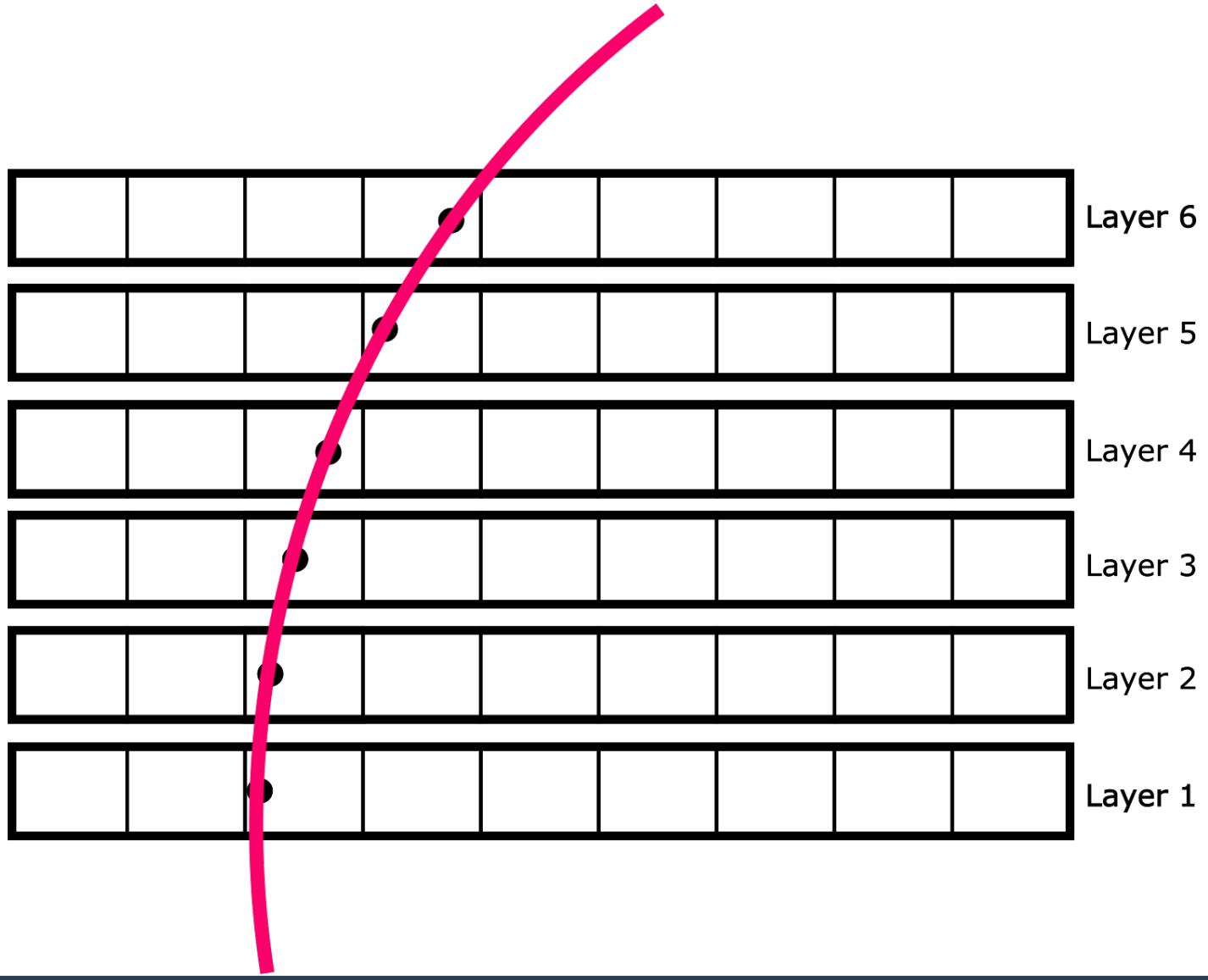
Cut on chi-squared and remove duplicates



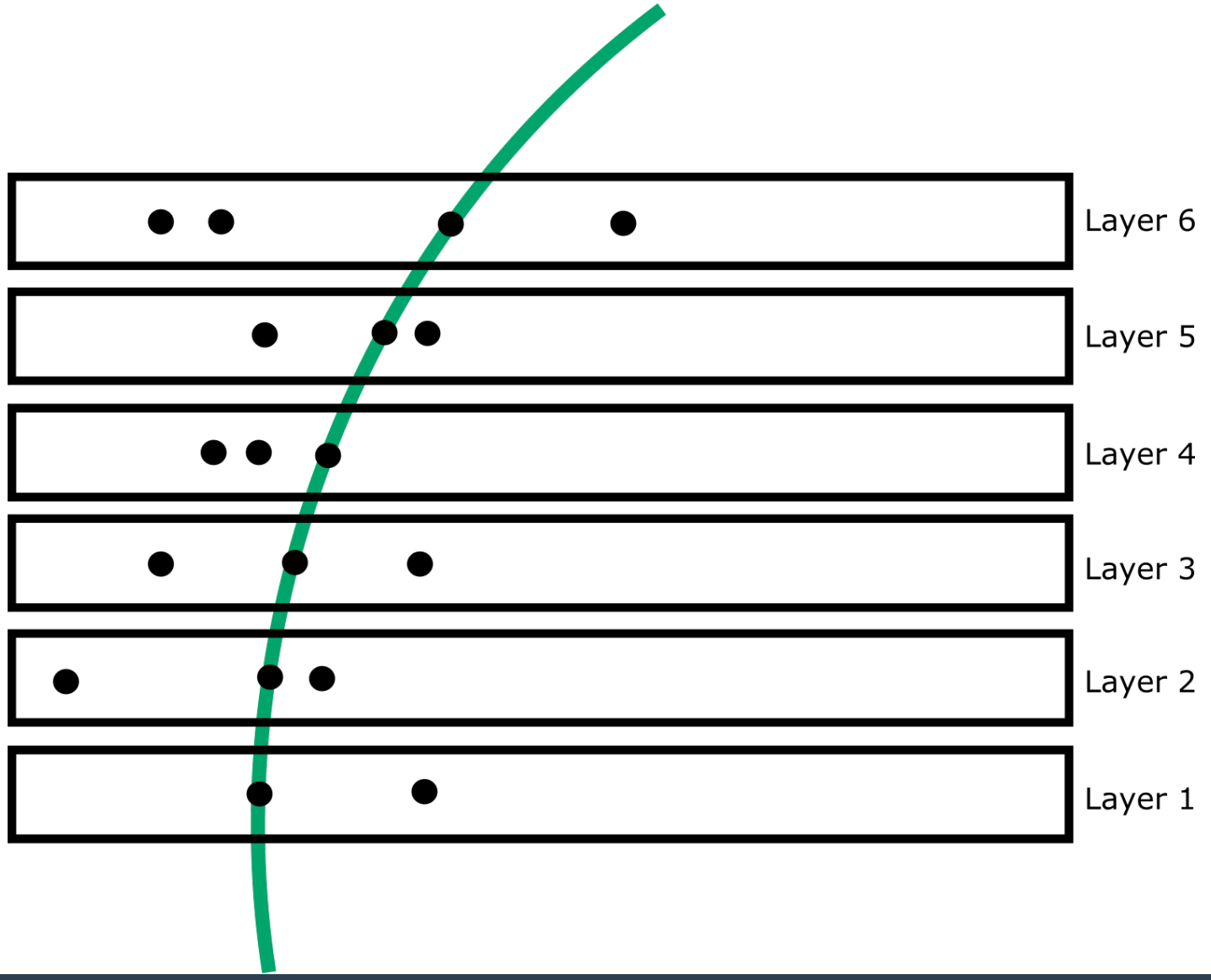
Extrapolate to superstrips in remaining layers



Compute full χ^2, make cuts



Compute track parameters



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The Fast TracKer (FTK)

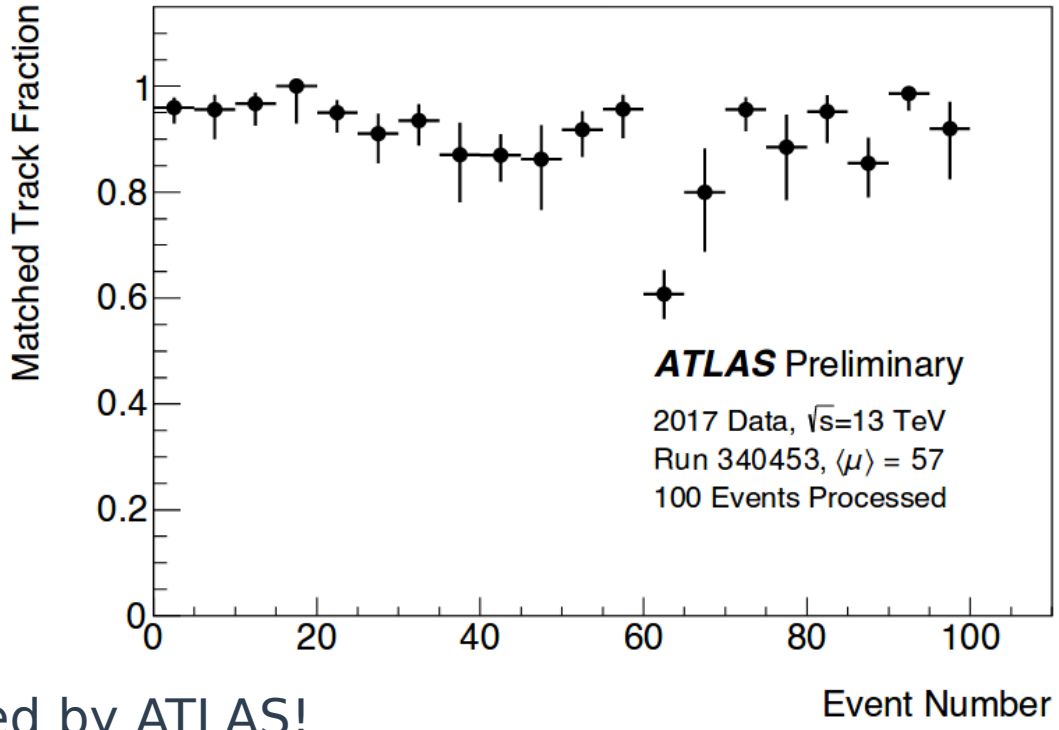
- **For use in LHC Run 3 (2021-2023)**
- **Provide full tracking for every event passing level-1 trigger**
- **Under commissioning**
  - "Slice"-based testing: Slice = 1 copy of each board
  - Slice works under ideal conditions, learning real ATLAS data conditions
- **Complex, heterogeneous system**

FTK Hardware

Sets of Firmware	15
FPGAs	1455
Boards	450
Associative Memory Chips	8192
Total Patterns	1 billion
Event Rate	100 kHz

FTK: Commissioning

- **Majority of boards at CERN**
- **Priorities**
  - Stable slice processing & live error handling
  - Writing and validating tracks while running with ATLAS
  - Firmware/software/hardware for scaling up
- **Successes**
  - Real FTK tracks have been recorded by ATLAS!
- **See Simone's slides for the challenge of controlling and monitoring FTK**



Hardware Tracking for the Trigger (HTT)

- **For use with HL-LHC (~2026-2038)**
- **Massive co-processor to CPU farm, tracking on request**
- **Regional and global tracking with same hardware**
  - Regional: 10% of detector; first stage tracking
  - Global: Full detector; full second-stage tracking
- **In design phase**
  - Defining technical specifications
- **Simpler, more homogeneous system – applying FTK experience**

HTT Hardware

Sets of Firmware	~5
FPGAs	~3000
Boards	2040
Associative Memory Chips	13824
Total Patterns	5.3 billion
Event Rate	1 MHz regional 100 kHz global

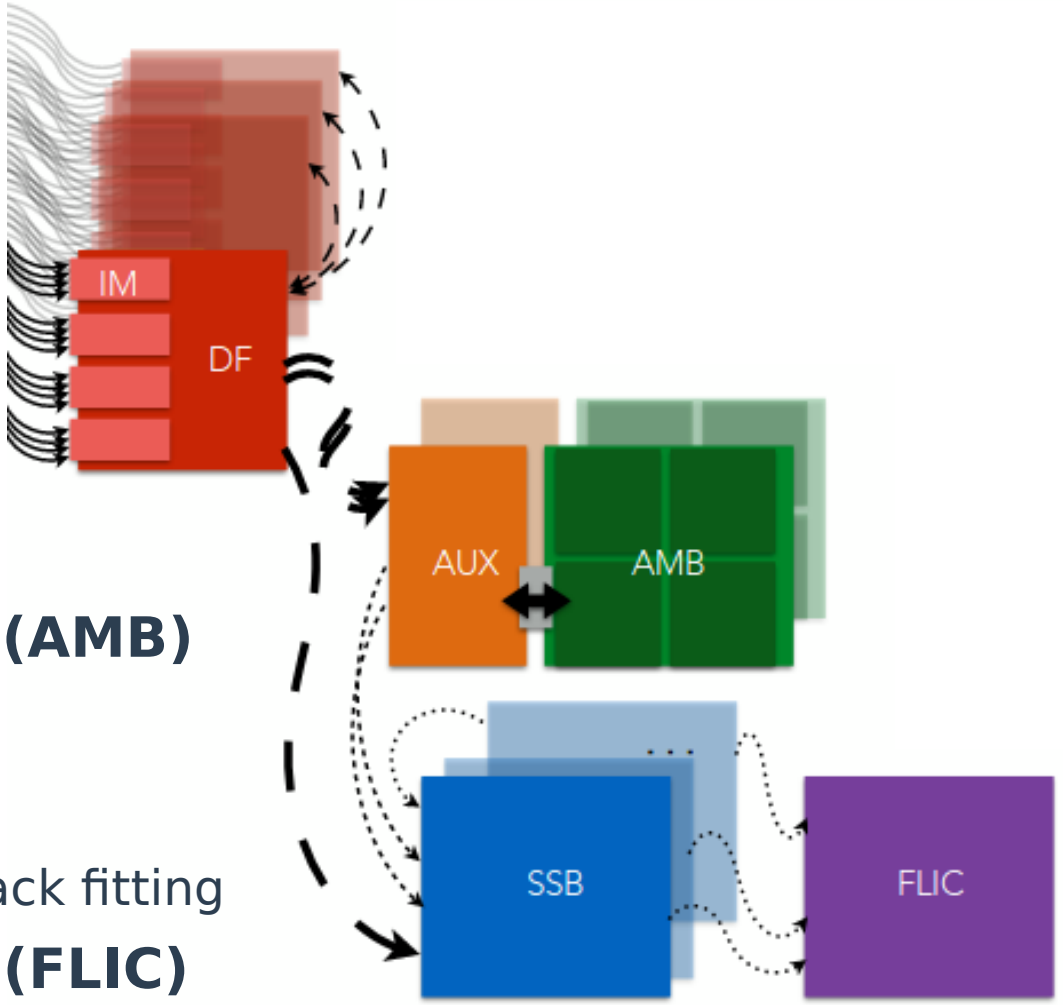
Conclusion & Outlook

- **Hardware tracking is difficult and ambitious technology**
  - Algorithms are not simple
  - Implemented entirely on FPGAs & ASICs
- **FTK under commissioning; HTT in design, will improve on FTK**
- **Physics goals of ATLAS will benefit hugely from hardware tracking**
  - Significant improvement in performance of b-jets, taus, MET, pileup suppression, lepton isolation, etc.
- **Thank you to the FTK and HTT teams!**

BACKUP

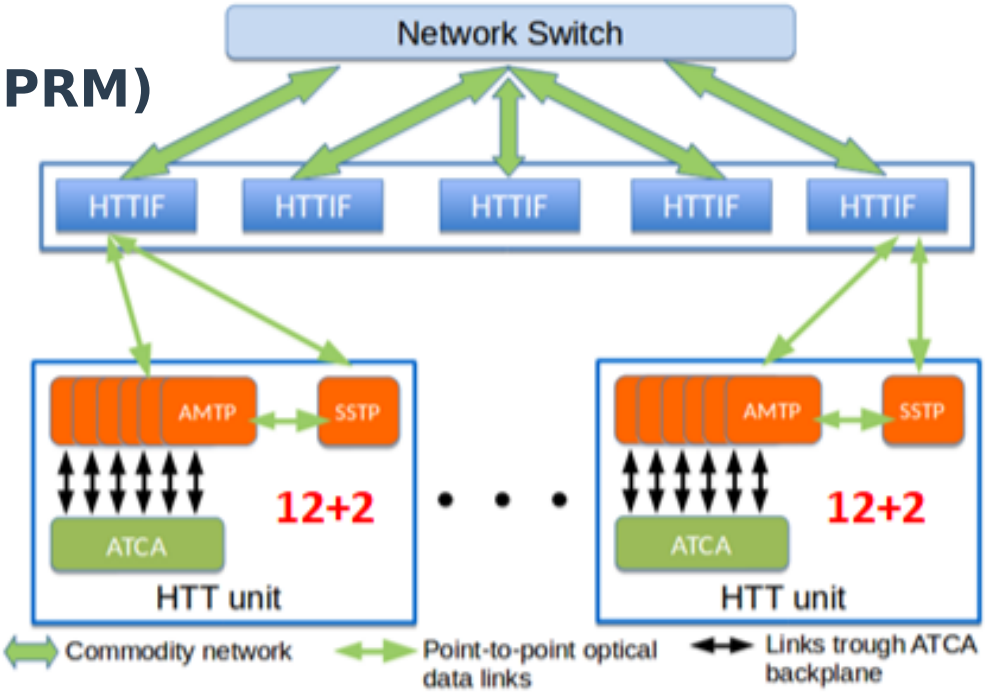
FTK: Architecture

- **Input Mezzanine (IM)**
  - Hit clustering
- **DataFormatter (DF)**
  - Cluster routing
- **Auxilliary Card (AUX)**
  - Superstrip lookup
  - First stage track fitting
- **Associative Memory Board (AMB)**
  - Pattern matching
- **Second Stage Board (SSB)**
  - Extrapolation & second-stage track fitting
- **FTK Level-2 Interface Card (FLIC)**
  - Global coordinate lookup



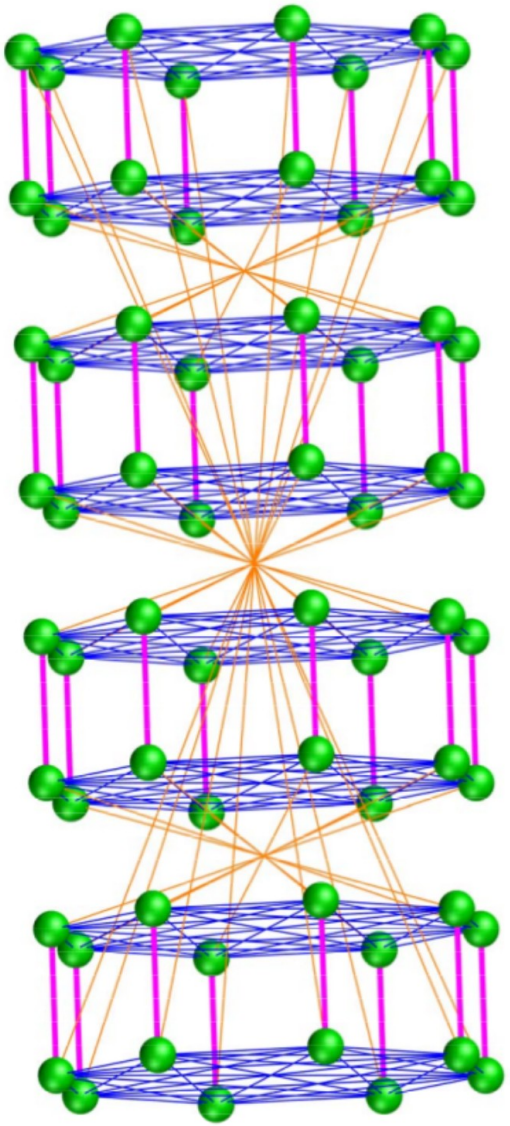
HTT: Architecture

- **Pattern Recognition Mezzanine (PRM)**
  - 24 AM chips + 1 FPGA
  - Pattern matching and first stage fitting
- **Track Fitting Mezzanine (TFM)**
  - 1 FPGA for Extrapolation and second-stage fitting
- **Track Processor (TP) Board**
  - Common hardware to hold either 2 PRMs or 2 TFMs
  - Associative Memory TP (AMTP): Holds PRMs
  - Second Stage TP (SSTP): Holds TFM
  - Does clustering, data-sharing, track duplicate removal
- **HTT Interface (HTTIF)**
  - Interfaces with CPU farm network
  - Routes hits into correct HTT unit and routes tracks out



Hardware Tracking: Algorithm

1) **Cluster raw hits**
   - Sliding window clustering
2) **Route Clusters into tracking regions**
   - Inner detector is divided into independent parallel tracking regions
3) **Reduce Resolution of clusters**
   - Needed for pattern matching



Hardware Tracking: Algorithm

4) Pattern Match with Reduced-Resolution Clusters

- Use Associative Memory ASICs

5) First-Stage Tracking (subset of tracking layers)

1) Restore Resolution
2) Compute χ^2 for all combinations of one hit per layer in each pattern; cut on χ^2

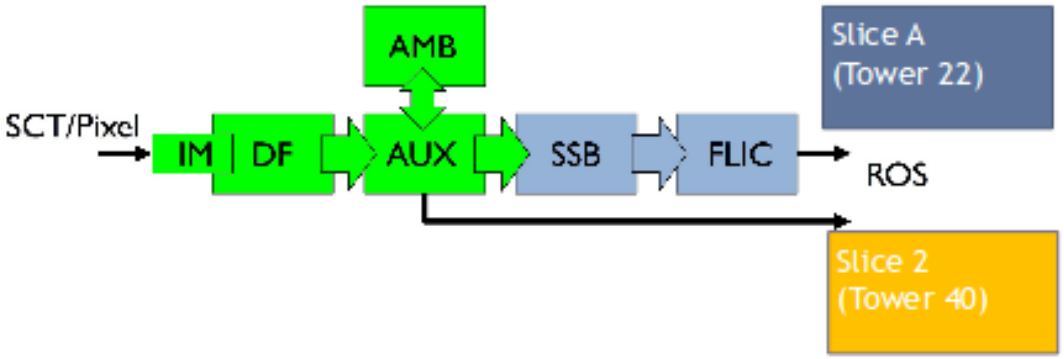
    Linearized computation (Taylor expansion in track parameter phase space)

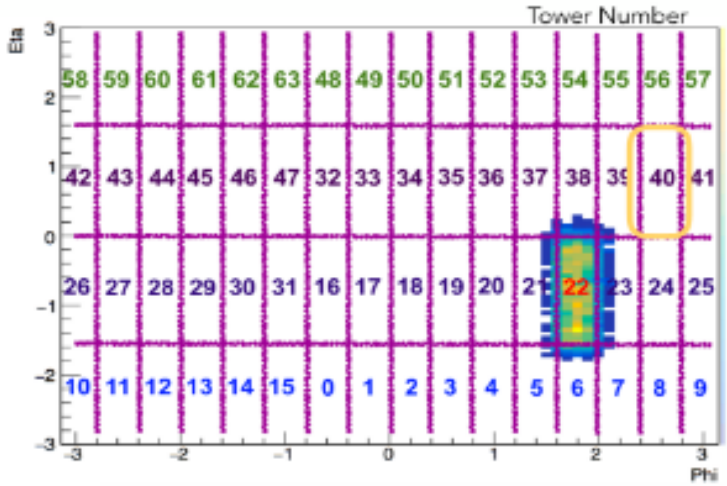
6) Second-Stage Tracking (all tracking layers)

1) Extrapolate first-stage tracks
2) Compute χ^2s for all combinations of one hit per layer in each extrapolation; cut on χ^2
3) Compute track parameters (linearized computation)

FTK Commissioning

- FTK commissioning focused on two slices:
  - Slice A: full slice including all boards
    - outputs 12-layer tracks
  - Slice 2: reduced slice outputting directly from AUX to ROS
    - outputs 8-layer tracks
    - used for commissioning upstream boards in environments for which downstream boards are undergoing debugging
- Inputs to both slices are chosen to have coverage over a small eta/phi range



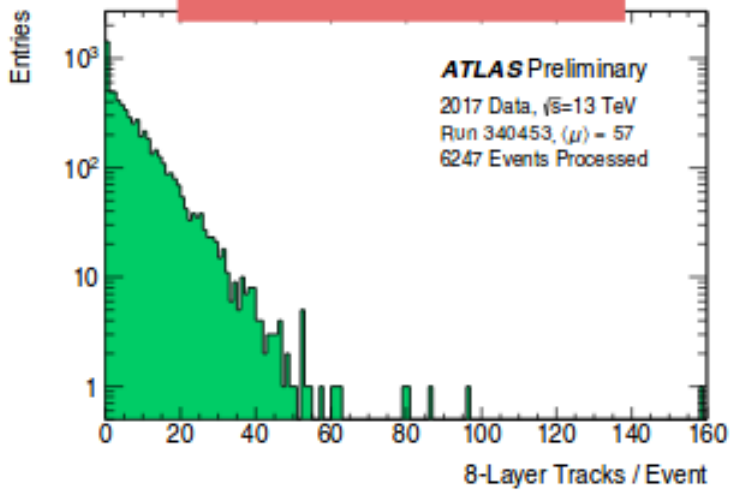


Slide from Tova Holmes

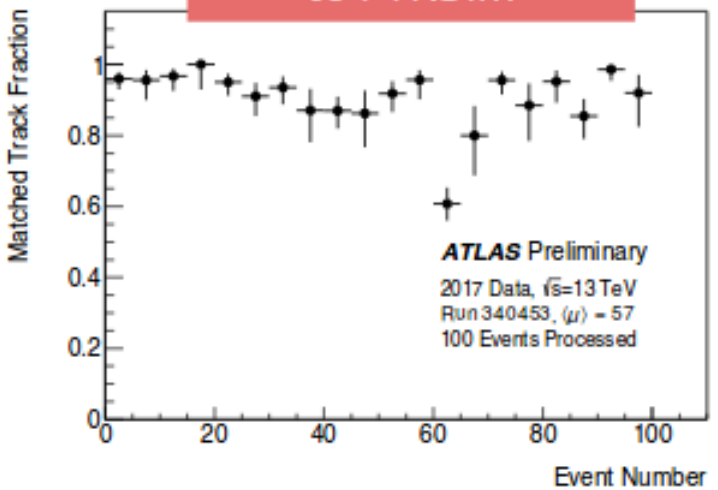
FTK Commissioning

- At the end of 2017, Slice 2 was incorporated into ATLAS
  - included during the 5 TeV runs (low mu), and ran for over 7 hours
- Slice 2 spied on ATLAS 13 TeV data (high mu)
  - ran for ~1s at a time before stopping due to track fitter bug (now fixed)
  - validated 8-layer data output with FTK functional simulation

n tracks



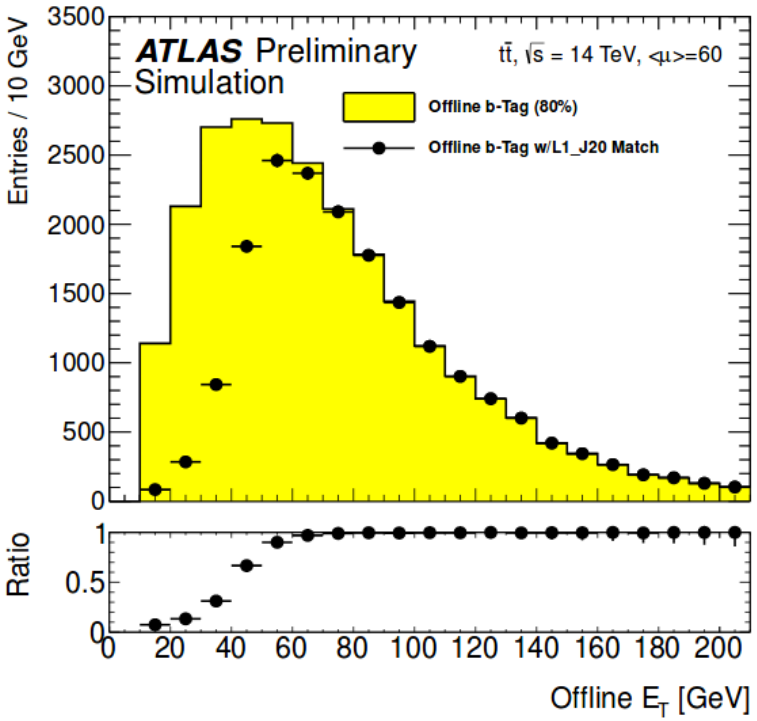
fraction matched to FTKSim

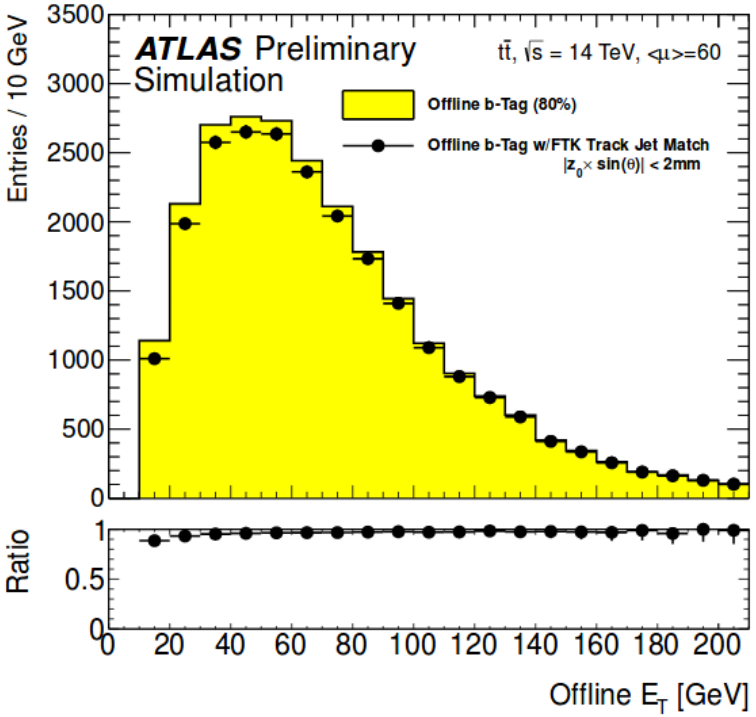


Slide from Tova Holmes

FTK b-jet Performance Gain

- **Much higher online b-jet efficiency at low pT**





Plots from John Alison, FTK Simulation