Trigger and Timing Distributions using the TTC-PON and GBT Bridge Connection in ALICE for the LHC Run 3 Upgrade

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Abstract

The ALICE experiment at CERN is preparing for a major upgrade for the third phase of data taking run (Run 3), when the high luminosity phase of the Large Hadron Collider (LHC) starts. The increase in the beam luminosity will result in high interaction rate causing the data acquisition rate to exceed 3 TB/sec. In order to acquire data for all the events and to handle the increased data rate, a transition in the readout electronics architecture from the triggered to the trigger-less acquisition mode is required. In this new architecture, a dedicated electronics block called the Common Readout Unit (CRU) is defined to act as a nodal communication point for detector data aggregation and as a distribution point for timing, trigger and control (TTC) information. TTC information in the upgraded triggerless readout architecture uses two asynchronous high-speed serial links connections: the TTC-PON and the GBT. We have carried out a study to evaluate the quality of the embedded timing signals forwarded by the CRU to the connected electronics using the TTC-PON and GBT bridge connection. We have used four performance metrics to characterize the communication bridge: (a) the latency added by the firmware logic, (b) the jitter cleaning effect of the PLL on the timing signal, (c) BER analysis for quantitative measurement of signal quality, and (d) the effect of optical transceivers parameter settings on the signal strength. Reliability study of the bridge connection in maintaining the phase consistency of timing signals is conducted by performing multiple iterations of power on/off cycle, firmware upgrade and reset assertion/de-assertion cycle (PFR cycle). The Intel[®] development kit having Arria[®] 10 FPGA is used for developing the first prototype of the CRU firmware. The test results are presented and discussed concerning the performance of the TTC-PON and GBT bridge communication chain using the CRU prototype and its compliance with the ALICE timing requirements.

1. Introduction

A Large Ion Collider Experiment (ALICE) at the CERN Large Hadron Collider (LHC) is designed to address the physics of strongly interacting matter and the quark-gluon plasma (QGP) at extreme conditions of temperatures and energy densities. By inclusive studies of proton-proton (pp), proton-lead (Pb) and lead-lead (PbPb) collisions at the LHC, ALICE aims to study the properties of QGP. ALICE has been acquiring data since the year 2009, and has achieved significant milestones and discoveries since then. An increase in the beam luminosity at the LHC will commence from the year of 2020s, which will extend the physics reach of the experiments. ALICE will fully exploit the scientific potential offered by this third phase of LHC data taking run (Run 3) by upgrading the major detector systems, associated electronics and data acquisition systems [1].

For Run 3 , the collision energy of pp will reach 14 TeV, with maximum instantaneous luminosity of $L = 5 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$. For PbPb collisions, the center of mass energy per nucleon pair, $\sqrt{s_{NN}}$ will be 5.5 TeV, at the instantaneous luminosity of $L = 6 \times 10^{27} \mathrm{cm}^{-2}\mathrm{s}^{-1}$. This will correspond to an interaction rate for PbPb collisions of 50 kHz, compared to the Run2 rate of 8 kHz. The ALICE upgrade would witness an upsurge in the data volume, with an estimated data flow of > 3 TB/s. Existing trigger based readout architecture is not suitable to cope with hundred times increase in the data taking rate. To handle such data volume, a dedicated data balancing system is introduced in ALICE upgrade of the readout and trigger system [2] in the form of a Common Readout Unit (CRU). Being at the crossing point of ALICE data streams, CRU manages the aggregation of detector data stream, flow of control requests and distribution of trigger and timing signal information simultaneously.

In this article, we focus on the discussion related to the trigger and timing distribution in ALICE using the CRU framework. The integrity of timing signal forms an important technical requirement of the Common Readout Unit (CRU) system. A detailed study has been performed to ascertain that the multiple high-speed communication links act together by being synchronous to the LHC clock signal to transmit the detector readout data and the timing signals with a constant latency. Moreover, phase information of the embedded clock needs to be preserved and the jitter introduced due to the effect of channel noise also to be retained at a low level. Tests are conducted to confirm the ability of the CRU system to retain the same behaviour with each power on/off cycle, firmware upgrade and reset assertion/de-assertion cycle (PFR cycle).

The trigger distribution system using the CRU is an amalgamation of multi-link technologies involving different protocol standards. For an entire system to operate synchronously and efficiently, the individual designs are optimized to be able to work in coherence to the neighbouring blocks. In essence, the GigaBit Transceiver optical link (GBT) and the Timing, Trigger and Control (TTC) system based on Passive Optical Networks (TTC-PON) link work in conjunction to communicate the TTC information from the Central Trigger Processor (CTP) to a detector through the CRU electronics system. The propagation path involves multiple transition points that involves different protocol conversions, however their concurrent executions might interact subtly. These interactions and their interdependencies at juncture points are prone to stochastic fluctuations, and hence proper characterization is needed to affirm the behaviour is deterministic. Hence, piece-wise qualification tests are done, before the final goal to integrate, implement and deploy the design elements. The Intel® Arria® 10 development board is chosen as the test board, which carries the same FPGA chip that will be used in the final CRU development card of PCIe40 [3]. The advantage of having a development board is that it provides easy access to the pins and ports to conduct the signal integrity analysis.

The article is organized as per the following. Section 2 gives an overview of ALICE trigger and the reasoning for trigger-less architecture for Run 3 . The data flow of the triggerless detector readout raises the need for the use of a new online data frame marker called the heartbeat (HB) trigger, which is also examined in the same section. The role of the TTC systems and the timing distribution to different parts of the ALICE experiment are outlined in the Section 3. High-speed serial links in the TTC communication is discussed in Section 4. The flow of detector raw data to the CRU using the GBT link is discussed in Section 5. In the Section 6, the use of a single CTP link to communicate with the multiple CRUs using a TTC-PON in a time multiplexing manner is elaborated. The symbiosis of the TTC-PON and the GBT link technology to form a TTC-PON and GBT link bridge made by the CRU firmware is discussed in brief in Section 7. The design integrates multiple links to detect any unwarranted behaviour in the system and to prevent a failure of cascaded type. Intrinsic system monitoring tools are built to gain statistics about the macroscopic behaviour of the system, which are explained in brief in Section 8. Section 9 covers the results related to the latency measurement, the jitter measurement, the Bit Error Rate (BER) measurement and the optimization of transceiver parameters. A discussion of the results is given in Section 10. Finally, a summary of the present studies and future outlook are presented in the last section.

2. Triggered and triggerless architecture in ALICE

The Central Trigger Processor (CTP) in ALICE manages the trigger decisions globally and supervise the production of trigger requests by combining the inputs from a system of trigger generating detectors. The CTP plays a pivotal role in identifying rare events, which are recorded for later analysis. In the Run2, the ALICE uses a hardware trigger strategy, where the signals from minimum bias data sample are selected using thresholds on event multiplicity, transverse momenta of tracks and other such observables combining several detectors [4, 5]. In Run2, the maximum readout rate was limited to 500 Hz for Pb-Pb events. In case the trigger rate exceeds a sub-detector read-out capability, the system saturates and asserts a busy signal.

In Run 3 , the ALICE would operate at *six* times the current peak luminosity of 10^{27} cm^{-2} s^{-1}, collecting over a *ten* times the targeted integrated luminosity of 1 nb^{-1} for the allocated runtime and operating at the collision rate 50 kHz for Pb-Pb ions instead of 8 kHz [1]. The physics objective of the upgrade is to improve the precision of the measurement of QGP signatures. The QGP physics processes do not exhibit signatures that can be selected by hardware triggers directly. In the triggerless readout scheme, all events are readout. The upgraded event selection strategy uses a combination of triggerless readout scheme and the minimum bias trigger generated from the First Interaction Trigger (FIT) detector system [2]. The new readout architecture for timing and/or trigger distribution topology in ALICE is briefly explained in the Section 3.

The principle of the ALICE upgrade read-out architecture relies on the Trigger and Timimg System (TTS) ability to efficiently distribute the critical TTC signals with constant latency over optical links to the read-out front-end cards and to receive the busy signal to throttle the trigger distribution when needed. All the data packets originating from the sub-detectors are time tagged. The transmission delay of the read-out data path is not stringent and can use non-constant latency links to the on-line farm. The triggerless data acquisition allows readout of multiple sub-detectors without stressing the trigger decision system when a sub-detector gets busy or faulty. In this manner, the continuous triggerless readout mode increases the event selectivity and allows sampling of the full luminosity. The only drawback that the upgraded system faces is to cope with the massive amount of total generated data that is approximately about 3.6 TB/s. The data flow before the final storage gets reduced by the combined effort of the Online and Offline (O2) computing systems. To delimit the overflow of the assembled events across the time frame boundary during data packet formation in the O2 system, a new trigger called *heartbeat* [6, 7] is defined, as explained in the next paragraph.

Heartbeat (HB) in a continuous readout mode are asserted periodically to delimit a stream of readout data [8]. As illustrated in Figure 1, HB trigger is used to generate a managable flow of the Heartbeat Frames (HBF). The HBFs are forwarded from the readout electronics to the CRU over the TTS links, where it is processed and forwarded to the First Level Processor nodes (FLP) and then to the Event Processing Node (EPN), as shown in Figure 2. For an each successful HBF delivery to the FLP, the CRU sends an HB acknowledge message to the CTP along with the information about the CRU data buffer. For the entire operation the LHC clock is used as a reference signal to synchronize the data flow. Under a nominal condition, the HBs rate correspond to one LHC orbit period of 89.4 μs or 10 kHz. One FLP accumulates 256 HBFs to generate a Sub-Time Frame (STF) every $\sim$ 22 ms, giving a rate of $\sim$ 50 Hz.

Within the EPN the STFs coming from all the FLPs are aggregated over the same time period, that includes both triggered or continuously readout detectors to form a complete Time Frame (TF). Keeping the anticipated customization needed, both the HBF length and number of the HBF in a TF are programmable. The HBF header, trailer and other IDs are defined to aid the flow managament for the TTS links. One hot encoding is used for the 16 bit trigger codes of the HB trigger.
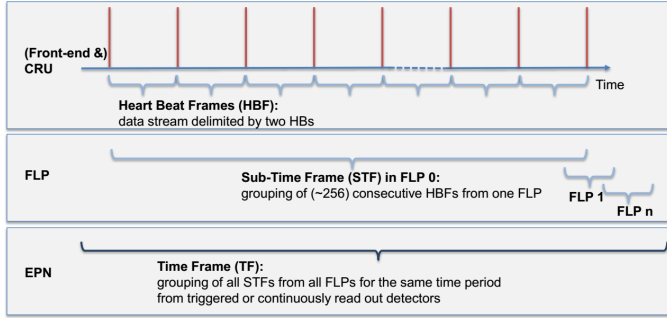

Figure 1: Role of Heart beat trigger in continuous readout mode

Figure 2: ALICE trigger distribution and detector read-out systems (The TTS distribution path is marked in green).

3. ALICE Clock Distribution strategy for Run 3

The ALICE detector read-out system has three configuration modes to receive the TTS information [2] : I. Detectors with non-trigger latency critical systems use the CRU connectivity only, such as the Time Projection Chamber (TPC) and Muon Tracking Chambers (MCH) systems; II. Detectors with latency critical trigger information connects directly to the CTP, such as the Inner Tracking System (ITS) ; and III. Detectors that would not upgrade to new readout architecture use the C-RORC (Run2 readout card) to receive the TTS information on the on-detector electronics via the TTC protocol. The details of the connectivity of the three modes are highlighted in the Figure 2.

The detectors which operate in Type I mode, use the TTC-PON and GBT bridge connection to forward the timing information as illustrated in the Figure 3. The detectors can operate in a continuous or a triggered readout mode. Depending on the configuration mode, the heartbeat trigger or physics trigger is employed.

4. High-Speed Serial Links in the TTC communication

For a communication system to operate reliably, one of the four classes of the clocking methods are employed, namely the asynchronous (uses no clock signal) scheme, the synchronous (uses same clock frequency and known phase) scheme, the mesochronous (uses same clock frequency and unknown phase) scheme and the plesiochronous (uses same clock frequency but with drifting phase) scheme [9]. In the implementation of the asynchronous serial links the clock is embedded within the data stream and behaves in the same manner as the synchronous communication system. The use of embedded clock removes
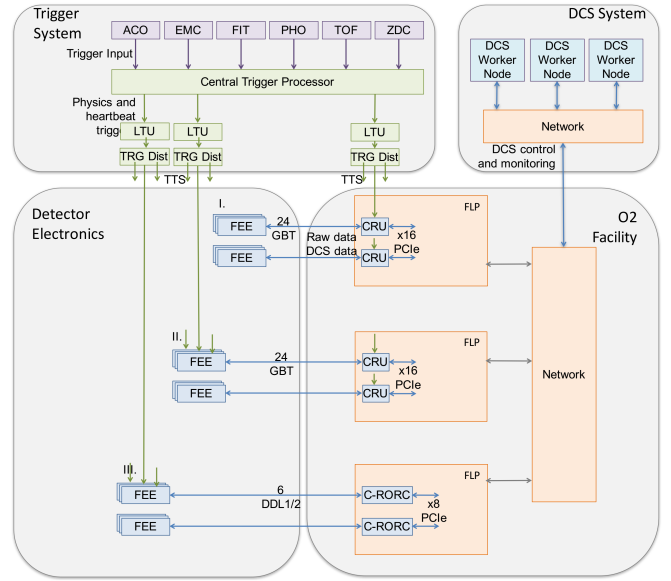
the need for a separate dedicated connection for a clock communication apart from the data stream. However, for the receiver side to recover the embedded clock with efficiency there need to be sufficient transition density in the transmitted bits. Bit transition density is maintained with the help of scrambling algorithm.

Plenty of commercially viable high-speed asynchronous link standards are available. However, those are not suitable for application in the LHC environment. The reason being the LHC operates at a unique frequency of 40 MHz that is not compatible with the standards of the other commercial links. The use of unconventional clock frequency for data payload communication led the CERN electronics team to develop a custom solution referred as the TTC interface link standards. The TTC standards used in CRU are the GBT and the TTC-PON. Comparison between the specification of the two standards are listed in the Table 1. For embedding the clock in the serial link and maintaining the bit transition density, the GBT uses the block interleaver while the TTC-PON uses the 8b/10b as channel encoding scheme.

To prevent an anachronistic behaviour in the data packet formation, use of elastic buffers are not preferable. This approach helps to maintain the constant latency in the link that is necessary for arranging the data types having no time-stamp. Synchronous relationship of flow of events between the source and the receiver over an asynchronous link are preserved by maintaining a certain timing relationship at the physical level of the communication chain. An analogy has been given with the distributed systems that behave in a fully synchronous manner only after abiding certain degrees of synchrony [14]. Similarly an asynchronous system can act as a synchronous system provided it abides by certain constraints. In the comparison Table 2 an attempt has been made to correlate the constraints. The causal relationship of the events are not preserved at the phys-
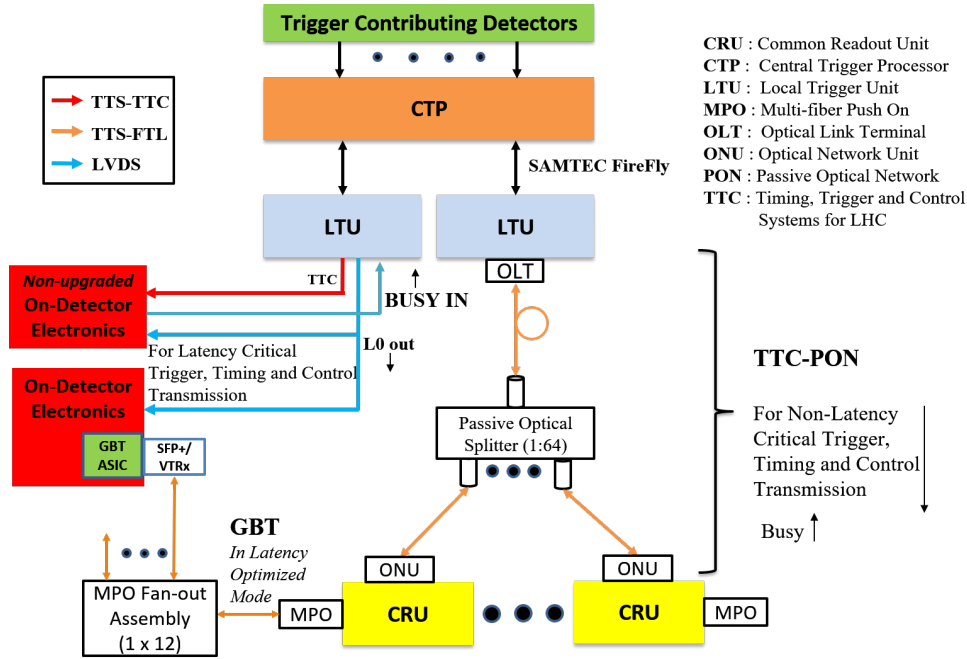
Figure 3: CRU as Trigger Distribution Unit

Table 1: Showing the basic parametric difference between GBT and TTC-PON

Parameters	GBT [10, 11, 12]	TTC-PON [13]
Technology Specification	Custom	XGPON1 with modifications
Designer Group	CERN	ITU-T with CERN modifications
Line Rate	4.8 Gbps	Downstream: 9.6 Gbps Upstream: 2.4 Gbps
Payload Rate	3.2 Gbps	Downstream: ~7.68 Gbps Upstream: 640 Mbps
Payload Size	120 bits@40 MHz	Downstream: 192 bits@40 MHz Upstream: ~16 bits@40 MHz
Wavelength	850 nm (Multi-mode Tx) 1310 nm (Single-mode Tx)	Downstream: 1577 nm Upstream: 1270 nm
Network Topology	Point-to-Point	Point-to-Multipoint
Encoding	RS Encoding with Block Interleaver	8b/10b
Synchronous Trigger Support	Yes	Yes
Trigger Latency	Optical loop-back Round-trip: 150 ns	Downstream: ~100 ns Upstream: 1.6 μs
Commercially Available	No	No

Table 2: Degrees of Synchrony to behave as a fully synchronous system

For Distributed systems (Bounded and known)	For Asynchronous systems (Design Contraints)
Processing speed	Frequency locked
Message delivery delay	Fixed latency
Local clock rate drift	Low Jitter
Load pattern	Data Time-stamped
Difference between local clocks	Phase locked

ical level of the protocol stack. Joint use of the clock synchronization and the syntonization for the recovery of the embedded clock is employed at the physical level. The approach ensures frequency stability with low jitter of the recovered phase locked clock. If the links are operated in latency optimized mode [15] then the latency or the delay path of the data lines remains constant, and is needed for the Timing, Trigger and Control (TTC) data communication. While other levels of complex synchronous information handling like the time-stamp and the trigger management are preserved at the higher level of the CRU firmware logic stack.

5. GBT Specifications

The GBT framework [11] defines the technology standards necessary to allow high-speed time critical data communication with high error resilience to communicate reliably from the LHC radiation zone to the readout electronics situated remotely. The GBT ecosystem, shown in the Figure 4 is composed of three parts, namely, the GBT ASIC that houses the Versatile Link chip along with the GBT slow control ASIC, Optical Fibre connection operating in a single mode (1310 *nm*) or a multi-mode (850 *nm*) , GBT the Slow Control ASIC and an FPGA programmed with the GBT logic core.

The GBT link supports two modes of operation, the standard mode and the latency optimized mode. The latency optimized mode is needed for a time critical applications that requires constant latency. The GBT link supports two types of data frame formats, namely the GBT frame format or the Widebus format. The GBT frame format appends an error correction code formed from the Reed-Solomon algorithm cascaded with the interleaver and the scrambler. While the Widebus frame for-
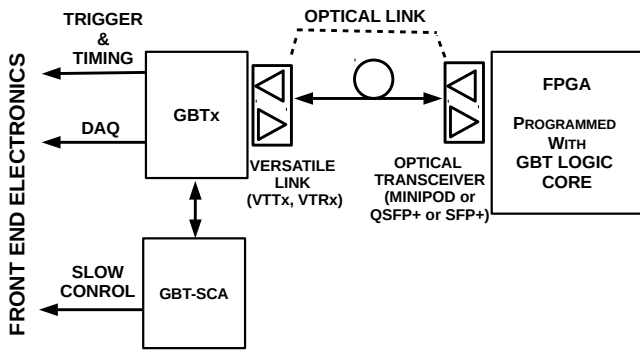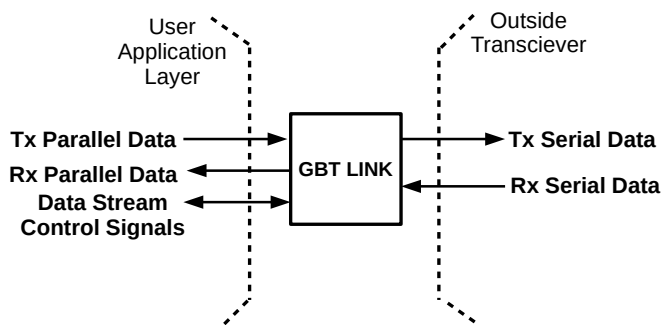
Figure 4: GBT ecosystem

Figure 5: Flow connection of a GBT Link

mat implies that the entire bus is available for the user data and no redundant error checking bits are appended. The line rate of the GBT link is 4.8 *Gb/s*. For the GBT scheme the effective data transfer rate is of 3.36 *Gbps* and for the Wide-Bus scheme the effective data transfer rate is of 4.64 *Gbps*.

In ALICE, maximum 24 GBT links are required per CRU board. Most part of the CRU FPGA resources are needed for the detector specific logic. To consider a way to save on the GBT specific periphery logic resources a new design approach is required. The effect of optimization on saving the logic resources is studied by Baron et. al. [16] by sharing one decoder block for several links. Another level of optimization solution possible in the Arria® 10 FPGA that saves on clocking resources and reduces intra-link clock skew is by using a x6 Physical Medium Attachment (PMA) bonded mode [17]. The PMA bonded mode allows *six* GBT links to be packed closely. Together the links are referred as the *GBT Bank*. In other words, the GBT Bank is that largest common group formed of the GBT links that are bonded or clubbed together for an FPGA resource optimization, which is six in this case. The bonded architecture comes with a constraint that all the links need to follow the same standards for a particular GBT lank. Individually the settings for the GBT banks are completely configurable. For example, if a designer needs to have 20 links per CRU board then one can split it as three GBT banks of six links and one GBT bank with two links.

6. TTC-PON architecture

Passive Optical Networks (PON) for the particle physics applications at CERN was first proposed in 2009 [18]. It was later extended for higher speed in 2013 [19]. The article by Papakonstantinou et. al. (2011) suggested the future use of Time Division Multiplexing (TDM) in PONs for the TTC information and the possibility of using Wavelength Division Multiplexing (WDM) PONs for the Data Acquisition (DAQ) applications. Since then the protocol has went through much up-gradation. In our study we have used 2016 version of TTC-PON as shown in Table 1.
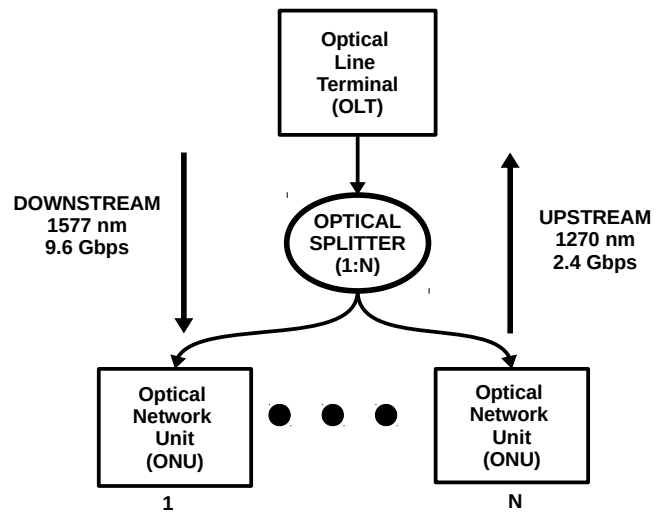

Figure 6: Flow connection of TTC-PON link

The TTC-PON architecture is based on PON technology that finds application in Fiber To The Home (FTTH, FTTx) networks. TTC-PON is a single fibre, bi-directional, point-to-multipoint network architecture that uses optical splitters to enable a master node or Optical Line Terminal (OLT) to communicate with multiple slave nodes or Optical Network Units (ONUs) [13], as illustrated in Figure 6. The downstream (from OLT to ONUs) runs at 9.6 Gbps at operating wavelength band of 1577 nm, while the upstream (from ONU to OLT) runs at 2.4 Gbps operating in wavelength window of 1270 nm. Using the TTC-PON technology, the Timing, Trigger and Control (TTC) information from the CTP are communicated over an optical link in a time multiplexed fashion, that allows a single link to transmit the TTC information to be splitted among the multiple CRUs [20, 21], as shown in Figure 3. The link topology reduces the number of links to be used and hence minimizes the hardware costs involved significantly.

7. TTC-PON and GBT bridge for TTC communication

The TTC-PON and GBT bridge connection is the interconnection between the two mutually independent GBT and TTC-PON links connected using a firmware defined logic. The bridge connection is dedicated for the delivery of the TTC payload. Different types of topology for the bridge connection are

possible. For CRU design, the star topology is used for interconnection, where the TTC-PON forms the central nodal hub for forwarding the TTC information to 24 GBT links, as shown in the Figure 7.
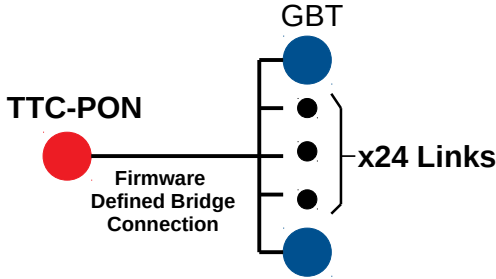

Figure 7: TTC-PON and GBT bridge in star topology connection

The link connection between a TTC-PON to the multiple GBT is elaborated. Initial implementation and testing was based on the scheme where the 240 MHz clock is recovered from the TTC-PON'15 protocol and then fed into the jitter cleaner before forwarding it to the GBT at 120 MHz as shown in the Figure 8 as the configuration-I. However, the implementation on the GBT side suffered from phase inconsistency of the forward clock with each power cycle or reset cycle. The issue arised because the divider of the Multi-Gigabit Transceiver (MGT) locks the recovered fabric clock at any of the rising edges of the serial clock. In the Figure 9 it is exhibited that for the 10,000 soft reset cycles of the firmware, the phase variation exhibits a uniform distribution over the range of [-4 ns,4 ns]. This has been solved by calibration logic that slips the GBT Tx clock to align with the phase of the recovered clock using a Finite State Machine (FSM) [17] .

An improved design option emerged in the version upgrade of the Intel FPGA technology that allows the feedback compensation mode in the transceiver PLL to ensure the deterministic nature of the clock. However, the feature constraints the design solution to operate 240 MHz frequency [22]. Hence, the latest CRU firmware design uses frequency of 240 MHz to cross the entire link chain, instead of stepping down the frequency and stepping up again. The development led to the TTC-PON and GBT connection configuration-II as shown in the Figure 10. In both the configurations given in the Figures 8 and 10 the trigger data path has to cross two clock domains. Even if the clocks are phase locked and of the same frequency, the FPGA sees it coming from two different sources. Hence to avoid the metastability issue in the firmware design synchronizers are added [23]. Moreover, proper fitter constraints are applied in the firmware logic to lock the logic placements to reduce intra-links skew variation with each firmware upgrade.

8. Design Resilience

The CRU being a complex heterogeneous system has to deal with multiple links of different communication standards. During a stressful run-time scenario the stochastic fluctuations
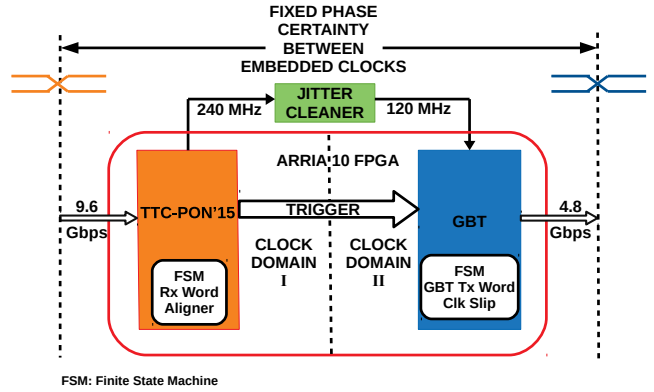

Figure 8: Configuration-I: TTC-PON and GBT bridge connection
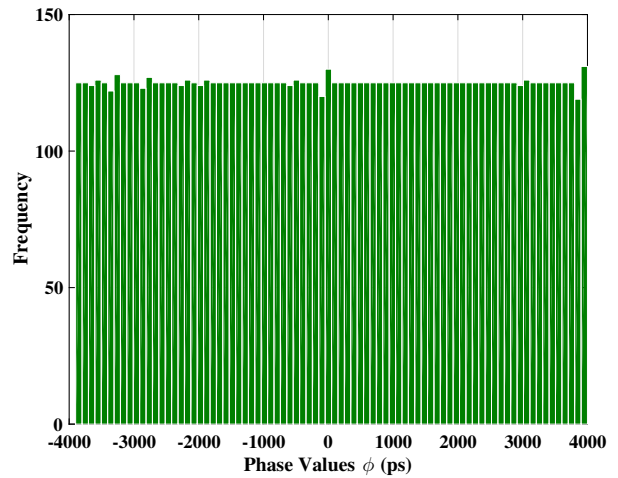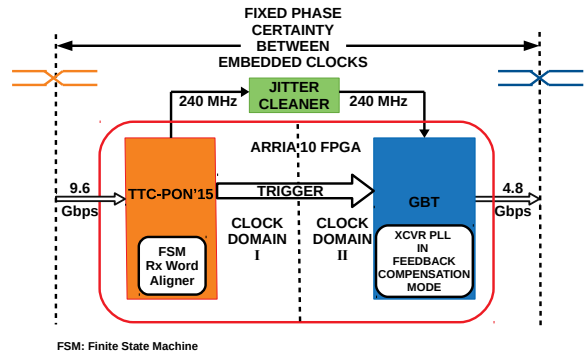

Figure 9: GBT Phase Uncertainty in Tx

Figure 10: Configuration-II: TTC-PON and GBT bridge connection

in the data link pathways might go outside the tolerable zone. The stochastic behaviour is associated with uncertainties and can trigger a chain of cascading upsets in the link chains. Hence, a quantifiable autonomous acquisition system is required to monitor and trace for any unwarranted behaviour.

As a fall back solution the house keeping tools are included with the main CRU firmware to act as a caretaker to predict any errors and disruption by tracking the macroscopic behaviours of the CRU system. Any deviation of the system behaviour

if registered then flags it as a warning or an error to the system management console at the online computing system of the AL-ICE. The inclusive monitoring system involves the three main tools to detect any aberration in the system behavior, as shown in the Table 3. The monitoring system aids in the increase of the resilience and reliability of the system.

Table 3: Basic monitoring system to detect macroscopic behaviour

Measurement Parameter	Monitoring Signal	To Detect
Frequency	Derived or recovered clock	Presence of Clock
Phase	Pico-seconds resolution phase measurement between the related clocks [24]	PLL and xcvr PHY working correctly
Temperature	The FPGA chip & the CRU board	Cooling system is functional

9. Results and Discussions

The entire trigger related logic involves role and functioning of multiple blocks. Each sub-blocks are treated individually, tested, characterized and then integrated in the design system. The test systems are buffeted with various stress scenarios, before compiling the final result in optimum environment condition.

Since the work deals with timing information transmission, hence tests that give information about the clock quality during a link transition are included. Tests that are entailed in the following sub-sections, are the latency measurement, the jitter measurement, the BER measurement and the optimization of transceiver parameters.

9.1. Latency Measurement

The latency measurement gives an estimation of the logic path delay involved and also senses whether the path traverses through an elastic or an inelastic buffer. Lower the latency is more suitable it is for communication of time-sensitive information, such that service response can be delivered in the shortest period. However, variable latency means the path is ideal for data payload but not for time-critical payloads like in the case of timing and trigger. So, it is the challenge for both the protocols, the TTC-PON and the GBT, to meet the low latency with the high throughput and yet be able to preserve the same latency without any variation over the entire run period. Since the serial links traverse through the multiple clock multiplication and the subsequent division zones, the links are subjected to the risk of sudden major variations in the latencies. In the latency measurement also checked for any significant deviations that can perturb the entire time-critical pathway.

A special comma is used to measure latency in the TTC-PON. The comma character is sent every 8 μs (K28.1) and a flag at the Optical Line Terminal (OLT) level is created to indicate the value is send. A match-flag is created when the Optical Network Unit (ONU) received the special character (just after 8b10b decoder). The latency between those two flags are then

measured using the oscilloscope. Several ONU_RX resets were performed and the position between those flags was deterministic, as shown in the Figure 11.
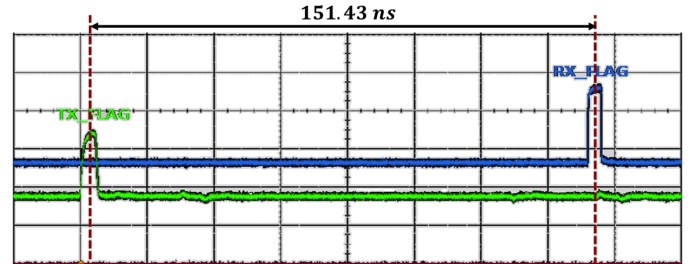

Figure 11: Latency of 151 ns is detected between Transmitting data and Receiving Data

For the GBT measurement, an initial version of the PCIe40 DAQ Engine with the Arria® 10 FPGA engineering sample is used. Since the setup does not allow to probe at the individual points, an ingenious solution to give a coarse estimate of the latency using firmware based measurement logic is defined. For the measurement a 32-bit ripple counter is used as the generated pattern to communicate over the GBT stream. The principle of the measurement is to enable the loopback, receive the packet, unwrap from the received GBT payload and then compare the received counter value with the sender's to estimate the round trip delay. As the GBT frame arrival rate is of 40 MHz, hence the course measurement of the round trip delay achieved is of 25 ns resolution. The round trip delay corresponds to the length of time a signal takes to be sent plus the length of time it takes for the reflected echo of that signal from the receiver to be registered. It includes the serialization and the deserialization time along with the propagation delay. For the measurement as can be seen in the Figure 12, *three* loopback points are chosen, those are : (1) Electrical loopback within the FPGA; (2) Optical loopback; (3) Loopback enabled at the Versatile Link Demo Board (VLDB) side. In the Table 4 the latency of the GBT protocol with Tx and Rx configured in the latency optimized mode or the standard mode are tabulated. However, the measurement for the Wide-Bus mode is skipped, as there was no requirement from any ALICE detector group at the time of measurement. The GBT firmware used for this measurement is the development version used in the year 2015-16 that has got 120 MHz as word clock.

Both the links exhibited stable latency even when presented with multiple soft or hard resets and power cycles. No unwanted significant deviations are registered. However, the addition of jitter is present which is a standard behaviour due to the unwanted channel interference and the system noises involved. Details about the jitter measurement of the recovered clock are covered in the following sub-section 9.2.

9.2. Jitter Measurement

The asynchronous fast serial trigger links (in the CRU application the GBT and the TTC-PON) embed clock signal in the serial data transmission line. The deterministic latency of the timing information transmission is maintained by embedding
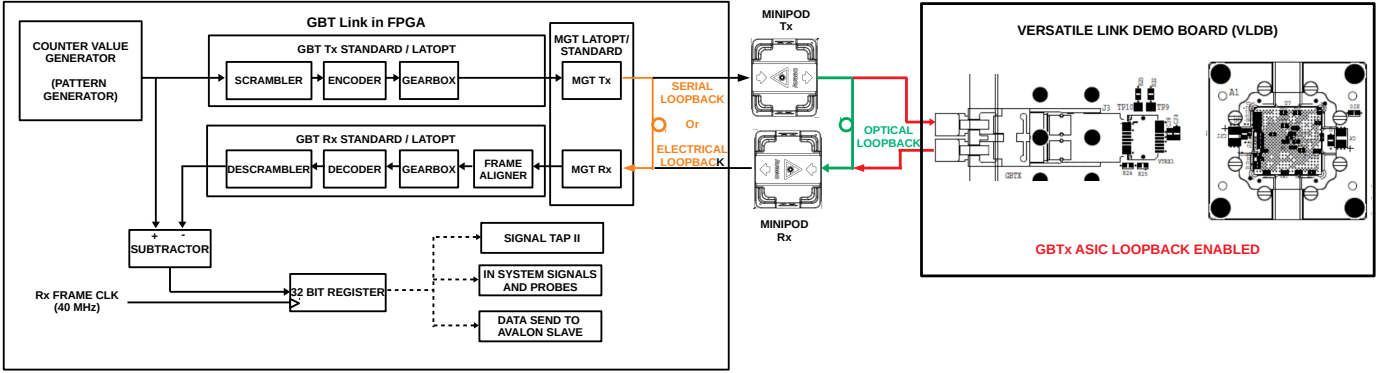
Figure 12: Test Setup for *three* types of round trip delay measurement where each loopback arrangement are marked by different colours

Table 4: The GBT round trip delay measurements for the multi-level loopback in the PCIe40

| GBT Protocol | | ROUND TRIP DELAY | | |
| | | (Resolution of one LHC Bunch clock cycle i.e. 25ns) | | |
Transmission Side	Receiver Side	Serial or Electrical Loopback	Optical Loopback	GBT ASIC Loopback
Latency Optimized	*Latency Optimized*	150 ns	175 ns	275 ns
Latency Optimized	*Standard*	325 ns	350 ns	450 ns
Standard	*Latency Optimized*	200 ns	225 ns	325 ns
Standard	*Standard*	450 ns	450 ns	550 ns

the synchronization information in the serial data transmission. The embedded clock is recovered by the front end electronics of the detector to generate the *detector specific data packet*. The clock goes through the multiple link transitions, and becomes susceptible to the system and the channel noises. The permissible range of the Root Mean Square (RMS) value of the clock jitter is specific to each sub-detectors requirement and varies with the criticality of the timing of the communication needed. The range of the RMS jitter inclusive of the specifications for all the sub-detectors of the ALICE, typically lies within the range of $300\ ps - 20\ ps$. A preliminary study is conducted to determine if the RMS jitter value of the forwarded clock is less than the lowest jitter requirement of $20\ ps$. The test uses the TTC-PON 2016 version and the GBT version operating at 240 MHz clock domain. In the Intel® Arria® 10 FPGA devices three types of transmitting PLLs are available: (a) the Advanced Transmit PLL (ATX PLL); (b) the Fractional PLL (fPLL); (c) the Clock Multiplier Unit PLL (CMU PLL) or the channel PLL. Since the design uses bonded application, hence the ATX PLL and the fPLL can only be used. The best jitter performance is seen using the ATX PLL over the fPLL. However, the recommendation based on the data rates from the Intel is to use the fPLL for the transmit PLL [22], hence in the design fPLL is used.

During the pre-validation test the ideal test scenarios are prototyped with the FPGA development boards having the same family of FPGAs as the final production version. To emulate the CTP and the CRU hardware, the Kintex Ultrascale and the Arria® 10 development boards are used respectively. For rapid prototyping of the test design, a *split hardware* setup is used to model the behaviour of the CRU. It means that the GBT pro-

tocol is implemented in one Arria® 10 FPGA board and the TTC-PON in other Arria® 10 FPGA board, while the clock is transmitted from one board to the other after jitter cleaning it in the SI5344 PLL module. The split hardware model allows an easy access to the *Test Points (TP)* for the jitter measurement test setup as can be seen in the Figure 13. The settings of the configuration parameters of the SI5344 PLL module and the Versatile Link Demo Board (VLDB) used for the test is given in the Table 5 and the Table 6 respectively.

Table 5: SI5344 *Rev B* PLL Configuration

Parameters		Status
Free Run Only Mode	:	Not Enabled
Zero Delay Mode	:	Not Enabled
Loop Bandwidth	:	200 Hz
Fastlock Enable	:	ON
Fastlock Loop Bandwidth	:	1 kHz
Hitless Switching	:	Not Enabled
HoldOff Mode	:	Disabled [2]
Termination	:	LVCMOS In-Phase 1.8 V 31 Ω

[1] REG: 0x052C[0] = 0x0

Table 6: VLDB Configuration

Parameters		Status
Elink Number	:	0
Channel Number	:	0
Data Transmission	:	Off
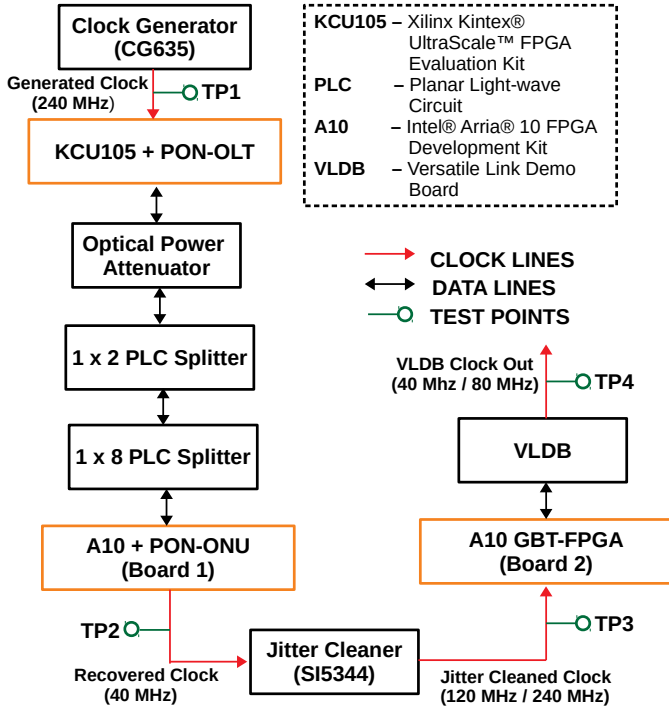
Figure 13: Jitter measurement test setup for the TTC-PON and GBT bridge connection

Figure 14: Oscillator phase noise in dBc/Hz vs. frequency offset [25]

The *Phase noise* representation used for the jitter measurement gives an accurate estimation of the phase fluctuations in the frequency domain analysis. Phase noise is determined as the ratio of the noise in a 1-Hz bandwidth at a specified frequency offset, f_m, to the oscillator signal amplitude at frequency f_O. The unit used is dBc/Hz, where dBc (decibels relative to the carrier) is the power ratio of a signal to a carrier signal, expressed in decibels. It is conventional to characterize an oscillator in terms of its single-sideband phase noise as shown in the Figure 14, where the phase noise is in dBc/Hz plotted as a function of frequency offset, f_m, with the frequency axis on a log scale. The RMS jitter (in linear terms not dB) is calculated from a piecewise linear integration of the single sideband phase noise data points. The Equation 1 used for calculation is adapted from the Tutorial MT-008 Analog Devices [25]. The results are correlated with the Phase Noise Analyzer software generated values.

$$A = Area = Integrated\ Phase\ Noise\ Power\ (dBc),$$

$$RMS\ Jitter \approx \frac{\sqrt{2 \times 10^{A/10}}}{2\pi f_O}, \tag{1}$$

where f_O is the oscillator frequency.

For performing the integration on the *phase noise power values*, the *trapezoidal rule* [26] is used over a defined bandwidth given by the Equation 2.

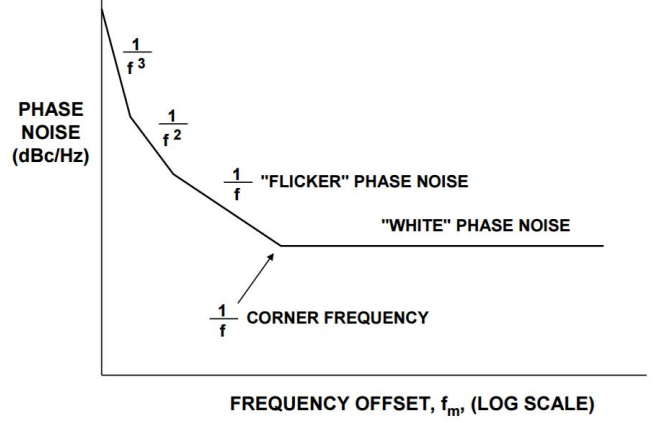$$\int_a^b f(x)dx \approx (b-a)\frac{f(b) + f(a)}{2} \tag{2}$$

The experiment calculates the RMS Jitter value from the phase noise power within the bandwidth of **10 Hz to 20 MHz**. As the zone of operation is in the high frequency range, hence the effect of the lower frequency phase noise is neglected [27]. This implies that even though the integrated jitter value computed over the plot A is evaluated higher in relative to the other curve B does not implies that the curve A is better than the curve B. However, if the phase noise curve at the high frequency region of interest for the curve A is below the curve B, then the curve A is considered to be better in performance than the curve B. Such concept is applied in the interpretation of the phase noise measurement plots shown in the Figures 15, 16, 17, 18 and 19. The oscilloscope settings are kept same for the different measurements for the sake of consistency.

The results contain the measurement of phase noise of clock output from the different test points (TP) in the link chain. The Arria® 10 transceiver specific phase noise data points [28] relative to the reference clock phase noise are also included. The Arria® 10 transceivers in the Intel data-sheet [28] gives the phase noise points for the reference clock operating at 622 MHz frequency. The REFCLK phase noise requirement at frequencies other than the 622 MHz is calculated using the Equation 3 adapted from the Intel data-sheet [28].

REFCLK phase noise at f (MHz)

$= $ REFCLK phase noise at 622 MHz + 20 ∗ log($f/622$) (3)

The details of the tapping points used during the measurement is given as illustration in the Figure 13. Following measurements are conducted to evaluate the performance and to achieve the best jitter cleaning effect.

9.2.1. Performance comparison between SI53XX PLL family

The initial purpose for the study of phase noise measurement is to determine the PLL family that fulfills the CRU requirement. PLLs from the different vendors are characterized by the CERN electronic team members, out of which the PLLs from Silicon Labs SI53XX family found to be suitable for the jitter cleaning requirement for the LHC timing signal. Figure 15 gives comparative result of the jitter cleaning performance of

PLLs belonging to the SI53XX family namely the SI5338 and the SI5344. The test demonstrates that the SI5344 PLL jitter cleaning is a better match for the phase noise requirement at 240 MHz reference clock frequency for the Arria® 10 FPGA SerDes. The test points used for the measurements are TP1 and TP3. The study plays a significant role in deciding the PLL type to be installed in the CRU hardware PCIe40 DAQ Engine. The SI5345 PLL having 10 output nodes, is a variant of SI5344 PLL family [29], which is chosen as the onboard jitter cleaner for the CRU PCIe40 DAQ Engine [30].
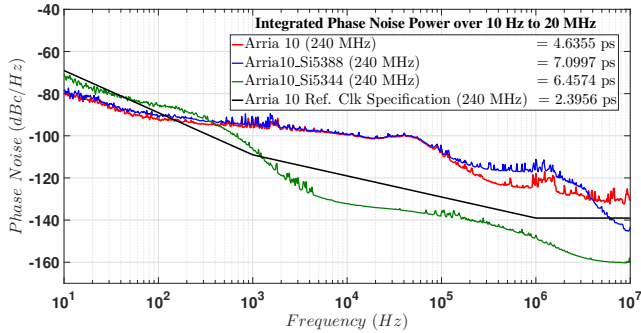
Figure 15: Comparison of jitter cleaning performance between the two jitter cleaners

9.2.2. Performance comparison with PLL bandwidth variation

Following test is to determine at which bandwidth configuration the PLL performs at its best. The Figure 16 shows the phase noise study done on the clock signal tapped at the test point TP3. The test is to evaluate the effect of the bandwidth variation on the integrated RMS jitter. From the plot it can be inferred that the PLL gives best jitter cleaning performance for the 200 Hz bandwidth configuration mode.
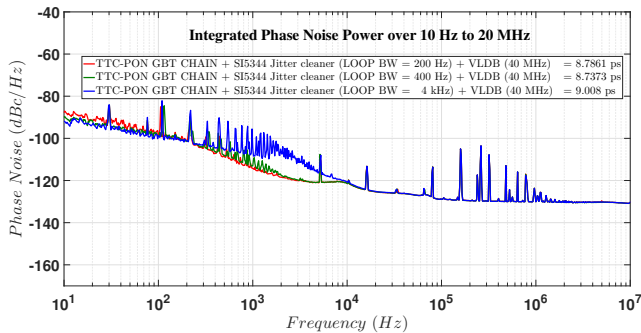

Figure 16: Phase Noise Analysis (Total Jitter) for VLDB clock output at 40 MHz frequency having the full TTC-PON and GBT bridge connection with the PLL configured at loop bandwidth 400 Hz and 4 kHz

9.2.3. Performance comparison with variation in output clock frequency

After investigating the effect of the operational bandwidth on the jitter cleaning PLL, the other study that requires attention is the choice of the output clock frequency of the PLL that gives a better jitter attenuation. The CRU firmware design can work

at two operational frequencies namely 120 MHz and 240 MHz. The tests with the two frequencies at test point TP3 is shown in the Figure 17. The CRU firmware with the latest specification uses 240 MHz frequency to make transit of the timing signal from the TTC-PON to the GBT without stepping down of frequency at intermediate points. The result shows that the jitter cleaner is able to satisfy the requirement of the Arria® 10 FPGA jitter specification of SerDes at 240 MHz reference clock frequency.
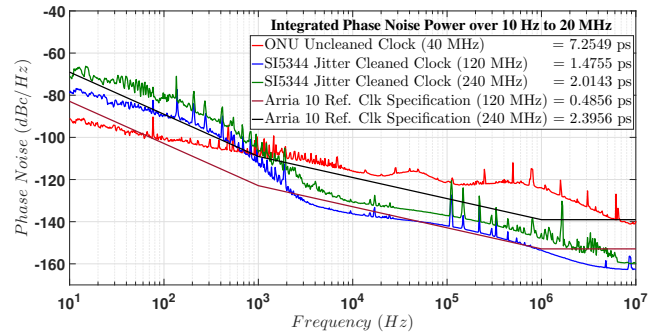

Figure 17: Phase noise analysis (total jitter) for ONU uncleaned clock (40MHz), SI5344 jitter cleaned clock (120 MHz) and SI5344 jitter cleaned Clock (240 MHz)

9.2.4. Effect of jitter cleaning performance on integrated GBT and TTC-PON chain

The subsequent test for the SI5344 PLL performance is conducted while fitted in the integrated system. The test points TP1, TP2 and TP3 are used to derive the phase noise plot as shown in the Figure 18. The test result validates that the jitter cleaning performance of the PLL keeps the jitter within the tolerable level as specified for the Arria® 10 FPGA.
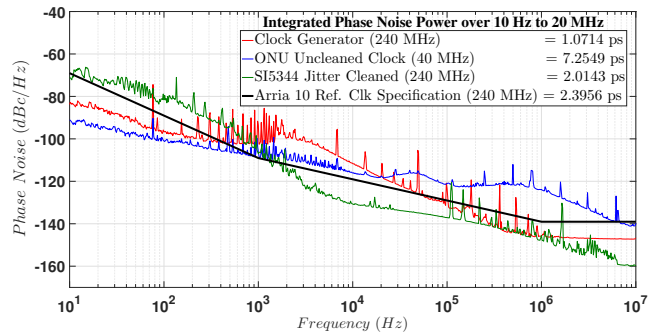

Figure 18: Phase noise analysis (total jitter) for source clock (240MHz), ONU uncleaned clock (40 MHz) and SI5344 jitter cleaned clock (240 MHz)

9.2.5. Comparison of jitter cleaner performance against an ideal test case scenario

The purpose of the test is to compare the presence of jitter in an ideal experimental condition against the practical scenario with jitter cleaner in use. The terminal destination of the embedded clock signal in the link chain is the delivery to the GBT chipset. In our test case, we have used VLDB, as it houses

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the GBT chipset. The quality of the embedded clock received by the end-point VLDB is studied, where the recovered output clock frequency is set at 40 MHz and 80 MHz respectively. Two types of connection chains are constituted for the test. For the ideal test scenario, all the noisy source points are dropped and the transition points are minimized. It is composed of clock signal originating directly from the clock generator, that gets embedded using the CRU firmware to GBT payload and finally getting communicated to VLDB to be recovered in 40/80 MHz frequency. The setup connection is shown in the Figure 20. For the practical test scenario, the formerly used experimental setup is utilized as shown in the Figure 13. The results are plotted in the Figure 19 and test result are referred as "VLDB CLK OUT WITH GBT" and "VLDB CLK OUT WITH TTC-PON GBT BRIDGE" respectively. The results of the two test setups show strong positive correlation, hence it can be concluded that the SI5344 jitter cleaner can successfully be employed for the cleaning of the embedded clock during traversal of the TTC-PON and GBT bridge connection.
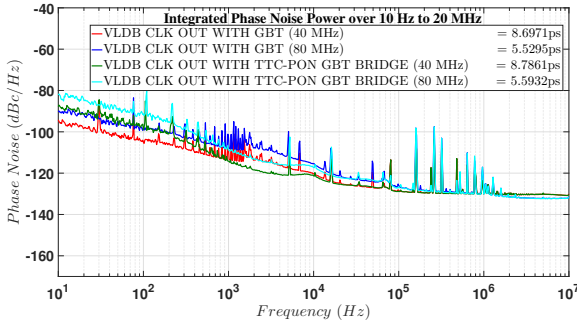

Figure 19: Phase noise analysis (total jitter) for the VLDB clock output of : 40 MHz o/p with the GBT link connection, 80 MHz o/p with the GBT link connection, 40 MHz o/p with the TTC-PON – GBT bridge connection and 80 MHz o/p with the TTC-PON – GBT bridge connection

Table 7: Comparison of *RMS Jitter* results

CONNECTION TYPE	RANDOM JITTER (ps)	PERIODIC JITTER (ps)	TOTAL JITTER (ps)
Clock generator (240 MHz)	0.967	1.071	1.071
ONU uncleaned clock (40 MHz)	6.481	7.298	7.255
Si5344 jitter cleaned clock (120 MHz) with loop BW 200 Hz	1.327	1.447	1.475
Si5344 jitter cleaned clock (240 MHz) with loop BW 200 Hz	1.265	1.407	2.014
VLDB clock out with GBT (40 MHz)	7.409	8.697	8.697
VLDB clock out with GBT (80 MHz)	3.501	3.884	5.529
VLDB clock out with TTC-PON and GBT bridge (40 MHz) having SI5344 loop BW 200 Hz	7.507	8.799	8.786
VLDB clock out with TTC-PON and GBT bridge (80 MHz) having SI5344 loop BW 200 Hz	3.615	4.048	5.593
VLDB clock out with TTC-PON and GBT bridge (40 MHz) having SI5344 loop BW 400 Hz	7.439	8.738	8.737
VLDB clock out with TTC-PON and GBT bridge (40 MHz) having SI5344 LOOP BW 4 kHz	7.727	9.018	9.008

9.2.6. Comparison of jitter value at intermediate points

A comparison of all the configurations discussed in the phase noise plots for the integrated RMS jitter is tabulated in the Ta-

ble 7. The table information is used to derive the Jitter Transfer Function (JTF) of the individual composite link elements in the link chain. The JTF [31] is the ratio of the output jitter to the applied jitter on the reference clock, where both the signals are measured as a function of the frequency. The calculated values of the JTF are given in the Table 8. To summarize the SI5344 PLL satisfies the jitter cleaning requirement of the clock needed in the TTC-PON and GBT bridge connection transition.

Table 8: Comparison of the *RMS Jitter* at each intermediate points in CRU TTC-PON GBT bridge connection

CONNECTION TYPE	INPUT TOTAL RMS JITTER (ps)	OUTPUT TOTAL RMS JITTER (ps)	JITTER TRANSFER (dB)
Clock generator (240 MHz) to ONU Uncleaned Clock (40MHz)	1.071	7.255	16.616
ONU Uncleaned Clock (40MHz) to Jitter Cleaned Clock (240 MHz)	7.255	2.014	-11.132
Jitter Cleaned Clock (240 MHz) to VLDB Clock Out (40 MHz)	2.014	8.697	12.706

9.3. BER Measurement

Jitter is not the only contributing factor to bit errors; it can also be a consequence of amplitude noise. Bit Error Rate (BER) analysis is done for quantitative measurement of signal quality. The Intel® Arria® 10 development board is used for conducting the test. A 10G 850 nm Multimode Datacom SFP+ optical transceiver is configured to operate at 4.8 Gbps, the operating line rate of the GBT protocol. A customized variable fiber optic solution having in-line attenuator capability within the range of 0-60 dB is used for providing attenuation to the signal. For optical power measurement, a hand held power meter with a SC-ST connector is used. The attenuator cable adds an additional *insertion loss* of $\leq 3\ dB$ to the entire test chain. Individual snapshot of the measurement setup is provided in the Figure 21. Interested users can use the firmware uploaded at the CERN Gitlab link [32] to reproduce the results in other hardware conditions. For the BER measurement default transceiver configuration is used.

BER is evaluated from the ratio of the number of errors received to the total number of bits transmitted. Ideally as the number of transmitted bits approaches infinity, the BER becomes a perfect estimate. However, for practical tests there is a need for test procedure that allows to measure BER with a high confidence level. J. Rudd [33] has documented a method for reducing the test time for stressing a system, by calculating the number of bits needed to be transmitted to estimate error probability with a particular statistical confidence level. Equation (4) shows the trade-off between test time (T) and confidence level (CL).

$$\left. \begin{array}{ll} n & = -\dfrac{\ln(1-CL)}{BER} + \dfrac{\ln\left(\sum_{k=0}^{N} \dfrac{(n*BER)^k}{k!}\right)}{BER} \\ T & = n/R \end{array} \right\} \quad (4)$$
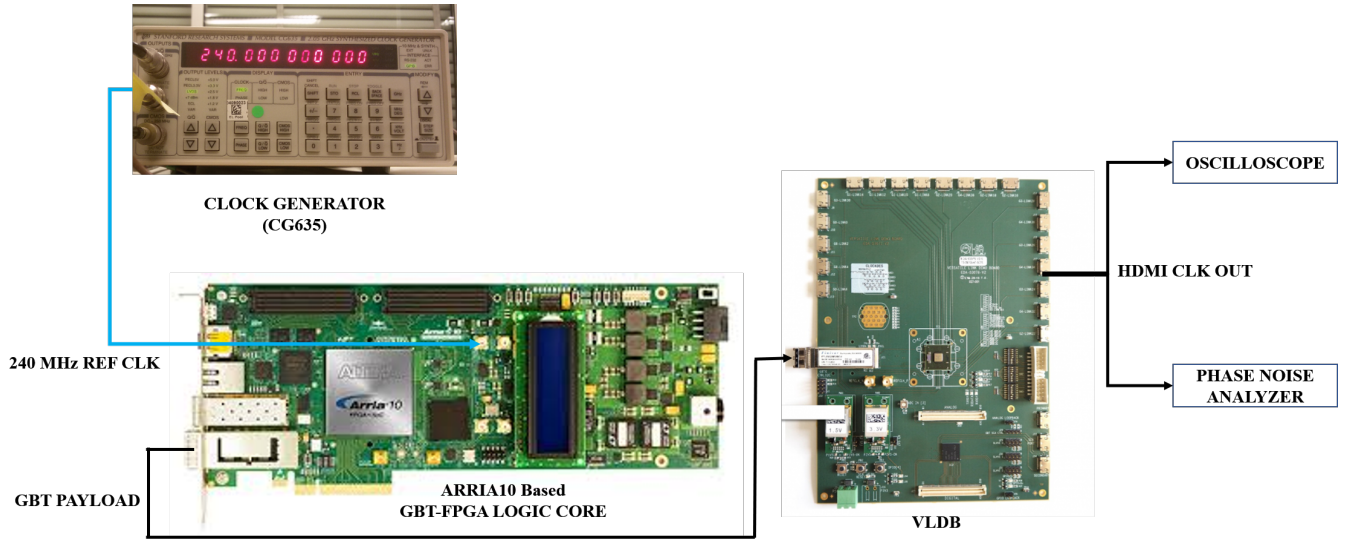
Figure 20: Jitter measurement test setup with GBT CHAIN and VLDB only
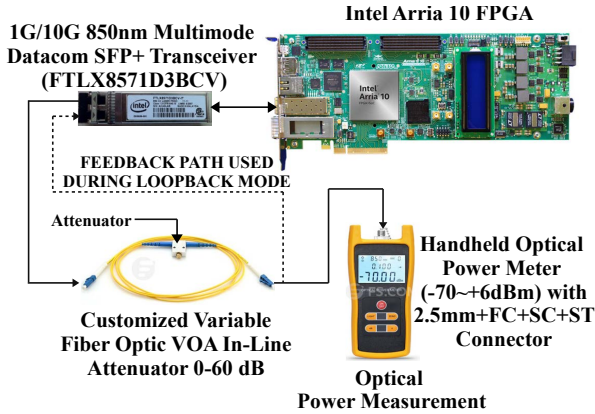

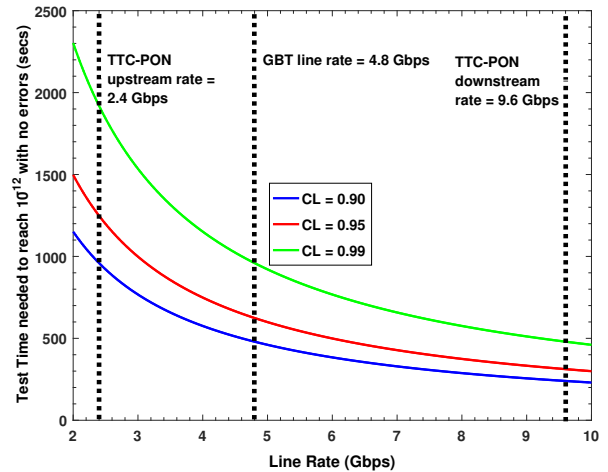Figure 21: GBT Measurement Setup

Figure 22: Time required to reach 10^{-12} BER vs. line rate. Showing the cases for GBT and TTC-PON.

where n is the total number bits transmitted, N is the number of errors that occurred during the transmission and R is the line rate. For $N = 0$ the solution is trivial. In the work of Detraz et. al. [34] an effort has been made to define the minimum experiment time required for GBT BER measurement with different level of confidence as derived from the Eq. (4). Further the concept is extended and marked for the minimum measurement time needed for TTC-PON link also, as shown in Figure 22.

9.3.1. BER Measurement for the GBT

The GBT BER measurement for the GBT encoding scheme operating in the GBT mode and the Widebus mode is plotted in the Figure 23. An exponential fit to the readout data is done. Below -17 dBm receiver sensitivity, due to loss of clock, further BER measurement cannot be pursued. However, the plot can be extrapolated based on standard 'erfc' based nature of the curve, assuming Gaussian noise.

Margin of Receiver Sensitivity for targeted BER 10^{-12}

between both the scheme $= (15 - 12.9) \ dBm = 2.1 \ dBm$ (5)

The difference measured is 2.1 dBm as given in Eq. (5). The result is in close agreement to the measurement conducted by Csaba Soos for GBT protocol implementation implemented on Xilinx FPGA [35], that is around 2.5 dBm.

The GBT link Signal Quality. Data from the FPGA transceivers are transmitted using QSFP+ transceiver modules to convert the electrical signals to the optical signals for communication over a single mode fibre. A Lecroy Serial Data Analyser (SDA) oscilloscope is used for analyzing the signal quality. An eye diagram is used as an indicator to measure the quality of the optical transmission signals at the GBT line rate of 4.8 Gbps. The signal to noise ratio of the high-speed data signal is directly indicated by the amount of eye closure or Eye Height. For the GBT transmission signal using a QSFP+ transceiver module, an *eye height* of 406.6 *mV* and an *eye width* of 173.3 *ps* is achieved as shown in the Figure 24.
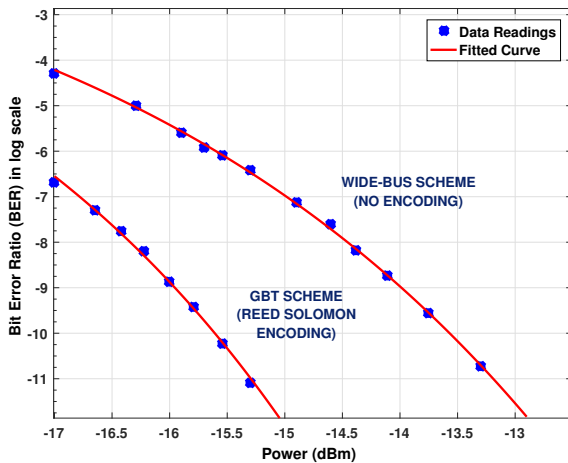
12

Figure 23: Showing GBT BER measurement for GBT and widebus FEC scheme
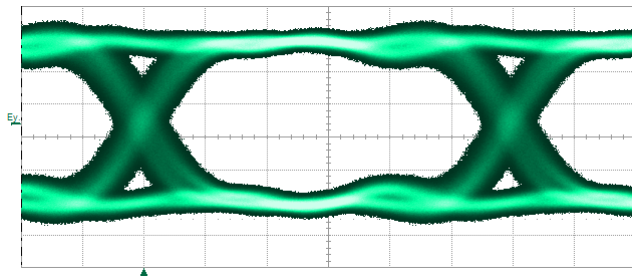

Figure 24: Showing the Eye Diagram for Tx Optical using GBT encoded data for Arria® 10

Power Measurement. Intel internal monitoring tools are used to register the power consumed and the temperature of the Arria® 10 FPGA chip during the test measurement. Figure 25 shows

Table 9: Power consumed by a single GBT link for different encoding scheme

Encoding	Board Temp.	FPGA Temp.	RMS Current (I_{RMS})	Voltage (V)	Power ($P = V \times I_{RMS}$)
Scheme	° C	° C	(mA)	(mV)	(mW)
GBT	37	42	4911.42	914.77	4492.82
Widebus	37	42	4463.20	914.66	4082.31

the power variation plot as monitored using the tool and Table 9 summarizes the results collected when a single GBT link under the different encoding scheme consumes different power.

In the CRU project, the link connecting the radiation hard component to the non-radiation hard component, is based on the GBT link technology operating at 4.8 Gbit/s using a 850 nm multimode optical fibre. The link is connected between the versatile link transceiver to a Multifiber Push-On (MPO) optical connector at the CRU PCIe40 DAQ Engine using an optical fibre splitter. A study has already been conducted by Schwemmer et. al. [36] to note the performance on 400 m long OM3 and OM4 cables. So, further test on optical cable characterization is not pursued.
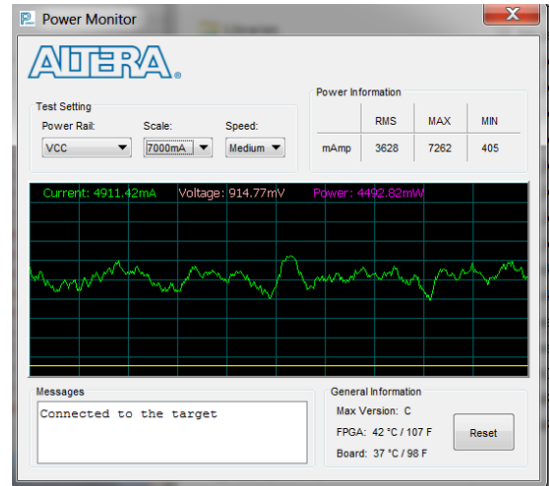
(a)
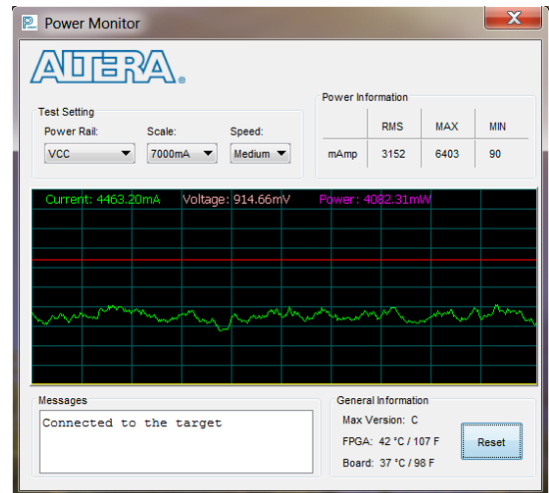
(b)

Figure 25: Showing power Monitor of GBT Firmware during data communication mode in : (a) GBT Scheme and (b) Widebus Scheme

9.3.2. BER Measurement for the TTC-PON

The test setup used for TTC-PON BER measurement is different from the GBT BER measurement. The test setup involves an optical connection from the Kintex® Ultrascale^{TM} FPGA having a Optical Line Terminal (OLT) module to the Intel® Arria® 10 FPGA having a Optical Network Unit (ONU) module. For emulating the real experiment conditions an in-line power attenuator and an optical splitter is used. Details of the experimental setup is illustrated graphically in the Figure 27. The transmission part on the ONU-SFP on the Intel FPGA board was disabled for the upstream path as it was not implemented during the pre-validation measurement test. The ONU just acted as a receiver. A pseudorandom binary sequence (PRBS) generator was incorporate in the OLT Kintex® Ultrascale^{TM} design side while a PRBS checker was used in the

ONU Arria® 10 design side in order to perform the test. Attenuation was changed in the range of 10.0 dB : 1.0 dB : 20.0 dB. For each attenuation value, the average optical received power at the ONU level was measured using the JDSU OLP-87 PON Power Meter. The results are tabulated in the Table 10. Transmitted power of the OLT is +3.67 dBm. For each change in the attenuation value, 5×10^{11} bits are transmitted to measure the quantity of errors.
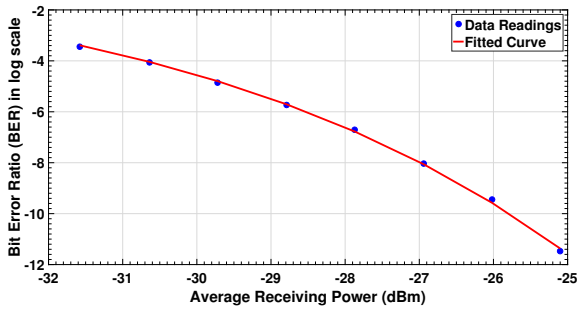

Figure 26: Downstream Bit Error Rate (BER) from the OLT to the ONU

Table 10: Variation of the received power with change in the attenuation

Attenuation (dB)	Received Power (dBm)
20	-31.58
19	-30.64
18	-29.72
17	-28.79
16	-27.87
15	-26.94
14	-26.02
13	-25.10
12	-24.19
11	-23.25
10	-22.32
0	-13.13

The TTC PON Arria® 10 Signal Quality. Figure 28 shows the transmission quality of the optical signal of the TTC-PON from the CTP prototype board, that uses a Xilinx Ultrascale FPGA. The Figure 29 shows the receiving signal quality of the TTC-PON as monitored within the Arria® 10 FPGA using a transceiver toolkit (TTK). The Eye Width to the Eye height ratio of 53/39 is registered in the TTK for the test bits of 1.1E12 using the PRBS31 stress pattern.

9.4. Transceiver Optimization

Transceiver parameter tuning plays a significant role to reduce BER. A test procedure is developed to tune the high-speed link using the signal conditioning circuitry provided in the Arria® 10 transceivers. Quartus v15.1 transceiver testing toolkit [37] is used to monitor the signal characteristics. Several articles
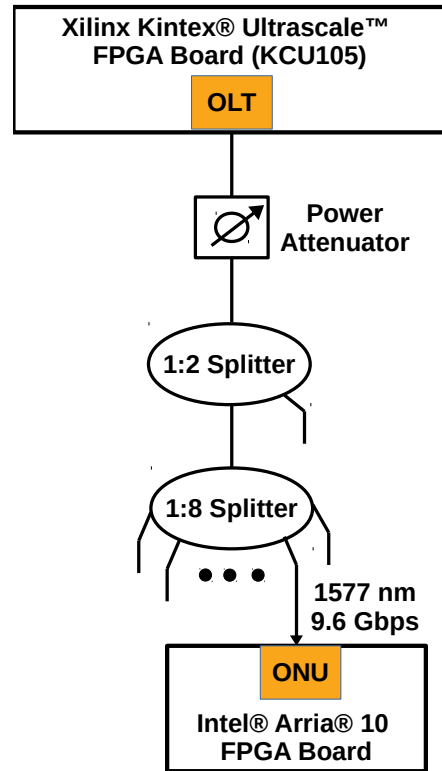

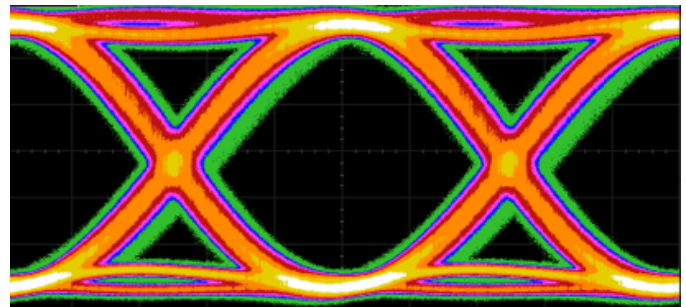Figure 27: The TTC PON signal quality measurement setup.

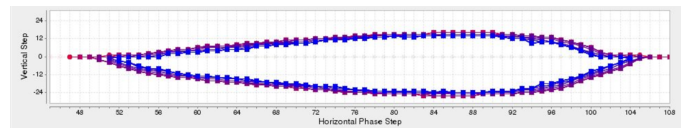Figure 28: TTC PON signal quality analysis in an Agilent Scope by plotting an eye diagram

Figure 29: TTC PON signal quality monitoring using Transceiver Toolkit (TTK) in serial loopback mode.

are mentioned in the Altera (now Intel) literature the need for proper optimization of transceiver for a maximum performance [38] [37] [39] [40]. All those articles are dedicated to the old generation FPGAs like Stratix IV, Cyclone and others, hence a study was necessary to have a first-hand result of the effect of the transceiver tuning on the Arria® 10 FPGAs [22]. For the transceiver tests, the line rate of the GBT that is 4.8 Gbps is

Table 11: The default range of configuration parameters

Parameters	Range			No. of cases
V_{OD}	00	–	31	32
Pre-emphasis 1st post-tap	- 31	–	31	63
Pre-emphasis 1st pre-tap	- 31	–	31	63
Pre-emphasis 2nd post-tap	- 15	–	15	31
Pre-emphasis 1st post-tap	- 07	–	07	15
Equalization	00	–	15	16
VGA	00	–	07	08

Table 12: The optimized range of individual configuration parameters

Parameters	Range			No. of cases
V_{OD}	28	–	31	4
Pre-emphasis 1st post-tap	- 13	–	- 11	3
Pre-emphasis 1st pre-tap	- 03	–	00	4
Pre-emphasis 2nd post-tap	- 04	–	01	6
Pre-emphasis 1st post-tap	- 01	–	01	3
Equalization	00	–	08	9
VGA	04	–	07	4

Table 13: The optimized value of configuration parameters

Parameters	Optimized Value
V_{OD}	28
Pre-emphasis 1st post-tap	-13
Pre-emphasis 1st pre-tap	-03
Pre-emphasis 2nd post-tap	-04
Pre-emphasis 1st post-tap	01
Equalization	00
VGA	05

used in an optical loopback mode. The majority of the links used in the CRU are of GBT standard hence the GBT link rate is selected to carry out the test.

The transceiver optimization by testing for all the combinations would be an inefficient approach as the time required would be very long. A short calculation is given to show the exact measurement time needed to scan for all the configurations. Empirically the reading time for each test configurations is found to be of 10 secs. With the allowed modifiable transceiver properties in Arria® 10 , the configuration range possible for each parameter is listed in the Table 11. The total number of tuples of the configuration cases possible is a pure product of all the test cases, which is given by 32 x 63 x 63 x 31 x 15 x 16 x 8 or 7,559,516,160 (approx 7.5 billion) test cases. The total time needed to execute all the configurations is 2397 years (= 7,559,516,160 x 10 secs = 20,998,656 hrs = 874,944 days).

Instead of spending huge computational time to look for an optimal solution, a good enough workaround is to find a potential suboptimal solution. Individual parameter configuration range are scanned by keeping all other parameters fixed at Intel default values, and obtained a range of optimized values determined from the eye-width to the eye-height ratio in the EyeQ signal monitoring tool. The linear nature of the configuration parameters causes the evaluated optimized values to appear in contiguous subsequence as depicted in the Figure 30. Out of the multiple parameters, the variation of only VOD parameter against the eye height and the eye width using a spider chart is plotted in the Figure 31 to illustrate the procedure.

The parameters can be grouped to optimize separately without having any notable interference effect on the adjacent parameters. Like {VOD}, {Pre-Emphasis 1st Post Tap, Pre-Emphasis 1st Pre Tap}, {Pre-Emphasis 2nd Post Tap, Pre-Emphasis 2nd Pre Tap} and {VGA, EQUALIZATION} can be grouped separately. However, for the fast approximation, the order of optimization is kept same as in the order mentioned. The pictorial representation is illustrated in the Figure 30. Users can change the order for further optimization. By this method, the time taken reduced significantly. The total number of configuration cases comes down to 70 (= 4 + (3 x 4) + (6 x 3) + (9 x 4)). The total time needed is of 11.66 mins (= 70 x 10 secs = 700 secs). The major reason to opt for the quick estimation is to characterize for more than 24 links per CRU board and repeat it for over 100 CRU boards in a short period of time where the result of one board cannot be applied to the other board. Hence, this

heuristic approach is developed.

After the parameters are optimized, the values for the default and the best conditions are shown in the Figure 32. For the entire test, PRBS31 is used to stress the system as it shows the maximum bit transitions among the other available patterns. The eye diagram against the default parameter and the optimized parameter are shown in the Figure 33. The different parameter configurations of the transceiver can share the same eye diagram values or the performance metrics. The set of those values or the configuration parameter tuples are referred as the *solution space*. The obtained best configuration parameters of the device under test is tabulated in the Table 13. The optimized configuration values are highly sensitive and depend on the FPGA process technology, the system temperature and the optical transceiver used. Hence, even for a minor hardware modification, the configuration parameter values need to be re-evaluated.

10. Discussions

The behaviour of all the composite elements in the TTC-PON and GBT bridge connection is analyzed for compatibility regarding interconnection and interoperability. A detailed characterization test on the integrated prototype design is conducted to check for any unanticipated design faults before the final commissioning in CRU firmware. Four performance measuring metrics are used in the characterization: (1) Latency; (2) Jitter; (3) BER and (4) Transceiver parameter settings. The testing phase of the firmware has passed through several iterations of power on/off cycle, firmware upgrade and reset assertion/de-assertion cycle (PFR cycle) for the reliability test of the communication bridge. During the entire study, large sets of empirical results are collected for analysis. The analysis of the statistics confirms that the TTC communication bridge connection with
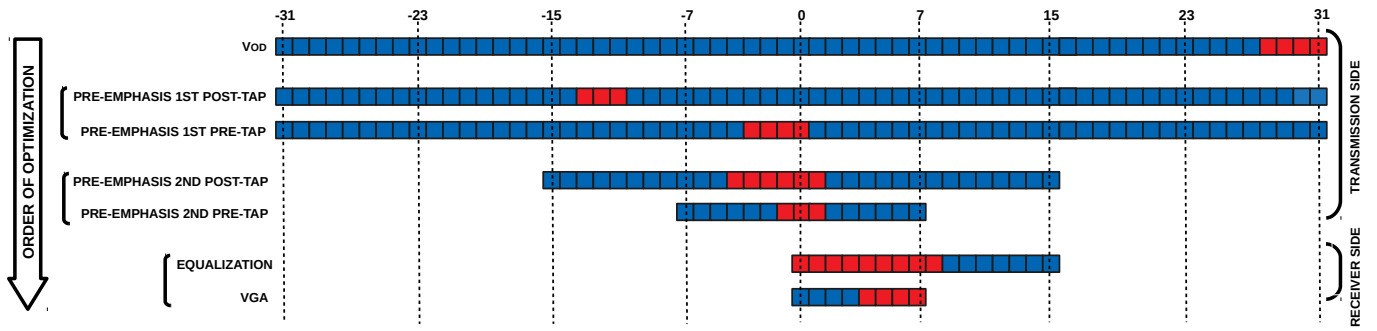
Figure 30: Choice of the optimized values from the complete range of configuration parameters
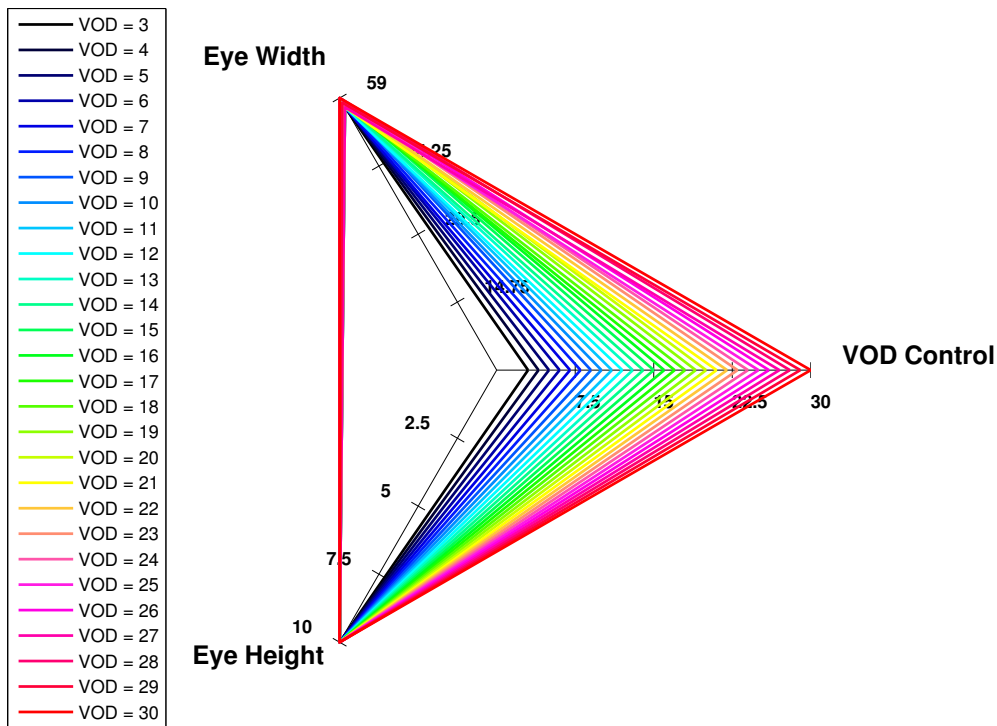

Figure 31: Transceiver parameter tuning plot with VOD variation

its present design configuration showed complete deterministic behaviour with no points of uncertainty over the several rounds of PFR cycle.

The results meet the specified trigger and timing communication standards hence no further compensatory measures are needed. To avoid any unprecedented failure during the data taking; a set of monitoring logic is integrated along with the CRU firmware logic core to register the macroscopic behaviour of the system, as a preventive measure, as mentioned in Section 8. The intrinsic details related to the CRU firmware designs are available at the ALICE-CERN CRU TWiki page [41].

11. Summary and Outlook

We have carried out a detailed study of the trigger and timing distributions using the TTC-PON and GBT bridge connection in ALICE. The study is carried out using the CRU development boards for rapid dissemination of performance metrics. The results show that the TTC-PON and GBT can work in synergy to communicate successfully the timing and trigger information and can effectively be deployed. The study confirmed that the system behaviour is completely deterministic with multiple rounds of PFR cycle. The FPGA used in the CRU board is 20 *nm* Intel® Arria® 10 . The CRU firmware logic uses static placement configuration, hence the stress points remain fixed over the operation runtime. Future scope is to do a reliability study by accelerated stress scenario to mimic the ef-
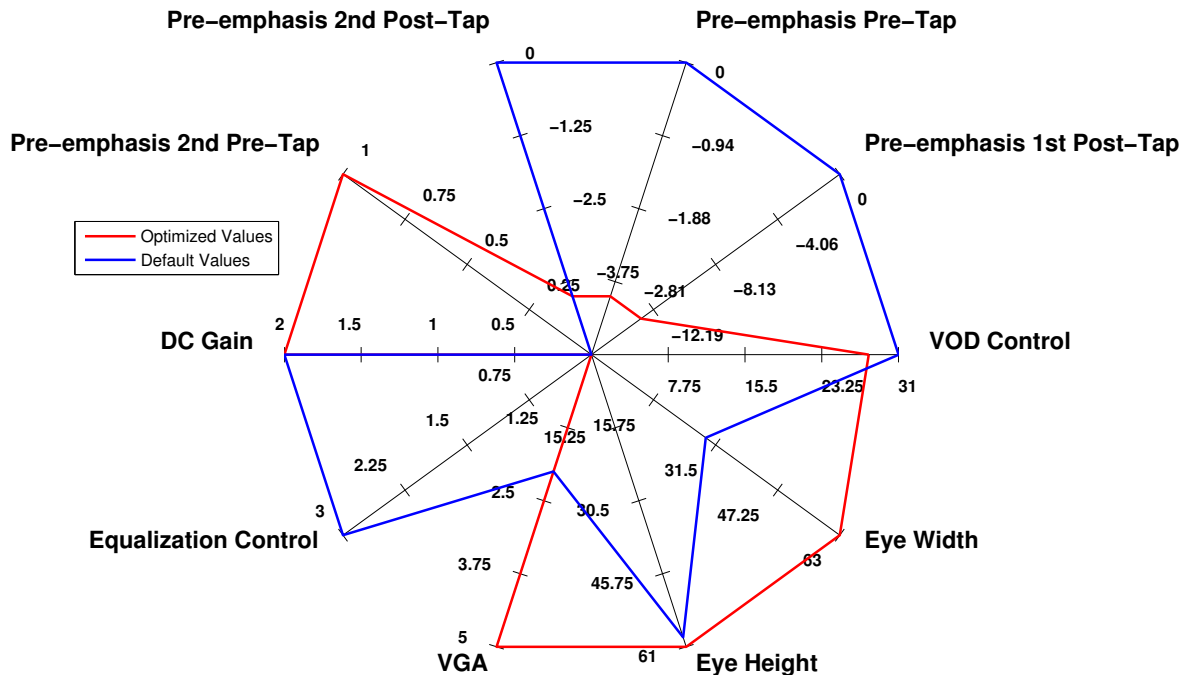
Figure 32: Transceiver parameter tuned showing values for the default settings vs the best settings
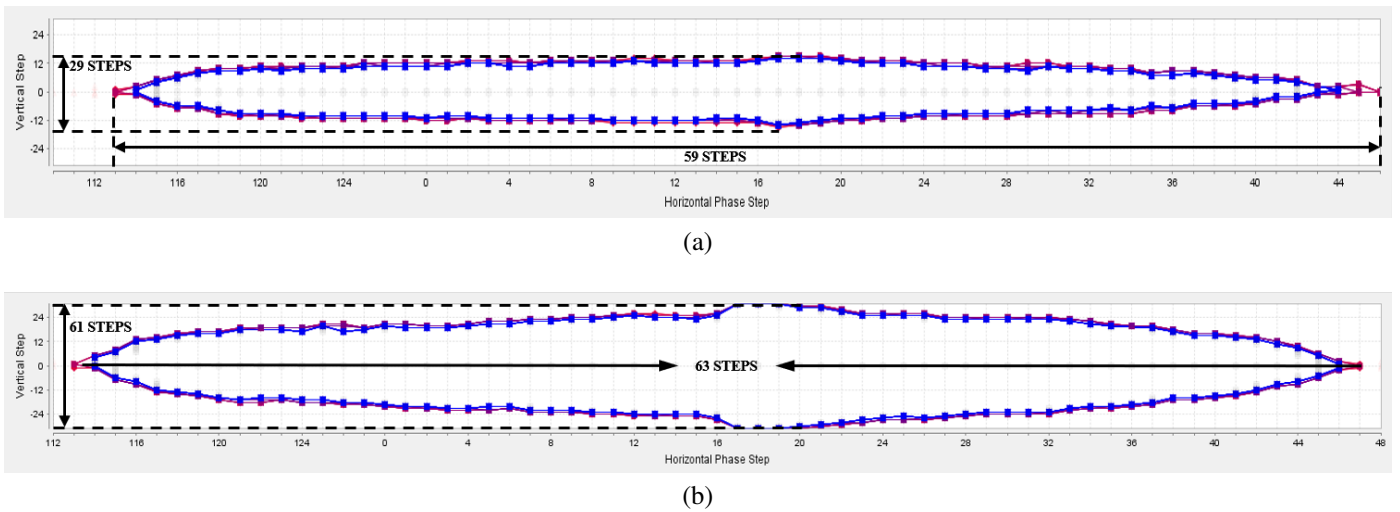

(a)

(b)

Figure 33: Eye Diagram (a) Default parameter settings; (b) Optimized parameter settings

fect of degradation in the timing circuits and wearability in the logic/memory cells [42]. These would identify the stress hotspots and allow us to overcome the system faults by applying the mitigation solutions accordingly. Another study that is equally important is to have a data flow analysis of the spatiotemporal behaviour of the data traffic [43] for each sub-detector system to arrange and reallocate the CRU peripheral logic resources in an optimized manner.

12. Acknowledgement

13. References

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