A Novel Radiation Hardened CAM

O. Anagnostou [1], V. Liberali [2,3], M. Mews [1], **S. Shojaii** [1,3]

[1] The University of Melbourne, Australia
[2] Università degli Studi di Milano, Italy
[3] INFN — Sezione di Milano, Italy

Abstract

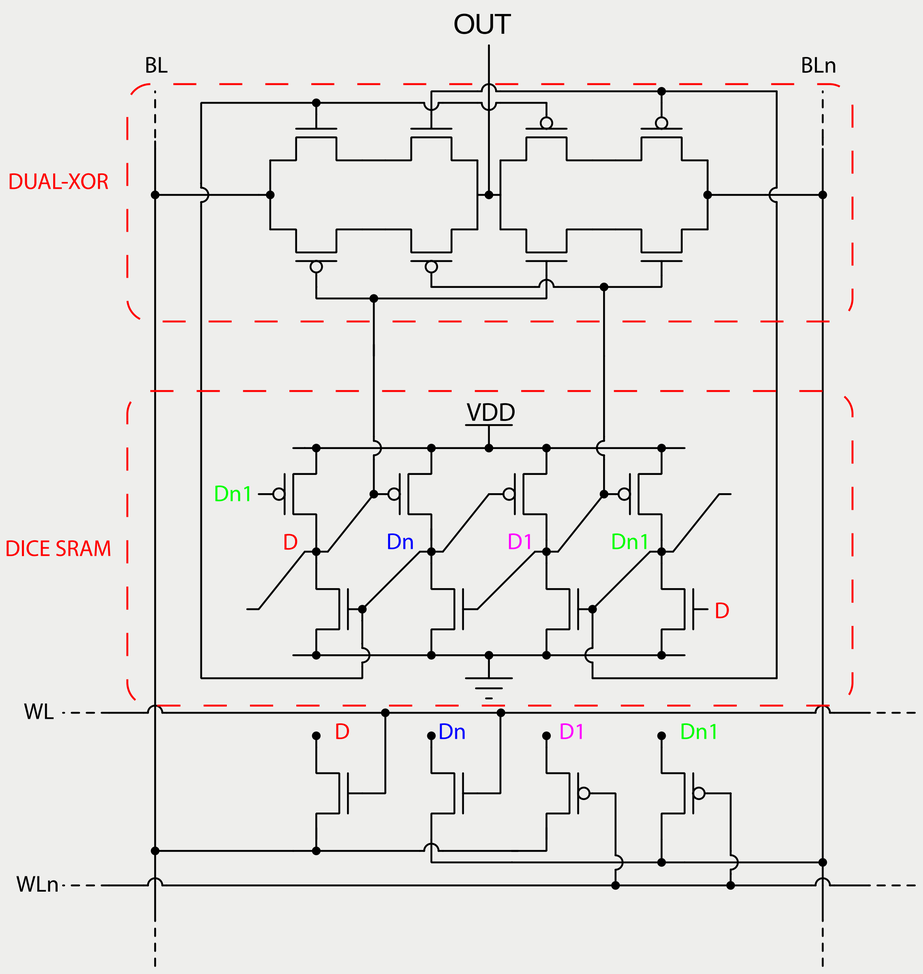
This poster describes an innovative Content Addressable Memory cell with radiation hardened (RH-CAM) architecture. The RH-CAM is designed in a commercial 28 nm CMOS technology. The circuit has been simulated in worst-case conditions, and the effects due to single particles are analyzed by injecting a fault current into a circuit node. The proposed architecture can perform on-time pattern recognition tasks in harsh environments, such as front-end electronics in hadron colliders and in space applications.

Radiation Effects on Electronics

Radiation effects on electronics can be divided into two categories: (1) cumulative effects from long-term exposure, and (2) Single Event Effects (SEE) due to the interaction with a single particle. A soft error is a non-destructive SEE and it occurs when the total charge generated by the impinging particle is larger than the critical charge of the affected node. There are two main types of singe event effect:

- A **Single Event Transient (SET)** is a transient glitch which affects the voltage of a node in combinational logic. Transients are temporary, however, they may propagate to adjacent nodes where the effect of other SET can be added. Sometimes, the sum of SET can trigger damaging effects.
- A **Single Event Upset (SEU)** occurs when an SEE changes the logic value of a memory cell (e.g., a latch), or when SET propagation toggles the data stored into a memory.

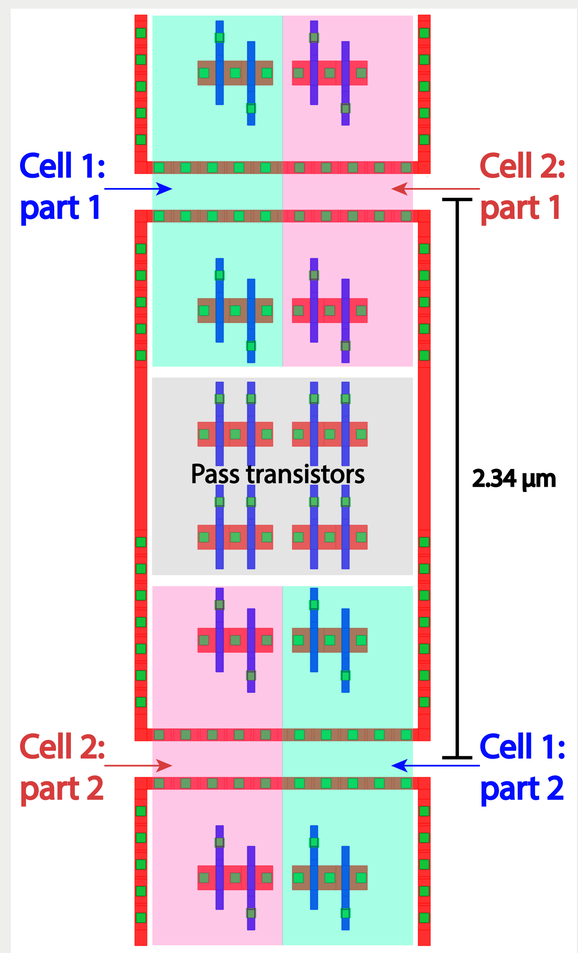
Schematic Diagram and Layout of the RH-CAM Cell



Schematic Diagram of the Radiation Hardened CAM

To avoid the damaging radiation effects on CAM cells in the environments with high level of radiation, an innovative radiation hardened architecture is presented. This architecture has two main parts:

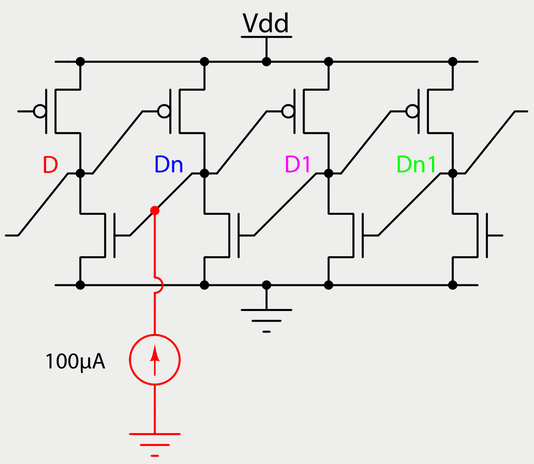
1. Single bit memory cell: The **Dual Interlocked Storage Cell (DICE)** architecture is employed to increase the tolerance of the memory cell to SEU in Radiation Hardened By Design (RHBD) methodology. The DICE memory element employs circuit-level design techniques to prevent SEU: it contains duplicated data. Nodes D and D1 in the figure (left) are *'homologous'* nodes, as they contain the same logic value (nodes Dn and Dn1 are the homologous pair at the opposite logic value). Change of the stored data requires the simultaneous change of both identical bits. Therefore, if a single particle affects the voltage of only one of the nodes in a DICE, then the cell will not exhibit an SEU.
2. Dual-XOR logic: To avoid the Single Event Transient effect of radiation, a dual-XOR gate compares the input logic value which comes from BL and BLn with both the identical bits of DICE cell simultaneously. The output goes to 0 only if the input data matches with both stored bits independently. In this way, any transient effect on each part of both dual-XOR logic and DICE SRAM is mitigated and can not effect the result of the comparison.



Interleaved layout of two Radiation Hardened CAM cells

The layout of HR-XORAM is designed and simulated in 28 nm CMOS TSMC technology. The two identical parts of single DICE memory are interleaved by merging two near-by cells. In this way, the interlocked parts of each DICE SRAM are distanced by **2.34** μm that optimize the tolerance of design to SEU effects.

Simulation of Single Event Effects



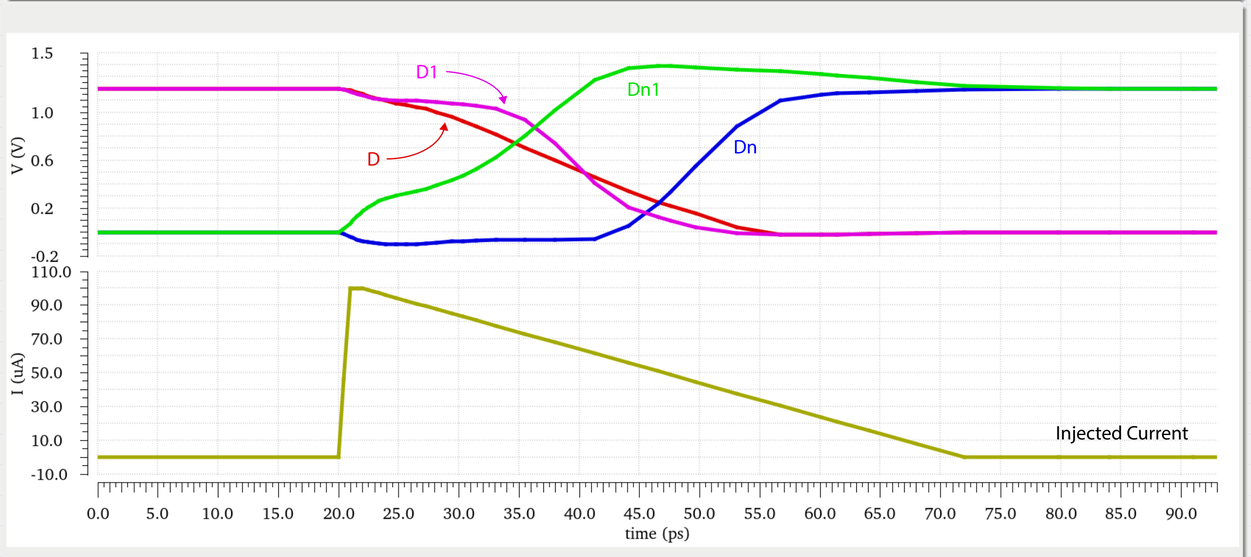
Current injection simulation

Current injection methodology is employed to simulate the Single Event Effects on the most sensitive node of the circuit. The energy required to generate a Hole-Electron Pair (HEP) in silicon is **3.6** ***eV***; thus the collision of a **18** ***MeV*** proton generates $\mathbf{5}\times\mathbf{10^6}$ HEPs, corresponding to total charge of $\boldsymbol{Q = 8 \times 10^{-13}}$ C. The area affected by charge generation has a diameter equal to **1.94** μm, and the charge density is modelled as a discrete triangular distribution.
The transistor nodes only intersect a small fraction of the area of the generated charge, hence only a fraction of the total current will be injected into a node. By taking the ratio of charge dispersion area to transistor active area from the total charge which is generated from collision of **18** ***MeV*** proton, $\mathbf{2.8 \times 10^{-15}}$ ***C*** is dissipating to a single node. We assume an average dissipation of charge at $\boldsymbol{\Delta t = 50}$ ***ps***, giving a current:

$$\boldsymbol{Q = \int Idt = \frac{I \cdot \Delta t}{2}} \quad \Rightarrow \boldsymbol{I} = 112\,\mu\text{A}$$

Simulations were performed by injecting the current into each one of the four nodes, with both possible stored bit values. The flow of the current is adjusted, to obtain the appropriate voltage fluctuation. Nodes with a logic value set to 1 exhibit a voltage spike with recovery proportional to the fall time. However, nodes storing a logic value equal to 0, experienced a permanent logic value change, which propagates to all nodes of the DICE SRAM, thus resulting in the loss of the stored data and causes a SEU event.

Optimization of the Radiation Hardened CAM Cell



DICE simulation injecting 100 µA *on Dn1 fall-time:* **50** ***ps***

The Radiation Hardened CAM design has been modified to withstand the SEU by increasing the transistor width. The optimal solution to the SEU problem (at the cost of increased size) from the simulation results is to use **400** ***nm*** as the width for both P- and N-type MOS transistors.

Conclusion

A novel Radiation Hardened CAM (RH-CAM) architecture is presented. The proposed design has high tolerance to Single Event Effects due to the architecture and high radiation hardness to total ionized dose due to intrinsic radiation tolerance of the 28 nm CMOS technology.
An array of RH-CAM cells can be employed in read-out electronics in extreme applications for real-time pattern recognition tasks. It has the advantages of being programmable during the operation by changing the stored data which will be used for the comparison. Moreover, a preliminary data elaboration in front-end level can decrease significantly the traffic of output data for further elaboration out of experiment environment.

References

S. Shojaii et al., A new XOR-based Content Addressable Memory architecture, Proc. ICECS, Seville, 2012.

shojaii@unimelb.edu.au