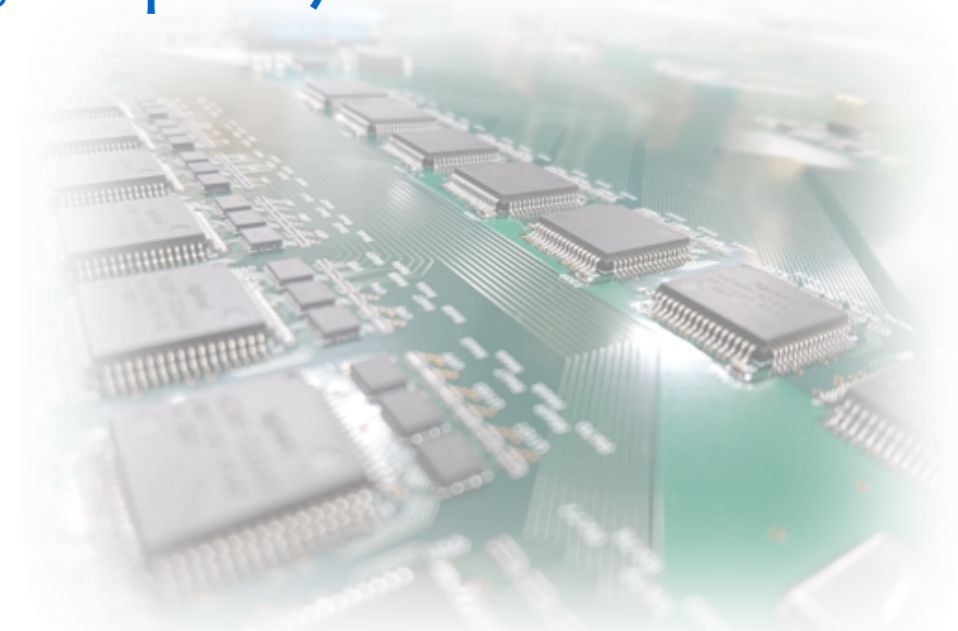# The Phase-1 Upgrade of the ATLAS Level-1 Endcap Muon Trigger

Shunichi Akatsuka (Kyoto University, Japan)

on behalf of the ATLAS Collaboration
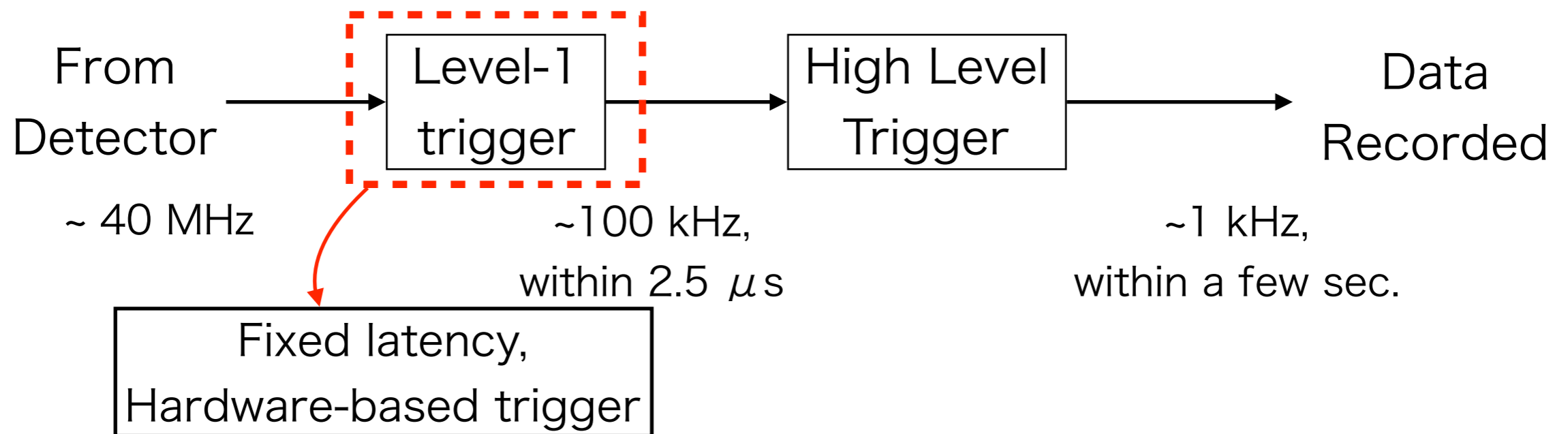
RealTime 2018 @Williamsburg, 9th-15th June, 2018

Introduction

◆ LHC Run 3: 2021~ 2023

▸ $\sqrt{s}$ = 14 TeV, instantaneous luminosity will be 3.0×10^{34} cm^{-2}s^{-1}

+50 % compared to Run 2 luminosity of ~2.0×10^{34} cm^{-2}s^{-1}

▸ Integrated luminosity estimated to be ~150 fb^{-1} → Run 2 + Run 3 = 300 fb^{-1}

◆ ATLAS Trigger System - basic scheme will remain the same in Run 3

From Detector	Level-1 trigger	High Level Trigger	Data Recorded

~ 40 MHz   ~100 kHz,   ~1 kHz,
                  within 2.5 μs   within a few sec.
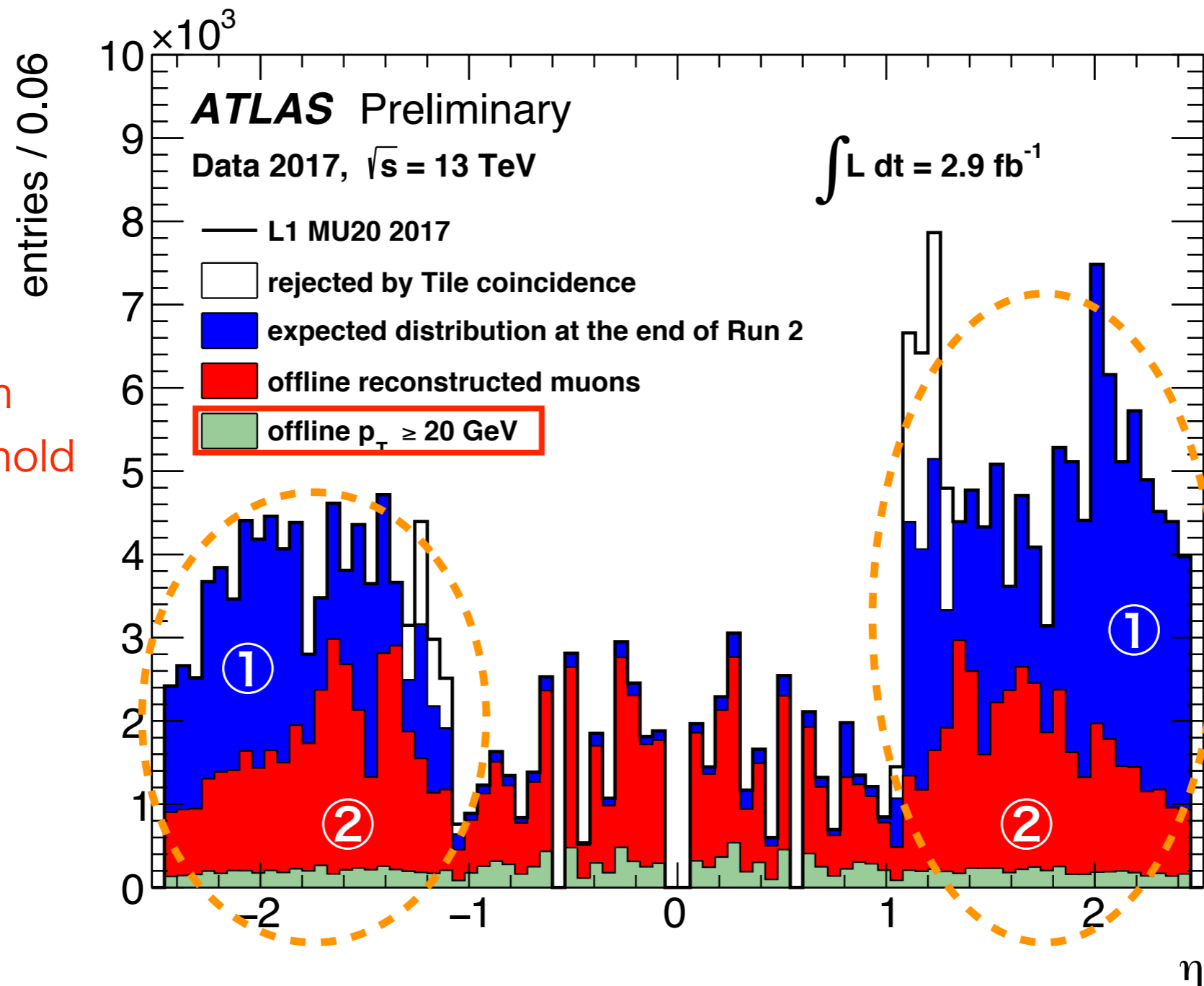
Fixed latency,
Hardware-based trigger

◆ Phase-1 Upgrade for Level-1 Muon Trigger

▸ With Run 2 trigger algorithm, the rate for muon trigger with p_T > 20 GeV (L1_MU20) will become **30 kHz** @ 3.0×10^{34} cm^{-2}s^{-1}

▸ Run 3 requirement at this luminosity is **15 kHz** (TDAQ TDR, ATLAS-TDR-023)

▸ More powerful trigger strategy is needed to reduce the trigger rate, while keeping the trigger threshold and the efficiency

L1 Muon Trigger in Run 2

◆ Run 2 Level-1 muon trigger rate is dominated by:
  ① Triggers with **no matching real muons (Fake triggers)**
  ② Triggers by **Low p_T muons**
  especially in $|\eta| > 1$ region (Endcap region).
 → **Strategy: Reject these triggers by introducing new "coincidence logic"**

muons with p_T over threshold

ATLAS Preliminary
Data 2017, $\sqrt{s}$ = 13 TeV

$\int L\,dt$ = 2.9 fb^{-1}

— L1 MU20 2017
☐ **rejected by Tile coincidence**
■ **expected distribution at the end of Run 2**
■ **offline reconstructed muons**
■ **offline $p_T \geq$ 20 GeV**

L1 Muon Endcap Trigger in Run 3

- ◆ Run 3 Trigger scheme overview
  - ‣ TGC BW hit position defines the RoI, which will be the trigger seed.
  - ‣ TGC Big Wheel local dR/dPhi coincidence logic calculates the p_T of the track.
  - ‣ Require additional inner coincidence to reject fakes, and also to re-calculate the p_T
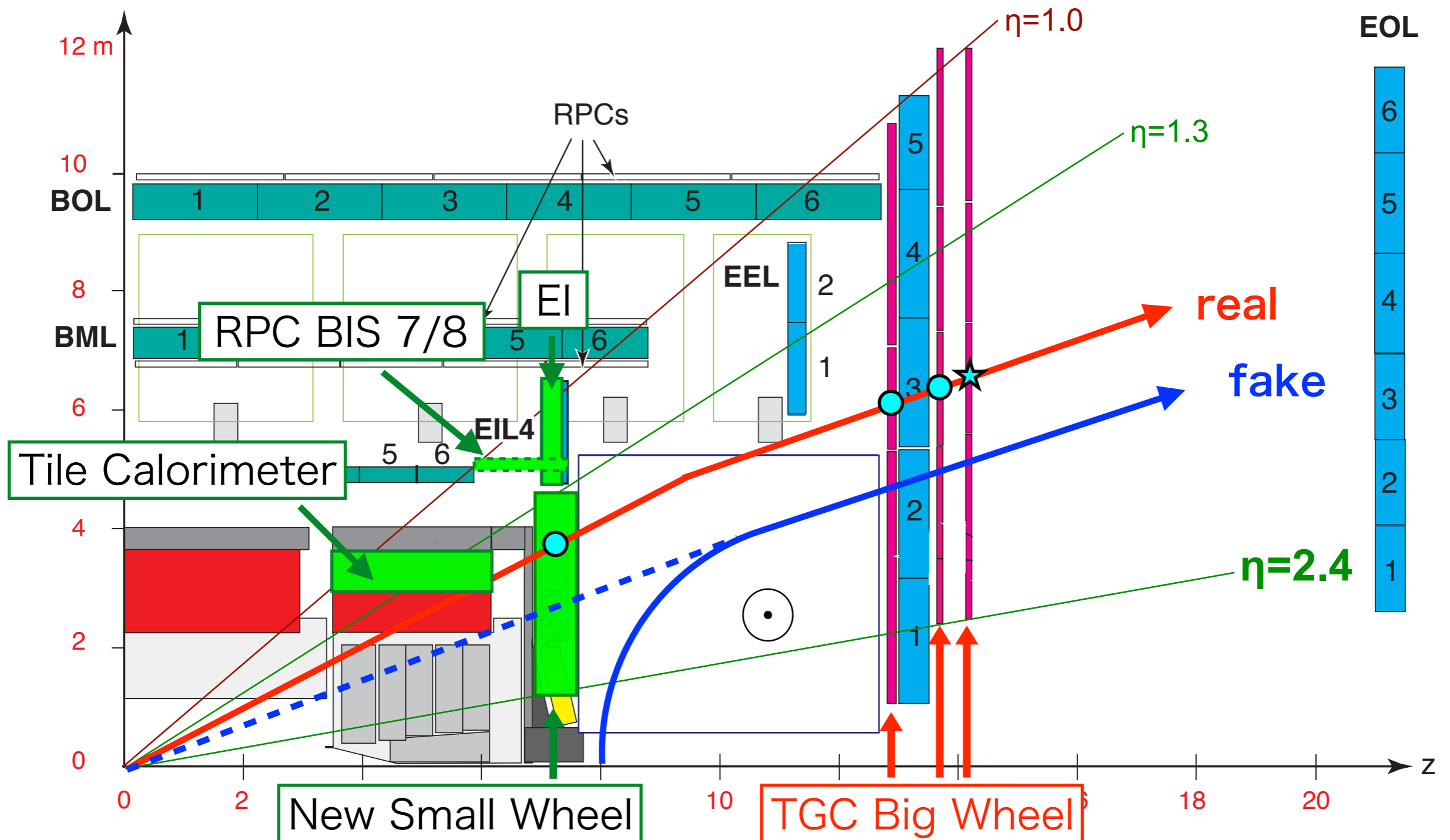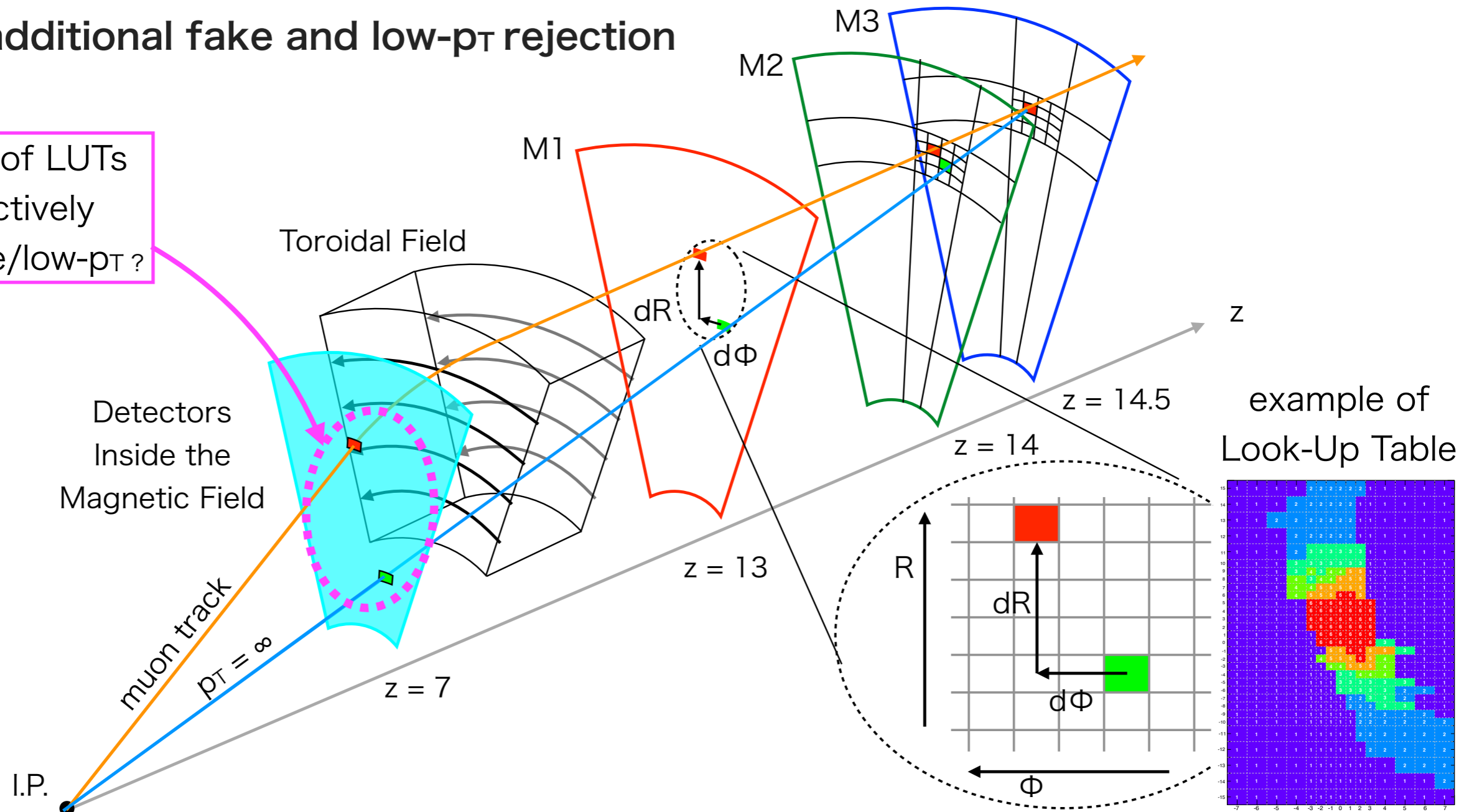
Online hardware triggering

◆ Main idea of the trigger logic:

‣ dR, dϕ defined as the hit position difference between M1and M3

‣ dR, dϕ are handed over to a Look-Up-Table,
which immediately returns the trigger decision and the candidate's p_T

‣ Similar logic to take coincidence with detectors inside to reject fake/low-p_T muons
→ **New LUT for the Inner Coincidence is needed**
for additional fake and low-p_T rejection

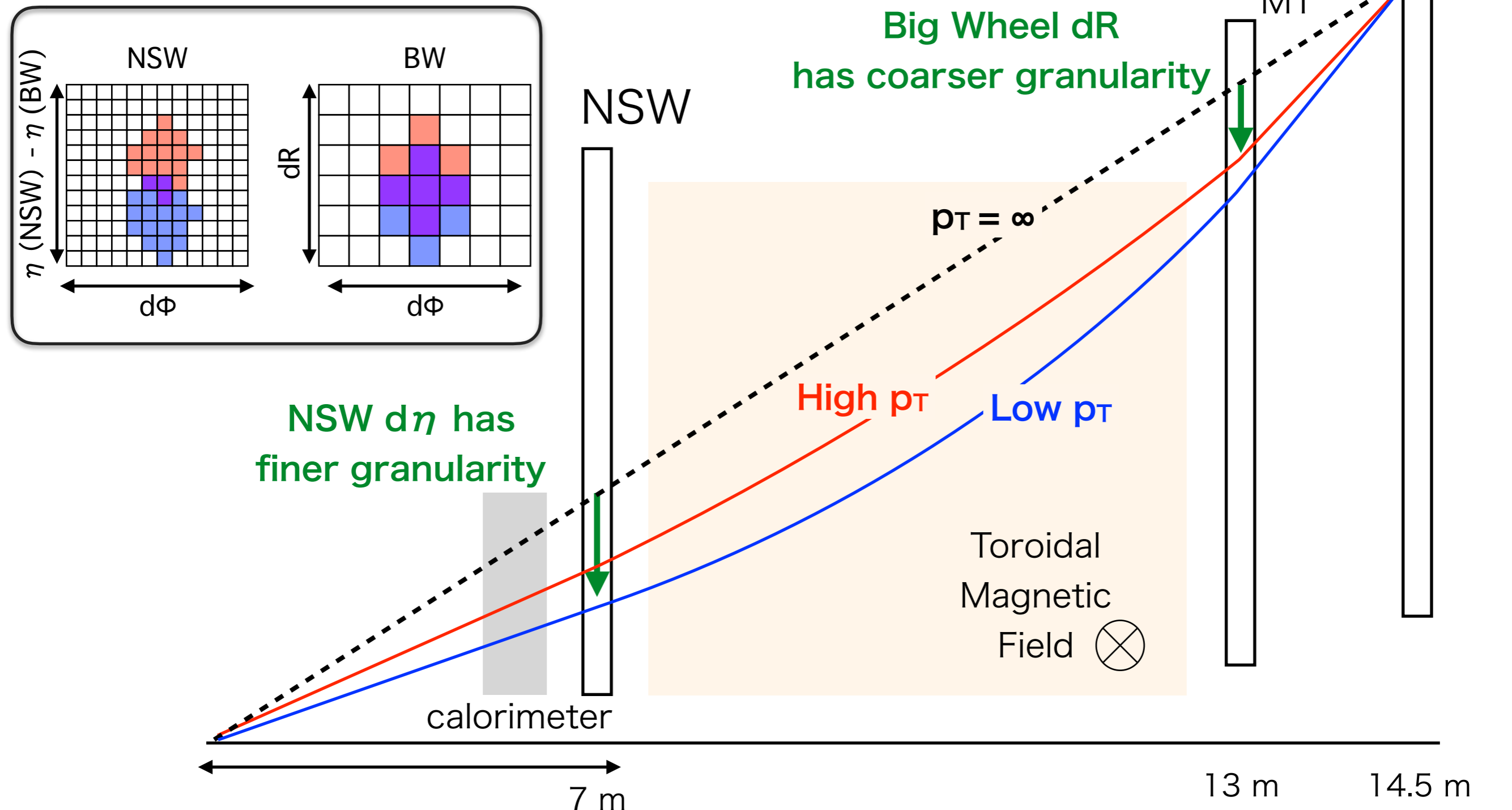What sort of LUTs can effectively reduce fake/low-p_T ?

M3

M2

M1

Toroidal Field

dR

dΦ

z

Detectors Inside the Magnetic Field

z = 14.5

z = 14

z = 13

example of Look-Up Table

muon track

$p_T = \infty$

z = 7

R

dR

dΦ

Φ

I.P.

Inner Coincidence Logic (1)

◆ Position matching
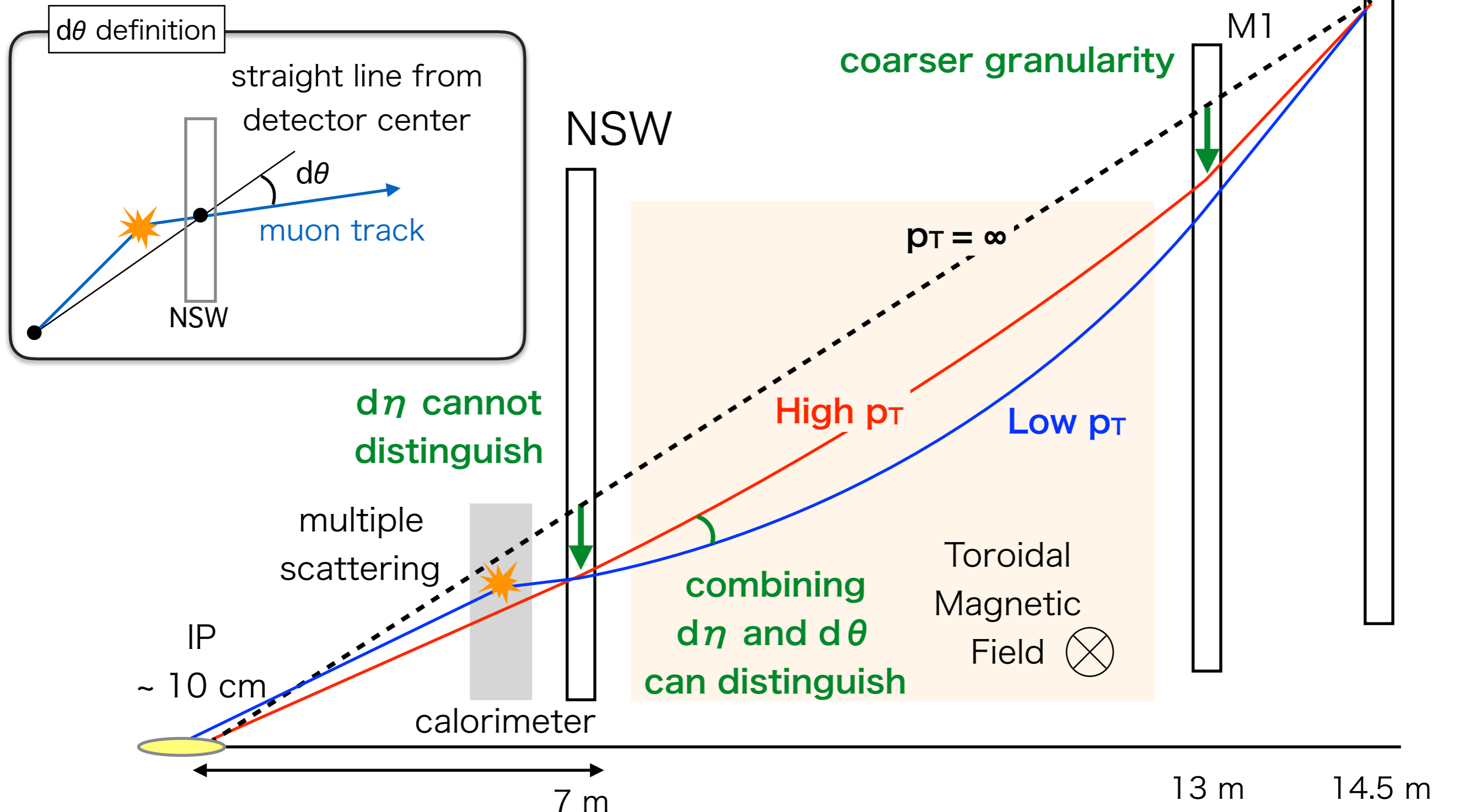
  ‣ Matching between TGC BW and Inner station hit position.
  ‣ Fake triggers can be rejected dramatically
  ‣ Low-p_T muons can also be rejected (with enough granularity at inner station)

TGC BW

M3

M1

Big Wheel dR has coarser granularity

NSW

NSW dη has finer granularity

$p_T = \infty$

High p_T **Low p_T**

Toroidal Magnetic Field $\otimes$

NSW   BW

η (NSW) - η (BW)

dR

dΦ dΦ

calorimeter

7 m   13 m   14.5 m

Inner Coincidence Logic (2)

- Angle matching
  - Angle information at the inner station can be used to further reject the low-p_T triggers.
  - Combine position and angle to tag muons with large incident angle

dθ definition

straight line from detector center

dθ

muon track

NSW

TGC BW

M3

M1

coarser granularity

NSW

$p_T = \infty$

dη cannot distinguish

High p_T

Low p_T

multiple scattering

combining dη and dθ can distinguish

Toroidal Magnetic Field $\otimes$

IP ~ 10 cm

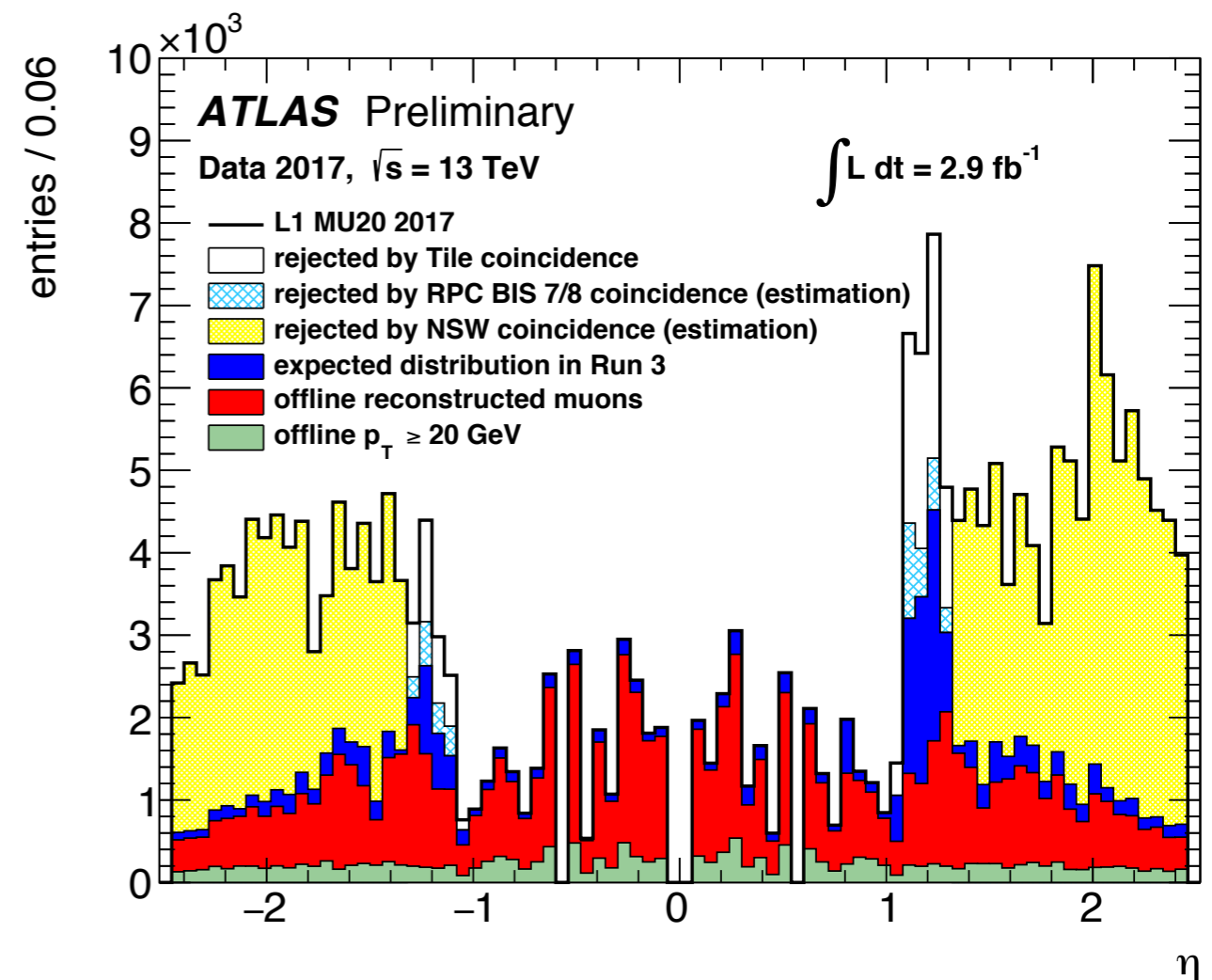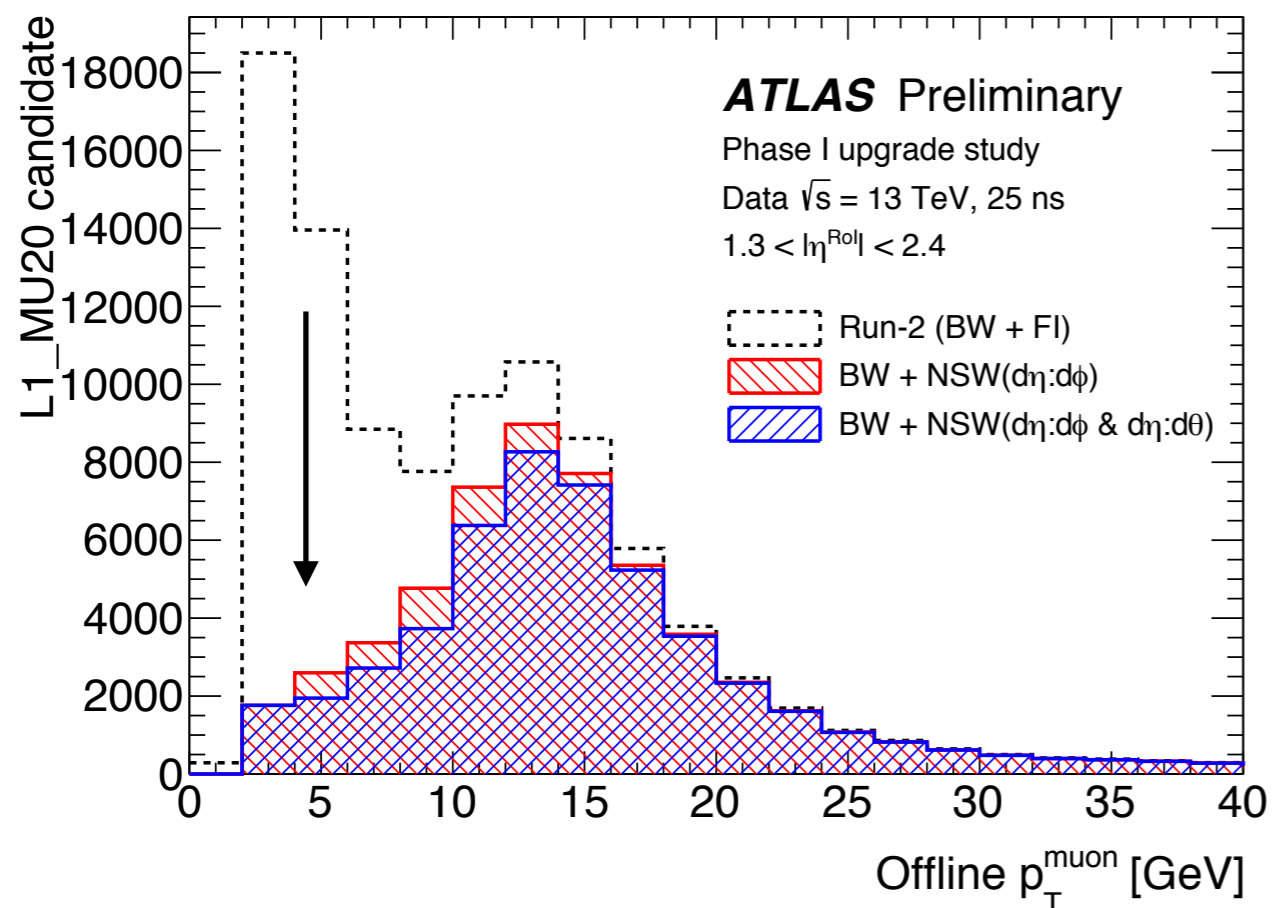calorimeter

7 m

13 m

14.5 m

Trigger performance studies (1)

◆ Fake rejection power estimation

- ‣ Fakes cannot be modeled in MC, so we used 2017 data for the estimation.
- ‣ MDT segments are used to emulate NSW, by smearing its position and angles resolution to NSW resolution for the Level-1 trigger
- ‣ ~90% fake triggers are rejected with η- and (rough) phi- position coincidence

◆ Low-p_T rejection power estimation

- ‣ Single muon MC is used to estimate low-p_T rejection for NSW and RPC BIS7/8.
- ‣ Low-p_T candidates are rejected effectively: -50% @10 GeV, -85% @5 GeV

Trigger performance studies (2)

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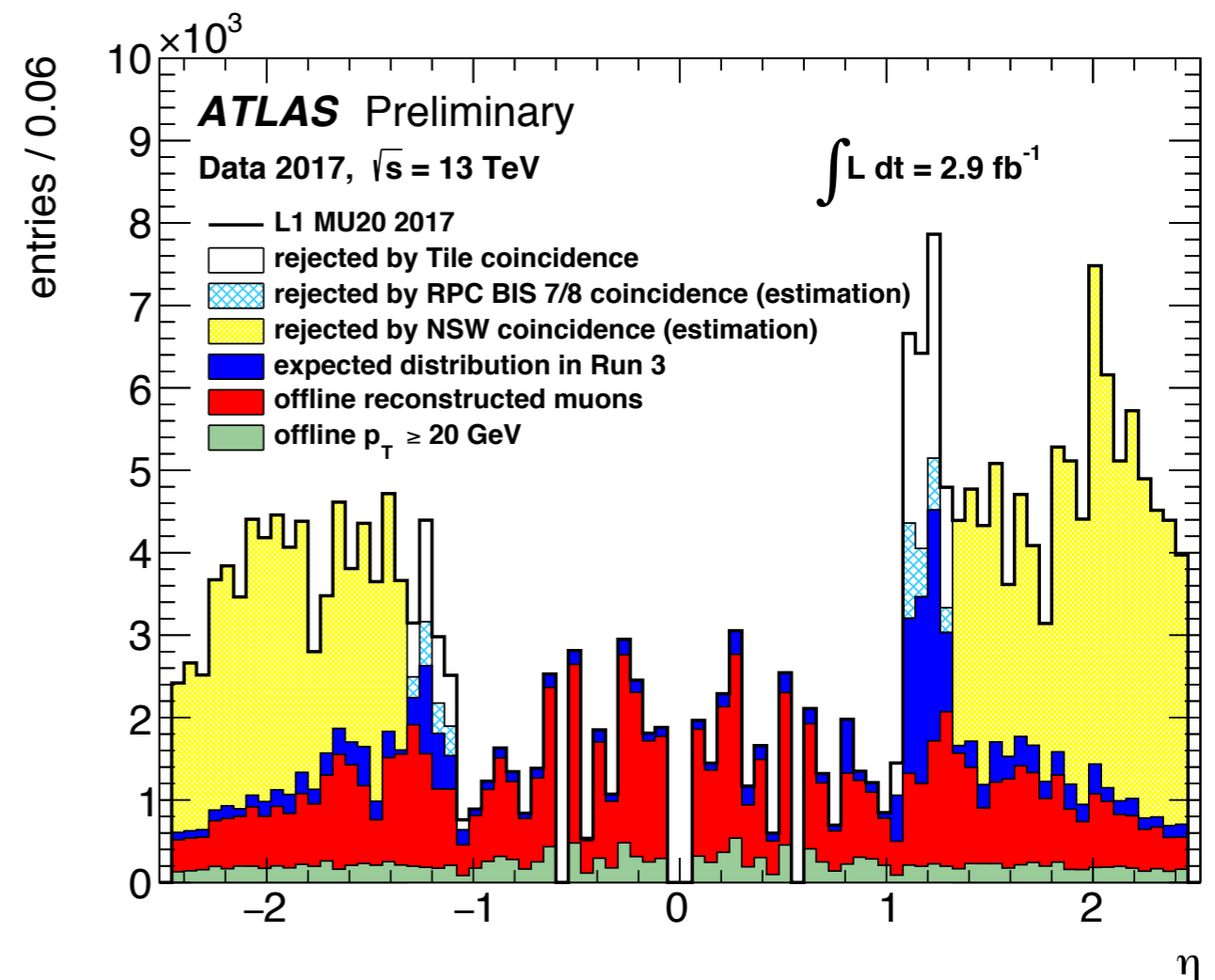
◆ Rate reduction and efficiency
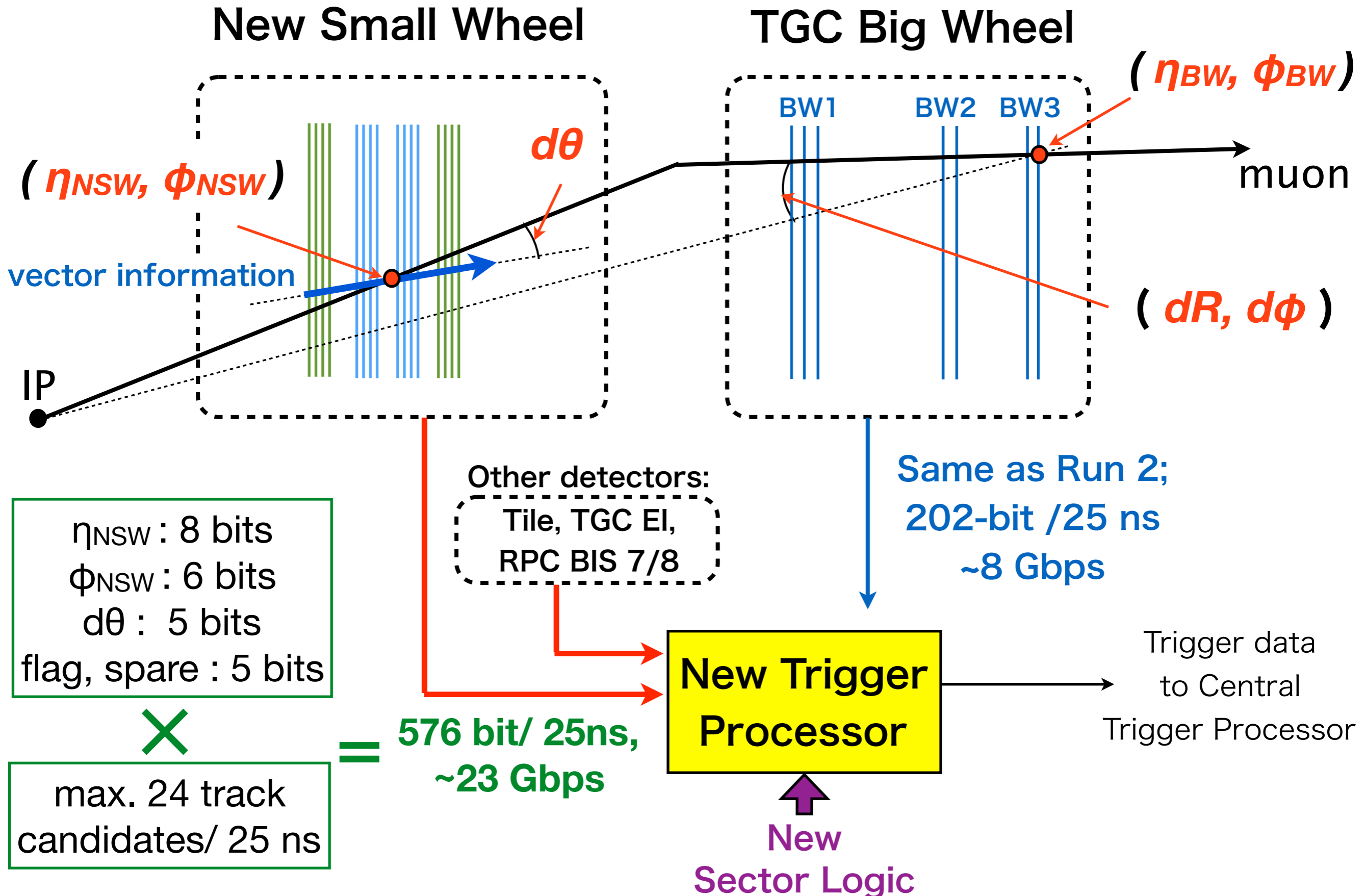
‣ Rate reduction
Run 2 extrapolation: **30 kHz**
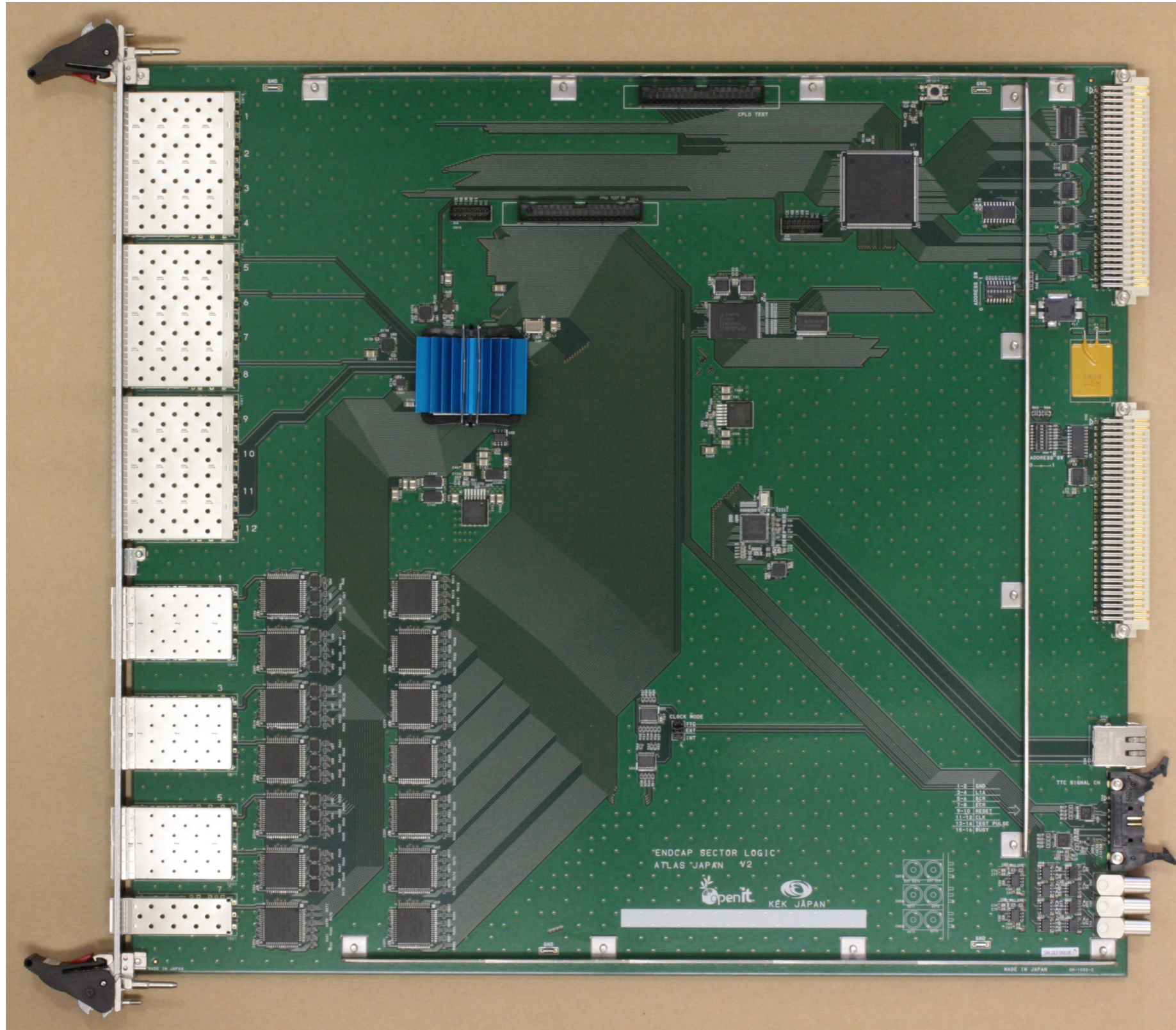Run 3 **14.2 kHz (~53% rate reduction)**

‣ Efficiency
~ 95% for muons with p_T > 20 GeV, relative to Run2 trigger
(assuming NSW segment finding efficiency 97%)

New Small Wheel

TGC Big Wheel

(η_{BW}, ϕ_{BW})

BW1   BW2   BW3

(η_{NSW}, ϕ_{NSW})

$d\theta$

muon

vector information

$(dR, d\phi)$

IP

η_{NSW} : 8 bits
ϕ_{NSW} : 6 bits
$d\theta$: 5 bits
flag, spare : 5 bits

$\times$

max. 24 track candidates/ 25 ns

Other detectors:
Tile, TGC EI,
RPC BIS 7/8

Same as Run 2;
202-bit /25 ns
~8 Gbps

= **576 bit/ 25ns,
~23 Gbps**

**New Trigger
Processor**

Trigger data
to Central
Trigger Processor

**New
Sector Logic**

New Sector Logic Board design

Optical interfaces to use
GTX transceiver* at 6.4 Gbps
12 lanes × 6.4 Gbps = 76.8 Gbps
for NSW and Tile, BIS7/8 **

Xilinx Kintex-7
XC7K410T

795 × 36 Kb Block RAM
→ × 20 times the resource compared to
the FPGA for the current trigger board

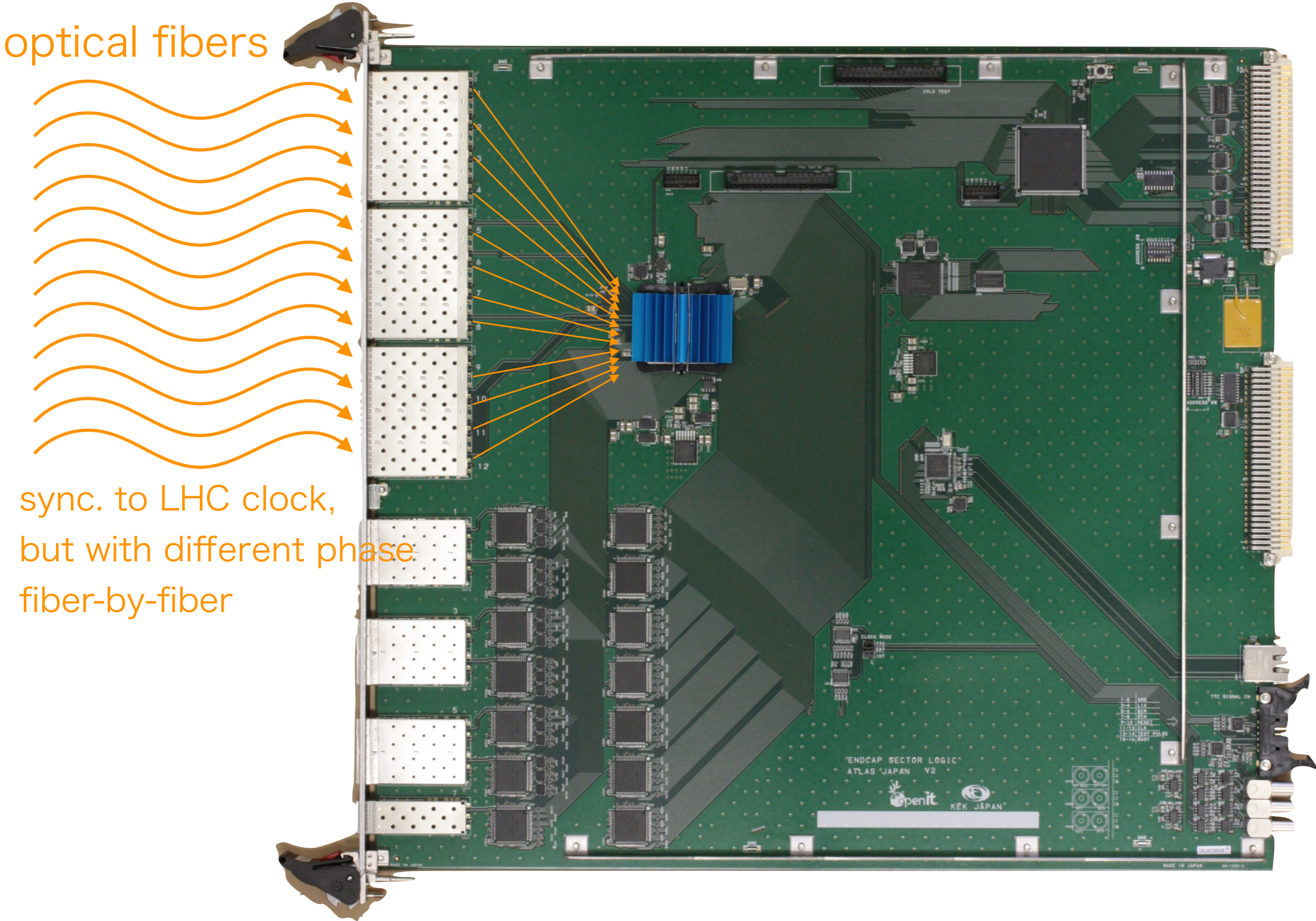Optical interfaces for
G-Link connection at 0.8 Gbps
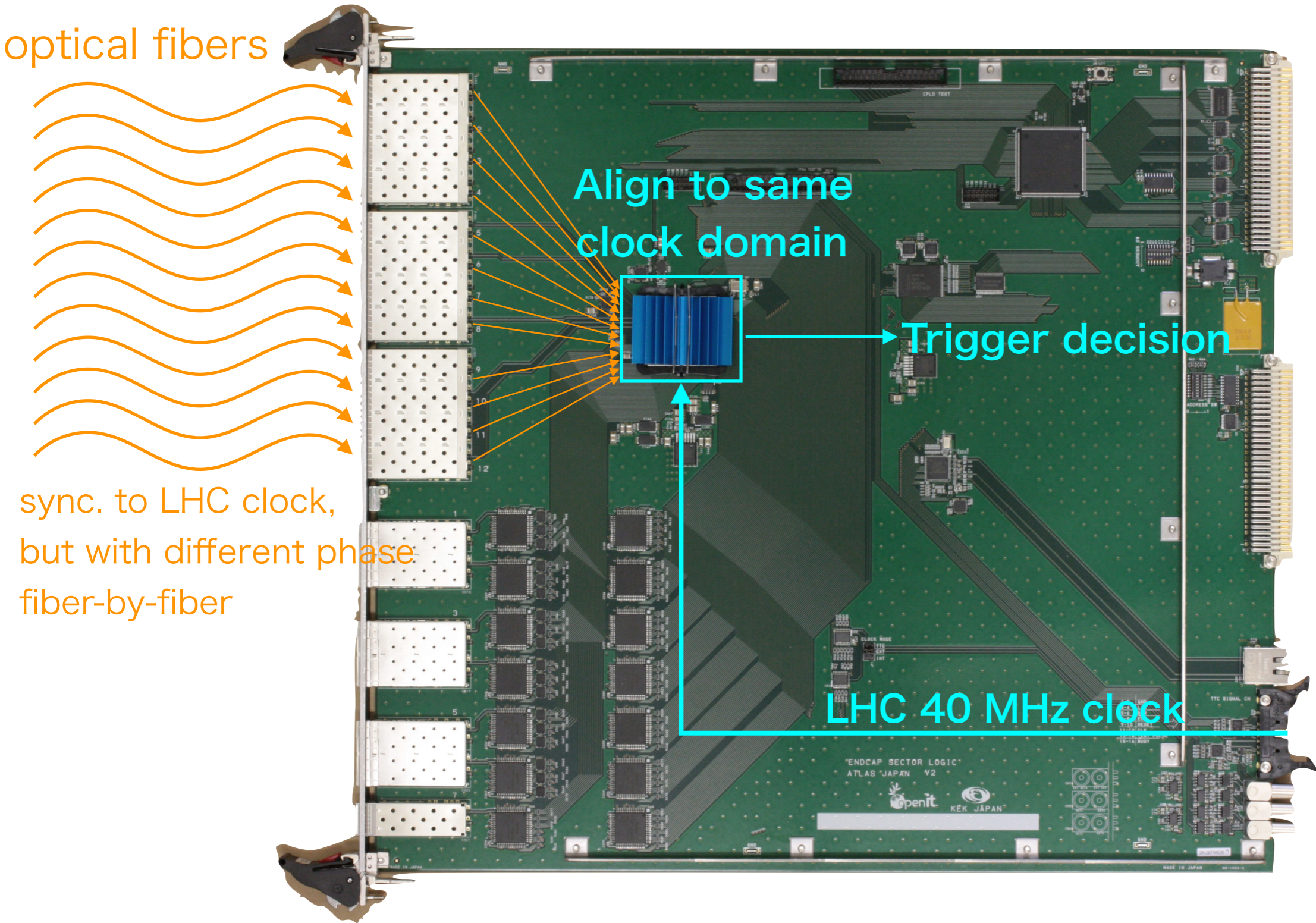14 × 0.8 Gbps = 11.2 Gbps
for TGC BW and EI

* GTX: multi-gigabit transceivers for Xilinx Kintex-7 FPGAs [Link]

** For Tile, we actually use 1.6 Gbps × 2 lanes

Firmware design for Fixed Latency

optical fibers

sync. to LHC clock,
but with different phase
fiber-by-fiber

optical fibers

Align to same
clock domain

Trigger decision

sync. to LHC clock,
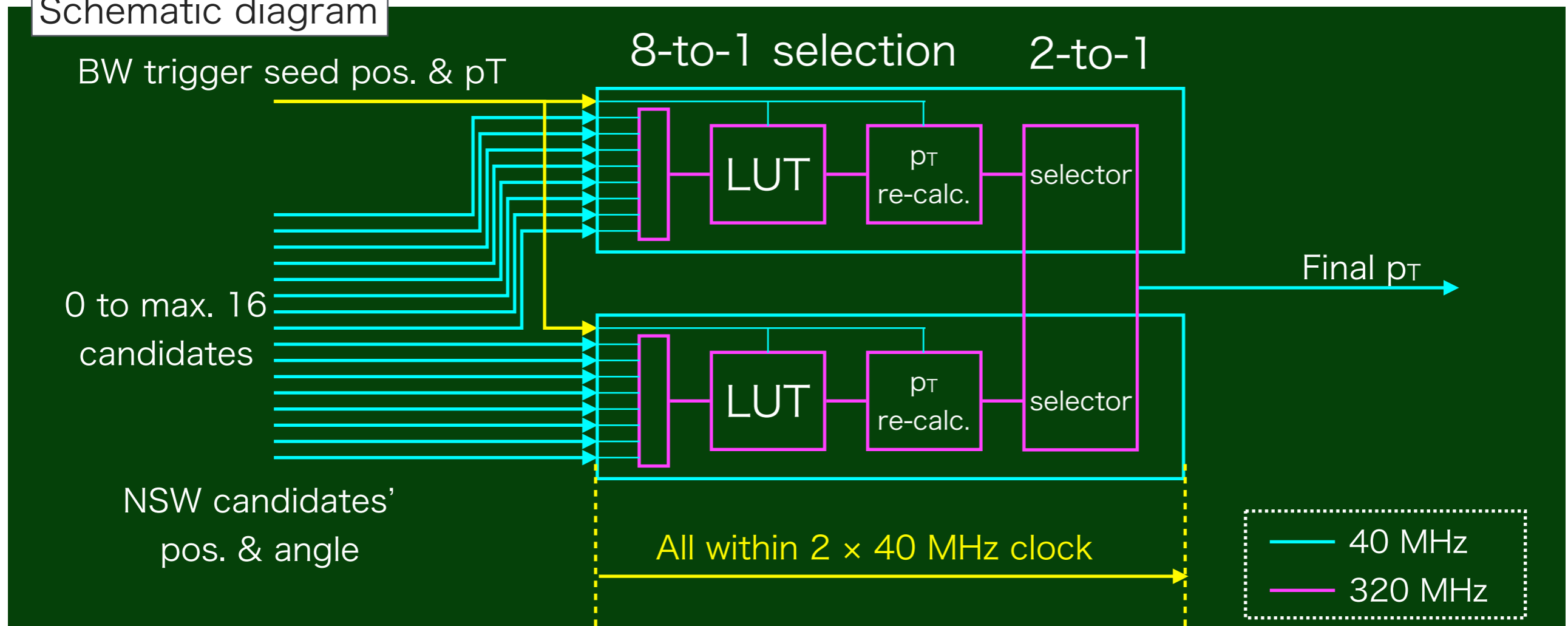but with different phase
fiber-by-fiber
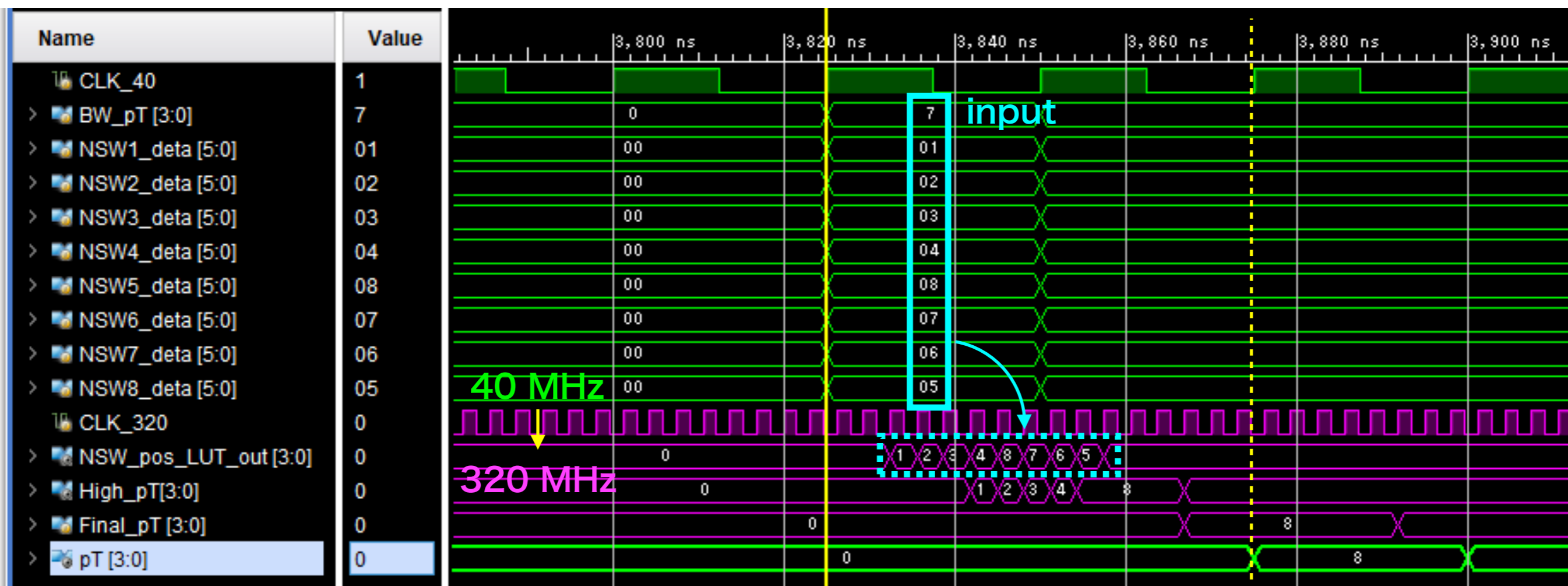
LHC 40 MHz clock

Firmware design for Fixed Latency

◆ Trigger decision part

‣ Maximum 16 inner station candidates will be given for 1 BW trigger seed

‣ Regardless of the number of candidates, we need the trigger decision in a fixed (and small) latency. What can we do?

-> Try taking coincidence with all 16 candidates, choose the best one among them

‣ In a simple implementation, this requires 16 times the latency, or 16 same LUTs, which is not realistic in terms of latency/resource on FPGA.

-> Use a faster clock to re-use the same LUT while keeping the latency small
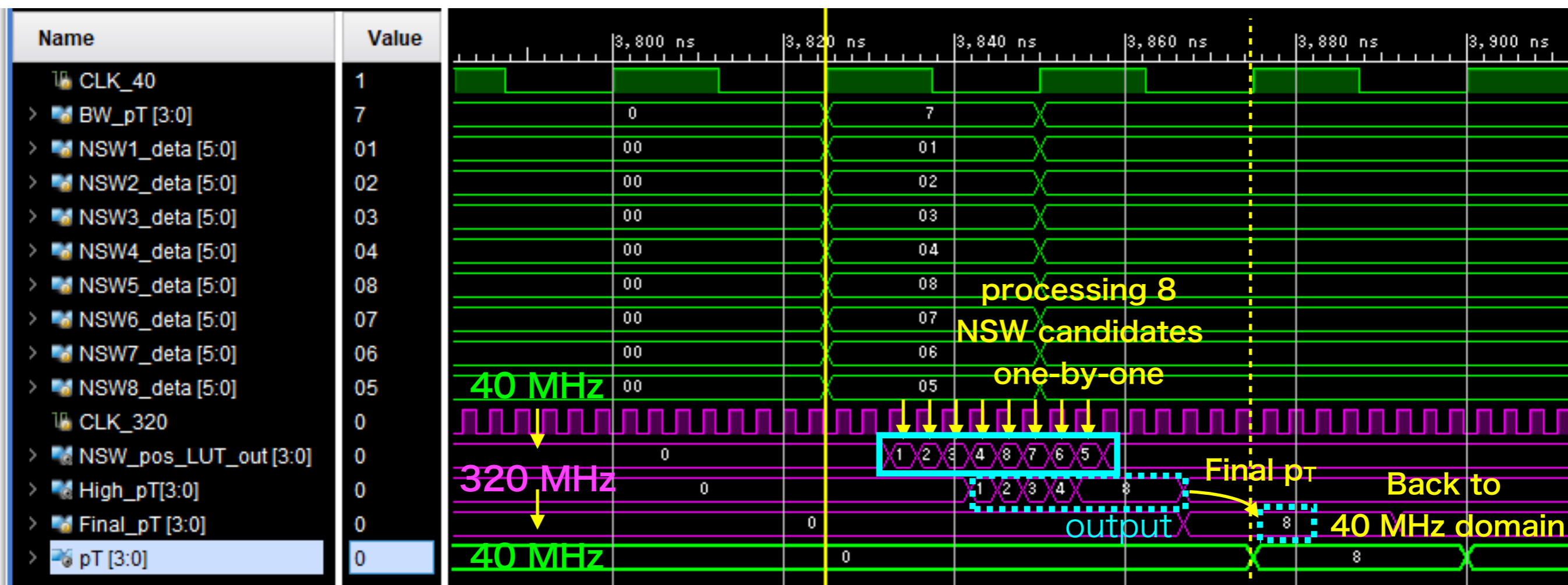

Schematic diagram

Test results

◆ Firmware logic test for trigger part

‣ Simulation test for trigger part, on Vivado software (Xilinx compiler, Link)

‣ Shown below is an example of very simple test, where:

  ‣ 1 LUT is implemented to process 8 candidates one-by-one, on 320 MHz clock.

  ‣ The LUT simply returns least-significant 3 bits of the input address.

‣ Other tests are successfully done with different input patterns,
  not only on simulation but also on the actual SL board.

‣ Tests using more realistic LUTs (created from MC data), is ongoing.

Test results

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Summary

- Upgrade of the muon trigger system is essential for Run 3:
  - The main strategy is to take coincidence with NSW and other detectors, to reject fake and low p_T muons.
  - New hardware is needed to combine data from current trigger chamber BW, NSW, and several other detectors.

- Trigger Logic and Performance
  - Taking position matching and angle matching between BW and NSW can reject low p_T muon candidates effectively.
  - The estimated rate is 14.2 kHz @ L = 3.0×10^{34} cm^{-2}s^{-1}, which meets the Run3 requirement of 15 kHz. (ATLAS-TDR-023)

- Hardware and Firmware development
  - New trigger processor board, New Sector Logic, has been produced for Run3.
  - Firmware is fully-designed with all the trigger LUTs implemented.
  - Fast clock is used in the trigger logic to overcome the latency limitation while keeping the FPGA resource usage reasonable.

backup slides

Physics Motivation

◆ Run 3 trigger rate estimation   ◆ Physics Acceptance
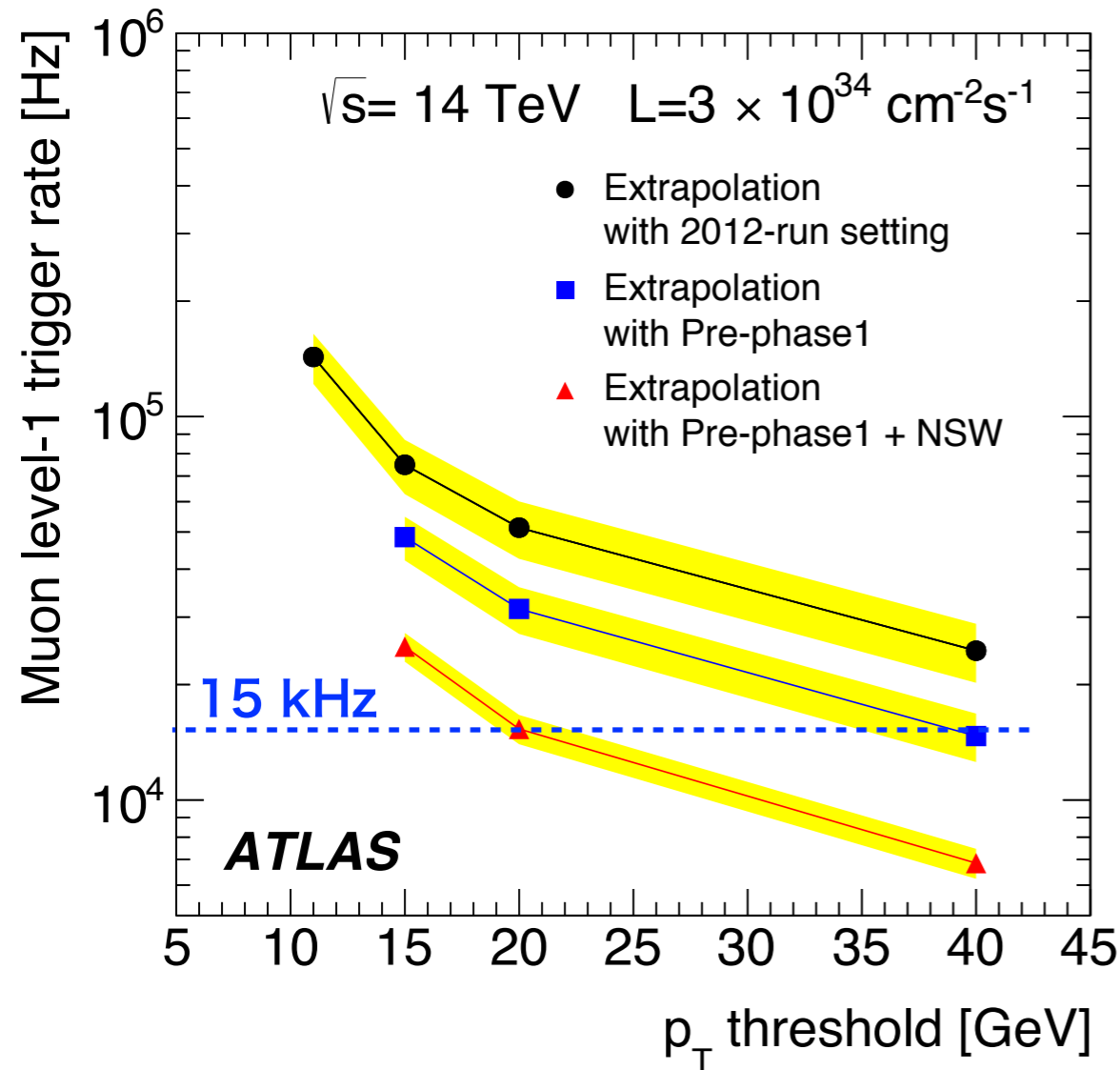
‣ Without the phase-1 upgrade, to keep the trigger rate to the require level, the p_T threshold will need to be raised to ~40 GeV.
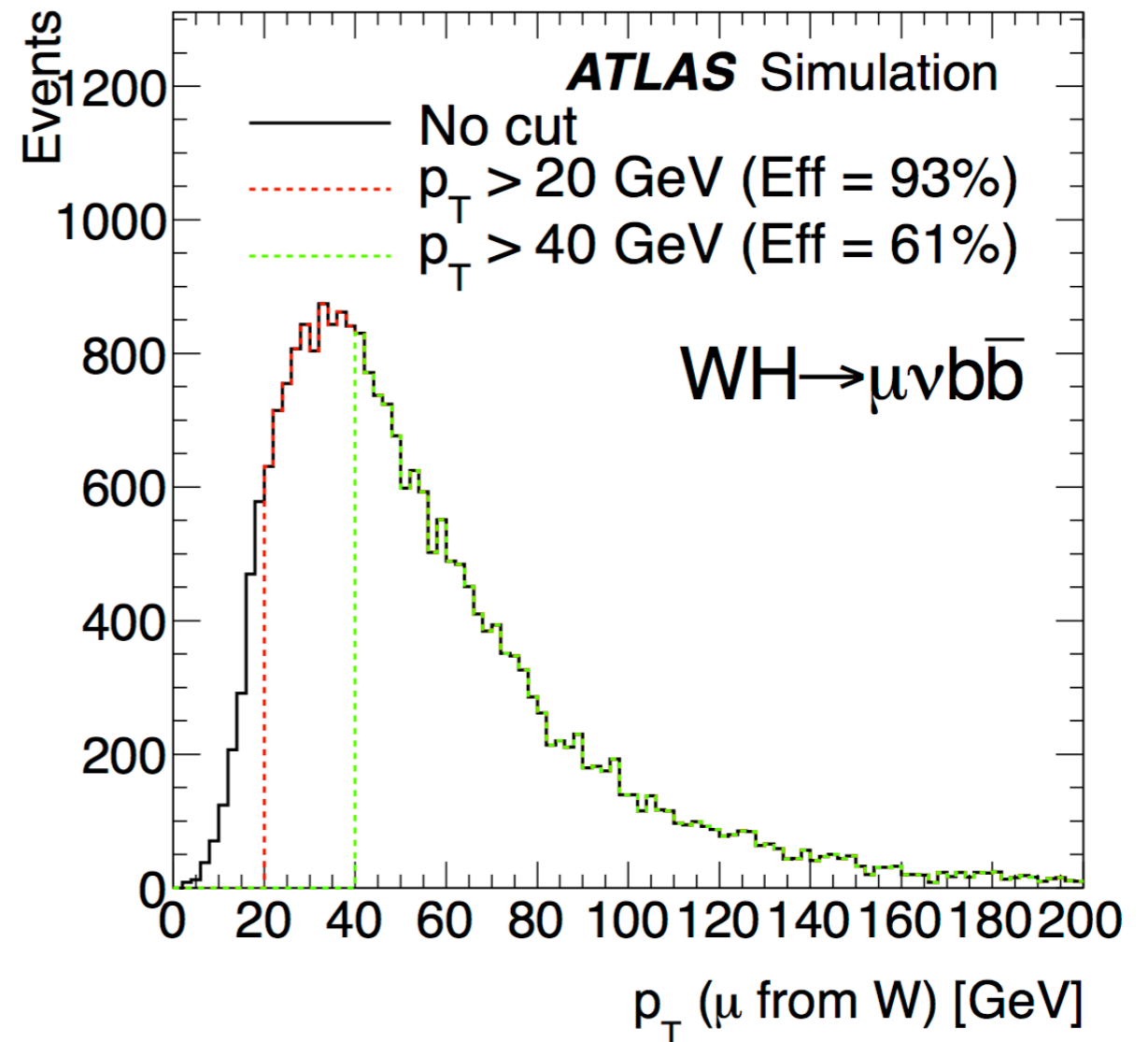
◆ If the threshold is raised to 40 GeV, the efficiency for muons from the decays of W boson produced in association with Higgs will be 61%.

New Small Wheel

◆ Consists of sTGC and Micromegas

‣ **sTGC: small strip TGC**

  ‣ TGC chamber with strip width of 3.2mm, smaller than the strip width of current TGC (> 15 mm)

  ‣ 4 wire-strip pairs are combined to make 1 module.

  ‣ position resolution 60~150 μm

‣ **Micromegas: micro mesh gaseous structure**

  ‣ position resolution ~90 μm

  ‣ 8 layers are sandwiched by sTGC 4-layer modules, to compose the New Small Wheel

sTGC 4 layers   Micromegas 8 layers   sTGC 4 layers

~36 cm
~22 cm

Resolution: position ~30 μm
            angle ~0.3 mrad.

NSW Technical Design Report, ATLAS-TDR-020
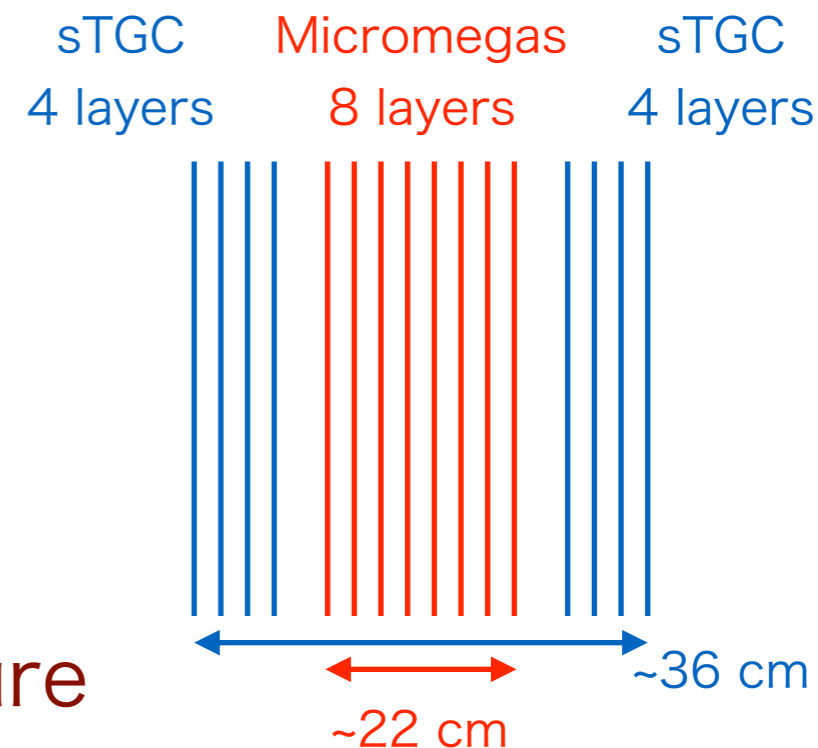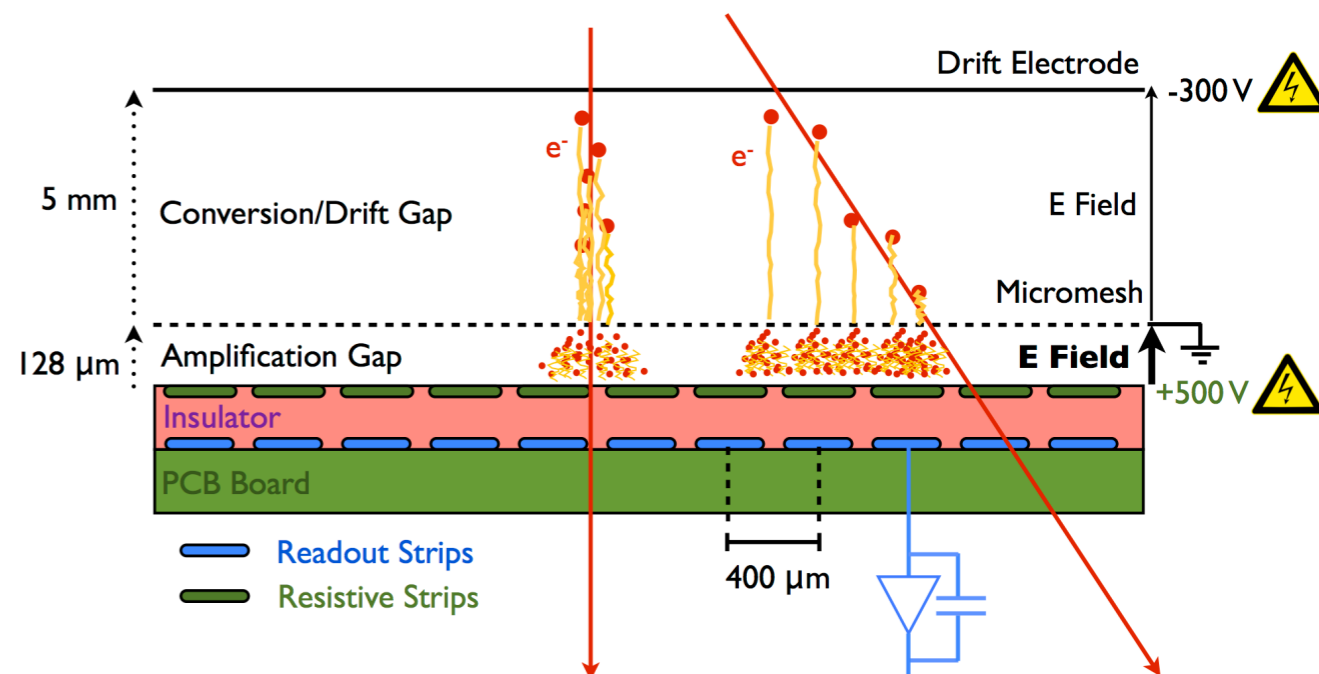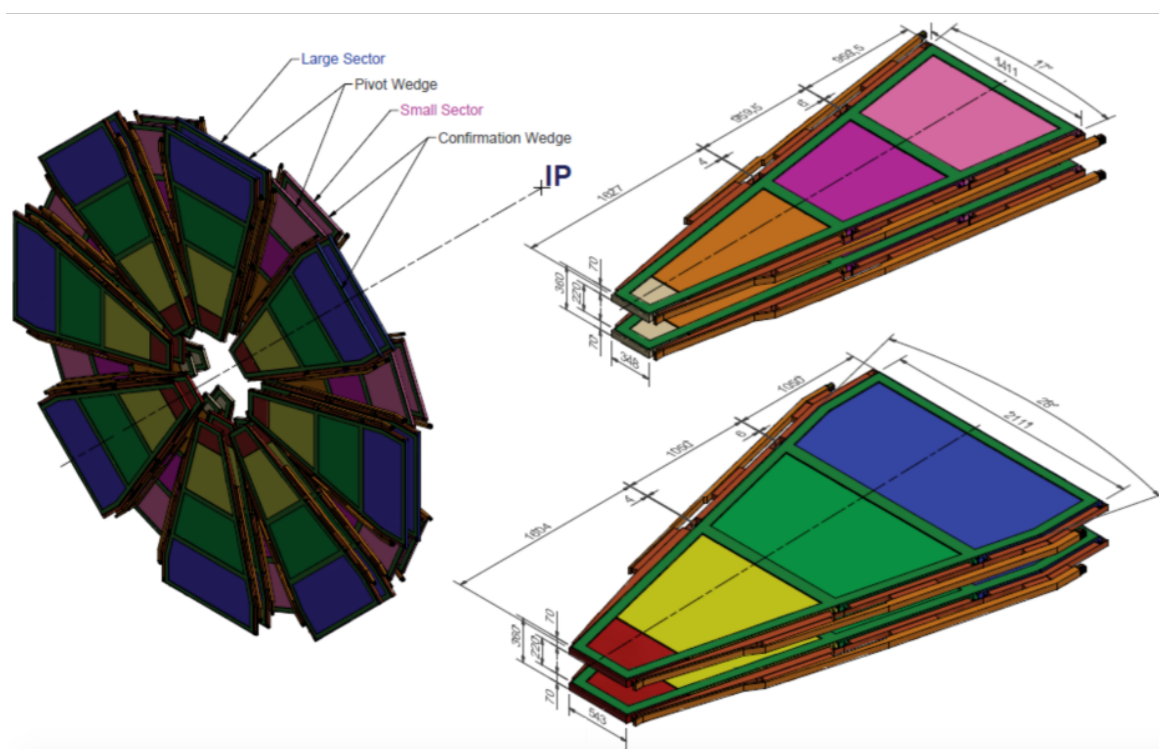
Region of Interest

- ◆ The smallest unit for the Level-1 Muon Trigger:

  - ‣ Each side is divided into 72 parts, shown as green line in this figure

    → 72 'Sectors' per side,

      48 × Endcap sectors and
      24 × Forward sectors

  - ‣ Each Endcap (Forward) sector is divided into 148 (64) 'Regions of Interest' = RoI

  - ‣ One Endcap (Forward) SL board handles 2 Sectors,
    i.e. 296 RoIs (128 RoIs)

  - ‣ Trigger decision is performed RoI by RoI

    → 296 trigger decision logic should run in parallel on a single FPGA
    → 296 different LUTs need be implemented

$\Delta\phi = 0.1$

RoI

$\eta = 1.0$

coverage per Endcap SL

Trigger Sector

37

RoI = 37 x 4 = 148

coverage per Forward SL

16

RoI = 16 x 4 = 64
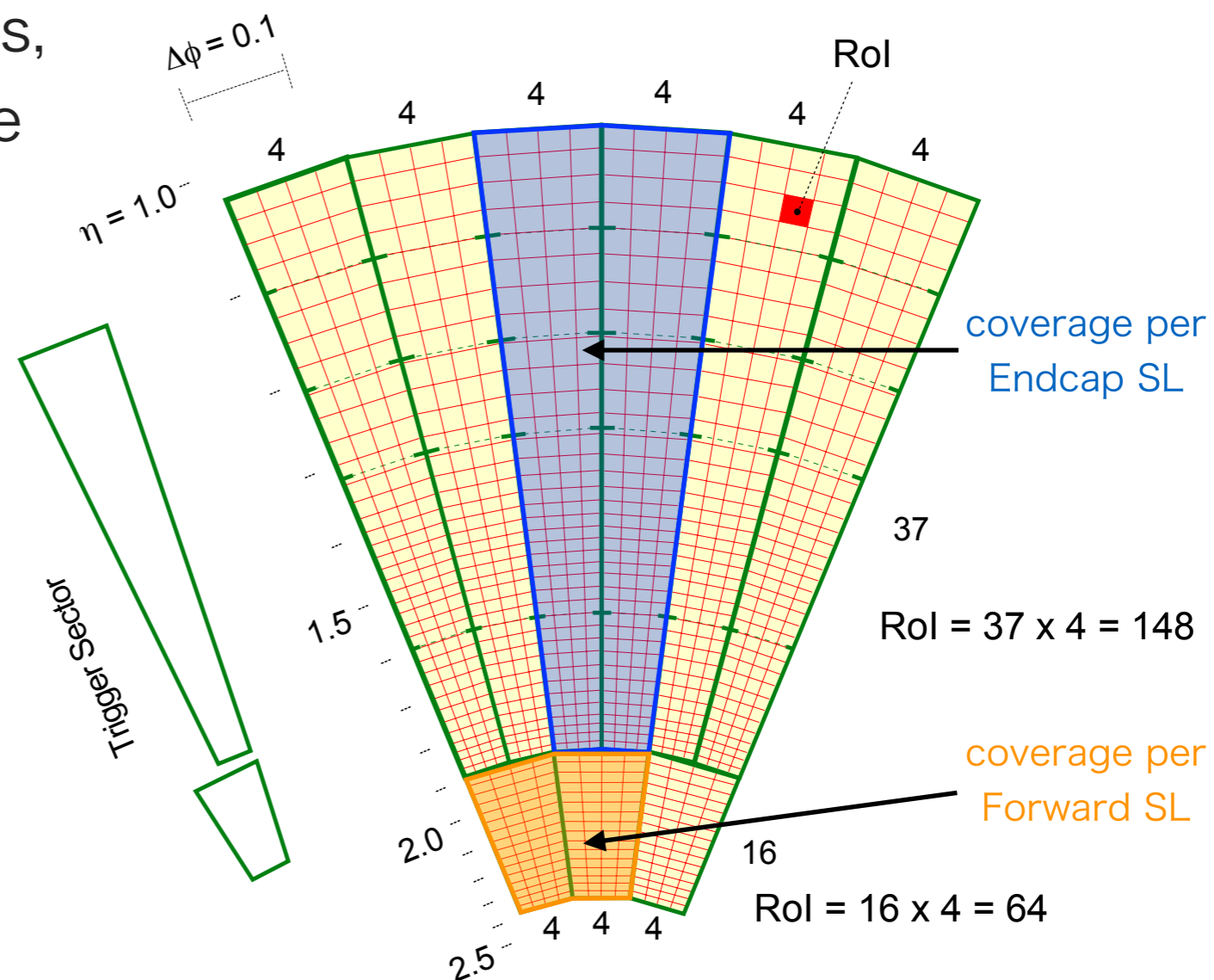
New Sector Logic Board design

6 optical inputs (6.4 Gbps) **from NSW**
SFP+ with GTX RX in FPGA

6 optical inputs
for other detectors
SFP+ with GTX RX

2 optical outputs
(6.4 Gbps) **to MUCTPI**
SFP+ with GTX TX

14 optical inputs (800 Mbps) **from BW-TGC**
SFP RX + G-Link RX chip
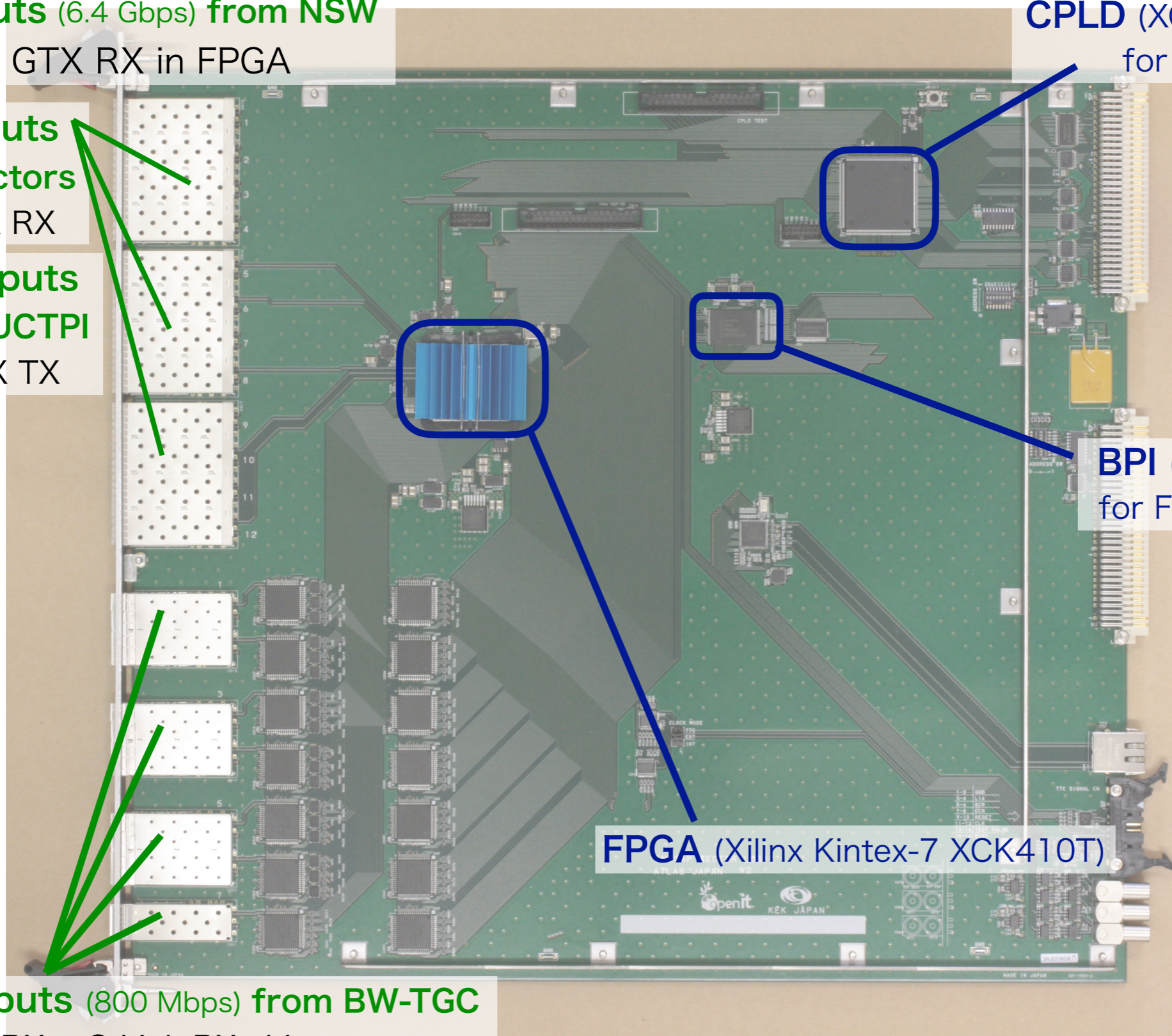
CPLD (XC2C256-7PQ208C)
for VME control

BPI (PC28F256P30TF)
for FPGA configuration

FPGA (Xilinx Kintex-7 XCK410T)

RJ45 connector
for readout (SiTCP)

16-pin connector
to receive trigger/
timing information

LEMO IN/OUT

Input Data Format (1)

- ◆ **TGC BW**
  - ‣ G-LINK 16 or 17 bits/BC per fiber
  - ‣ Endcap: 12 fibers per Sector Logic, 202 bits/BC
  - ‣ Forward: 6 fibers per Sector Logic, 100 bits/BC

- ◆ **TGC EI**
  - ‣ G-LINK 16 bits/BC per fiber
  - ‣ Endcap only, 2 fibers per SL, 32 bits/BC

- ◆ **New Small Wheel**
  - ‣ GTX 6.4 Gbps (= 128 bit/BC, with 8B/10B) per fiber
  - ‣ Endcap: 6 fibers per SL, 768 bit/BC
  - ‣ Forward: 8 fibers per SL, 1024 bit/BC

	Second Byte								First Byte							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word-0	comma (K29.5)								comma (K29.5)							
Word-1	track0[15:8]								track0[7:0]							
Word-2	track1[7:0]								track0[23:16]							
Word-3	track1[23:16]								track1[15:8]							
Word-4	track2[15:8]								track2[7:0]							
Word-5	track3[7:0]								track2[23:16]							
Word-6	track3[23:16]								track3[15:8]							
Word-7	BCID[11:4]								BCID[3:0]					ID[3:0]		

Bit	Assigned information
7-0	$\eta[7:0]$
13-8	$\phi[5:0]$
18-14	$\Delta\theta[4:0]$
20-19	MM type
22-21	sTGC type
23	spare

Input Data Format (2)

- **Tile Cal.**
  - GTX 1.6 Gbps (= 32 bits/BC with 8B/10B) per fiber
  - Endcap only, 1 fiber per SL

	Second Byte								First Byte							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word-0	BCID[3:0]				TMDB[3:0]				comma (K29.5)							
Word-1	0	Mod3[2:0]			Mod2[2:0]			Mod1[2:0]			Mod0[2:0]			Cable[1:0]		

- **RPC BIS 7/8**
  - GTX 6.4 Gbps (= 128 bits/BC with 8B/10B) per fiber
  - Endcap only, 1 fiber per SL

	Second Byte								First Byte							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word-0	comma (K29.5)								comma (K29.5)							
Word-1	track0[15:8]								track0[7:0]							
Word-2	track1[7:0]								track0[23:16]							
Word-3	track1[23:16]								track1[15:8]							
Word-4	track2[15:8]								track2[7:0]							
Word-5	track3[7:0]								track2[23:16]							
Word-6	track3[23:16]								track3[15:8]							
Word-7	CRC[7:0]								BCID[7:0]							

Bit	Assigned information
5-0	$\eta[5:0]$
11-6	$\phi[5:0]$
14-12	$d\eta[2:0]$
17-15	$d\phi[2:0]$
19-18	2/3 flag[1:0]
23-20	spare

Output Data Format

- Output to Muon-to-CTP Interface (MUCPTI)
  - GTX 6.4 Gbps (= 128 bits/BC with 8B/10B) per fiber
  - 1 fiber per trigger sector, 2 fibers per SL board
 - Commas are sent at the end to gain latency.

				Second Byte							First Byte					
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word-0	Muon Candidate1 [15:0]															
Word-1	Muon Candidate2 [15:0]															
Word-2	Muon Candidate3 [15:0]															
Word-3	Muon Candidate4 [15:0]															
Word-4	Global flag [3:0]				BCID[11:0]											
Word-5	CRC[7:0]								0xFD (K29.7)							
Word-6	0xC5 (D5.6)								0xBC (K29.5)							
Word-7	0xC5 (D5.6)								0xC5 (D5.6)							

Muon candidate data format. 16 bits are assigned for each muon candidate. 8 bits are used to indicate the RoI of the candidate, 4 bits for the p_T value, and 4 bits for other flags. 1 bit of the flag bits are used to indicate the sign of the muon candidate's charge. The other flag bits can be used for inner coincidence debug signals, during the commissioning period.

Bit	Assigned Data
7-0	RoI
11-8	p_T value
12	Candidate sign
15-13	NSW/Inner Coincidence flags

Trigger Performance
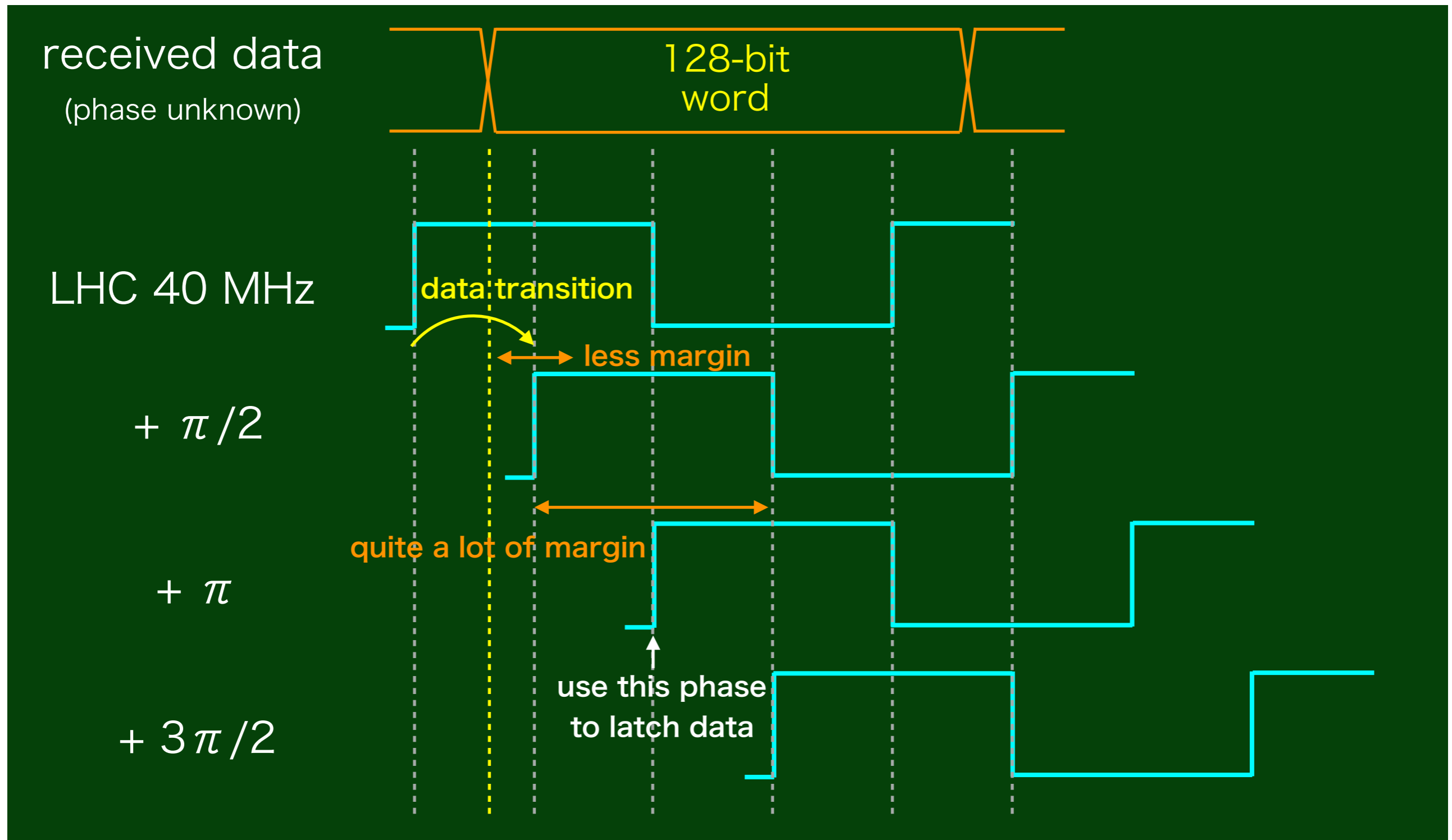
‣ New Inner LUTs uses NSW <u>position</u> & <u>angle</u> information

‣ Efficiency is calculated by simulation, for L1_MU20

  (L1_MU20: Level-1 trigger for muon with p_T > 20 GeV)

‣ The track finding efficiency is assumed to be 97%
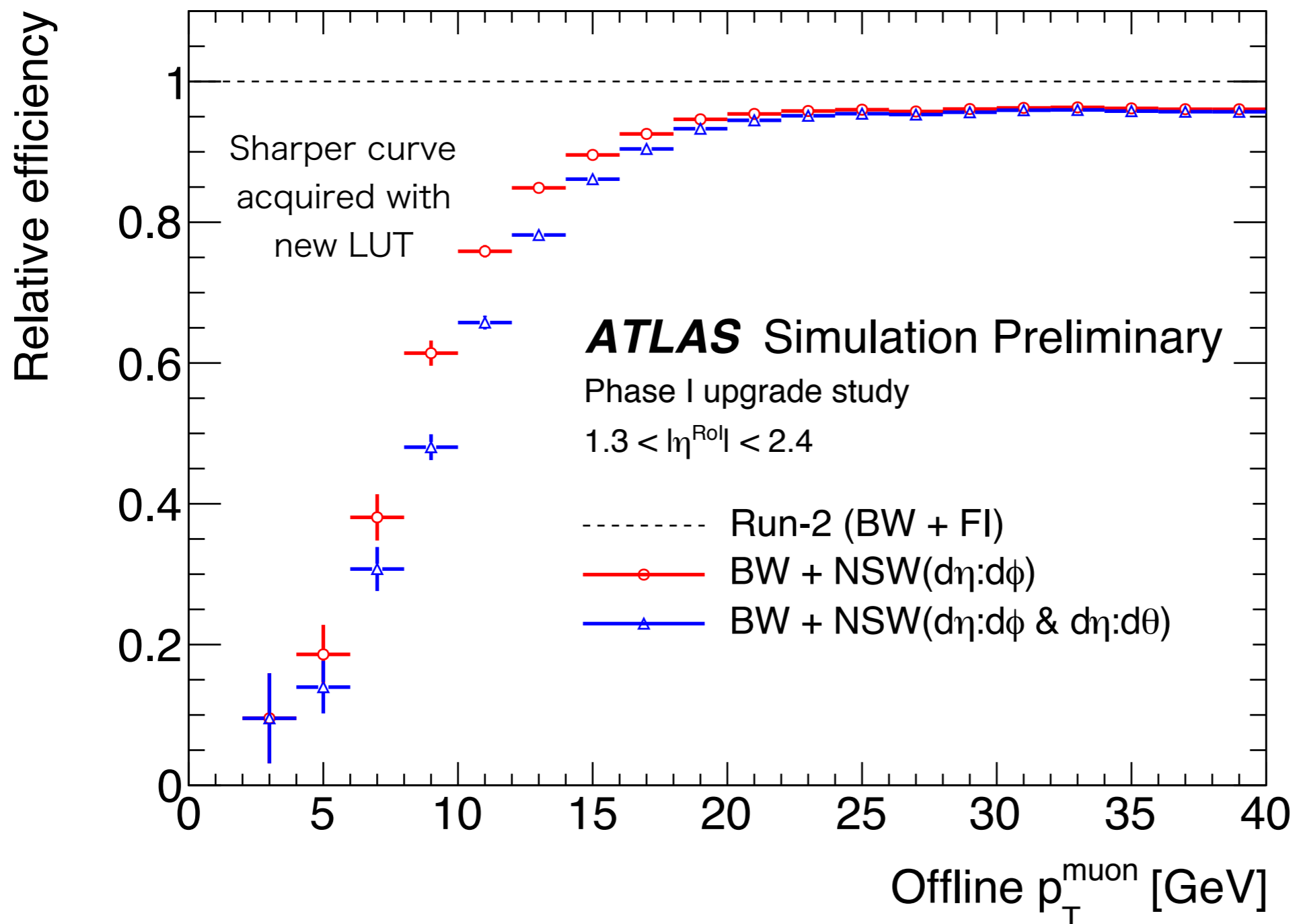
Efficiency > 95%
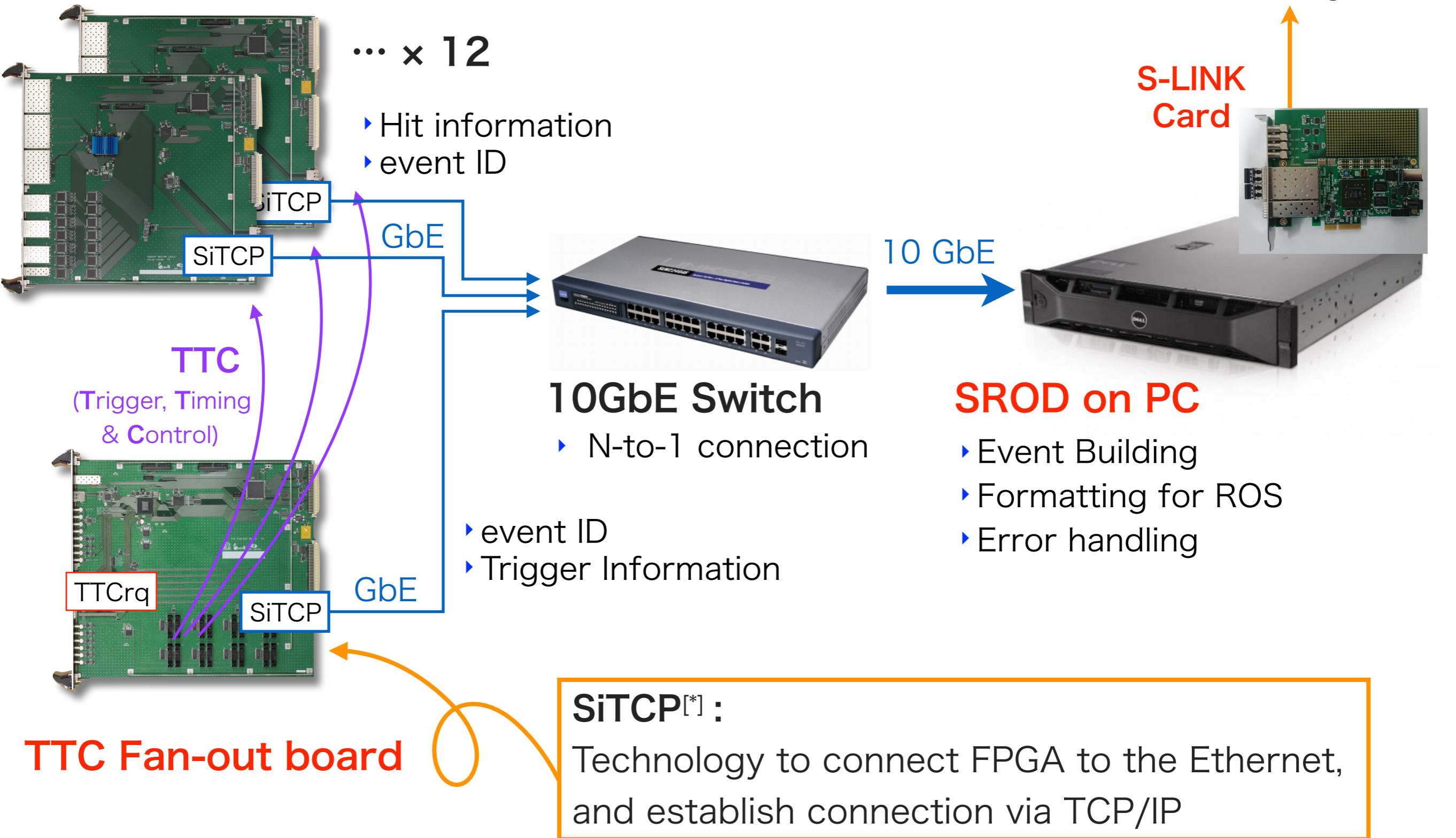for p_T > 20 GeV

Firmware design for Fixed Latency

◆ Data reception Clock-Domain-Crossing part

‣ choose a phrase of 40 MHz to latch the received data, so that they will have enough margin from the data transition point:

Run 3 Readout system

New Sector Logic

Read Out System

⋯ × 12

S-LINK Card

‣ Hit information
‣ event ID

SiTCP

SiTCP

GbE

10 GbE

TTC
(**T**rigger, **T**iming & **C**ontrol)

10GbE Switch

‣ N-to-1 connection

SROD on PC

‣ Event Building
‣ Formatting for ROS
‣ Error handling

TTCrq

‣ event ID
‣ Trigger Information

SiTCP

GbE

TTC Fan-out board

SiTCP[*] :
Technology to connect FPGA to the Ethernet, and establish connection via TCP/IP

[*] Tomohisa Uchida, "Hardware-Based TCP Processor for Gigabit Ethernet",
IEEE Trans. Nucl. Sci. Vol.55, No.3, June 2008, [_LINK_]