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The SDC Silicon Tracking System

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Abstract

The silicon tracking system is a critical element of the tracking system of the Solenoidal Detector Collaboration's (SDC) experiment to meet the physics requirements at the Superconducting Super Collider (SSC). It will provide full-pattern recognition, vertexing, and stand-alone momentum measurement capabilities complementing the outer tracker. The key component of the system is a double-sided silicon microstrip sensor (DSSS) with fast-readout front-end electronics. The SDC DSSS design addresses problems associated with radiation damage on the surface and in the bulk of the silicon microstrip sensors. The SDC silicon tracking system, being the largest semiconductor tracking detector ever planned, requires a state-of-the-art design of the electro-mechanical system in order to minimize the dead regions, minimize the radiation length, cool and operate the system at 0° C, and have the mechanical precision necessary to match the spatial resolution of the microstrip sensors. The silicon ladders, shells, space frames, and butane evaporative cooling system are achieving the requirements imposed by the goals of the SDC experiment.

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1. Introduction

The superconducting super collider (SSC) has been designed to address the most fundamental research issue in elementary particle physics of today: the study of electroweak symmetry breaking. Associated with the symmetry breaking, an interesting object, the Higgs boson, will appear. It has a very small production cross section and involves large momentum transfers. Other interesting heavy objects, such as $W^{\pm}$'s, Z^{0}'s, and $t\bar{t}$'s, which are rare at today's hadron colliders, will be produced copiously.

Most of the events at the SSC, however, will involve small momentum transfers and will occur at rates several to many orders of magnitude larger than the interesting processes. To resolve the signals from the background, it is essential to detect characteristic signals, such as (isolated high-energy) photons, leptons (e's and μ's), secondary b-decay vertexes (for $t \rightarrow b$ decays), and low-multiplicity decays of τ's and J/ψ's. For SSC physics, the capabilities for pattern recognition, vertexing, and high momentum-resolution are key features. Furthermore, a detailed picture of each event may become critical for finding and understanding unexpected phenomena.

The SDC silicon tracking system [1] has been designed, in conjunction with the outer trackers, for the SDC tracking system to meet those requirements at a minimum cost within the constraints of our assessment of the technological maturity and capabilities of the various options [2]. It would be extremely difficult to meet the physics goals without the use of silicon detectors.

2. Design of the SDC Silicon Tracking System

2.1 Requirements for the SDC Tracking System

The SSC will provide proton-proton collisions at a center-of-mass energy of 40 TeV and a design luminosity of 10^{33} $cm^{-2}s^{-1}$ with a beam-crossing frequency of 60 MHz (16.68 ns interval) [3,4]. The physics requirements for the SDC tracking system have been analyzed and quantified [5]. The important quantities relevant to the silicon system are summarized in Table 1 and discussed in the following.

(1) The acceptance of charged tracks (α_{accept}: $|\eta| \leq 2.5$ [6]) is to provide >60% geometric acceptance for the leptons from the decay of Higgs→4 charged leptons for the mass m_H>200 GeV/c^2.

(2) Isolated high p_t tracks are critical signals to identify heavy objects. The efficiency (ε_{recon}) must be kept high (≥97 % for $p_t \geq 10$ GeV/c)), including the combined losses from pattern recognition, reconstruction, and selection. Isolated leptons (e's and μ's) are particularly important to tag Higgses, t's, and b's.

(3) The transverse-momentum (p_t) resolution ($\sigma_{p_t}/p_t \leq 20$ % at 1 TeV/c) is to reconstruct the Z° mass in the $Z^\circ \rightarrow \mu^+\mu^-$ decay mode within its natural width for a Z° produced at a typical p_t of 50 GeV/c. The momentum resolution impacts a broad range of physics analyses: reconstruction of such states as $H^\circ \rightarrow Z^\circ Z^\circ \rightarrow 4$ leptons (e's and μ's); sign-of-charge determination of the decay leptons of a new heavy Z'; and the in-situ calibration of the electro-magnetic (EM) calorimeters using electrons from $W^\pm \rightarrow e^\pm$ and $Z \rightarrow e^+e^-$.

(4) The impact-parameter resolution ($\sigma_b \leq 20$ μm for $p_t \geq 10$ GeV/c) is to efficiently identify secondary vertices so as to provide a b-jet tagging efficiency of ≥25 % in $t \rightarrow b$ decays.

(5) The z-resolution at the interaction point ($\sigma_{z\text{-}vertex}$<2 mm) is to separate pileup interactions which occur at an average rate of 1.6 events per crossing with a z-distribution of σ_z~5 cm. The z-resolution at the calorimeter shower maximum detector ($\sigma_{z\text{-}cal} \leq$ 2.5 mm) is to identify electrons by matching the track incident points and the EM shower center positions.

The resulting SDC tracking system (Fig. 1) features a large instrumented volume with a radius of 1.7 m and a half length of 4.3 m in a 2 T solenoidal magnetic field and is configured out of three sections: the silicon tracking system (r<50 cm, half length 2.6m, $|\eta| \leq 2.5$); the 5 superlayers of stacked straw-drift-tubes (r>50 cm, $|\eta| \leq 1.8$); and the 3 superlayers of gas-microstrip-

chamber arrays per end ($1.8 < |\eta| \leq 2.5$). The spatial resolutions of the subsystems are summarized in Table 2, including the projected local alignment errors.

Adoption of multiple technologies for tracking is primarily based on a consideration of the performance (*e.g.* momentum resolution), size and cost, but also on complementary functionality. The silicon tracker, with its superior spatial segmentation and position resolution, provides capabilities of full pattern recognition, secondary vertex reconstruction, as well as stand-alone momentum resolution (for low p_t tracks). Complementing the silicon tracker, the outer tracker will provide the 1st-level triggers (within 4 μs) and improved momentum and impact-parameter resolutions utilizing the large value of BL^2 (B is the magnetic field strength and L is the lever arm) in conjunction with the silicon tracker.

The transverse momentum resolution and the impact parameter resolution of the SDC tracking system are shown in Fig. 2. The p_t resolution has been evaluated both with and without a pseudo measurement at the beam axis (beam constraint) of 20 μm precision. The effect of multiple scattering is included in the calculations.

2.2 *SDC Silicon Tracking System*

The silicon tracking system uses double-sided silicon microstrip sensors (DSSS) to minimize the amount of material and to maximize the information. The strip pitch is 50 μm in the barrel section (<50 μm in average in the disk section). Recording hit/no-hit information, the resulting spatial resolution is ≤13 μm per side of DSSS, which has been demonstrated in the beam test discussed in Section 3.4. The strips on the stereo-strip side have a small stereo angle of 10 mrad to those of the axial strip side. This pitch and the small stereo angle allow all readout circuitries to be located at the ends of a detector.

The silicon tracking system is configured so as to have 8 layers of concentric cylinders in the central (Barrel) region and 13 layers of disks per end in the forward and backward (Disk) regions perpendicular to the beam

axis (Fig. 3) [7]. The subassembly dimensions are given in Table 3. The configuration and dimensions are determined so that more than 6 layers will be hit for high-p_t tracks and an impact parameter resolution of better than 25 μm will be achieved. For high-p_t tracks the outer tracker improves the impact parameter resolution by a factor of two over that of the silicon system alone. The full silicon area is about 17 m^2. The resulting number of readout channels is 6.5×10^6.

Compared to previous collider tracking systems, the tracking technologies that are matched to SSC physics have intrinsically more mass. The most significant impact of material is on the identification of electrons due to the degradation of momentum through Bremsstrahlung [8]. However, that impact is reduced, since the material is uniformly spaced in the tracking volume, and the SDC silicon tracking system is by itself capable of reconstructing tracks and measuring their momenta for use in E/p and trajectory/impact-point matching against the calorimeter. In fact, the most efficient E/p cut for electrons in the SDC detector makes use of the momentum measured in the silicon alone (Fig. 4) [9].

3. SDC Double-sided Silicon Strip Sensor and Frontend Electronics

3.1 Radiation damage to the silicon strip sensors

The tracking detectors experience a large fluence of charged hadrons produced directly from the beam-beam interactions [10] and neutrons (typically 1 MeV) from the albedo of subsequent particle interactions in the calorimeters. For one year of running at the standard SSC luminosity (1 SSCY), the fluence of charged particles (Fig. 5), including those trapped in the magnetic field of the SDC (looper), scales as $1.2\times10^{15}\times f(r)/r^2$ [charged particles/cm^2/SSCY], where the looper correction factor ($f(r)$) is given by $f(r)=1+0.014\times r$. At r=9 cm the fluence of charged particles is 1.7×10^{13} particles/cm^2/SSCY. The neutron fluence is approximately uniform over the whole tracking volume, and is about 2×10^{12} neutrons/cm^2/SSCY with a polyethylene liner at the face of the endcap calorimeters [11].

Radiation damage to the silicon detectors has been extensively studied, and is understood to result from two basic mechanisms: bulk damage and

surface damage. The bulk damage is due to the displacement of atoms from their lattice sites, which leads to an increased leakage current, carrier trapping, and changes in the dopant concentration. The surface damage is due to charge build-up in surface layers, and leads to an increased surface leakage current and changes in the characteristics of structures near to the surface.

3.1.1 Bulk Damage

Neutrons and charged hadrons, such as protons and pions, cause bulk damage. For our application, the most important effect is a change in the dopant concentration. In n-type bulk, the removal of donors and the creation of acceptors [12] result in

(1) type inversion from n- to p-type at a fluence of around $\phi=2\times10^{13}$ particles/cm^2, and
(2) universal increase of the effective dopant concentration beyond type inversion, since the donors diminish for a large fluence.

The depletion voltage is proportional to the dopant concentration and, eventually, exceeds the breakdown voltage of the AC coupling capacitors, leading to detector failure. The present estimate is that without the annealing effects described below the detectors at a r = 9 cm would begin to fail after about 10 years of operation.

Recently, two components, annealing and anti- (or reverse-) annealing effects, have been observed with regard to radiation-induced dopant concentration changes. They were found to have very different time constants; and furthermore, the time constants were found to be extremely dependent on the temperature [13]. Following exposure to fluences greater than those needed to achieve type inversion, the depletion voltage decreases rapidly with time and approaches a fairly stable minimum value. This is annealing. At a considerably later time, the depletion voltage begins to increase again and eventually saturates at a value which is greater than the value found when the device was removed from the beam. This is anti-annealing. Cooling the detector to 0 °C slows the annealing process by

increasing its time constant to several days; it essentially stops the anti-annealing process by increasing its time constant to tens of years. As a result, by cooling the detector to 0 °C, one can gain the benefits of the reduction of the depletion voltage, which results from the annealing process, without experiencing the increase caused by anti-annealing.

Another effect of the bulk damage is the creation of carrier-trapping centers in the bulk, which apparently reduce the collected charge. However, the effect is found to be small (<10 %), even at fluences as large as 10^{14} charged particles/cm^3. There is also an increase in the leakage current due to bulk damage. For the SDC DSSS operated at 0 °C, the current is expected to be ≤1 μA/strip at 10^{14} particles/cm^2. The shot-noise at the detector p-n junctions due to the current is small (~500 electrons) compared with the noise associated with the amplifier (<1,400 e).

3.1.2 Surface Damage

Silicon microstrip sensors have been developed by utilizing planar processing techniques for microelectronics. Its important functional structures, such as implanted strips, bias feeding mechanisms, and signal readout structures, are implemented in a thin layer at the surface. The surface of the silicon is covered with a SiO_2 layer for insulation. This layer is known to trap positive charge when exposed to ionizing radiation [14]. That positive charge can induce a high electric field which affects the characteristics of the structures underneath. Studies have shown that the positive charge in the SiO_2 layer saturates at a surface density of about 10^{12} e/cm^2. The development of a radiation-hard DSSS is contingent on the ability to cope with that positive charge density.

3.2 Radiation-hard SDC Double-sided Silicon Strip Sensor [15]

SDC has chosen to use DSSS's to attain the maximum amount of information with a minimum material thickness. The readout is AC-coupled so as to avoid the effects of leakage current on the amplifiers. The principal structure of the SDC DSSS is shown in Fig. 6, and its specifications are summarized in Table 4. The unit sensor is a 60 mm×34 mm rectangle

for the Barrel section and a 60 mm×70 mm(max.) trapezoid for the Disk section.

The development of a radiation-hard SDC DSSS required three innovations:

(1) strip isolation of the n-side with densely doped p^+ isolation lines;
(2) bias resistors for individual strips made of polycrystalline silicon; and
(3) the use of AC electrode strips that are narrower than the implanted strips.

Items (1) and (2) are related to the surface damage and item (3) to the bulk damage. One of the fundamental concerns of the double-sided silicon strip sensor is strip isolation on the n-side. The surface SiO_2 layer is known to be positively charged. The immobile positive charges attract negative carriers to the surface of the silicon bulk and make a thin undepleted layer at the surface. To avoid a continuous undepleted layer, which effectively shorts the n^+ strips together, p^+ implanted lines are inserted between the n^+ strips in the SDC DSSS. The charge-up in the SiO_2 layer is enhanced with irradiation, but has been found to saturate at a surface density of about 10^{12} e/cm^2. A densely doped (~10^{14} Boron atoms/cm^2) p^+ ensures strip isolation even after large irradiation doses.

A biasing scheme can also be affected by the radiation damage. Schemes that use subtle techniques, such as a punch-through effect or a surface accumulation layer, are affected by the surface charge-up. In contrast, polycrystalline silicon, which works as a simple resistor, is found to be very resistant to radiation effects.

The third innovation required for radiation-hard sensors is related to bulk damage, specifically an increase in the depletion voltage. SDC has chosen to apply the bias voltage symmetrically to the implant strips of the p- and n-side in order to reduce the maximum voltage across the AC coupling capacitors. The strength of the electric field along the edge of the implant strips in the silicon bulk depends on the voltage difference between the AC electrode strips (Ground) and the implant strips (±1/2 V_{bias}) and on the

relative location of the AC electrode edge and the implant-strip edge. Unless the AC electrode strips are narrower than the implant strips, the strength of the electric field at the edge exceeds the critical strength (E_c ~30 V/μm) to cause an avalanche breakdown in silicon, resulting in a large noise and leakage current.

3.3 *Front-end Readout Electronics*

Fig. 7 shows a block diagram of the front-end electronics system. A detector channel is read out with analog and digital chips. The analog chip, fabricated using bipolar technology, provides low-noise preamplification, pulse shaping, and discrimination [16]. The digital chip, made of CMOS, provides time stamping, data buffering, and sparse readout functions. The amplified and discriminated data from each strip at every beam crossing will be stored for a period of time called the Level 1 latency, presently being estimated to be 256 beam crossings (~4 μs); after Level 1 accept, the data will be encoded and serially transmitted off the chip through optical fibers [17].

The preamplifier design is strongly influenced by the speed, noise, and power requirements. The electronic noise is governed by the amplifying device, the shaping time, and the strip length, *i.e.* the input capacitance. The noise for a bipolar transistor is given in the next section. The pulse shaping time is dictated by the bunch crossing frequency of the SSC (60.0 MHz). The power consumption is limited by the restrictions on the amount of material allowed to provide the electrical power and to remove waste heat.

The r.m.s. noise is required to be 0.2 fC, as derived below. In 300 μm thick silicon, the lower-end spectrum of the fluctuations of the charge generated by a minimum ionizing particle (MIP) is ~2 fC. This charge could be shared by ≥2 strips, depending on the position of the particle traversal. Hence, a discrimination threshold of ~1 fC is required to maintain a good detection efficiency. To achieve an acceptable false hit rate and timing jitter, the threshold must be kept at ~5 standard deviations away from the noise, dictating in a noise limit of ~0.2 fC (1200 electrons).

After reviewing realistic signal simulations, including the effect of magnetic field[18] and the measured gain and threshold variations [19], the following design objectives have been set for the front-end electronics:

(1) <1400 electrons noise for the 12 cm strip length including cross-talks ;
(2) <12 ns time walk for 1.25 fC to 10 fC dynamic range; and
(3) <1.5 mW/(analog + digital channel) power consumption.

With these design objectives, bipolar technology is identified to offer superior performance over CMOS for the analog circuitry because of the relation between the speed, noise, and power consumption [16,20]. For the digital circuitry, CMOS is the choice because of both circuit density and power consumption. The main voltages and currents required to drive the 6.5 million electronic channels of analog and digital chips are summarized in Table 5.

3.3.1 *Noise of a Bipolar Transistor Amplifier*

The noise of a preamplifier using a bipolar junction transistor input is given by

$$Q_n=\left[480\sqrt{\left(\frac{I_c}{100\,\mu A}\right)\left(\frac{100}{\beta}\right)\left(\frac{\tau}{20\,ns}\right)}\ \oplus\ 60\sqrt{\left(\frac{100\,\mu A}{I_c}\right)\left(\frac{20\,ns}{\tau}\right)}\times C_{in}[pF]\right]e \qquad (3.3.1)$$

with the constants normalized for a collector current (I_c=100 μA), a DC current gain (β=100), and a shaping time constant (τ=20 ns), for a simple CR-RC unipolar shaping circuitry. It should be noted that the noise is not only proportional to the input capacitance, $C_{in}=C_i+C_{det}$, where C_i is the input capacitance of the amplifier and C_{det} is the detector capacitance, but also has a substantial offset term. The symbol ⊕ indicates making a quadratic sum of the two terms.

3.4 *Beamtest of the SDC DSSS and front-end electronics*

To evaluate the behaviors of the radiation-hard SDC DSSS and front-end readout electronics, a series of beamtests has been started at KEK using the

pion beams from the 12-GeV proton synchrotron. The momentum used is 4 GeV/c. Although that is rather low, the effects of multiple scattering can be reduced to a negligible amount by placing the detectors close together (*e.g.* 8 mm).

The first beam test was executed with the first full-size prototype double-side SDC DSSS. Three planes of detectors were used. Each plane comprised a single DSSS (6 cm strip length) connected to two 64 channels of front-end analog and digital chip pairs on each side of the detector. The analog chip was a TEKZ chip developed for the ZEUS experiment [19], which had a unipolar shaping with a time constant of ~30 ns. The digital chip was a CMOS SRAM Buffer chip [21]. The electronics were driven and read out with a 10 MHz clock asynchronously with beam triggers. The detectors were placed in a null and a 1.0 T vertical magnetic field. The direction of the strips was vertical to the beam axis and the detectors were rotated about the vertical axis (ϕ-rotation) and the horizontal axis (θ-rotation) so that the beam varied up to ±9° in ϕ and ±54° in θ from normal incidence. The thresholds were set at ~1.2 fC.

Preliminary results indicated that the p- and the n-side were equally responsive; the efficiencies were >99% for normal incidence; the spatial resolutions were ~13 μm; the multi-strip hit fraction changed as a function of the ϕ-rotation angles from 12 - 40% without a magnetic field, and from 12 - 65% with a 1.0 T magnetic field; despite the increase in the multi-strip hit fraction with the rotation, the efficiencies and resolutions remained constant; and, the signal-to-noise ratio of this analog chip was found to be >16 for normal-incident particles [22].

For the future we are planning to beam test the following enhancements on our way to building the final SDC DSSS ladder assembly: new SDC baseline analog chips together with new 60.0 MHz clock CMOS SRAM buffer chips; irradiated full-size prototype SDC DSSS's (up to a 10^{14} protons/cm^2 fluence); wedge prototype SDC DSSS's; new SDC baseline digital chips with optical-fiber data-transmission; and, finally, complete SDC DSSS ladders (multiple sensors assembled with multichip readout hybrids).

4. Electro-Mechanical Design

4.1 Requirements

For the silicon tracking system to achieve its physics goals, the system must have the following capabilities and features:

(1) the smallest possible dead region which is not covered with the silicon detectors;
(2) a minimum of additional mass;
(3) operation of the detector system at uniform temperature of 0° C, while removing up to 13 kW of the waste heat, which is mainly generated by the front-end electronics;
(4) stable support of the 17 m^2 of silicon detectors to the tolerances given in Table 6 (*e.g.* ≤5 μm in the circumferential direction). That stability is required to keep the misalignment error ≤40 % of the measurement error;
(5) achieve the above goals in a high radiation environment; and
(6) have a maintainable system with an operating life of at least 10 years.

4.2 SDC DSSS Ladder

To meet the requirements of the minimal dead region, the readout hybrid is placed directly on the DSSS. To meet the minimal material requirement, the hybrid will be made of a Be substrate, and an aluminum/Kapton ribbon-cable for bussing the signals. The electronics-detector sandwich is shown in the cross section in Fig. 8. The Be substrate suppresses cross-talks between the sensor and the readout chips and also provides a good thermal path from the readout chips to the cooling section. The electrical connection of readout channel is based on aluminum-wire bonding. An alternate design is to mount the chips inverted so that the bonding pads are face-down to the hybrid (flip-chip bonding).

To minimize the use of additional material, the silicon ladders are designed so as to be a structural element of the silicon shell assemblies. A 24-cm ladder in the barrel section (Fig. 9) is made of two pairs of electrically independent 12-cm unit elements. A 12-cm unit element is made of two 6-cm DSSS's, which are edge-glued and electrically connected channel by

channel with aluminum-wire bonds. Readout hybrids are located at each end of the ladder assembly. The silicon ladder unit is stiffened by glueing two thin graphite/cyanate-ester (G/CE) composite strips along the length of the detector edges. In the Disk section, a 12-cm ladder with electronics near its outer edge is the fundamental unit.

4.3 *Silicon Shell*

Fig. 10 shows a cut-out view of the silicon tracker in the barrel section. The silicon ladder assemblies are glued to the inner and outer surfaces of a pair of structural support rings made of G/CE, which combines adjacent layers into superlayer shell assemblies. Three silicon shell assemblies, two 24-cm and one 12-cm long, comprise a 60-cm-long central region superlayer. The four superlayers in the central region are supported pair-wise by two support cylinders made of G/CE. The detectors in the central region are tilted at an angle of 7.4° to overlap the detectors and to account for the different Lorentz angles for the holes and electrons in the 2 T magnetic field [18].

The forward regions comprise silicon annular disks. The detector modules in the forward region are not tilted. Individual modules are arranged circumferentially around the beam axis (Fig. 11). Circumferential hermeticity is preserved by overlapping adjacent trapezoidal modules on alternating sides of the disk.

Each shell assembly is supported with kinematic mounts (*i.e.* a 3-point support arrangement) so that the delicate silicon shell does not receive extraneous loads. The mounting method is required to allow a repeatable, high-precision location of the shell assemblies, while at the same time maintaining their orientation and the location of their centers as the entire assembly is cooled down to an operating temperature of 0° C.

4.4 *Cooling*

Although the heat load from the front-end electronics of the whole silicon tracker is estimated to be 10 kW, there will be additional heat leaking

into the system. To allow for that heat load and to maintain a safety margin, the cooling system is presently being designed to easily handle a heat load of 13 kW and a heat flux of 1.0 W/cm^2 at the electronics. A 0° C detector operating temperature has been selected to keep the detector leakage currents within tolerable levels, and also to prevent anti-annealing while still allowing the beneficial annealing to proceed as discussed in 3.1.1.

For the cooling system, a liquid-vapor phase-change system (evaporative cooling) has been identified as being best suited for the requirements of zero vibration, isothermal operation for mechanical stability, low mass, and the capability to handle a large thermal load. Butane has been selected as the working fluid based on its normal boiling point (-0.5° C), availability, and cost. Subcooled liquid from the condenser is distributed to the heated surfaces by a combination of gravitational forces and capillary forces of a wick. The wick is the key component in terms of technology. Fine-size pores of less than 10 μm diameter maintain the hydrostatic pressure difference between the condenser and the wick, and minimize bleeding of the liquid. The wick thickness required to distribute an adequate supply of liquid over the heated surface is a function of the wick pore size, wick permeability, capillary pumping distance, and power density.

Polystyrene microcelluar foams have densities of less than 0.1 g/cm^3 and high porosity (~95%) with a pore radius of between 1 and 6 μm. A cooling test of a molded polystyrene wick was conducted at Los Alamos National Laboratory. The temperature difference between the heaters and the normal boiling point of butane was measured as a function of the pore radius of the polystyrene wicks (Fig. 12). An inverse relationship between the pore radius and the temperature difference was observed. This result implies that the evaporation of butane occurs within the wick, which is not desirable for our application. Other wicks made of porous beryllium and carbon were also measured; their performances are also shown in the Fig. 12. The porous Be shows very desirable characteristics with the right pore size and very low temperature difference. This result implies that evaporation occurs at the wick surface, possibly due to the high thermal conductivity of beryllium.

The current design of the cooling system is based on porous beryllium wicks directly mounted on the Be substrate of the readout hybrids. Adjacent wicks are connected with small U-tubes to distribute the liquid along the detectors (Fig. 13). A finite element model thermal calculation shows that the temperature of the analog chips will be at about 6° C for a heat flux of 1.3 W/cm^2.

An alternate cooling method based on heat conduction to a water-alcohol mixture is also being explored. The mixture would flow through a channel located near to the electronics. The system would be operated under flow condition so as not to cause vibrations, and under a negative pressure in order to prevent liquid leaking out of the channels. Problems associated with trade-offs between the temperature rise and system mass remain to be solved.

4.5 Space Frame and Enclosure

A space frame has been configured so as to provide support for both the Barrel and Disk regions (Fig. 14). It will be constructed of magnesium metal matrix composite (Mg-MMC) tubes and assembled with demountable joints, which are adhesively bonded. The key features are a zero coefficient of thermal expansion (CTE) along the tube axes, immunity to moisture absorption (butane or water), resistance to radiation damage, and an extremely large elastic modulus.

The entire silicon tracking system is enclosed within a vessel configured to safely contain the butane vapor of the cooling system, serve as a thermal shield, and act as the primary conduit for transferring the mechanical loads on the space frame to the outer tracker support frame from which the silicon system is supported. An ultra-light weight G/CE sandwich wall comprises the outer enclosure and the two end-cover plates. A very thin beryllium wall (0.5 mm) is used for the inner shell with reinforcing ribs in several locations. The introduction and removal of butane into and out of the containment vessel is accomplished in a manner imposing only slight differential pressures (0.1~0.2 ATMs) across the containment vessel walls.

4.6 Radiation length consideration

Throughout our design, the need for ultra-light weight, low-Z, radiation resistant materials has been stressed. Table 7 lists the contributing components and their current estimated contribution to the radiation length of the silicon tracker (averaged over $|\eta|<2.5$). When a component is made of several materials, the element is given with an adjusted equivalent thickness of the primary material in the column, showing the effective thickness. The amount of material in front of the last silicon detecting element, including a beam pipe, is ~7.5% X_0. The total amount in front of the outer tracker is ~9.5% X_0. Since the amount of material is an area of concern, our design effort is addressing how further reductions in materials can be attained. The reduction must be made in every component, since no single item dominates the amount.

5. Conclusions

The silicon tracking system of the SDC detector utilizes double-sided silicon microstrip sensors with a fast shaping front-end electronics. With its fine segmentation of 50 μm, good position resolution of ≤13 μm, and placement in close vicinity to the interaction point, the silicon tracking system is a critical component, complementing the outer tracker, to provide full-pattern recognition, vertexing, and stand-alone momentum measurement capabilities, among them, the last being particularly useful for electron identification. To realize a radiation-hard silicon microstrip sensor, radiation damage and its effects have been well studied. The SDC design is overcoming the problems associated with radiation damages on the surface and in the bulk of the silicon sensors.

The SDC silicon tracking system, with its 1 m diameter and 5 m full length, is the largest semiconductor tracking detector ever planned. The electro-mechanical design is required to have minimal dead regions, minimal material amounts, the ability to cool and operate the system at 0° C, and the precision to match the precision of the microstrip sensors. The state-of-the-art design of the electronics, the silicon ladders, the silicon shells, the space frame, and the cooling system are achieving the

requirements imposed by the goals of the SDC experiment and the physics opportunities provided by the SSC.

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Table 1
Summary of the principal requirements for the SDC tracking system

Parameter	Requirement	Comment
α_{accept}	$\lvert\eta\rvert \leq 2.5$	
ε_{recon}	≥ 97 %	$p_t \geq 10$ GeV/c
	≥ 90 %	10^{-34} cm^{-2}s^{-1}
σ_{p_t}/p_t^2	$\leq 20\%$ TeV/c^{-1}	$\lvert\eta\rvert \leq 1.8$
	$\leq 100\%$ TeV/c^{-1}	$\lvert\eta\rvert \leq 2.5$
σ_b	≤ 20 μm	$p_t \geq 10$ GeV/c
	≤ 100 μm	$p_t = 1$ GeV/c
$\sigma_{z\text{-}vertex}$	≤ 2 mm	
$\sigma_{z\text{-}cal}$	≤ 2.5 mm	

Table 2
Spatial resolutions of the SDC tracking system. The resolutions are of a double-sides of a silicon detector and of a straw superlayer and of a gas-micro strip (GMD) superlayer, including the local alignment errors in Section 4.1..

Subsystem	$\sigma_{r\text{-}\phi}$	θ_{stereo}	σ_z[a]
Silicon	10.5 μm	10 mrad	1.1 mm
Straw	85 μm	3°	1.6 mm
GMD	50 μm	5.7°	0.5 mm

[a] $\sigma_z = \sigma_{r\text{-}\phi}/\sin(\theta_{stereo})$

Table 3
Dimensions of the SDC silicon tracking system

Barrel	r (cm)	-z (cm)	+z(cm)	Silicon area
(1)	9	-30	30	
(2)	12	-30	30	
(3)	18	-30	30	
(4)	21	-30	30	6.8 m^2
(5)	24	-30	30	
(6)	27	-30	30	
(7)	33	-30	30	
(8)	36	-30	30	
Disks	**z (cm)**	**r_{in} (cm)**	**r_{out} (cm)**	**Silicon area**
(1)	33	15	39	
(2)	38	15	39	
(3)	44	15	39	
(4)	52	15	39	
(5)	61	15	39	
(6)	72	15	39	10.2 m^2
(7)	85	15	39	(both ends)
(8)	102	15	39	
(9)	122	15	39	
(10)	146	22.5	46.5	
(11)	182	28.5	46.5	
(12)	218	34.5	46.5	
(13)	258	40.5	46.5	
			Total silicon area = 17.0 m^2	

Table 4
Specifications of the SDC double-sided silicon strip sensor (Barrel)

(1) Substrate	
Type	n-type Si
Resistivity	4–8 kΩ·cm
Thickness	300±10 μm
(2) Size	
Overall dimension[a]	60 mm×34.1 mm
Stereo-effective area	58.8 mm×31.4 mm
(3) Strip	
Pitch	50 μm
Implant width	≥10, ≤12 μm
AC electrode width	<10 μm
No. of readout strips	640 /side
Axial-strip side	n-side (ohmic side)
Stereo-strip side	p-side
Stereo angle	10 mrad
Strip isolation of n-side	p^+ isolation line
(4) Capacitances	
AC coupling	≥20 pF/cm
p-side (body+interstrip)	≤1.2 pF/cm
n-side (body+interstrip)	≤1.4 pF/cm
(5) Bias resistor	
Polycrystalline silicon	250±50 kΩ
(6) Bias voltage breakdown	
Bulk	>150 V
AC coupling per side	>100 V
Maximum leakage current[b]	
overall	≤1 μA
per strip	≤100 nA

[a] Actual dimension is 60 μm narrower due to sawing

[b] Before radiation damaged

Table 5
Specifications of the main voltages, powers per channel, and total currents

	V_{bias} (V)	Power (mW/ch)	I_{total} (A)
Analog chip	3.5	1.0	1860
Digital chip	5.0	0.5	650
Microstrip sensor[a]	±125	0.25	3.3

[a] maximum after a fluence of 10^{14} particles/cm^2

Table 6
Local and global alignment requirements. These tolerances are after calibration and for the stability over time; the placement tolerances could be as large as 5 times these numbers.

Local	Circum-ferential	z (barrel) or r (disk)	r (barrel) or z(disk)
Silicon	5 μm	250 μm	80 μm
Straw	35 μm	250 μm	1200 μm
GMD	40 μm	1000 μm	250 μm
Global		Azimuthal rotation	Centering
silicon to straw		10^{-2} mrad	15 μm
silicon to GMD		10^{-2} mrad	45 μm
Tracker to beam		--	500 μm

Table 7
Components of the silicon tracking system and their radiation length (averaged over $|\eta|<2.5$).

Component	Material[a]	Effective Thickness[b] (cm)	Rad Length Xo (cm)	Average Amount (% Xo)	Comment
Beam Pipe	Be	0.1	35.3	0.69	r=4 cm
Inner Enclosure	Be	0.05	35.3	0.34	r=5 cm
Silicon Ladder	Si/G/CE	0.032	9.36	3.34	10(5)% overlap in Barrel(Disk)
FE electronics	Si/Be	0.0517	9.36	1.18	L=1.3 cm
Support Ring	G/CE	0.125	24.9	0.98	incl. wick
Support Cylinder	G/CE	0.071	24.9	0.34	Barrel 2-3, 5-6
Filler Gas	Butane	41	16000	0.62	
Cabling Barrel	Be/Kapton	0.063	35.3	0.42	40% of total
Cabling Disk	Be/Kapton	0.063	35.3	0.33	r=50 cm
Space Frame	Mg-MMC	0.33	16.8	0.72	r=50 cm
Outer Enclosure	G/CE	0.071	24.9	0.58	r=55 cm
Grand total				9.54	

[a] Be: Beryllium, Si: Silicon, G/CE: Graphite/Cyanate-Ester composite

[b] Combination of materials is adjusted to a equivalent thickness of the primary material

Figure Captions

Fig. 1 SDC tracking system. The inner-most is the silicon tracking system, surrounded by straw and gas-microstrip detectors, imbedded in a superconducting solenoid magnet for a 2 T magnetic field.

Fig. 2 (a) Transverse momentum resolution, and (b) Impact parameter resolution of the SDC tracking system as a function of the pseudorapidity for p_t of 1, 10, 100, and 1000 GeV/c. Without a beam constraint (solid curve) and with a constraint (dashed curve).

Fig. 3 Layout of the silicon tracking system: r-z view and x-y view

Fig. 4 Transverse momentum dependence of the efficiency-loss of electrons for an E/p cut, $0.5 < E/p < 1.5$, with the silicon system only (solid curve) and the full tracking system (dashed curve). The electrons passed through materials of 3.2% X_0 in front of the silicon, 7.7% X_0 in the silicon, and 9.7% X_0 in the outer tracker.

Fig. 5 Charged particle (solid curve) and neutron (dashed curve) fluences as a function of the radius for one year of operation at the standard luminosity

Fig. 6 Structure of the SDC DSSS: (a) cross section along the strip, and (b) across the strip

Fig. 7 Block diagram of the SDC frontend electronics; analog with bipolar and digital with CMOS chips.

Fig. 8 Cross section of the electronics-detector sandwich

Fig. 9 SDC DSSS ladder

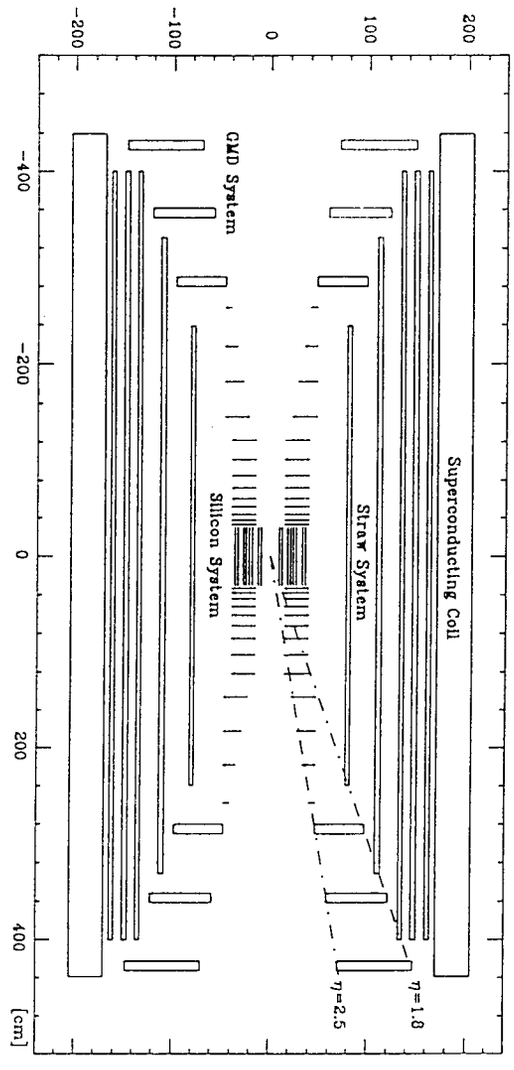
Fig. 10 Silicon shell assemblies of the barrel section

Fig. 11 Planar arrays of the forward disk region. The trapezoidal-shaped ladders are mounted alternately in the near and the far sides.

Fig. 12 Butane evaporative cooling test. Temperature at the heating surface over the saturating temperature as a function of pore radius of molded polystyrene (square), carbon foam (triangle), and porous beryllium (circle). The inverse relationship (dashed curve drawn to guide eyes) of the polystyrene indicates that evaporation occurs within the wick.

Fig. 13 Evaporative cooling scheme based on the use of porous beryllium on the surface of the beryllium hybrid substrate

Fig. 14 System assembly showing the silicon detectors, the space frames, and the outer enclosures



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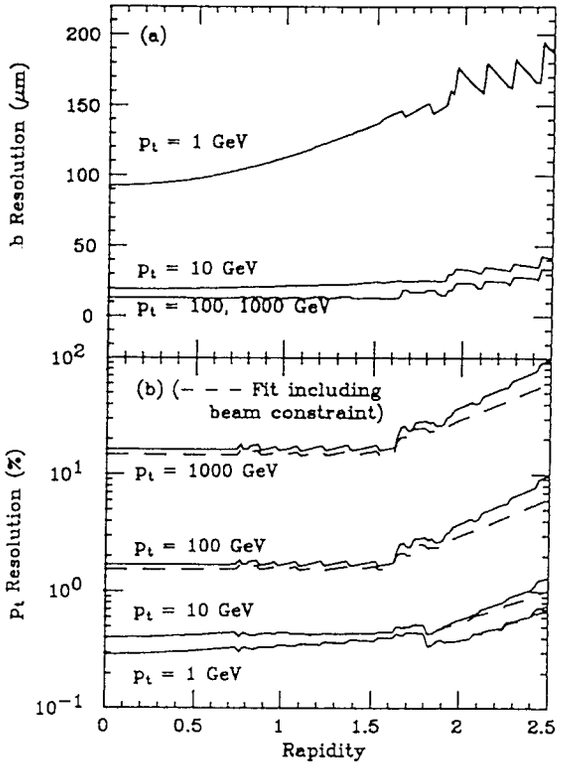

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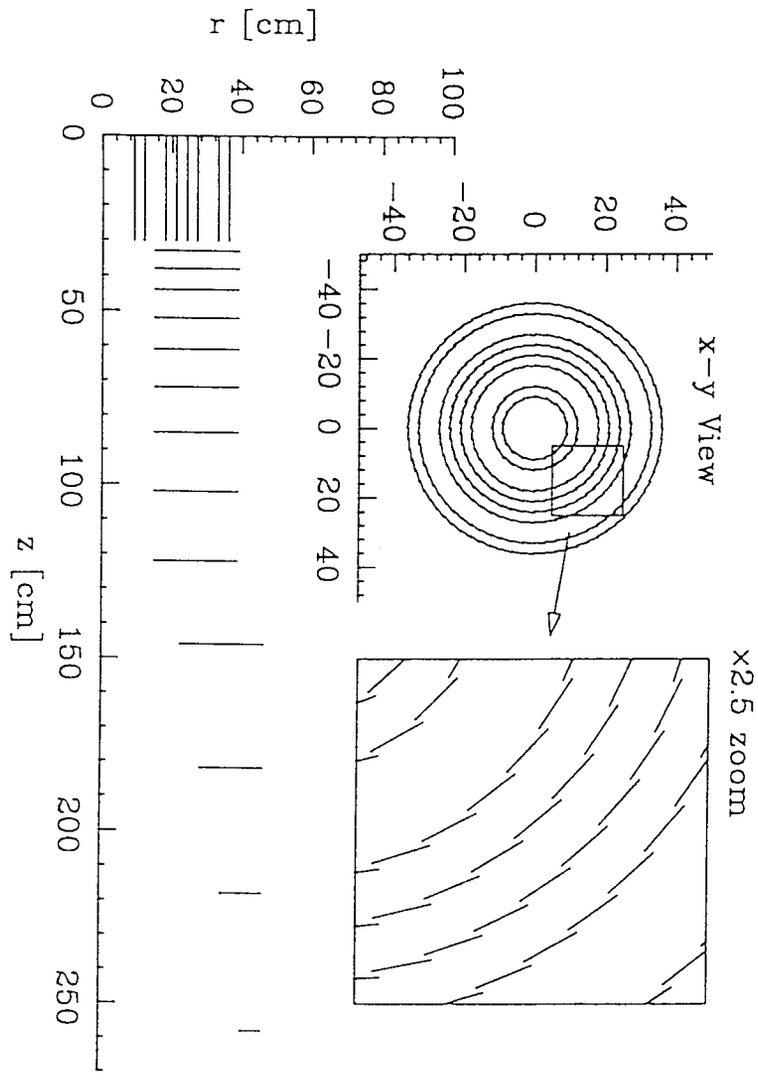

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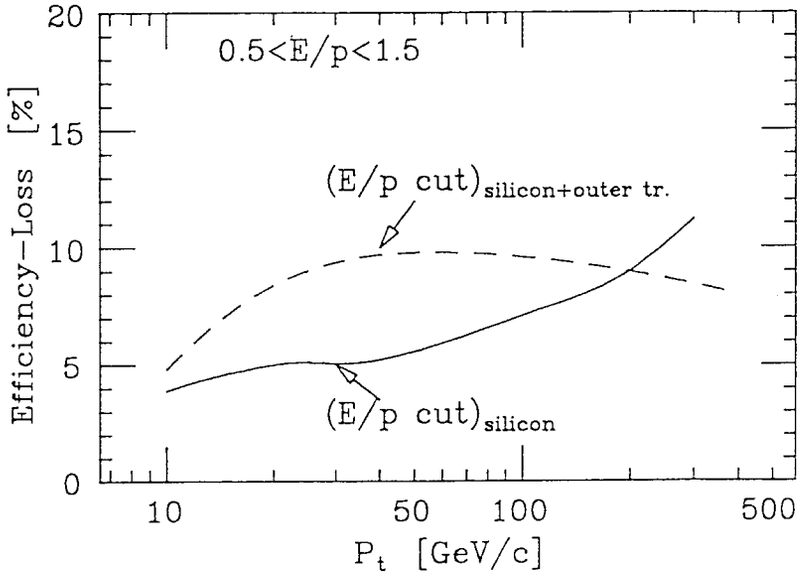

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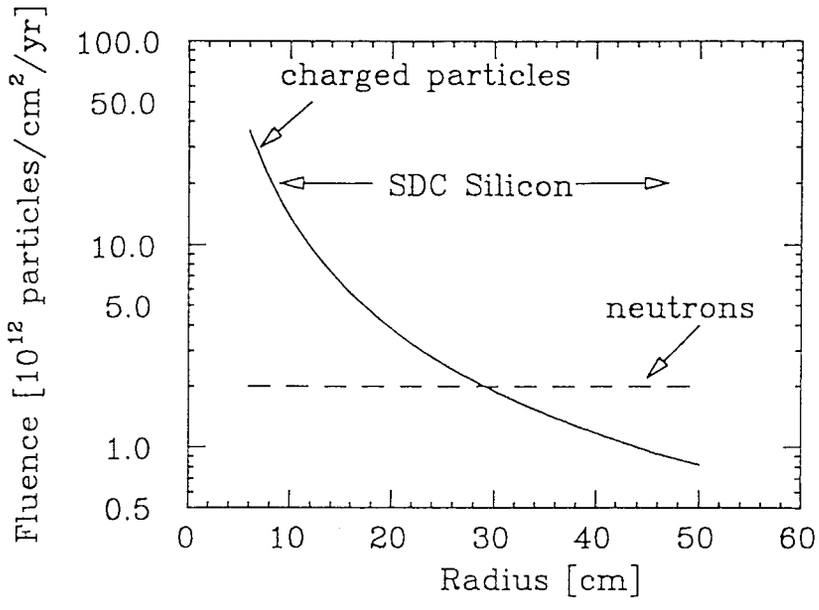

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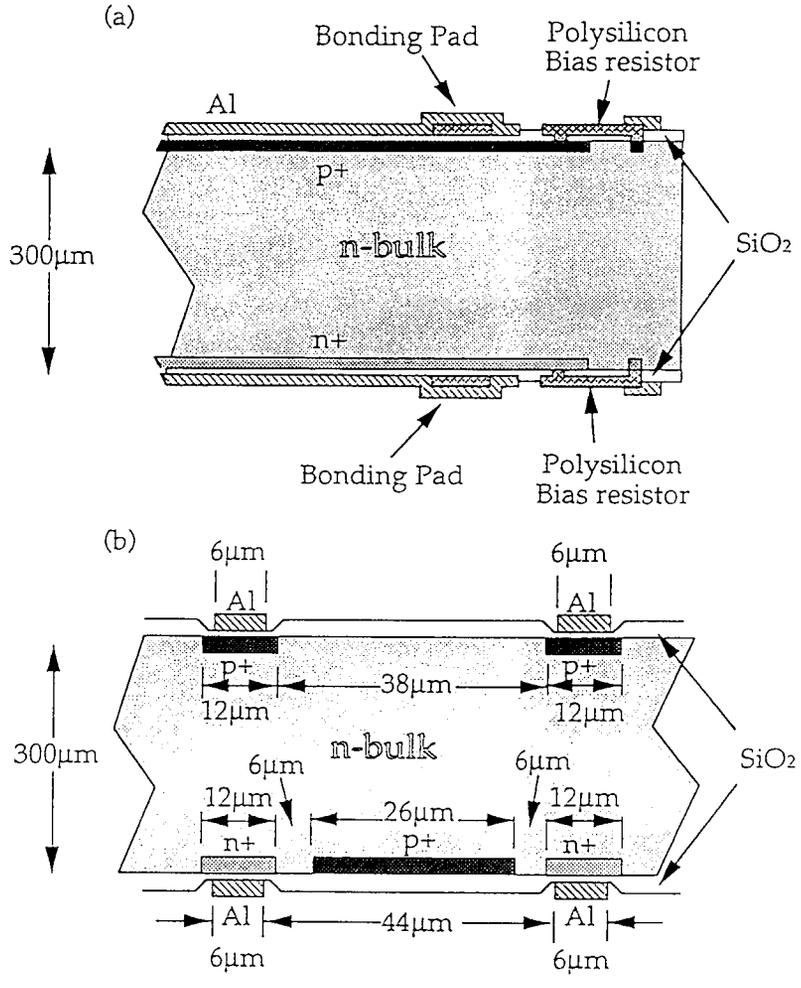

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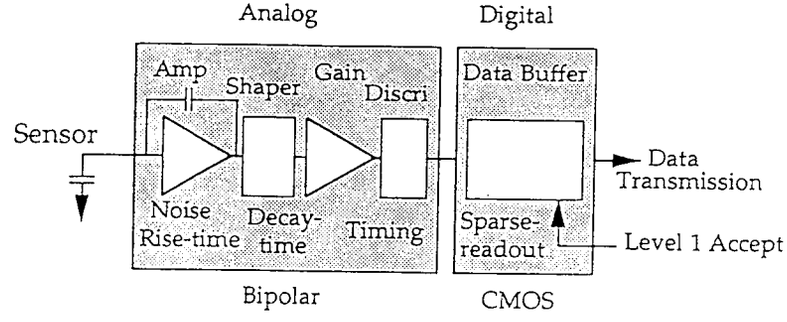

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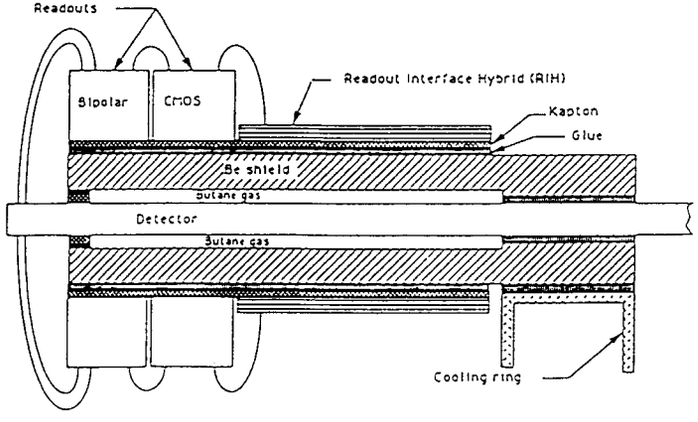
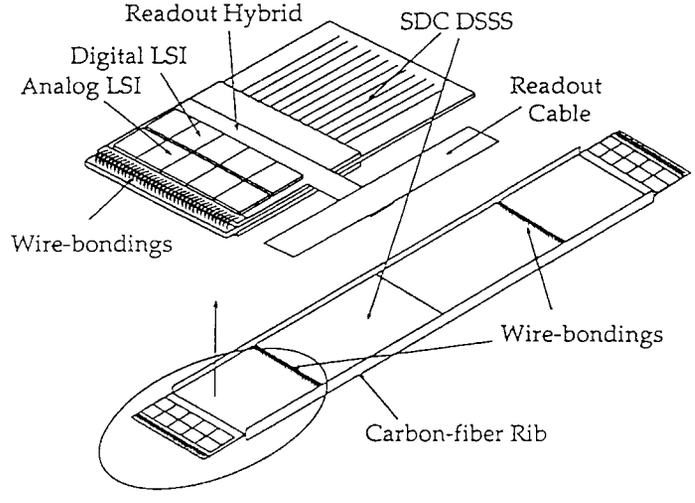


Fig. 8 Cross section of the electronics-detector sandwich



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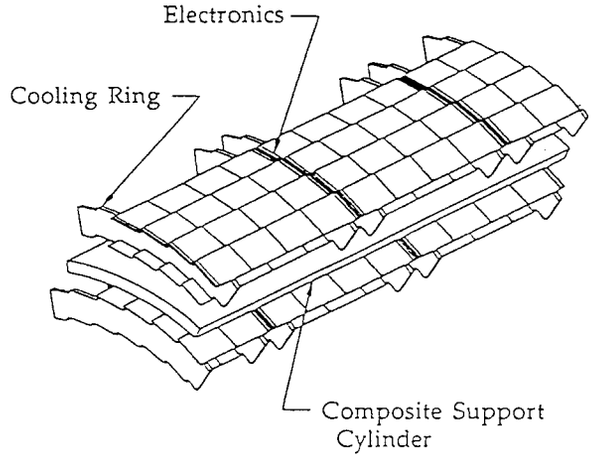

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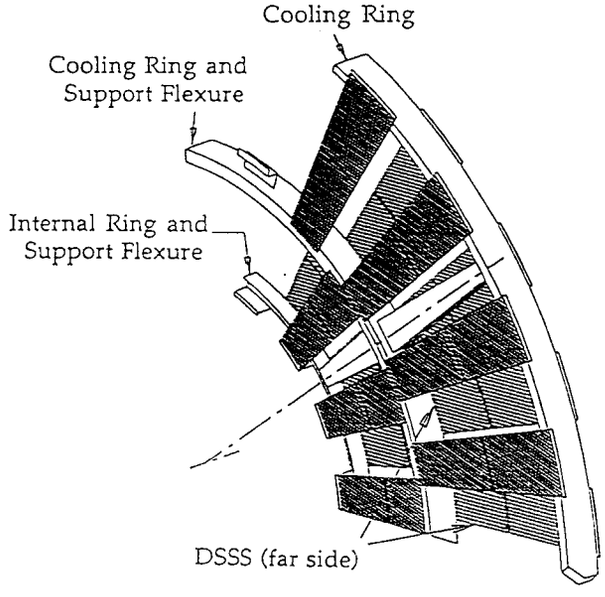

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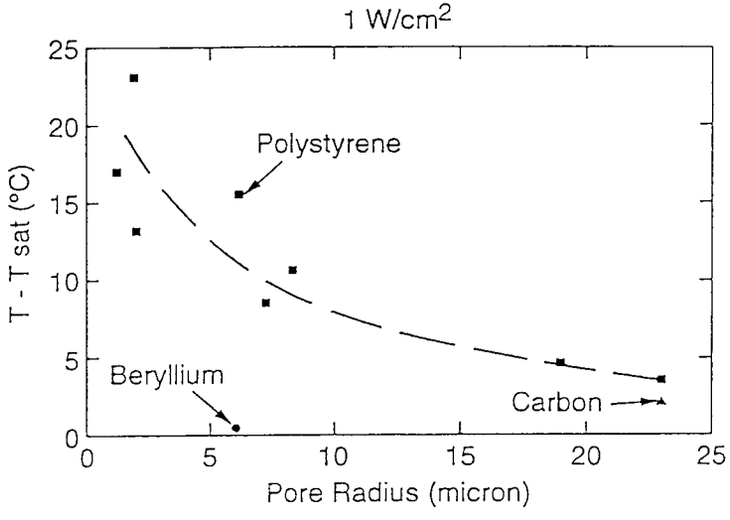

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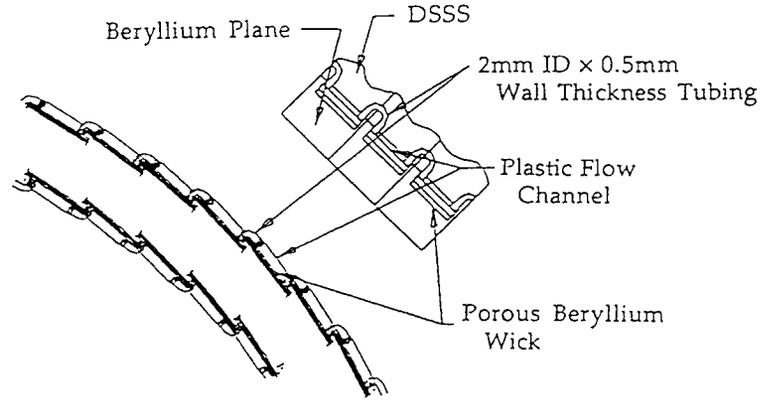

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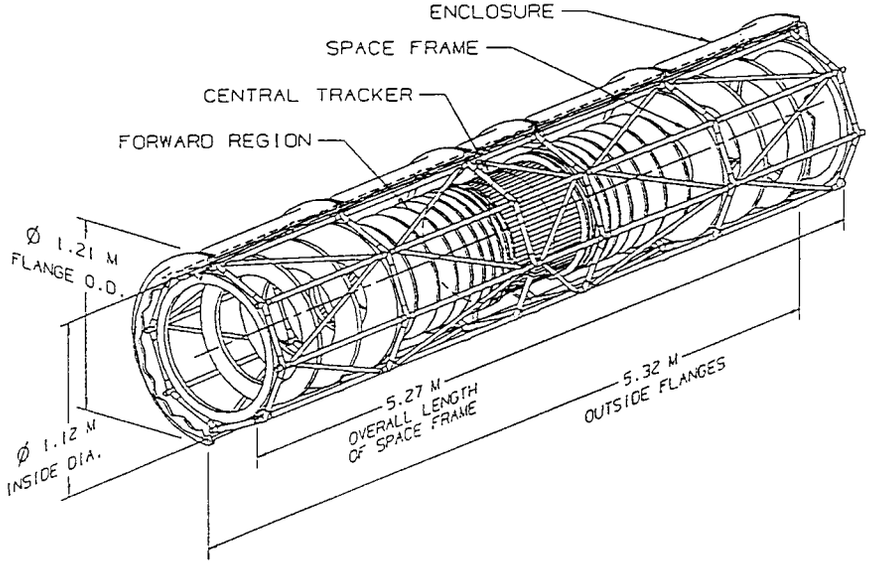

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