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# RADIATION TOLERANCE OF SINGLE-SIDED SILICON MICROSTRIPS

## The RD20 Collaboration

A. Holmes-Siedle, M. Robbins, S. Watts
*Brunel University, UK*

P. Allport
*Cambridge University, UK*

R. Brenner, H.-G. Moser, S. Roe, J. Straver, P. Weilhammer
*CERN, Geneva, Switzerland*

P. Chochula, I. Mikulec
*Comenius University, Bratislava, Slovakia*

S. Moszczynski, M. Turala
*Institute of Nuclear Physics, Cracow, Poland*

W. Dabrowski, P. Grybos, M. Idzik
*Faculty of Physics and Nuclear Techniques, Cracow, Poland*

D. Loukas, K. Misiakos, I. Siotis, K. Zachariadou
*N. C. S. R. Demokritos, Athens*

W. Dulinski, J. Michele, M. Schaeffer, R. Turchetta
*LEPSI, Strasbourg, France*

P. Booth, J. Richardson, N. Smith
*University of Liverpool, UK*

K. Gill, G. Hall, R. Sachdeva, S. Sotthibandhu, D. Vitè, R. Wheadon
*Imperial College, London, UK*

C. Arrighi, P. Delpierre, M.-C. Habrard, J.-C. Clemens, T. Mouthuy
*CPPM Marseille, France*

B. S. Avset
*University of Oslo, Norway*

L. Evensen, A. Hanneborg, T. A. Hansen
*Senter for Industriforskning, Oslo, Norway*

D. Bisello, A. Giraldo, A. Paccagnella
*INFN Padova, Italy*

L. Kurchaninov, E. Spiriti
*INFN Roma (Sanità)*

R. Apsimon
*Rutherford Appleton Laboratory, Didcot, Chilton, UK*

P. Giubellino, L. Ramello, W.L. Prado da Silva
*INFN Torino, Italy*

M. Krammer, M. Schuster
*IHEP Vienna, Austria*

## ABSTRACT

The RD20 collaboration is investigating the design and operation of an LHC inner tracking detector based on silicon microstrips. Measurements have been made on prototype detectors after irradiation with electrons, neutrons, photons, and protons for doses up to 5 Mrad and fluences up to $10^{15}$ particles/cm$^2$.

The annealing of effective doping changes caused by high neutron fluences, one of the major limits to detector lifetime at the LHC, is shown to be strongly inhibited by cooling below room temperature. Detailed results are presented on the critical issue of microstrip capacitance. We have also investigated bulk damage caused by high energy protons, interstrip isolation after neutron irradiation, and MOS capacitors irradiated with electrons and photons.

## 1. INTRODUCTION

The next generation of collider experiments in particle physics will be be carried out at high luminosity proton-proton machines, namely the Superconducting Super Collider (SSC) and the Large Hadron Collider (LHC), which are currently under construction or in the approval phase. Silicon detectors of several types are expected to be used extensively in the experiments being proposed for the SSC and LHC. Tracking of charged particles inside the experiments is of major importance and silicon microstrip detectors offer the granularity and spatial resolution required for excellent performance. Since they will be used quite close to the beams they will encounter high radiation doses from the flux of charged and neutral particles emerging from the interaction point. However it is important that the detectors should continue to provide excellent performance for many years of operation. In view of this, investigations are being carried out to define more precisely the detectors to be used in the LHC and SSC experiments and the limits to their operating lifetime.

Doses of up to 10 Mrad of ionising particles and fluences of $10^{13}$ - $10^{14}$ neutrons/$cm^2$ are expected over 10 years of high luminosity operation at LHC. This is a most challenging environment and major effects on the performance of silicon detectors result from damage to the crystal symmetry, by displacement of atoms from their lattice sites. Bulk damage causes lattice defects whose effect is dependent on their energy level within the band gap. The dominant effect of deep traps, with energy levels close to the centre of the band gap, is to increase the leakage current of the detector. Leakage current leads to shot noise in the readout electronics which, eventually, will obscure the signal. Shallow traps, close to the edge of the band gap, mainly alter the effective doping of the bulk silicon and therefore the minimum voltage required to deplete the detector. This voltage should not become greater than the breakdown voltage of the detector.

Since microstrip detectors are usually operated close to room temperature the evolution of the defect structures can also be of great importance. Many defects are mobile and move around the lattice until they are trapped or combine with others. Techniques such as Deep Level Transient Spectroscopy (DLTS) and Thermally Stimulated Current (TSC) have been applied to identify these changes [24]. For the case of high resistivity detector silicon, however, the microscopic picture, particularly of the annealing behaviour, remains uncertain. It is therefore still necessary to observe and quantify the overall macroscopic effects in an empirical manner.

Surface damage occurs through ionisation within the oxide. Charge build-up, due to holes being trapped in the oxide, causes the charge density of the electron accumulation layer at the interface to increase which will affect the interstrip capacitance (high oxide charge can also lead to junction breakdown). The density of the Si/$SiO_2$ interface states is increased, and these can also influence the performance of the detectors by changing both interstrip resistance and

capacitance. Surface damage is particularly important for reach-through [1,2] and FOXFET biasing techniques [3].

## 2. DETECTOR DESIGN

Although single-sided microstrips are considered to be a fairly mature technology, our application is sensitive to almost every aspect of the strip geometry. In addition, little data exists on their radiation tolerance at such unprecedentedly high doses. Because of this, we chose to produce a range of dedicated test devices in order to make a systematic study of the important strip parameters. They were designed at Imperial College, London and produced at the Senter for Industriforskning (S.I.), Norway [4]. Their major characteristics and the motivation behind them are summarised below.

A strip pitch of 50 μm was chosen because the large size of any LHC inner tracking detector means that precision better than about 20 μm will be made difficult due to mechanical constraints. 50 μm pitch is therefore perfectly adequate, and is also well matched to the V.L.S.I. readout amplifiers.

The high leakage currents caused by radiation damage mean that AC-coupling will be very desirable in order to avoid large currents flowing into the input stages of the readout amplifiers. Operational experience from experiments such as the DELPHI and OPAL micro-vertex detectors at LEP [5,6] has shown that integrated AC-coupling is a viable technique which would be invaluable for our application.

For AC-coupled microstrips, a biasing arrangement which allows the leakage current to flow to ground is required. We chose integrated polysilicon resistors, which have already been shown to be extremely radiation-hard [7]. Alternative bias schemes using reach-through or FOXFET techniques are cheaper to produce but they are sensitive to surface effects and have yet to be proven able to withstand the radiation levels expected at the LHC. However, since detector cost is also a major consideration, these methods of biasing are also being evaluated within RD20 [8].

We chose the nominal value of the resistors to be 200 kΩ, low enough that the leakage currents due to irradiation do not lead to large voltage drops, but still high enough so that they do not contribute significantly to the noise of the intended readout system [9].

Having made these choices, the geometrical layout can then be optimised. There are several factors which influence the design.

One of the most important parameters of a microstrip detector is the strip capacitance, which originates mainly from the geometry and dimensions of the surface conducting layers. In

an LHC tracking detector, power dissipation limitations mean that the electronics noise of read-out amplifiers is highly dependent on detector capacitance and therefore the strip capacitance must be minimised by making the strip width as narrow as possible. However, since almost all other strip parameters benefit from increasing the strip width, a compromise must be made.

If coupling capacitors are integrated onto the detector, their value must be high enough to ensure that all the signal charge is coupled to the amplifier rather than to neighbouring strips. This can be achieved by decreasing the thickness of the isolating oxide between the aluminium line and the $p^+$ strip, but processing considerations mean that it cannot be made too thin since it is also essential to avoid faults or breakdown in the oxide leading to a direct connection between $p^+$ and aluminium. At this point, the only alternative is to increase the strip width.

The resistance of the strip metallisation is greater for the narrower strips and can degrade the noise performance by introducing series resistance at the amplifier input. Some control is possible through making the metal thicker rather than wider but limits from lithography and deposition may still require wider strips.

For strips with integrated capacitors, a high $p^+$ sheet resistance is undesirable in the presence of high leakage currents since voltage drops along the length of the strip could distort the collection field within the silicon. However, increasing the $p^+$ doping too far could lead to poorer quality detectors, due to the higher temperatures required during processing, in which case wider strips would again become necessary.

As will be shown later, high bulk damage leads to a reduction in the resistance between neighbouring strips. This resistance is dependent on the strip gap, with the highest resistance being obtained from the largest gap - ie the narrowest strip.

## The RD20 p-side test structures

In order to study the optimisation of the geometry, microstrip structures with a range of strip widths were produced. Table 1 details the different geometries chosen.

The wide range of measurements necessary meant that one of the most important design considerations was to make the structures as easy to test as possible, with access to all strip parameters. Examples of the prototypes produced at S.I. are described below:

### a)    DC-Coupled Strips  (figure 1(a))

These were designed for simple probe station measurement of the strip capacitance. There are nine strips per strip width, which had been shown to be sufficient from previous simulations and measurements [10], with a common guard combining all the strips into a single structure. In order to reduce the number of probe connections, the outer three strips on each

side are joined by metallisation so that a total of only six probes is required. This configuration allows separate measurement of the dominant contribution to the capacitance from the two nearest neighbour strips, along with the contributions from the rest of the strips and from the backplane. One further point of note is that the normal S.I. 5-mask design rules for contact windows limit the minimum strip width for a continuous DC contact to a mask width of 25 μm. In order to make narrower DC-coupled strips, a "chain of contacts" technique was used (as can be seen in the figure) allowing the full range of strip widths to be covered.

## b)    AC-Coupled Strips  (figure 1(b))

These were designed as totally independent 20 strip units for each strip width. They have substantial probe pads for direct contact to the p+ strips themselves (important for repetitive testing of interstrip isolation), but in all other respects the strips are as they would be in a full-size detector. Each 20 strip unit has its own guard and bias line, with the strips being biased through polysilicon resistors at alternate ends.

The complete four-inch wafer layout included simple diodes for annealing studies, AC and DC microstrip test structures with lengths 1, 2, and 4 cm, test structures for reach through and FOXFET bias schemes, and general process evaluation test devices.

## 3.    PROCESSING OF THE PROTOTYPES

The process is identical to the process for double-sided silicon microstrip detectors [11] at the time of processing except for the lack of lithography on the n-side. It has a phosphorous field implantation ("Layer 0"), a uniform phosphorous doped layer on the backside for contact and gettering and the strips are deposited from boron nitride solid sources. A uniform layer of approximately 100 nm Low Pressure Chemical Vapour Deposited (LPCVD) silicon nitride is used as extra passivation on top of the oxide and is also an integral part of the coupling capacitors. The nitride is believed to have improved stability towards environmental changes and the diffusivity of alkali ions (fast diffusers in silicon oxide) is very low. Boron implanted LPCVD polysilicon is used for biasing. The mask set contains structures for punch-through biasing but the process and design rules are not optimised towards this feature. Several of the narrow gap devices were shorted because of sideways diffusion.

The n-type wafers were delivered by Wacker Chemitronic GmbH and have a resistivity between 3000 Ωcm and 5000 Ωcm, they are single sided polished with (111) orientation. The thickness is 280 μm. A 910 nm field oxide was grown with a combination of TCA and wet oxidation. TCA or 111-Trichloroethane is fed into the furnace with oxygen where it decomposes to HCl and water. Oxygen and hydrogen react in a chamber outside the furnace to create water vapour for the wet oxidation. This first oxide is removed from the backside in buffered

hydrofluoric acid while the front side is protected with positive photoresist. The oxide on the front side serves as a mask for the phosphine gas while depositing phosphorous on the backside. The areas to receive a phosphorous field implantation on the front side are opened by etching in buffered hydrofluoric acid and protecting the oxide with positive photoresist. A thin oxide is grown over the phosphorous doped layer on the backside and in the opened areas on the front side. The wafers are then implanted with phosphorous at a low energy and dose on the front side, before the implant damage is annealed out and a new thick field oxide is grown in the active region of the detector.

Openings for the p-strips are then defined by lithography in the 870 nm of oxide. A ramped furnace process with solid boron nitride wafers as the boron source [12] is used for doping the p-strips. The advantages of the solid deposition are the low sheet resistance achieved at low temperature, the uniformity of the boron layer across the wafer and the possibility to process large batches of up to 50 wafers, at the same time. A short and controlled injection of hydrogen at 900 °C activates the boron wafers and is followed by a soak at 995 °C. The sheet resistance varied between 23 $\Omega$/square and 28 $\Omega$/square in this run. The sheet resistance can be varied additionally by the length of a low temperature oxidation at 750 °C. The final junction depth of the p-strips is about 2.1 $\mu$m, with a sheet resistance of around 80 $\Omega$/square. A coupling oxide, 240 nm thick, is grown at 1000 °C with a combination of TCA and wet oxidation.

105 nm of LPCVD silicon nitride is deposited on the wafer and contact holes to the p+ diffusion are opened with lithography and Reactive Ion Etching (RIE). LPCVD polysilicon for the integrated resistors is deposited on the wafer and doped by boron implantation at an energy of 55 keV to a dose of $1.3 \times 10^{14}$ cm$^{-2}$. The ion implantation is annealed at 900 °C for 30 minutes in nitrogen before a 120 nm masking oxide is grown over the polysilicon by TCA oxidation. Photolithography defines the polysilicon pattern in the masking oxide before etching of the polysilicon. Finally, the masking oxide is stripped away in hydrofluoric acid. The polysilicon resistors are passivated by 240 nm silicon dioxide in a final high temperature oxidation at 1000 °C.

Photolithography and etching in buffered hydrofluoric acid opens contact holes in the polysilicon oxide. About 1 micrometer of aluminium is deposited on both sides of the wafers by sputtering and the metal is patterned before alloying in forming gas (10% $H_2$ in 90% $N_2$) at 450 °C for 15 minutes. All the wafers were left unmetallised on the backside to enable signal testing using pulsed infra-red light.

The purpose of the Layer 0 field implantation is to ensure good strip isolation under conditions of low oxide charge. Since it was not obvious that this would be necessary for operation under LHC conditions, half of the wafers were not given the Layer 0 treatment.

These wafers had the same process for the first field oxide and the phosphorous on the backside. All wafers were processed together after the implantation step and the process is identical except for the lithography step and growth of the thin implantation oxide.

## 4. RESULTS

### a) Leakage Currents

Figure 2 shows the typical leakage currents for the AC microstrips plotted against strip width. The values for the narrow strips are significantly higher than was expected, but still perfectly adequate for our application. There is a clear dependence on the strip width which indicates that most of the current is due to surface generation, and this was confirmed by measurements on gated diodes from the same wafers. It can also be seen that the strips with the Layer 0 treatment have lower leakage currents. This may be due to either the gettering properties of the phosphorus implant or different band bending at the surface, but, in any case, the differences are not large.

The source of the higher leakage currents is process-related and has yet to be established. The most likely cause is considered to be related to surface generation, along with extended defects within the bulk, possibly as a result of the nitride layer which can prevent annealing of interface states and also indirectly affect gettering performance. However, these currents are still orders of magnitude less than the currents from bulk damage due to irradiation, and are therefore of little consequence. The performance of the detectors was not observed to be degraded in any way.

### b) Bulk Damage Due to High Energy Protons

Irradiations were performed at the SATURNE cyclotron, Saclay, using 500 MeV protons to obtain fluences of up to $7.5 \times 10^{14}$ protons/cm$^2$. This is a good approximation to experimental conditions at the LHC where the mean energy of protons within the detector is expected to be in the same range [13].

The samples measured were $5 \times 5$ mm diodes from the S.I. RD20 p-side test structures. Three diodes were used, biased at 80 Volts during irradiation. All measurements were made a few minutes after irradiation, using an HP4284A LCR meter, a Keithley 237 source/measure unit, a $\pm 1000$ V Ortec voltage source and a probe station. Because of the fast access, it was possible to do cumulative irradiations on the same diodes without introducing problems due to annealing. Once the final doses had been reached, the diodes were left for 30 days at room temperature before measuring them again.

Figure 3 shows the variation of leakage current density with proton fluence, corrected to 20 °C but with no correction made for the effects of short-term annealing. Also included in

the figure is the corresponding data for neutron-irradiated diodes previously measured [14]. From the measurements made shortly after the end of the irradiation, the average value of the damage constant is found to be $3.6 \times 10^{-17}$ A/cm, and after 30 days annealing, the value is down to $2.0 \times 10^{-17}$ A/cm. These values are within the range of those from other experimenters [15, 16, 17] and indicate that the damage constants are not substantially different for protons and neutrons.

Figure 4 shows the variation of depletion voltage with proton fluence, again uncorrected for short-term annealing. This agrees well with results from both 800 MeV protons [18] and 1 MeV neutrons [14], with type-inversion occurring at around $2 \times 10^{13}$ protons/cm$^2$.

## c)   The Effect of Temperature on the Self-Annealing of Bulk Damage

It has previously been observed that, for neutron-irradiated silicon detectors, self-annealing at room temperature causes further changes in their effective doping concentration, resulting in the bulk silicon becoming more p-type with time [14]. We have made long-term studies of these doping changes in simple diodes produced by both Micron Semiconductor Limited, UK, and Senter for Industriforskning, Norway, using wafers from Wacker Chemitronic GmbH, Germany. These diodes are $5 \times 5$ mm with a thickness of 300 µm and an initial depletion voltage of around 30 - 40 V. All the diodes were irradiated at the ISIS spallation neutron source at the Rutherford Appleton Laboratory in the UK [19] where the neutron spectrum is similar to that expected at the LHC, peaking at around 1 MeV. Dose rates of up to $2 \times 10^{13}$ n/cm$^2$ per hour can be achieved.

In each case, pairs of diodes were irradiated at room temperature, and subsequently one of the pair was kept under controlled reduced-temperature conditions (stable to $\pm 1$ °C), whilst the other was left at room temperature (typically $25 \pm 3$ °C). Periodically, the depletion voltage of both diodes was recorded by measuring their CV characteristics, allowing the cooled diode to warm up to room temperature for the short time required to make the measurement. Figure 5 shows the time dependence of depletion voltage for four different pairs of diodes exposed to neutron fluences of up to $10^{14}$ n/cm$^2$. All controlled diodes were kept at 10 °C or less and it can be clearly seen that this modest reduction below ambient temperature is enough to halt the annealing process (within the experimental errors), independent of the initial dose. In particular, it can be seen from figure 5(d) that the cooled diode is maintained at an acceptable operational voltage whereas the depletion voltage of the diode at room temperature quickly rises beyond 200 Volts.

In order to determine the point at which the self-annealing begins to occur, the temperature of a few of the controlled diodes was raised to 15 °C. Figure 6 shows a typical result. The two diodes were irradiated to $(7.5 \pm 2.1) \times 10^{13}$ n/cm$^2$. About two months after the irra-

diation, one of them was transferred to a container maintained at 10 °C. Over the next 100 days, there was no significant change in the depletion voltage of the diode kept at 10 °C whereas the depletion voltage of the diode kept at room temperature increased from ~ 90 V to ~ 120 V. At that point, the temperature of the controlled diode was raised to 15 °C. Now, over a further 100 days, the depletion voltage of the controlled diode also began to increase. This behaviour has been observed consistently for several detectors, independent of dose, and so we conclude that the annealing of the doping changes can be strongly inhibited if the detectors are kept at or below 10 °C.

## d)   Interstrip Isolation

The interstrip isolation for p-side microstrips is not expected to be decreased significantly by electron or photon damage, and we have confirmed this up to 5 Mrad. Neutron damage, however, has already been seen to cause reductions by orders of magnitude in the isolation resistance between two p-type regions [14].

Figure 7 shows the bias dependence of interstrip isolation for RD20 microstrips irradiated at the ISIS neutron source. The values quoted are the resistance between a strip and both its nearest neighbours, with all other strips biased normally. Strips of various lengths were used in the measurement and so the numbers are extrapolated to 6 cm, assuming a linear dependence. No obvious difference was observed between the strips with Layer 0 and the strips without. Some of the measurements were made several months after irradiation, where the depletion voltage of the higher dose strips has increased significantly due to the doping annealing. For the two highest doses, which are well beyond the inversion fluence, it can be seen that the isolation resistance remains low until the bias reaches full depletion, at which point it rises sharply by a factor of ten or more. This is consistent with the bulk having become effectively p-type material.

Figure 8 summarises the results for the 5, 10, and 15 $\mu$m strips, with all values quoted at 100 V, except for the two highest doses where higher depletion voltages are required. Apart from the values before irradiation, which are so high that any surface contamination or moisture could have a significant effect, it can be clearly seen that the isolation resistance is dependent on strip gap, with the widest gap (ie narrowest strip) providing the best performance. No obvious differences were observed between strips with Layer 0 and strips without. Overall, we conclude that, for our application, the p-side strip isolation remains satisfactory for neutron doses up to at least $10^{14}$ n/cm$^2$.

# e) Strip Capacitance

## i) Before irradiation

Figure 9 shows the unirradiated microstrip capacitance at 100 V, measured at 100 kHz, for DC-coupled strips with and without Layer 0. The values were measured using 4 cm long strips and then scaled to pF/cm. The total capacitance of a strip is the sum of three distinct components: the capacitance to the backplane, the capacitance to its two nearest neighbours, and the capacitance to the rest of the strips (the *"other neighbours"*). In many of the results, the interstrip capacitance is quoted which is the capacitance to all strips, combining the nearest neighbour and other neighbour contributions. From figure 9, it is clear that the nearest neighbour capacitance is the dominant contribution, and this varies with strip width. The capacitance to the other neighbours and to the backplane are approximately independent of width.

It can also be seen from figure 9 that strips with Layer 0 have a higher capacitance than those without. Comparing the components, the increase is entirely restricted to the nearest neighbour capacitance, and we therefore attribute this to the enhancing effect of the field implantation on the conductivity of the surface accumulation layer.

The variation of the interstrip capacitance with frequency for unirradiated microstrips has been investigated up to 1 MHz. The results for 1 cm strips with Layer 0 are shown in figure 10, indicating almost no frequency dependence at 100 V.

## ii) Electron irradiation

4 cm DC microstrips were irradiated using the 2 MeV electron beam facility at Strasbourg [20]. This facility allows high doses to be achieved in short times, with dose rates up to tens of Mrad per hour. The devices were irradiated unmounted, and therefore electrically floating. Several doses were given to each device in a cumulative manner, with the capacitance being measured in the periods of a few days between each exposure. The nearest neighbour capacitance at 100 V is seen to increase with dose, whilst the other neighbour and backplane capacitances remain constant. Figure 11 show the dose dependence of interstrip capacitance at 100 V, measured at 100 kHz, for the 5, 10, and 15 $\mu$m strips. A fairly sharp rise is seen in the first 200 krad but then the rate of increase slows and the capacitance is close to being saturated beyond 1 Mrad. Layer 0 appears to have no discernible effect on either the magnitude of the capacitance increases or the dose rate dependence, remaining simply as a constant extra contribution to the total capacitance. Figure 12 summarises the results for the strips without Layer 0 after saturation.

Before irradiation, the interstrip capacitance is constant with bias once full depletion has been reached. After irradiation, the interstrip capacitance continues to decrease significantly as the device is biased beyond full depletion. Figure 13 shows this effect for one particular strip width; the depletion voltage is approximately 50 V.

### iii) Photon Irradiation

Irradiations of both 4 cm DC and 4 cm AC microstrips with Layer 0 were made at INFN Sanità in Rome using the $^{60}$Co source of the Italian I.S.S. The ionising dose rate from this source was 83 krad/hour. The devices were mounted on printed circuit boards allowing the possibility of irradiation under bias. One pair of AC and DC detectors was irradiated under bias at 100 V in steps to accumulated doses of 200 krad, 500 krad, 1 Mrad, and 2 Mrad, measuring the detector properties a few minutes after each exposure. A second pair was irradiated unbiased to 2 Mrad in a single exposure.

Figure 14 shows the dose dependence of the interstrip capacitance at 100 V, measured at 1 MHz, for both the DC and AC strips irradiated under bias. As with the electron irradiations, the capacitance is seen to be reaching saturation by about 1 Mrad. There is no significant difference between the behaviour of the AC and DC strips. Figure 15 summarises the saturation results for the unbiased DC strips at 100 V and figure 16 for the biased DC strips. There is no clear difference between the biased and unbiased cases, but the increases are clearly less than those in figure 12 which were measured at 100 kHz. Measurements on these devices made at 100 kHz were consistent with the results of the electron irradiation, and we therefore conclude that the physical mechanisms causing the increases in capacitance are frequency-dependent. Since 1 MHz is closer to the frequency range of interest for the signal processing speeds at the LHC, the results at this frequency are considered to be more relevant to our application than those at 100 kHz.

### iv) Proton Irradiation

Irradiations of 1 cm DC strips were made with 6 MeV protons at the Laboratori Nazionali di Legnaro-INFN, Padova. Although far from minimum-ionising (the average penetration depth of 6 MeV protons in silicon is ~ 300 μm), the aim was to investigate the effects on interstrip capacitance, and therefore only the damage to the surface region is important. Two structures were irradiated, to 100 krad and 500 krad (corresponding to fluences of $5 \times 10^{10}$ and $2.5 \times 10^{11}$ protons/cm$^2$) respectively. Figure 17 show the interstrip capacitance at 100 V, measured at 100 kHz. The increases are no worse than for the electron/photon damage, and, comparing the 100 krad and 500 krad increases, we would expect that saturation of the increases in interstrip capacitance will occur for proton irradiation also.

### v ) Neutron Irradiation

Microstrips designed for capacitance investigations produced by S.I. in a previous production run were irradiated at the ISIS neutron source. These strips have no nitride or Layer 0 treatment and are described elsewhere [10]. They cover a wide range of different geometries. Figure 18 shows the results measured at 100 V and 100 kHz. There are some increases in the nearest neighbour capacitance, but ionising radiation from the activation of the surrounding materials during the irradiation is considered to be the most likely cause.

### vi) Annealing behaviour

Figure 19 shows the interstrip capacitance measured against time, for one set of the DC strips irradiated with electrons at Strasbourg. It can be seen that there is no decrease in the capacitance at 100 kHz over 8 months, in fact there seems to be a small increase. The important issue here is the presence of the nitride layer, as will be discussed further in the next section, which is known to inhibit the annealing of oxide charge. However, as will also be shown in the next section, fields across the oxide region are very important. Figure 20 shows first results on annealing from the DC strips irradiated under bias at Roma. This does appear to show a decrease with time.

## f ) Electron and photon irradiation of MOS capacitors

MOS capacitors can provide important information about both the state of the oxide and the silicon/oxide interface [21]. MNOS (metal-nitride-oxide-silicon) capacitors from the S.I. RD20 p-side structures and normal MOS capacitors from a previous S.I. production run without nitride were irradiated at Strasbourg, at the same time and under the same conditions as the microstrips already described.

Figure 21 shows the variation of oxide charge density with electron dose for the different devices. For the MOS capacitors, the charge density is almost saturated at 1 Mrad, whereas the saturation for MNOS capacitors is slower. The saturated charge density is lower for the MNOS than the MOS. However, it is important to note that, since the devices were floating, the field across the oxide is undefined because charging effects can occur due to the very high impedance of the oxide.

Figure 22 shows the variation of oxide charge density with time after irradiation. For the MOS devices it can be seen that there is significant annealing of the oxide charge, whereas for the MNOS devices there is only a very slight reduction over a period of several months. This effect of the nitride layer inhibiting the oxide charge annealing has already been observed in radiation hardness studies on integrated circuits and also CCD's [22].

The effect of bias during irradiation on the flat band shift has also been investigated using a small $^{60}$Co source at Brunel University. Figure 23 shows the flat band shifts after 150 krad, at a dose rate of ~ 3 krad/hour, for different gate bias voltages. It can be seen that the zero gate bias leads to the lowest oxide charge build-up, with -100 V producing a substantially higher flat band shift. Both MNOS and MOS devices were also irradiated at +100 V which caused the flat band to become unmeasurably high - above 200 V. This effect of the bias is also well-known from radiation hardness studies for integrated circuits and also FOXFET biasing techniques [23], and clearly has implications for field plate isolation schemes for double-sided microstrips. It can be seen for the case of -100 V gate voltage that the initial charge build-up is higher for the MOS than the MNOS capacitors. In addition, there is now some visible annealing occurring for the MNOS capacitors with -100 V gate bias, although not for those with zero gate bias. This would be consistent with the interstrip capacitance of the microstrips irradiated under bias showing some annealing whereas those irradiated unbiased remain unchanged.

## g) Other strip parameters - coupling capacitance, p$^+$ and metal resistance

The other strip parameters of importance are the coupling capacitance, the p$^+$ strip resistance, and the readout metal resistance. Typical values for the 5, 10, and 15 µm strip widths are quoted in table 2; the spread of the values is not quoted due to a lack of statistics at this point in time but is expected to be generally no more than 20 %. For this process, the actual widths are about 3 - 4 µm greater than nominal due to the p$^+$ diffusion spreading. The coupling capacitance is measured quasi-statically, using a Keithley 595 Quasi-Static CV meter, in order to avoid frequency-dependence which would otherwise arise due to the p$^+$ strip resistance. None of the values are expected to change significantly under irradiation.

## 5. CONCLUSIONS

These results demonstrate that, with suitable design, single-sided silicon microstrips can be operated successfully as part of an inner tracking detector at the LHC for the projected lifetime of the project. One important requirement can be defined, which is that the detector system will need to be maintained below 10 °C in order to control long term annealing of effective doping changes.

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## Table 1

Dimensions of the RD20 microstrip test structures

| Geometry | Nominal P$^+$ Width (μm) | Nominal Metal Width (μm) |
|----------|--------------------------|--------------------------|
| 1 | 5 | 10 |
| 2 | 10 | 15 |
| 3 | 15 | 20 |
| 4 | 20 | 15 |
| 5 | 30 | 20 |
| 6 | 40 | 20 |

## Table 2

Typical values of important process-dependent microstrip parameters
measured for the RD20 microstrip test structures

| Nominal strip width (μm) | Coupling capacitance (pF/cm) | P+ resistance (kΩ/cm) | Metal resistance (Ω/cm) |
|--------------------------|------------------------------|-----------------------|-------------------------|
| 5 | 9.7 | 110 | 34 |
| 10 | 15.0 | 63 | 22 |
| 15 | 20.5 | 42 | 16 |

## Figure Captions

1. Mask details of (a) DC-coupled, and (b) AC-coupled RD20 microstrip test structures.

2. Leakage current of AC strips as function of strip width.

3. Leakage current density at 20 °C and 80 V as a function of proton and neutron fluence.

4. Depletion voltage as a function of proton fluence.

5. Comparisons of effective doping annealing after neutron irradiation for different fluences and temperatures.

6. Effective doping annealing after neutron irradiation for 10 °C and 15 °C.

7. Interstrip isolation resistance as a function of bias for 10 μm strips.

8. Interstrip isolation resistance as a function of neutron fluence for different strip widths.

9. Pre-irradiation microstrip capacitance at 100 V, 100 kHz for DC-coupled strips.

10. Frequency dependence, before irradiation, of interstrip capacitance at 100 V for DC-coupled strips with Layer 0.

11. Interstrip capacitance at 100 V, 100 kHz as a function of electron dose for DC-coupled strips with and without Layer 0, unbiased during irradiation.

12. Interstrip capacitance at 100 V, 100 kHz as a function of strip width for DC-coupled strips without Layer 0 after electron irradiation, unbiased.

13. Interstrip capacitance at 100 kHz as a function of bias voltage for DC-coupled strips without Layer 0 after electron irradiation.

14. Interstrip capacitance at 100 V, 1 MHz as a function of photon dose for DC-coupled and AC-coupled strips with Layer 0, biased during irradiation.

15. Interstrip capacitance at 100 V, 1 MHz as a function of strip width for DC-coupled strips without Layer 0 after photon irradiation, unbiased during irradiation.

16. Interstrip capacitance at 100 V, 1 MHz as a function of strip width for DC-coupled strips with Layer 0 after photon irradiation, biased during irradiation.

17. Interstrip capacitance at 100 V, 100 kHz as a function of strip width for DC-coupled strips without Layer 0 after 6 MeV proton irradiation, unbiased during irradiation.

18. Total strip capacitance after neutron-irradiation (non-RD20 DC-coupled devices).

19. Time dependence of interstrip capacitance after electron irradiation for DC-coupled strips with Layer 0, unbiased during irradiation.

20. Time dependence of interstrip capacitance after photon irradiation for DC-coupled strips with Layer 0, biased during irradiation.

21. Oxide charge as a function of electron dose for MOS and MNOS capacitors, unbiased during irradiation.

22. Oxide charge annealing for MOS and MNOS capacitors after electron irradiation, unbiased.

23. Effect of bias on oxide charge levels and annealing for MOS and MNOS capacitors after 150 krad photon irradiation.

Polysilicon
resistors

Probe
pads

Bond
pads

Bias Line

Guard

b) AC-coupled strips

Guard
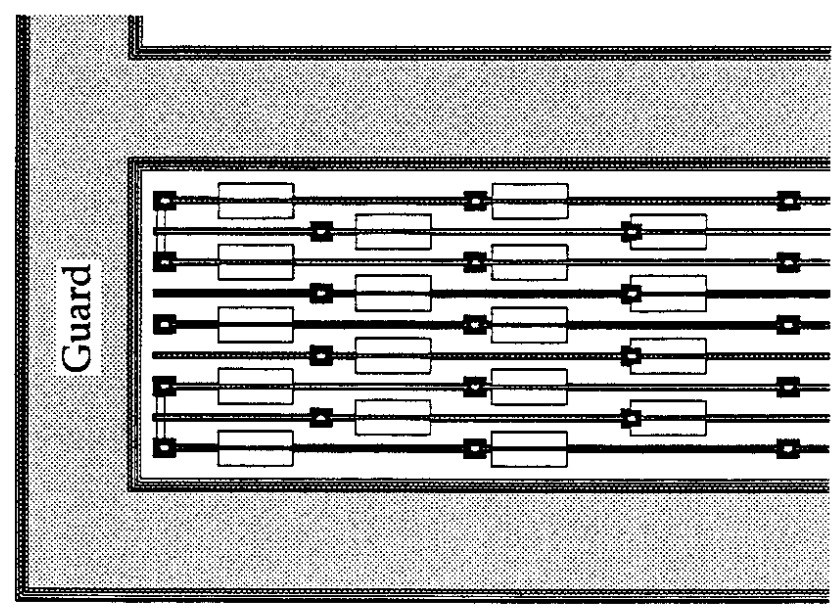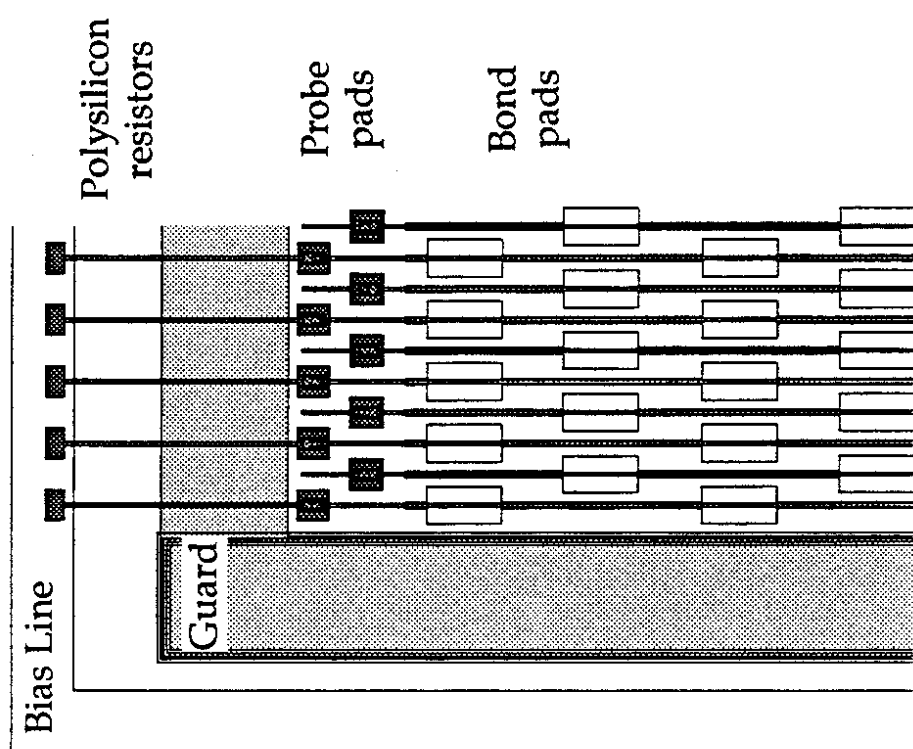
a) DC-coupled strips
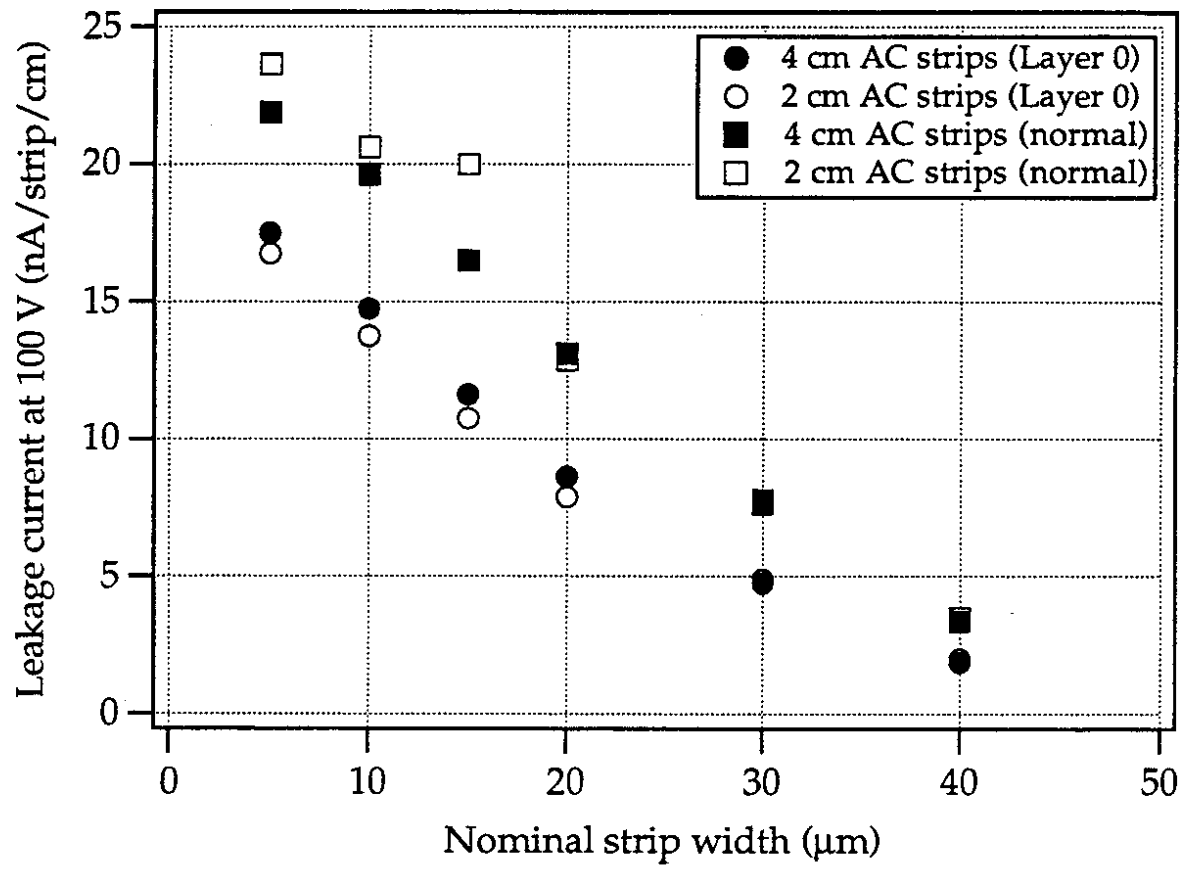
Figure 1

Figure 2
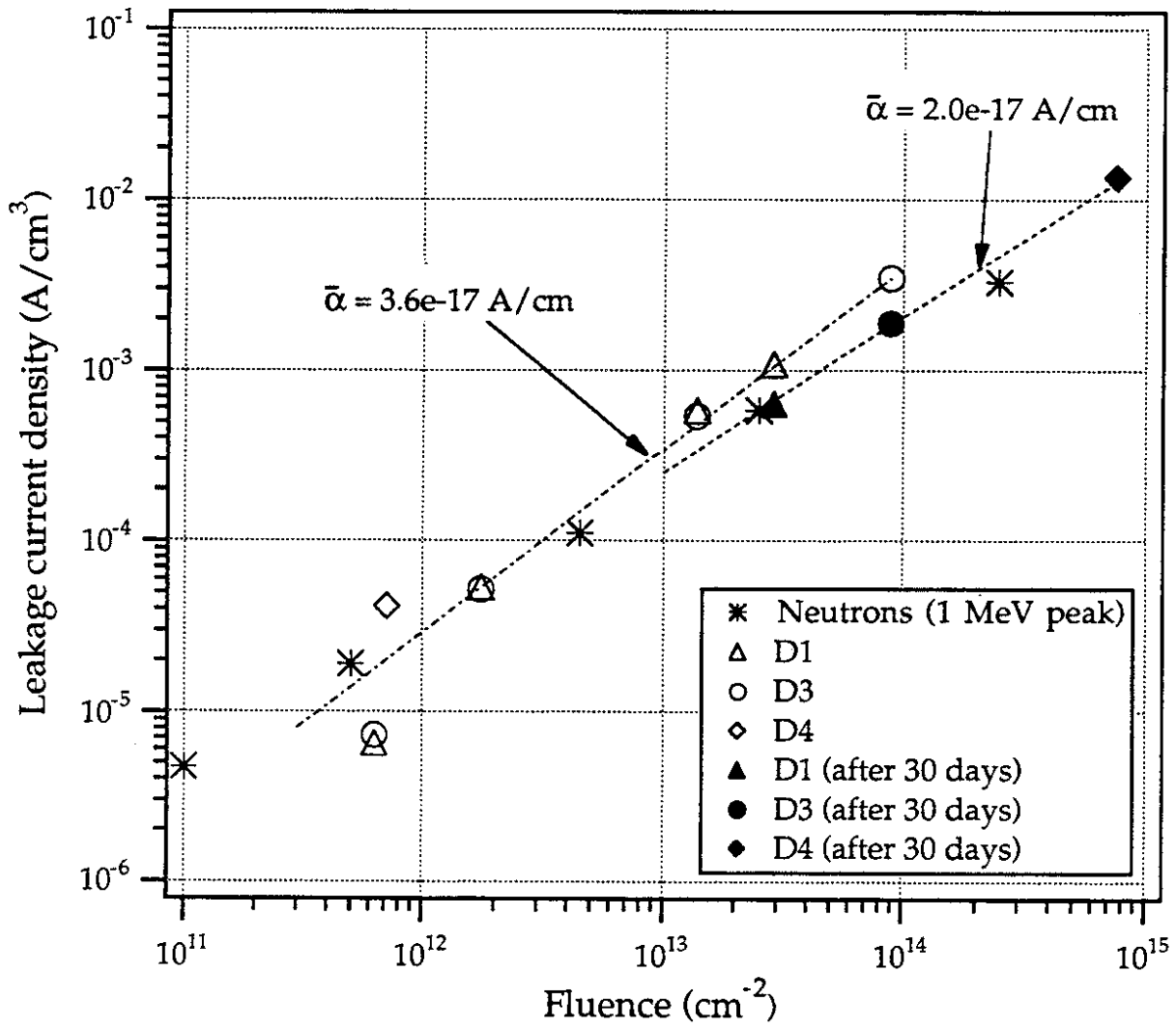
Figure 3
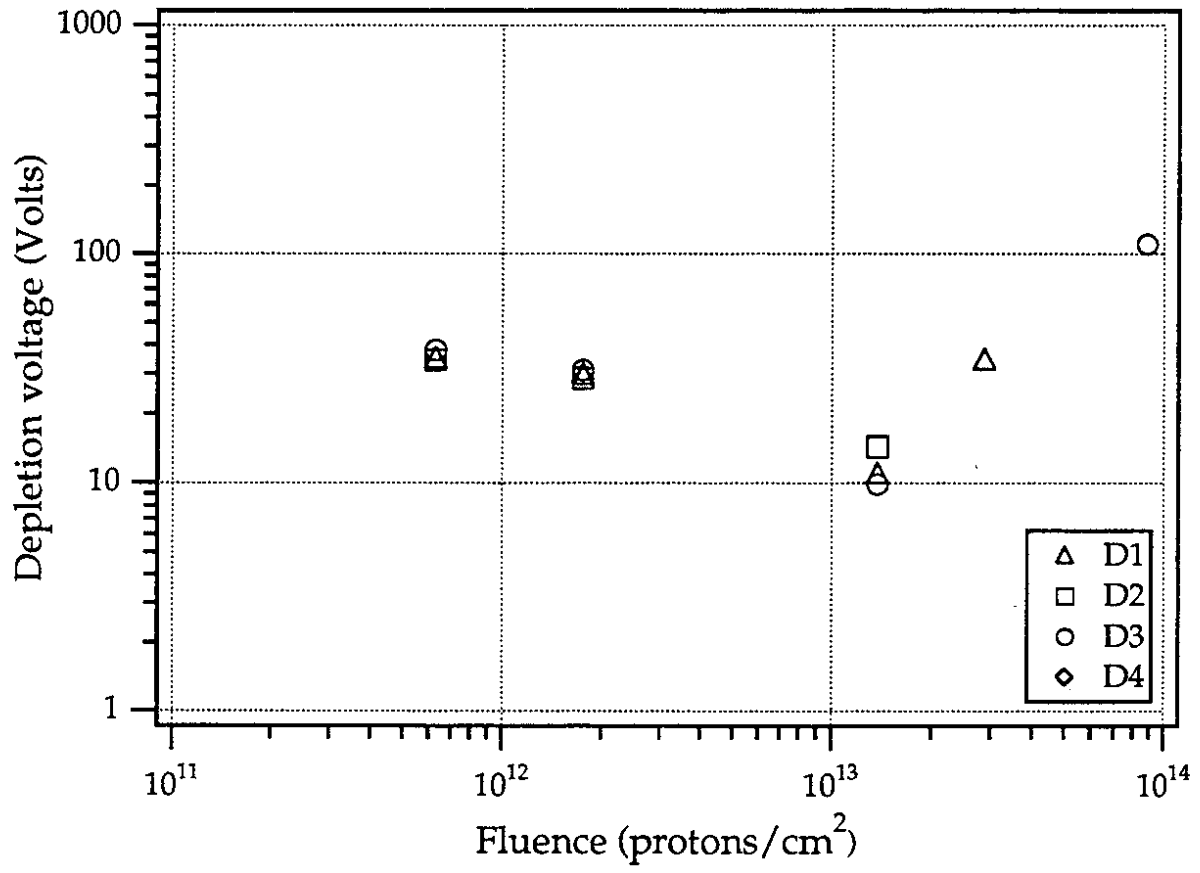
Figure 4
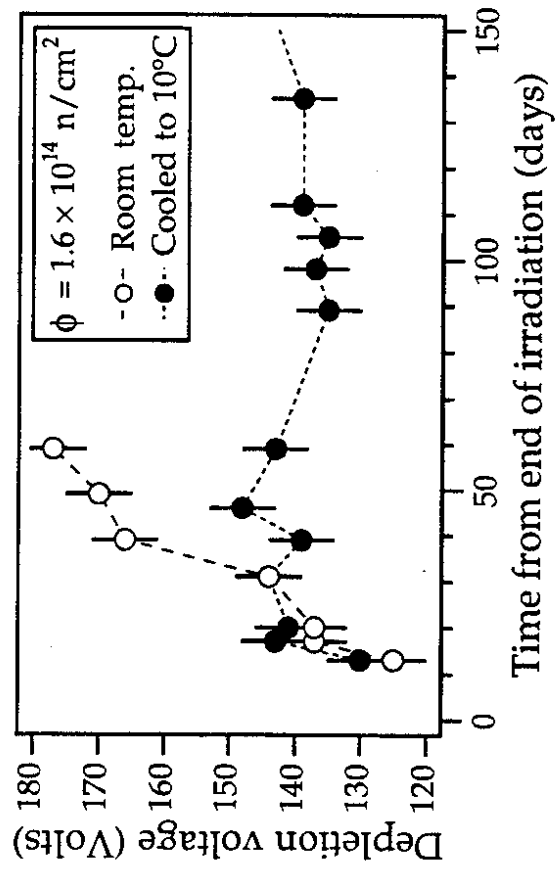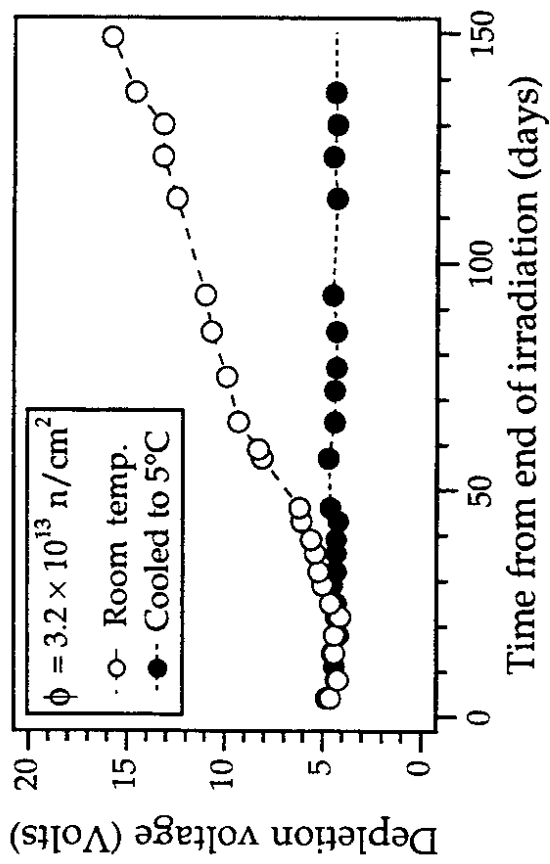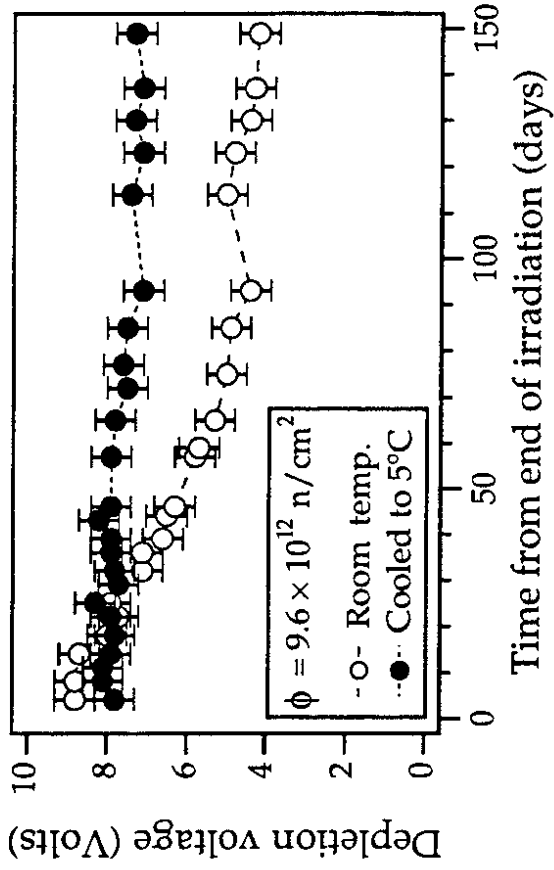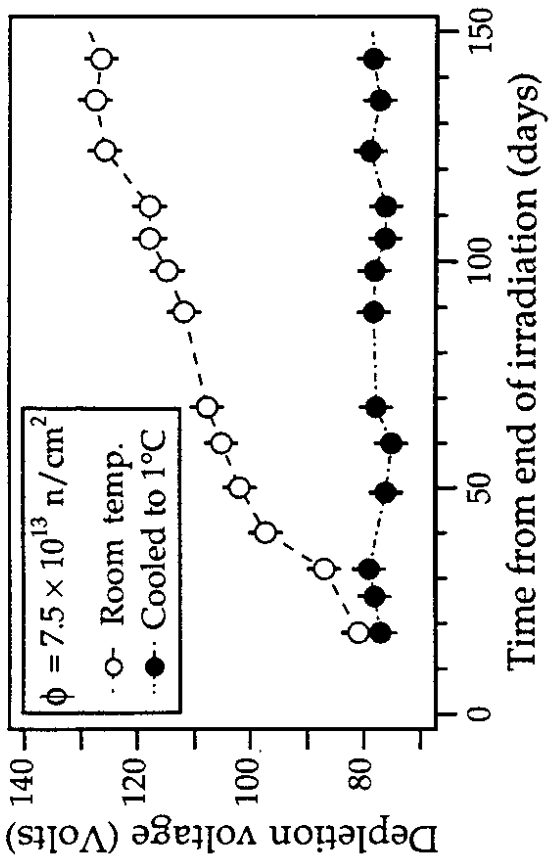
Figure 5
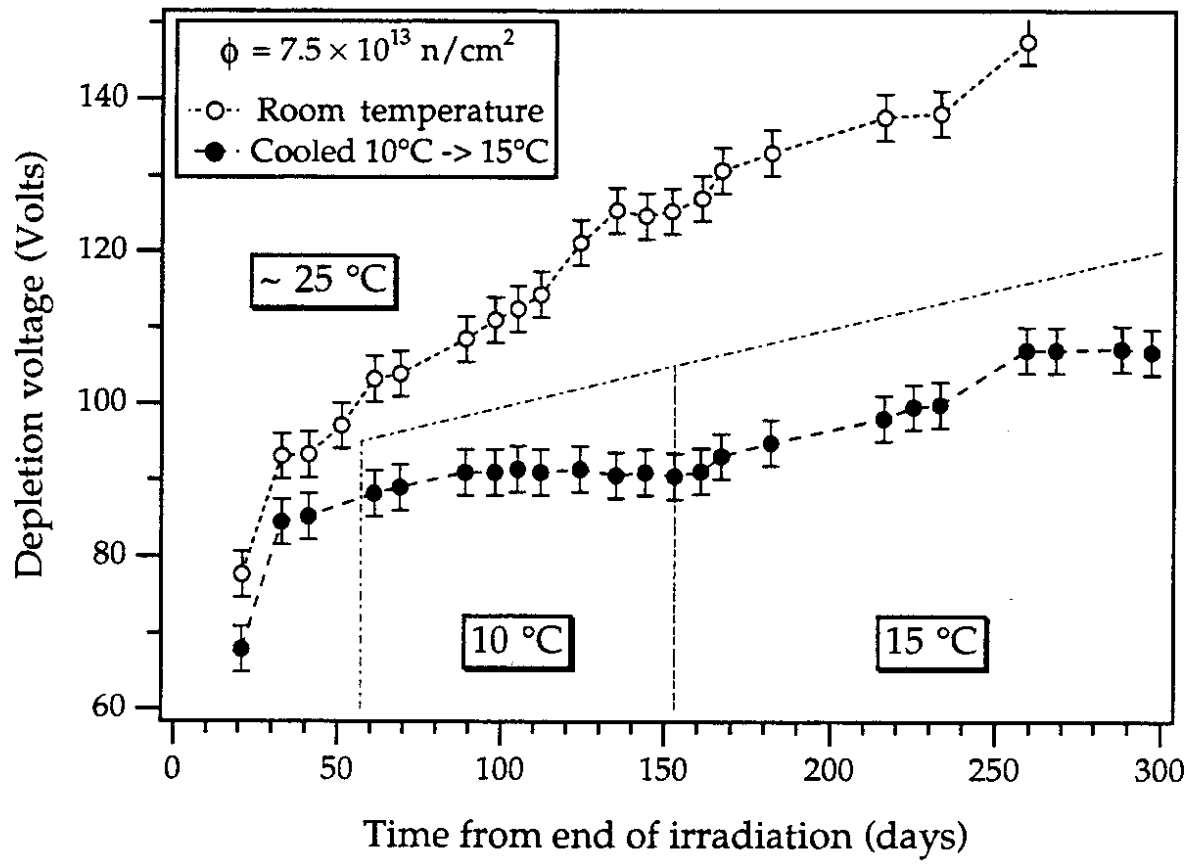
Figure 6
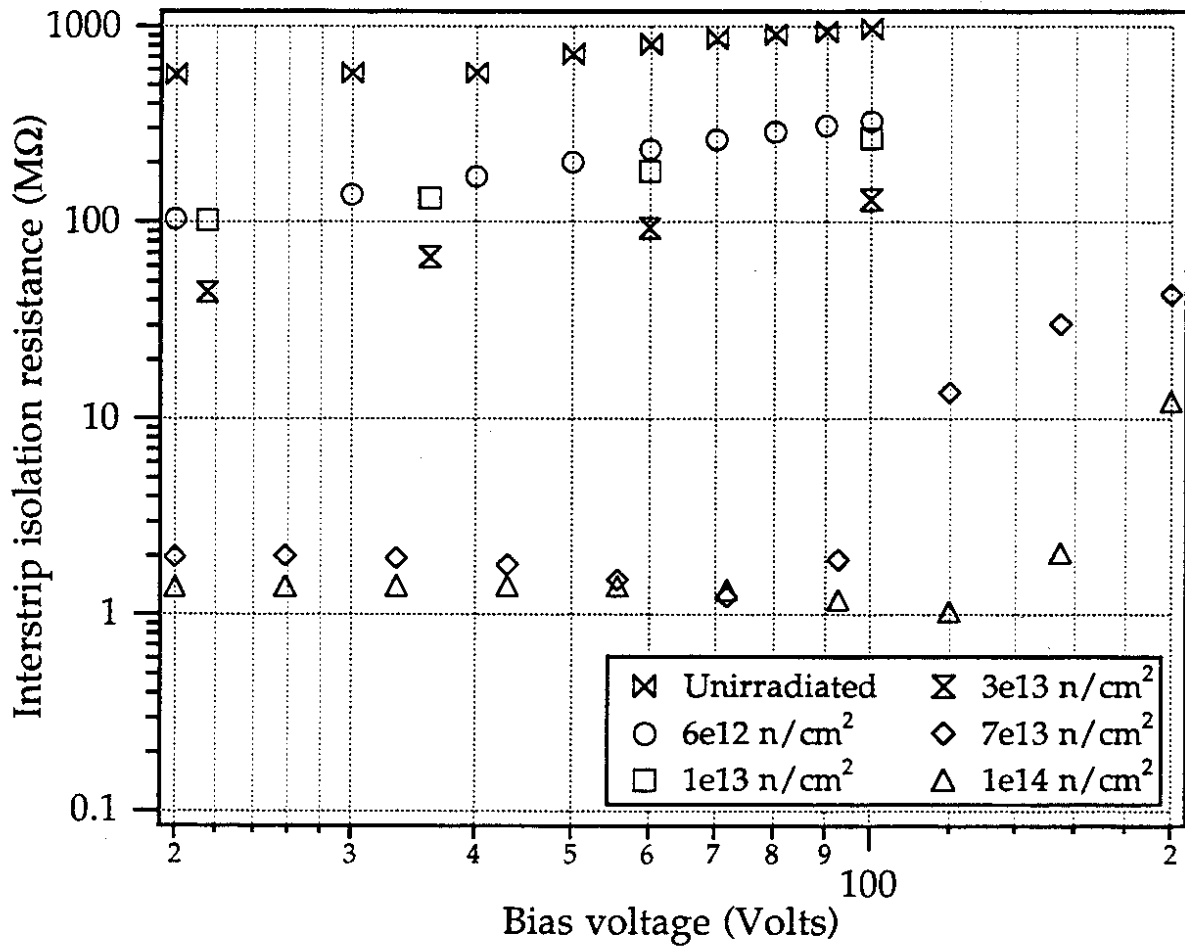
Figure 7
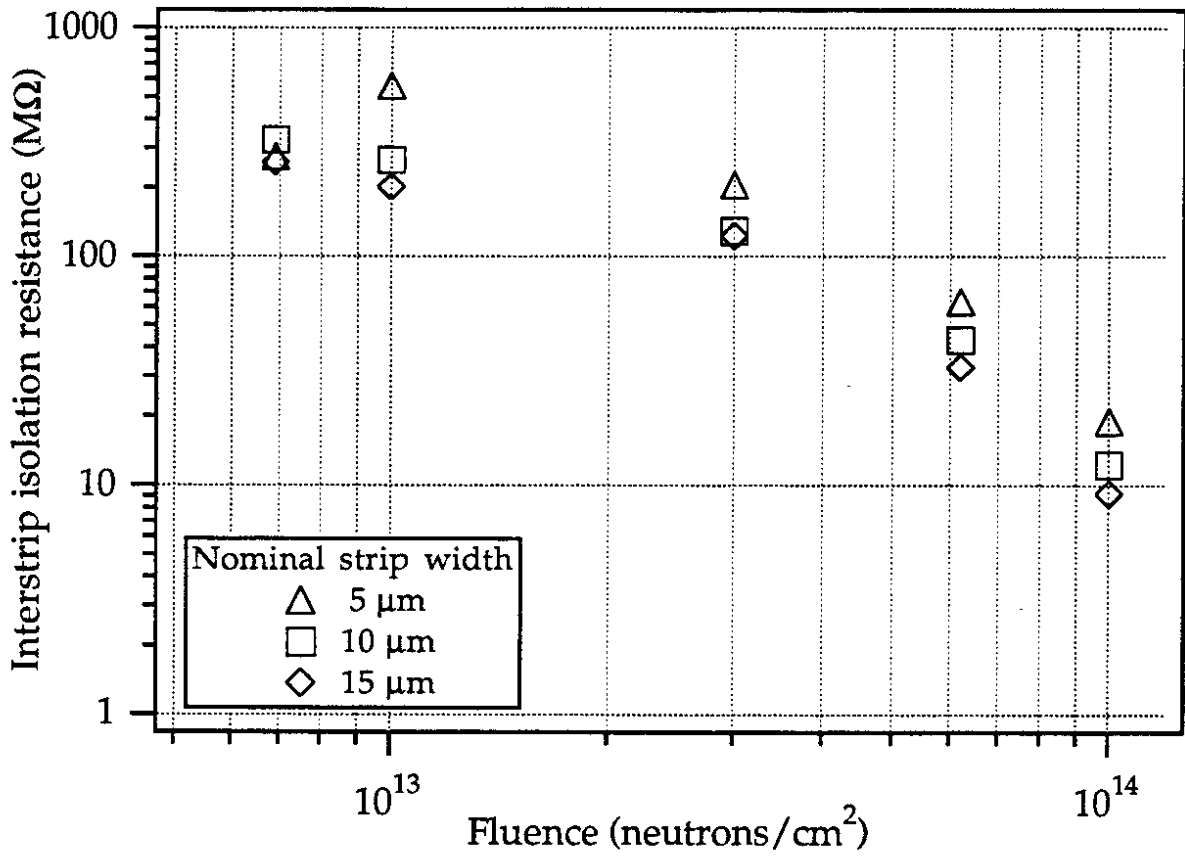
Figure 8
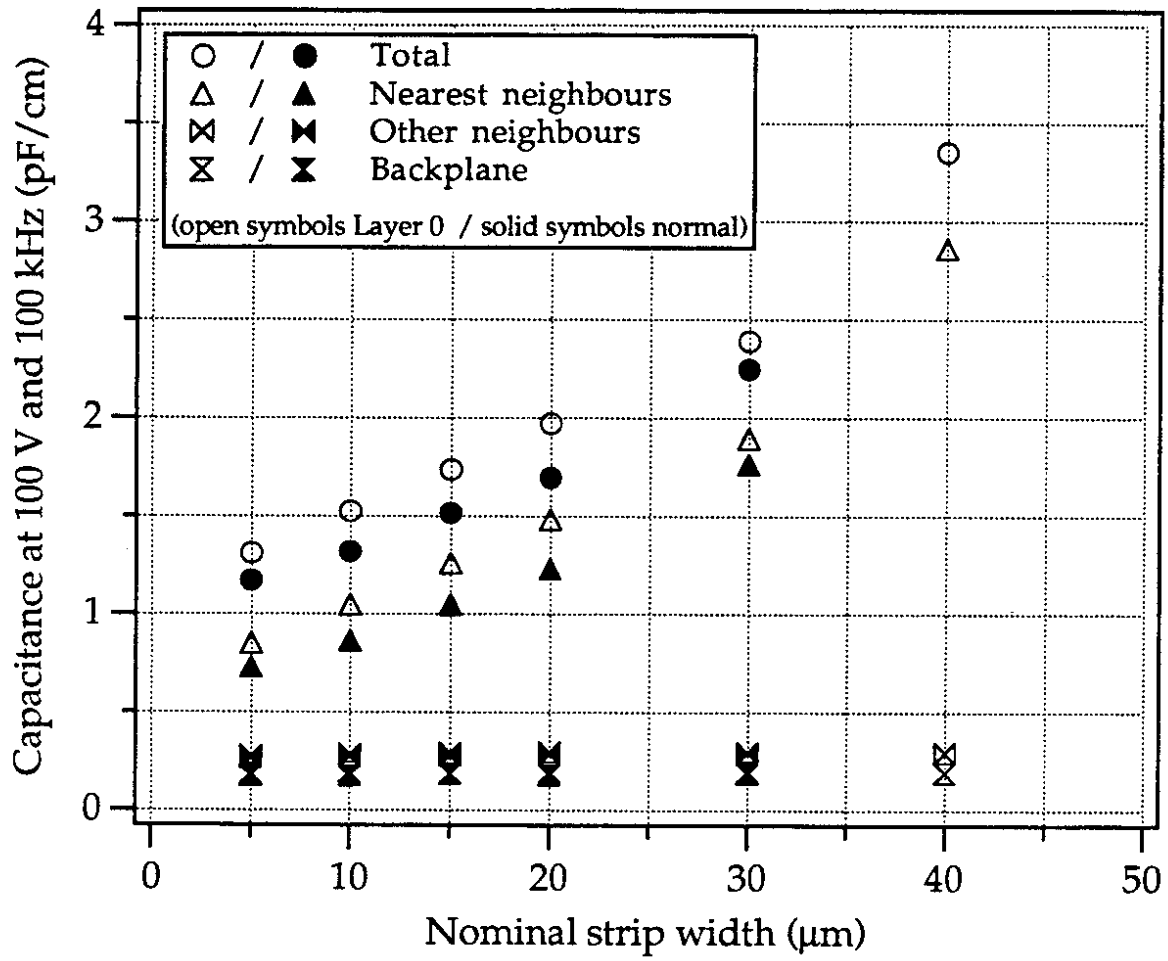
Figure 9
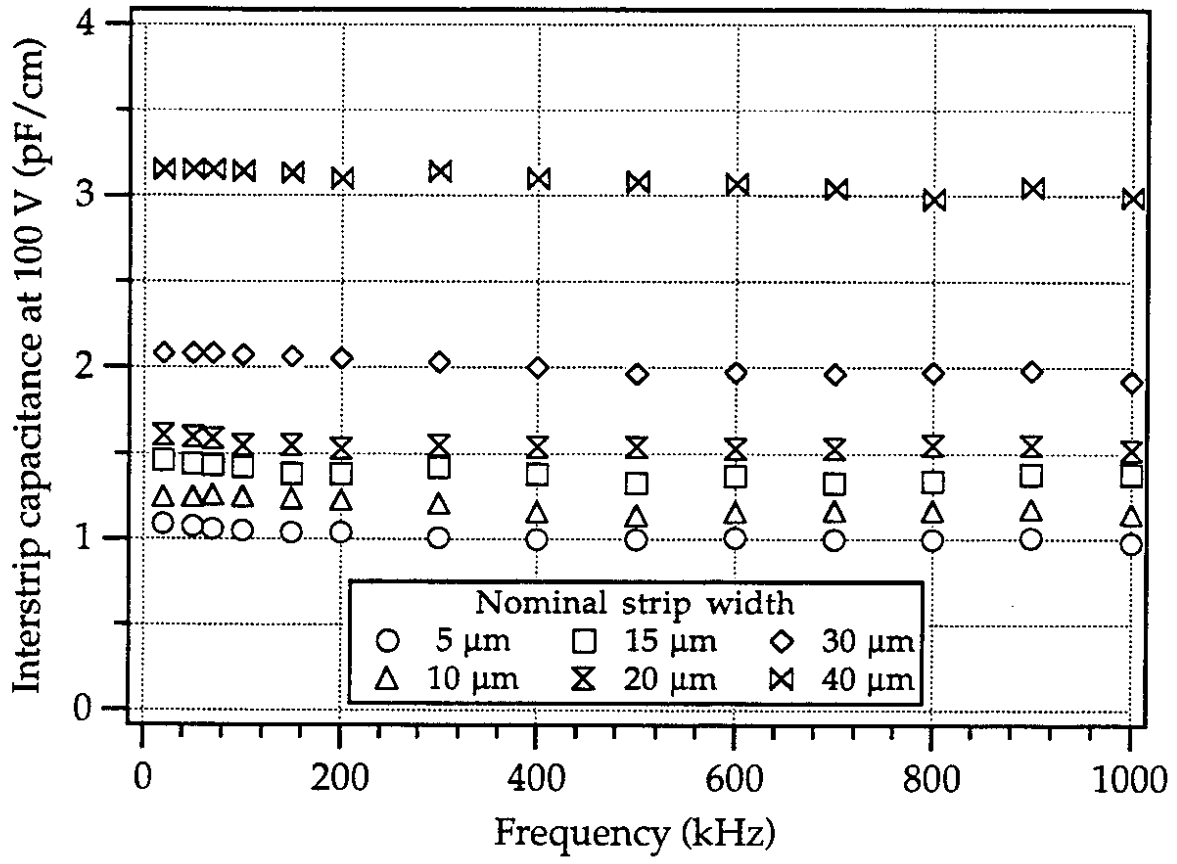
Figure 10

Figure 11

Figure 12

100 kHz

△ 5 μm DC strip, unirradiated
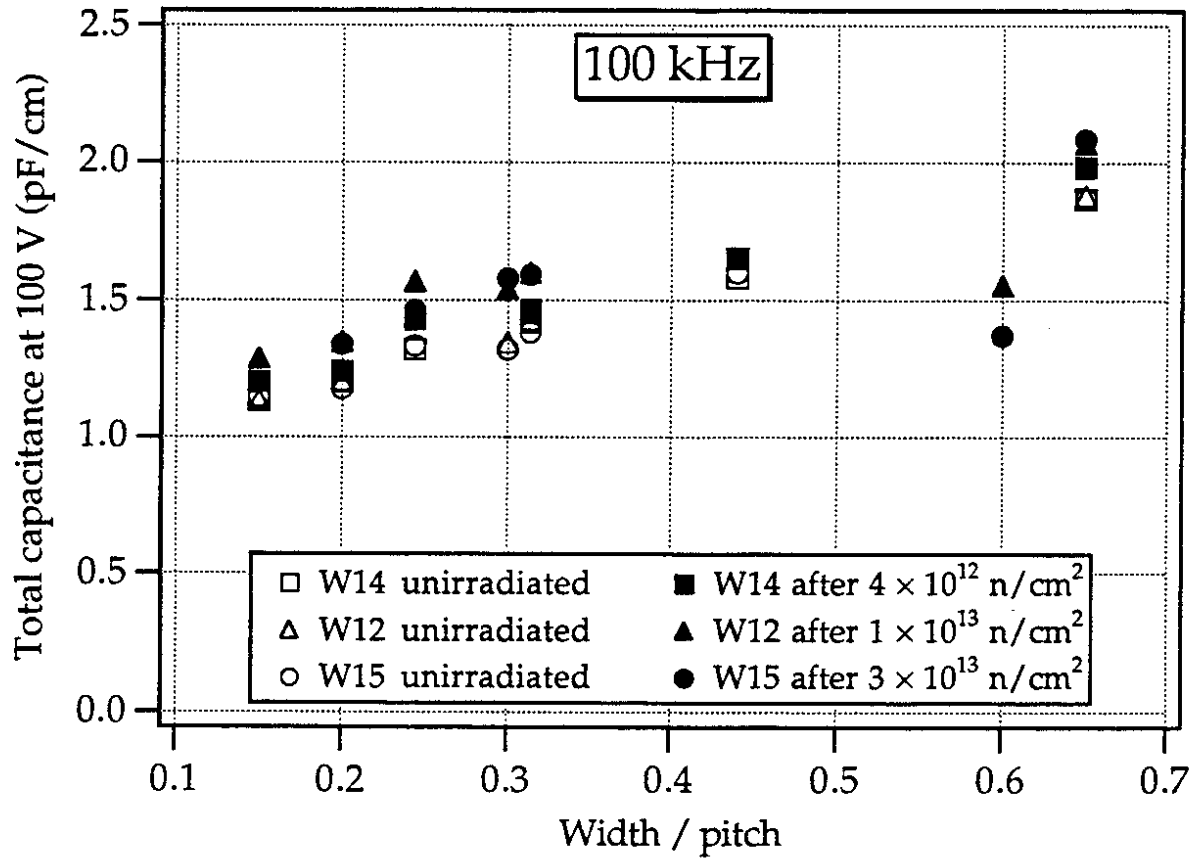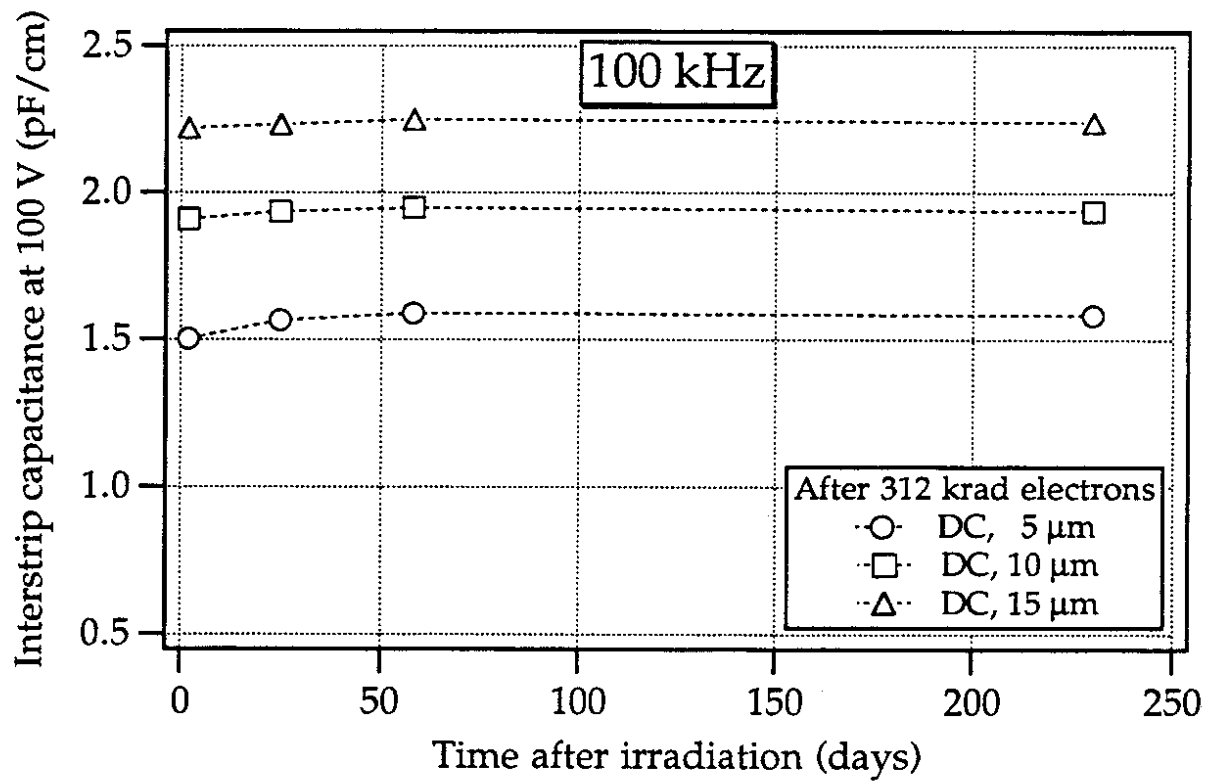▲ 5 μm DC strip, after 2 Mrad electrons
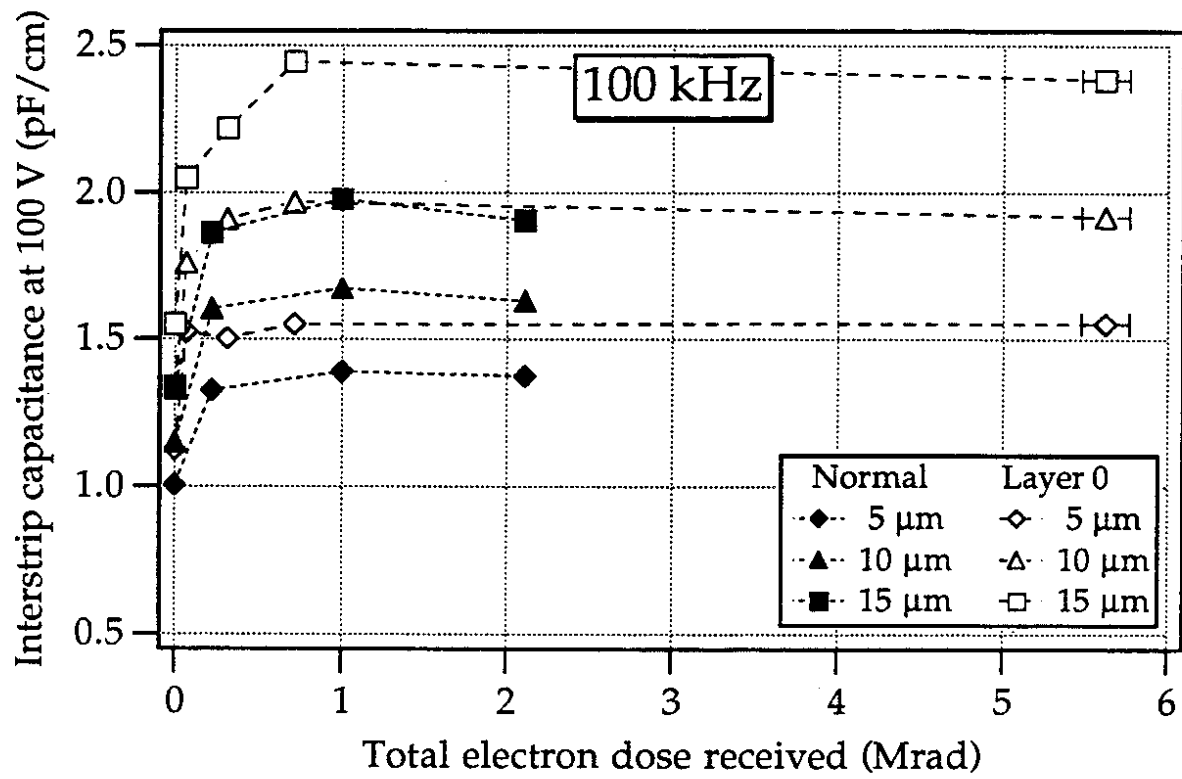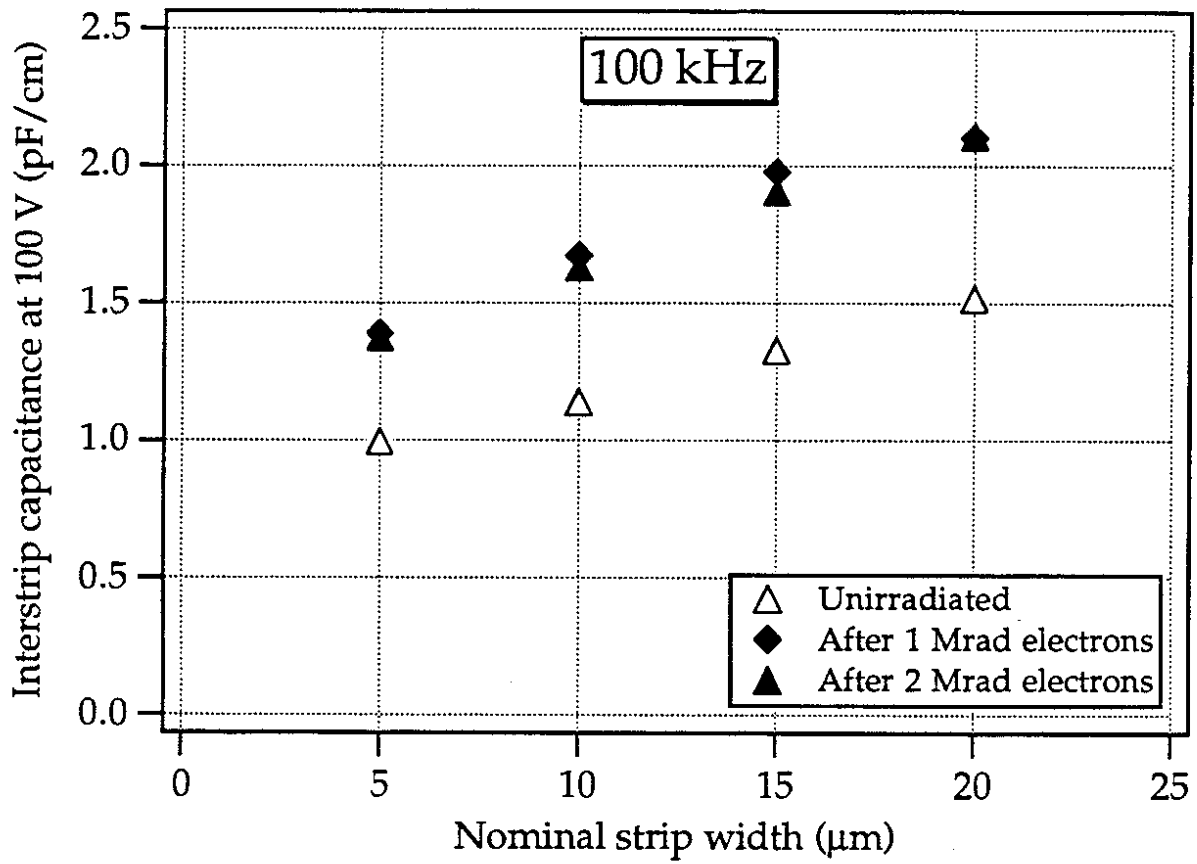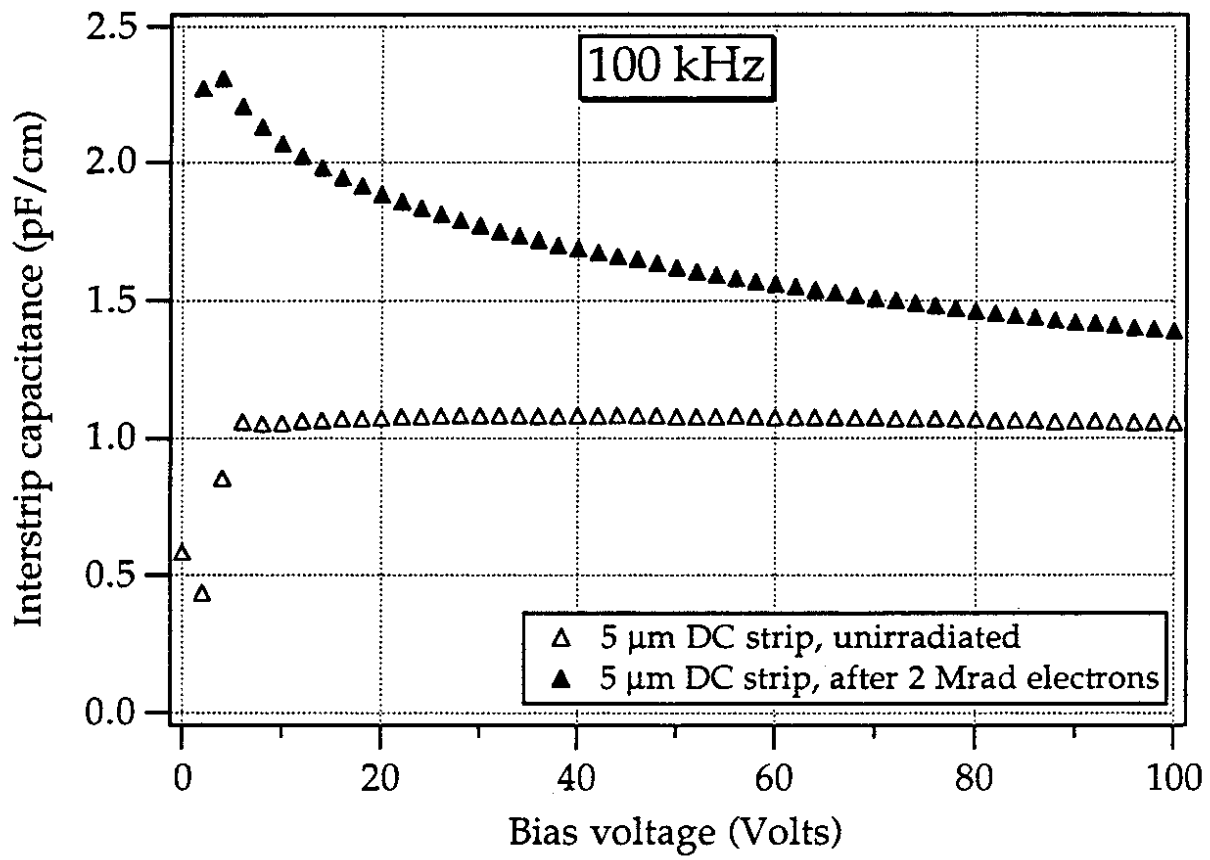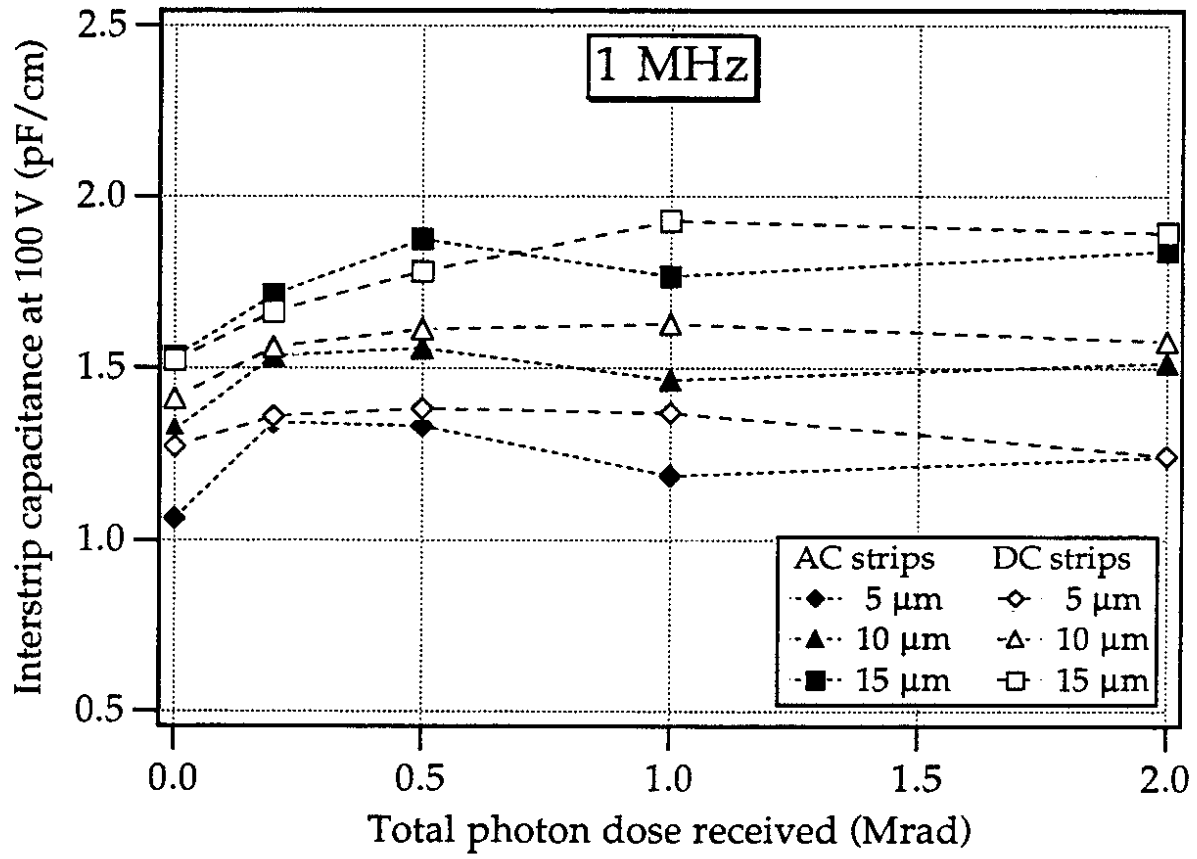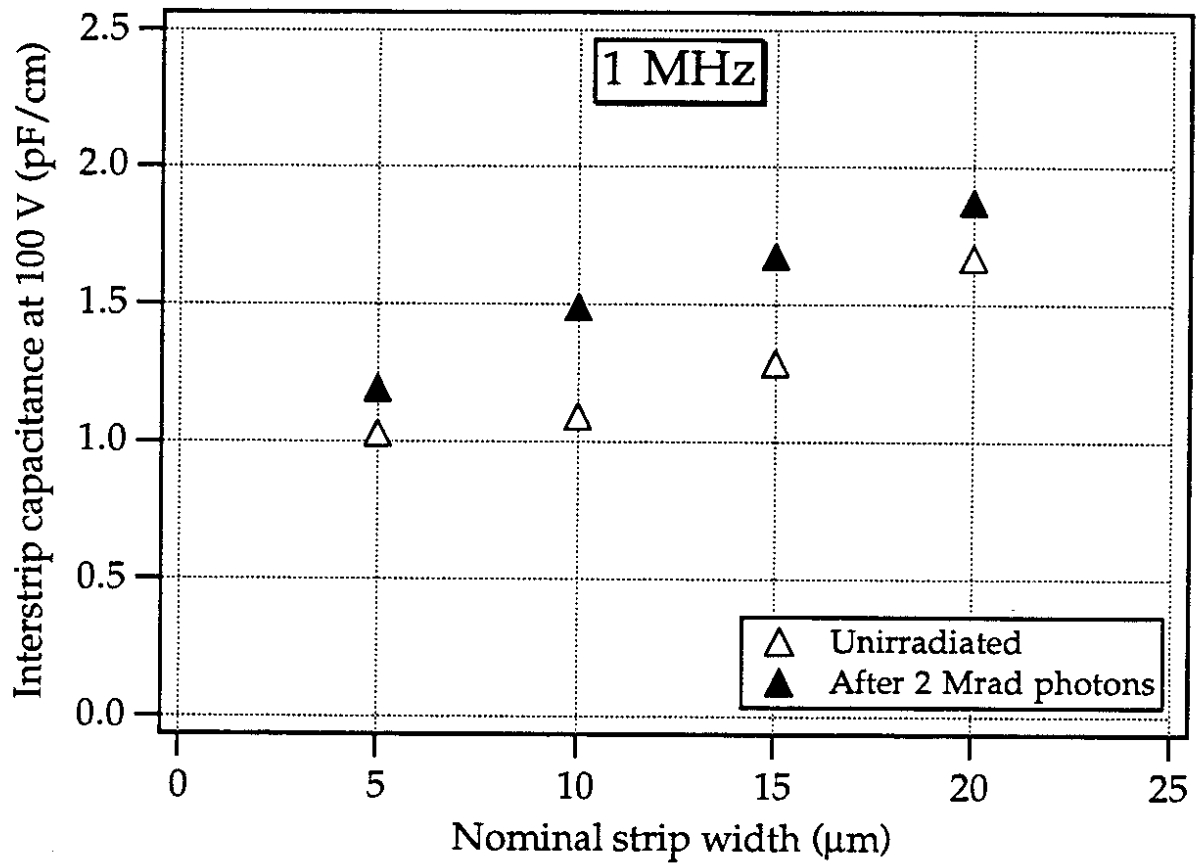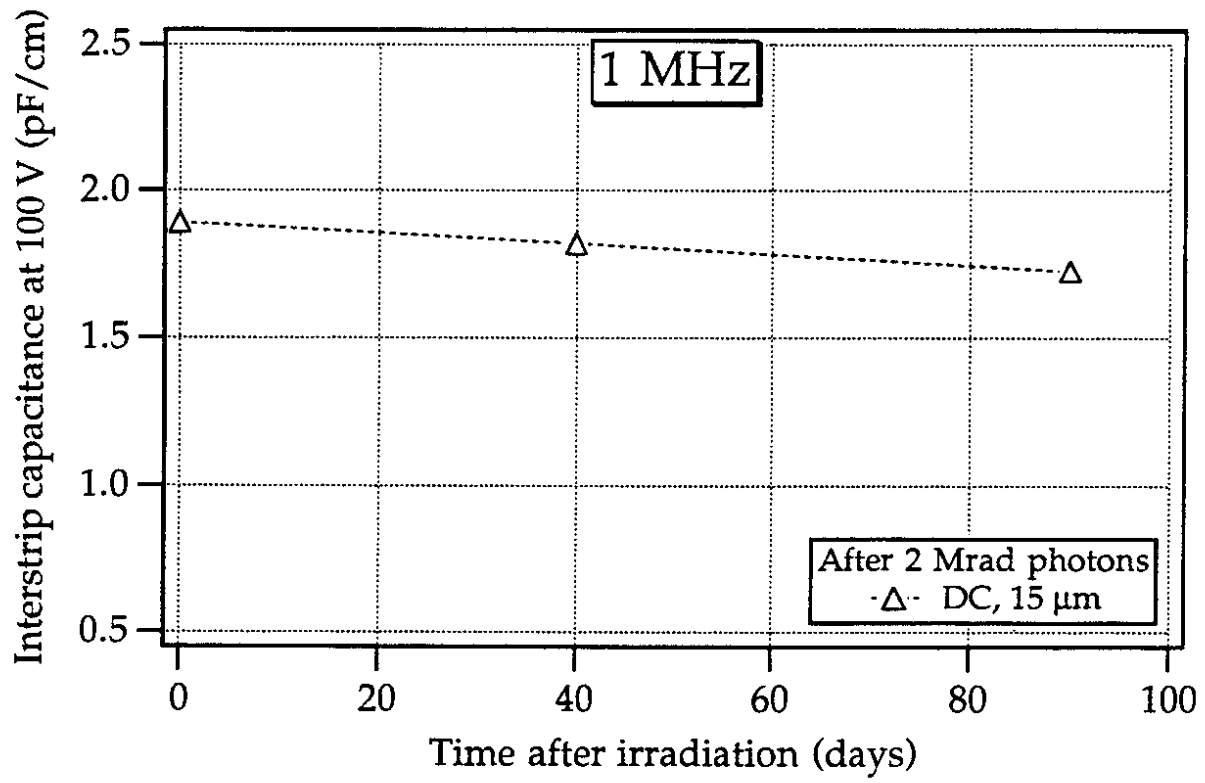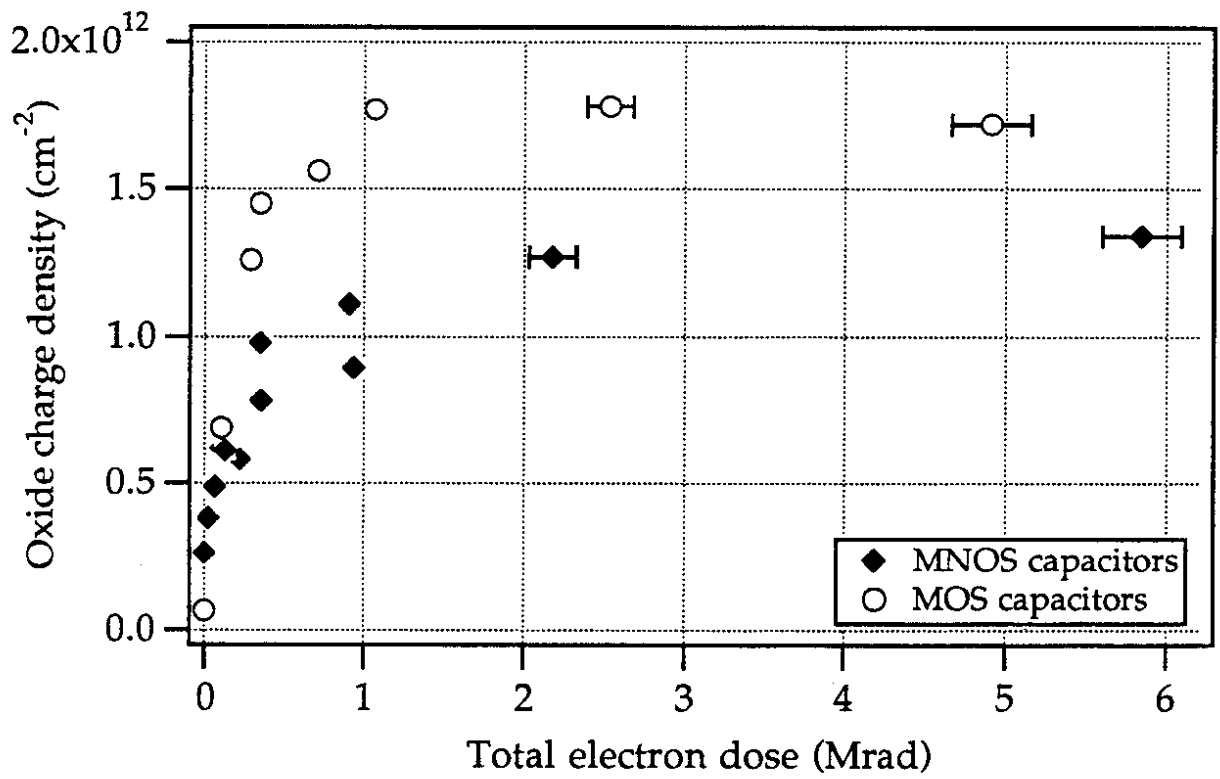
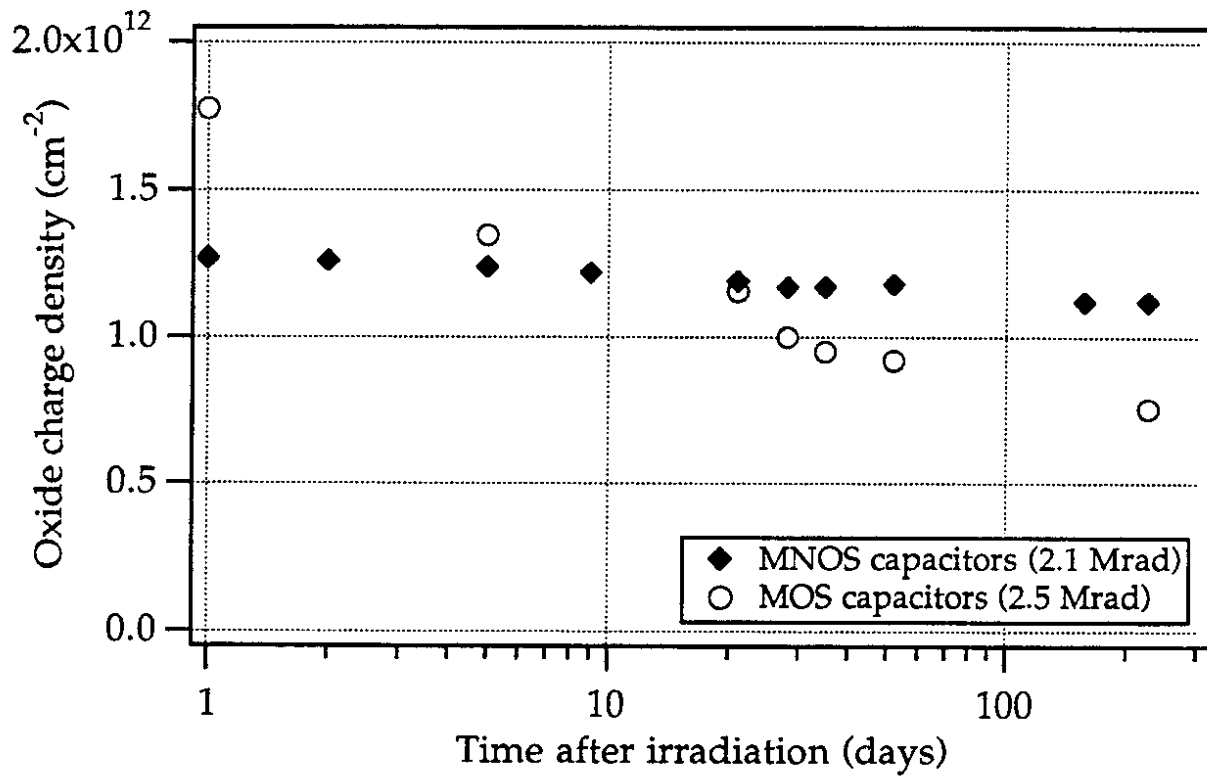Figure 13

Figure 14
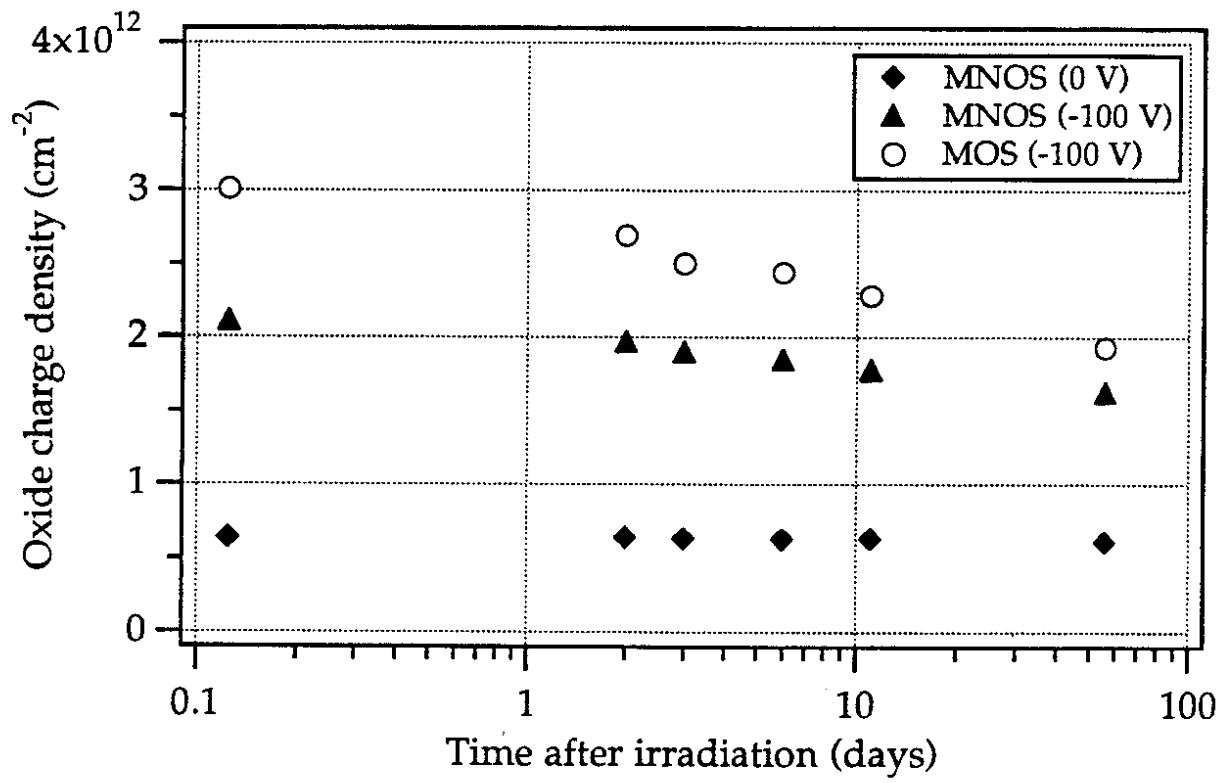
Figure 15
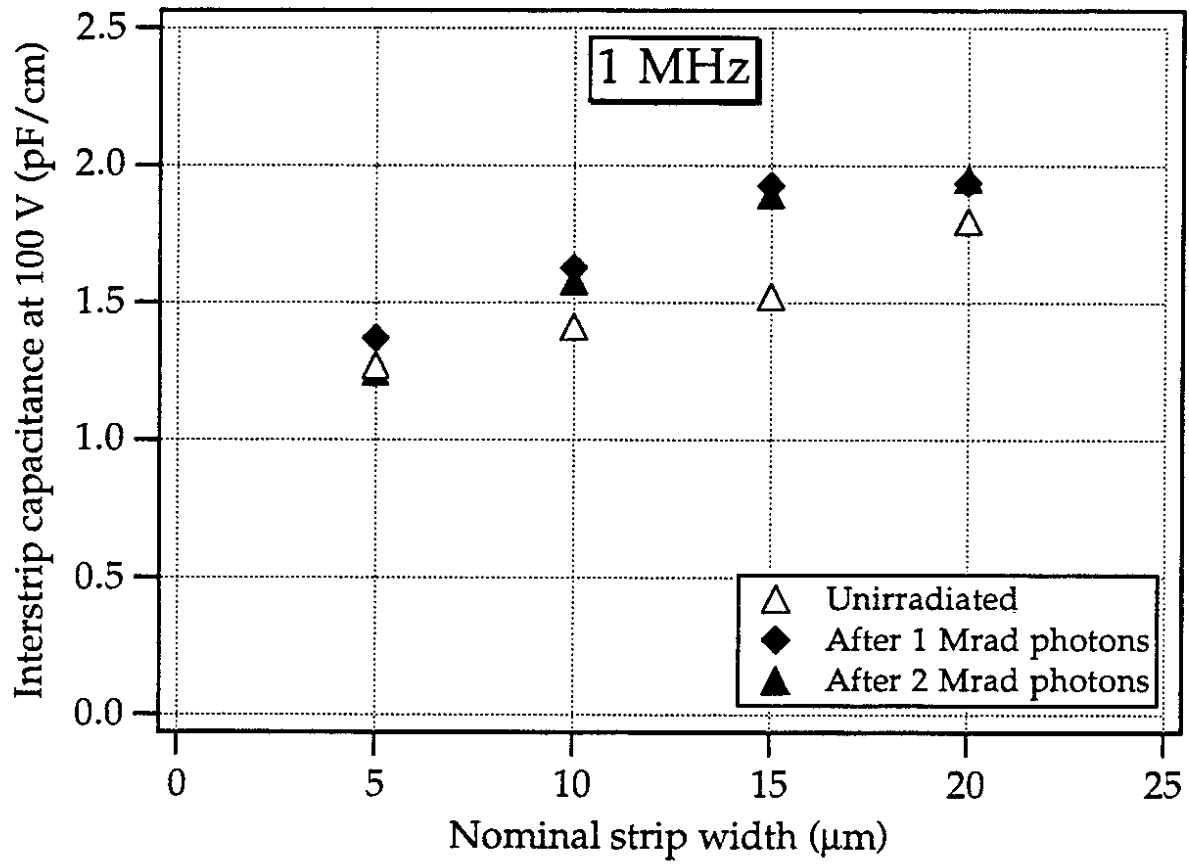
Figure 16
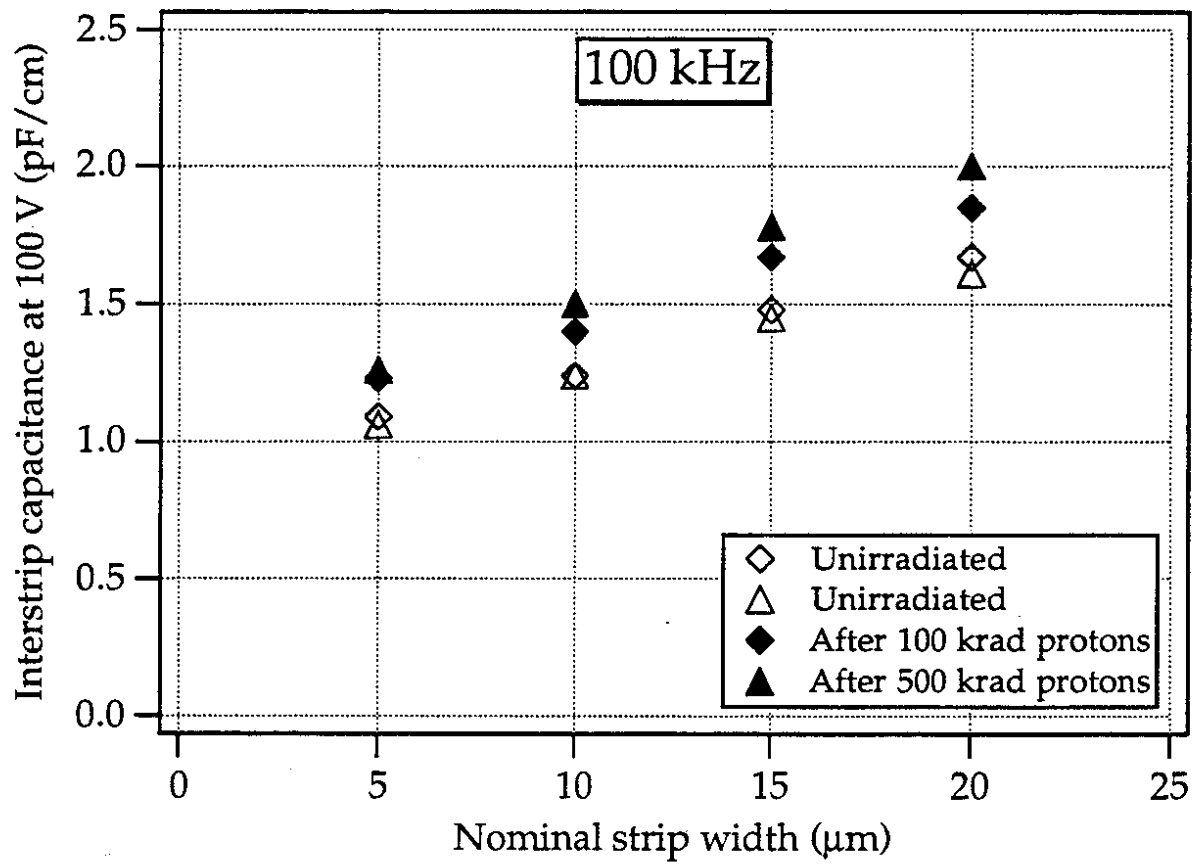
Figure 17

Figure 18

Figure 19

Figure 20

Figure 21

Figure 22

Figure 23