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IMAGING WITH 2D AND 3D INTEGRATED SEMICONDUCTOR DETECTORS USING VLSI TECHNOLOGY

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ABSTRACT

Sophisticated semiconductor imaging devices are being developed in elementary particle physics in view of future high-intensity collider experiments. These devices use contiguous silicon sensor elements with dimensions ~ 100 μm. They are capable of detecting charge signals generated by ionizing particles or photons in the low-keV range. The equivalent noise charge can be lower than 100 e^- r.m.s. (0.9 keV FWHM) even at room temperature and at 10 MHz rate. Such devices may constitute powerful radiation imagers in medical or biological applications and they would allow single X-photon counting, thus extending the dynamic range, improving the contrast and lowering the radiation dose required.

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1. INTRODUCTION

Most of the pioneering work on detectors for ionizing radiation has been done in nuclear physics research, but in the last decennia elementary particle physics has progressively become the stimulating factor in the development of detection techniques. Whereas it is hard to find practical applications for an exotic but very successful device such as the cryogenic bubble chamber, other detectors like the multiwire proportional chamber or the silicon microstrip detector have been already adopted in a variety of instruments, e.g. in medical equipment or for materials analysis. These new types of detectors are based on earlier established principles but they provide a basic improvement compared to their predecessors in that they allow simultaneous localization of a large number of incident particles or photons over a large area and/or with micrometer precision.

The typical approach for particle physics experiments is the use of a large number of parallel signal processing channels. In this way the detector system becomes an intimate mixture of the physical sensors and the readout electronics. Trade-offs can be made, e.g. the signal gain can be in the sensor or in the amplifier, the signal/noise ratio can be varied by more or less segmentation of the electrodes, etc. The development of very large scale integration (VLSI) microelectronics technology has a direct impact on the detector electronics but it can also determine new approaches to the sensor elements themselves as will be discussed in sect. 2.

Section 3 contains a brief overview of the recent semiconductor "pixel detectors", which are under development in Europe and the USA, in view of the future high-intensity hadron collider experiments. These pixel detectors aim at signal processing functions integrated in each of the pixels on the detector chips. They are in this respect distinct from earlier imagers such as semiconductor diode arrays or charge-coupled device (CCD) detectors which contain generally one single amplifier through which all the charge packets are transmitted off-chip for further processing. A further difference between "planar" CCD and the new "pixel detectors" is the use of the third dimension by stacking the processing electronics directly on top of the sensor elements.

A further stage in detector integration would be reached by including not only the signal processing but also part of the information processing functions onto the detector chip itself. Such a detector can be called: "micropattern detector" supposing that the useful information consists of some kind of pattern. An obvious case is the recognition of written characters. In a more modest approach one might transmit the addresses of pixels along a boundary of contrast, etc. A few developments in this direction are mentioned in sect. 4. For such "smart sensors" it becomes necessary to use several stacked layers with electronics. Three-dimensional electronics requires comprehensive technology development, in particular if the devices must be monolithic, i.e. consisting of a single silicon chip. If the device is made up of different chips for processing and sensor functions one speaks of a "hybrid device". In sect. 5 a short comparison is made between common features in particle physics applications and possible needs in medicine or biology.

2. IMPACT OF MICROELECTRONICS ON RADIATION DETECTION

It may often be difficult to achieve the best optimization between sensor elements and readout electronics. The detector designer and the system user may lack direct and early access to electronics specialists and the electronics designer may not be sufficiently involved in the exact definition of the system requirements. The introduction of microelectronics circuits in association with semiconductor detectors increases the flexibility in the system and the possibilities for trade-offs and optimization but also imposes an enhanced interaction between detector and electronics designers. Microelectronics technology is changing conceptions of detector readout and it is also changing the detector construction itself by allowing very precise segmentation and a large number of segments [1].

The application of VLSI technology in computers has increased the possibilities of information processing and it allows extraction of useful features from large amounts of data. This has enabled the construction and operation of ever larger detector systems in particle physics experiments, with over 100 000 detector readout channels. VLSI technology can also be used for detector readout electronics. Several circuits have recently been developed with 16 [2], 64 [3–4] or 128 [5–7] readout amplifiers on one chip. Size, cost and power consumption are orders of magnitude lower compared with earlier, discrete detector amplifiers. This allows in its turn another increase in the number of sensor elements in a detector system. The number of external readout channels may be reduced by data multiplexing and by on-chip zero suppression and encoding of the data addresses. This is a first step towards information extraction on-chip.

The construction of semiconductor detectors, in particular silicon detectors, is since 1980 dominated by planar VLSI technology. Kemmer [8] in that year showed that the state-of-the-art of silicon processing and lithography allowed manufacturing of silicon diode detectors with a diode reverse current below 10 nA cm^{-2} accompanied with low noise (~ 2 keV FWHM) at room temperature. Attempts in the early 70's to use oxidation and ion-implantation were generally unsuccessful, probably because of insufficient cleanliness and lack of understanding of the MOS (metal-oxide-semiconductor) structure.

Also in 1980 a renewed interest came up for segmented diode detectors [9–11] and the simultaneous introduction of compact and cheap readout electronics [10, 12] made these detectors this time more acceptable than at their first introduction [13–14]. The subsequent application of planar processing to the microstrip geometry [15] allowed the manufacturing of reliable, low-noise detectors with well-defined position detection. Several companies started commercial fabrication of planar silicon microstrip detectors and the performance has been improved steadily over the last years. Typical reverse diode current is at present often below 1 nA cm^{-2} and detectors with area of 25 cm^2 are manufactured with high yield. Arbitrary segmentation of the detecting sensor elements is, in principle, possible with lithography, but the problem of making contacts and providing readout electronics limited applications to linear microstrip arrays or coarse pad geometries. A finely segmented geometry, as shown in fig. 1, needs yet another step in electronic readout development: signal processing incorporated in each pixel.

3. SEMICONDUCTOR DETECTORS INCORPORATING SIGNAL PROCESSING

The first example of a true two-dimensional (2D) semiconductor detector used in particle physics is the charge-coupled device. The CCD is a matrix of MOS capacitors and each capacitor (picture element or "pixel") integrates all charge generated in the underlying thin depleted silicon layer (~ 10–20 μm) by ionizing particles or other incident radiation. After the integration period the charge packets are successively shifted (coupled) from capacitor to capacitor, like in a pipeline, into another, perpendicular pipeline, and finally into the output node. The CCD is a matrix of passively integrating sensor elements and only the output node performs a signal processing function on-chip. The thin layer of silicon provides sufficient signal charge for single minimum ionizing particles to be detected, due to the very low capacitance of the small CCD capacitor elements. In 1982 Damerell c.s. showed that with some precautions even at a rate of 10^5 s^{-1} incident particles CCDs can be used in a fixed-target experiment [16]. More recently, this group has built a 120 million pixel detector consisting of 400 CCDs for the inner region of the Stanford Linear Collider (SLD) experiment [17], where the rate of interactions between the colliding beams of electrons (events) is only a few per second.

In future high rate, high intensity experiments with 10^8 s^{-1} interactions, active signal processing circuits should be connected to each sensor element and on-chip data storage and timing information must be provided. The readout electronics can be incorporated in the detectors in several ways. Figures 2(a) and 2(b) illustrate monolithic solutions, whereas fig. 2(c) shows the hybrid approach. Advantages of a hybrid device with "flip-chip" readout are flexibility in the choice of silicon technology for the readout circuit, standard manufacturing for both detectors and electronics, and the possibility to use with the same readout chip various types of semiconductor detectors, like GaAs, CdTe, etc.

3.1 Monolithic pixel detectors

For particle detection a relatively thick depleted silicon layer may be necessary, e.g. 200 μm, if the sensor elements are not as small as in a CCD and then the detector has to be built using high-resistivity silicon. In different laboratories various elegant monolithic solutions are under investigation aiming at incorporation of active readout circuits in the high-resistivity silicon. This approach will allow thin detector assemblies and they may be eventually cheaper in the construction phase.

G. Vanstraelen [18] at IMEC has developed a processing technology that allows readout circuits to be situated in a p-well besides the sensor elements. A similar technology is develo ped by S. Holland [19] at Lawrence Berkeley Laboratory. In order to make transistors directly on top of the sensor Parker and Snoeys [20] at CIS-Stanford designed a technology which includes a patterned ion-implantation for segmented diodes at the backside of the wafer. At Max Planck Institute in Munich the group of G. Lutz is working with J. Kemmer on a new kind of charge-sensitive devices with non-destructive readout [21] which eventually can be arranged in arrays. In a different approach, in a collaboration between the CERN R&D Collaboration RD-19 and IMEC, readout circuits are made in a thin silicon-on-insulator (SOI) layer on top of high-resistivity wafers as shown in fig. 2(b) [22].

Until 1992 only the new monolithic devices produced by Parker and Snoeys have been actually tested in a high-energy particle beam [23]. These detectors consist of a matrix of 10 × 30 cells, each with an area of 125 μm × 34 μm. The noise on the analog output signals was ~ 400 e^- r.m.s. and the precision of the position measurement of particles crossing through a telescope of four imager planes was determined at 2.2 μm. In 2665 events in the fiducial region no inefficiency was observed.

The development of a dedicated manufacturing technology, as needed for monolithic sensors, is often tedious but there are interesting rewards if silicon is the appropriate detector material. Monolithic devices can be easily mounted in vacuum which is often not true for hybrids which use low vapour pressure metal bumps. Because of the low conversion efficiency of Si monolithic all-silicon devices may be less attractive, however, for X-ray detection above 20 keV.

3.2 Hybrid pixel detectors

Hybrid detectors are the choice for infra-red (IR) light detection and "focal plane" technology is very sophisticated. Various interconnect schemes using indium bumps, solder bumps or gold bumps have been developed and can be used for other applications as well. In IR imaging one is usually not concerned with uncorrelated event images at high speed. Integrating detectors with long integration times can be used and there is no need for pulse processing. In fact, one of the early publications on the possibilities of pixel detectors in particle physics described the use of an IR-imager for detection of α particles [24].

The first pixel detector with incorporated active signal processing having been operated in a particle physics experiment is the device called "D-Omega-Ion" [25] for which a few cells of the readout chip are shown in fig. 3. It is a hybrid detector of the type illustrated in fig. 2(c) with the contacts of the sensors on the detector chip (fig. 1) bump-bonded to the amplifier inputs on the readout chip. The present version has a binary (yes/no) output and the readout chip has 63 rows of 16 cells, with 1006 useable elements and an extra row for electrical testing. In each cell fits a low-power electronic readout chain with a "conventional" low-noise charge sensitive preamplifier, an adjustable asynchronous comparator (discriminator), an adjustable delay, a strobe coincidence logic and a flip-flop memory element. The block diagram of this readout chain is shown in fig. 4. It has been designed for operation in a fixed-target experiment where particle interactions occur randomly and a positive trigger is available within 1 μs after the interaction. After discrimination the binary result is stored in a delay line memory exactly until a strobe can transfer the bit into the D flip-flop. Afterwards, readout proceeds serially row per row and in parallel for all 16 columns into a 16-bit bus. The total readout time depends on the speed of the bus drivers and is 13 μs at 5 MHz. The maximum rate for recorded events is then ~ 70 kHz. The equivalent noise charge referred to the input of the combined preamplifier/comparator system has been measured to be $< 100\ e^-$ r.m.s. which corresponds to 0.9 keV FWHM.

The D-Omega-Ion pixel detector has been tested in the WA94 experiment in the Omega spectrometer at CERN during October 1991. Several million triggered events have been recorded. A typical on-line event display with three tracks is shown in fig. 5. Detection efficiency of 99.2% and position accuracy of 25 μm have been measured. An array of 5 cm × 5 cm has been designed and is now under construction. It uses 72 readout chips bonded on 12 parallel "ladders" of high resistivity silicon.

More sophisticated electronic readout schemes will be developed for use in collider experiments in particle physics. The interaction rate of 70 MHz will be a challenge and the radiation environment will impose the use of radiation hardened processing technology.

4. MICROPATTERN DETECTOR: ON-CHIP INFORMATION PROCESSING

Detectors with on-chip information processing or "smart-sensors" appeal to the imagination but in many cases in the past it has been a more economic solution to transfer raw data and execute the information processing on a standard digital computer. Nevertheless, under special circumstances it may be justified to design on-chip information processing of some kind, e.g. with limited data link capacity as on spacecraft, or if power for off-chip transmission can be saved by data compression. And with ever cheaper custom chip manufacturing the economic justification also may shift progressively towards on-chip integration.

An example of incorporation of advanced information processing has been recently published by Kioi et al. [26] of Sharp Laboratories. The block diagram of their character recognition chip is shown in fig. 6. This device is a true 3D electronics chip with 4 "floors" of functions. The first (lowest) floor of the chip contains the highest level logic functions of comparison, memory and information transmission in bulk nMOS technology. The second and third floors use SOI technology for data masking and digitization. The top floor contains the photodiodes and the input signal amplifiers. The processing technology development needed for the implementation of such a sophisticated design can at present only be provided in a few places. However, around 1965 the same was true for the basic MOS technology, and it has taken only two decades for this technology to be available worldwide, with about 1 µm feature size.

Until now, few ionizing particle detectors use on-chip digital information processing. One of the first examples is the FUGA sensor designed by Dierickx et al. [27] at IMEC. It provides the upper and lower bounds of the irradiated zone. Zero suppression is becoming more commonplace in detector readout chips [6] and it has also been implemented by Jaeger et al. [28] in one of the pixel readout circuits designed by the CERN RD-19 Collaboration. In view of the proposed construction of the high-intensity hadron colliders SSC in Texas and LHC at CERN, it can be expected that more complex prototype chips with on-chip information processing will be designed because of stringent requirements in power dissipation and full space coverage (hermeticity) of the sensitive area. In the interior of the experimental set-ups the capacity for cooling is limited and only tiny optical fibre links can be used, in order to reduce space for cabling, which is dead as far as particle detection is concerned.

5. 2D AND 3D IMAGING IN PARTICLE PHYSICS AND MEDICINE

It is useful to enumerate some of the characteristics of the imaging of the objects in particle physics and in medicine, while trying to use a common language. This may illustrate similarities and differences. In particle physics, images are desired from unique, three-dimensional particle interactions (events) and successive events are uncorrelated. Few sensor elements are illuminated (hit) in an average event, which provides a nearly empty image, but virtually all of these few hits are needed to make a meaningful reconstruction. Further, the imaging devices are themselves somewhere in the three-dimensional scene and influence the objects (particle tracks) to be imaged.

In medicine or in biology the images evolve relatively slowly in a continuous sequence which provides a form of redundancy and usually allows integration of the signal on the sensor element over a longer time. Mostly the imagers are at some distance from the object, although intrusive imaging is now frequently used. All the pixels in the images contain information and in most cases one is interested in a 3D object. A relatively large proportion of the pixels may be redundant for a good reconstruction of that object.

The main difficulty with particle physics imagers is the need for 100% efficient detectors over 100% of the area and the uniqueness of each event configuration, which has to be captured with high precision. However, only a small amount of data is generated in one image, and considerable data compression is possible, even if events follow each other at very high speed. The final data throughput then still is manageable.

Although in medical or biological applications the objects are slowly evolving one might obtain a much higher data throughput from the imagers because all pixels contain data. The requirements on speed and sensor element availability may be less stringent, but there is an advantage in good efficiency.

6. CONCLUSION

Very sophisticated semiconductor imaging devices are being developed in particle physics in view of future high-intensity collider experiments. These devices have sensor elements with dimensions in the 100 μm region and are capable of detecting charge signals corresponding to 5 to 50 keV with very low noise at a rate of 10 MHz. Such devices may be adapted to constitute powerful radiation imagers in medical or biological applications, which would allow single X-photon counting, thus extending dynamic range and improving image contrast. Photon energy analysis for e.g. Compton suppression may be considered.

For various applications like character recognition one is developing sophisticated devices with very complicated technologies. Particle imagers may incorporate some of these new technologies in order to become true "micropattern" detectors, capable of selecting useful information from a large amount of data.

Detector developments in particle physics may be relevant for applications in medicine and biology. One should always be careful to adopt an overall optimized system approach. This may lead to different trade-offs and different designs. However, the experience gained in building complicated systems is a new and essential ingredient for new approaches in medical imaging.

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FIGURE CAPTIONS

Fig. 1 Photograph of a part of a processed detector wafer. In the middle, a large silicon detector (8.3 mm × 6.6 mm) with two-dimensional segmentation is shown. Each segment (pixel) has dimensions 75 μm × 500 μm and is an individual diode element. The separation between segments is achieved by an oxide layer. Under total depletion condition 100% efficiency is obtained without any insensitive region between the segments. The various smaller structures seen around the main detector are test detectors to be cut off.

Fig. 2 The readout electronics can be incorporated in the detector in several ways:

(a) the circuits are built directly in the high-resistivity detector substrate;

(b) the circuits are in a silicon layer, created on top of an isolating oxide layer (SOI) and detector connections are vias in this oxide;

(c) the detector chip is separated from the electronics chip with a bump-bond connection.

Fig. 3 Scanning electron micrograph of a few cells of the CMOS readout chip which can be associated with the matrix detector of fig. 1. The dimension of each cell is 75 μm × 500 μm. Each cell has a solder bump of ~ 30 μm diameter which can connect to the sensor element. The vertical lines are the power supplies and clock lines for the binary output shift register.

Fig. 4 Block diagram of the pixel detector readout circuit in each cell of fig. 3. A charge-sensitive amplifier with integrating capacitor of 7 fF is followed by a comparator, an adjustable binary delay element, a strobed multiplexor and a D flip-flop. I_{fn}, I_{dn} and I_{dis2} are externally adjustable currents.

Fig. 5 A small telescope of three pixel detectors has been exposed in a high-density particle flux in a heavy ion experiment at CERN. In this on-line event representation the particles were entering from the top and the hits from three particle tracks can be distinguished. With this circuit a trigger rate of 2 MHz can be achieved.

Fig. 6 An advanced pattern recognition chip with four floors of signal and information processing circuits, in SOI technology, designed by Kioi et al. [26] at Sharp Laboratories.

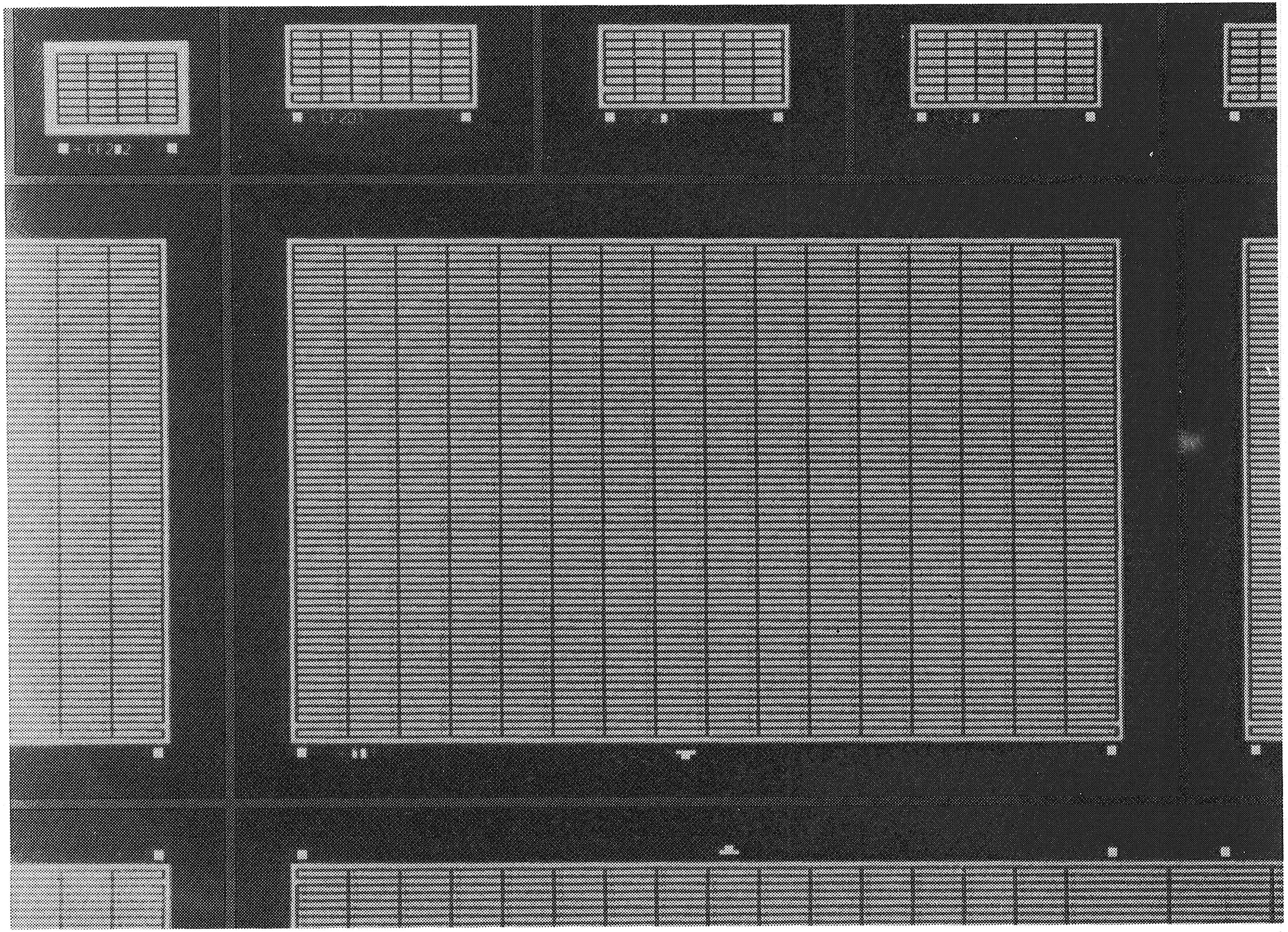
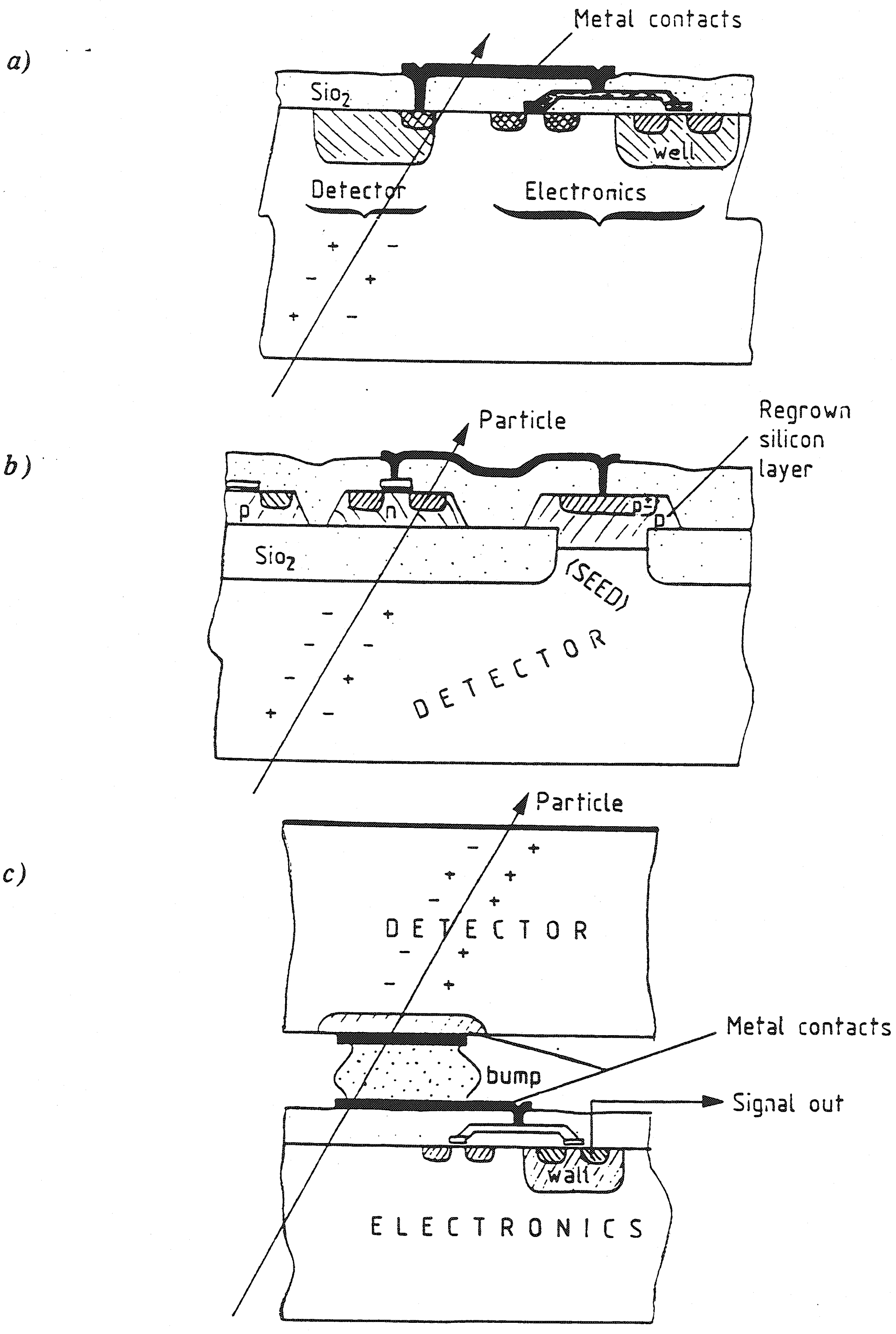


Fig. 1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DETECTOR
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Fig. 2

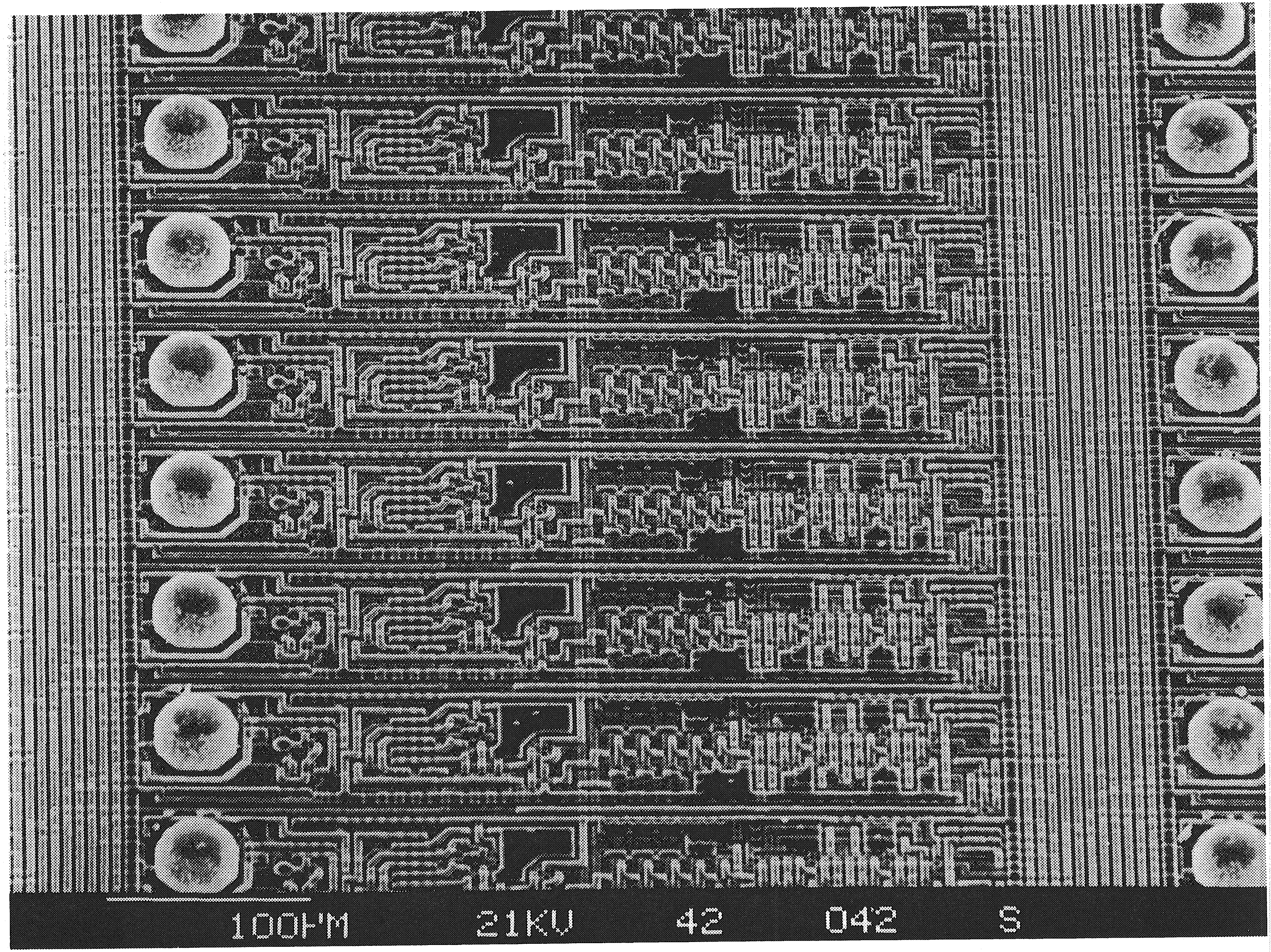

Fig. 3

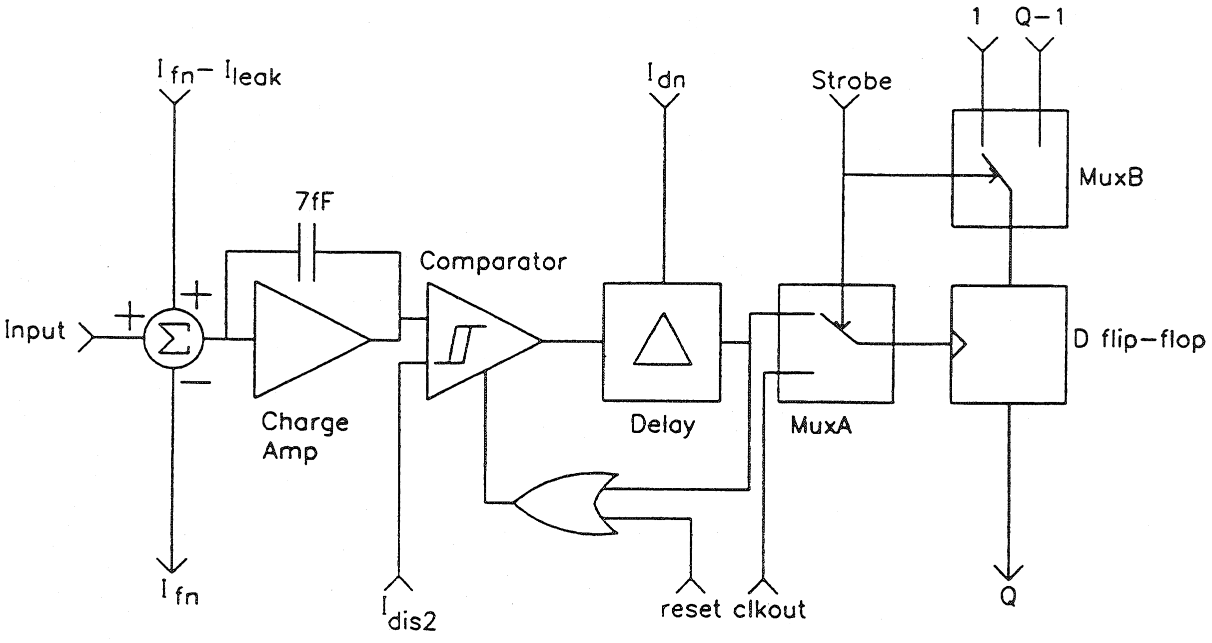
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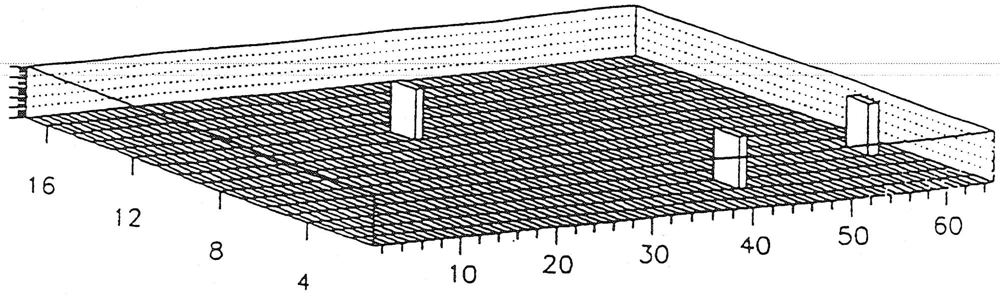
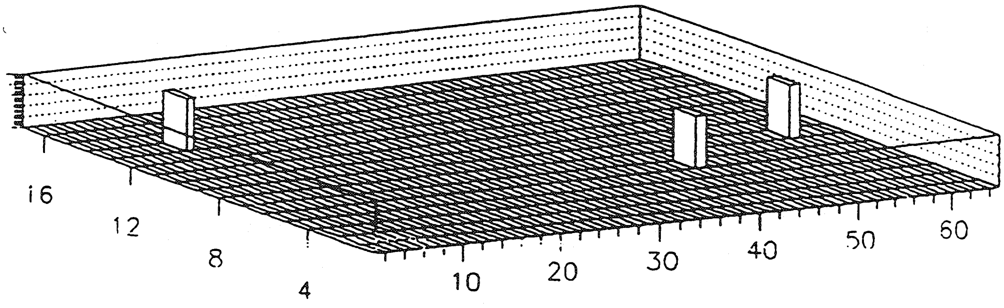
Fig. 4



PLANE 1



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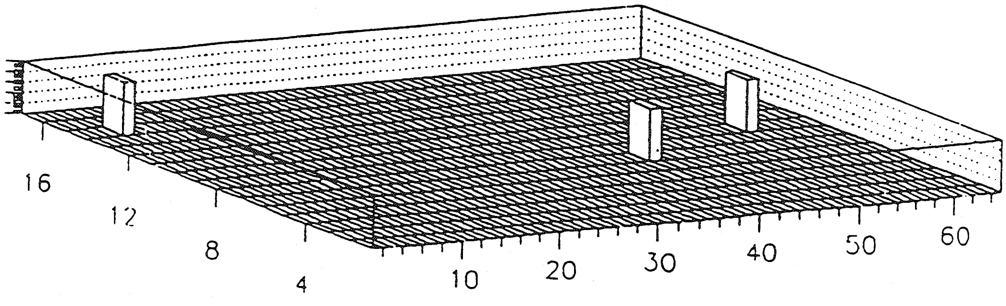

PLANE 3

Fig. 5

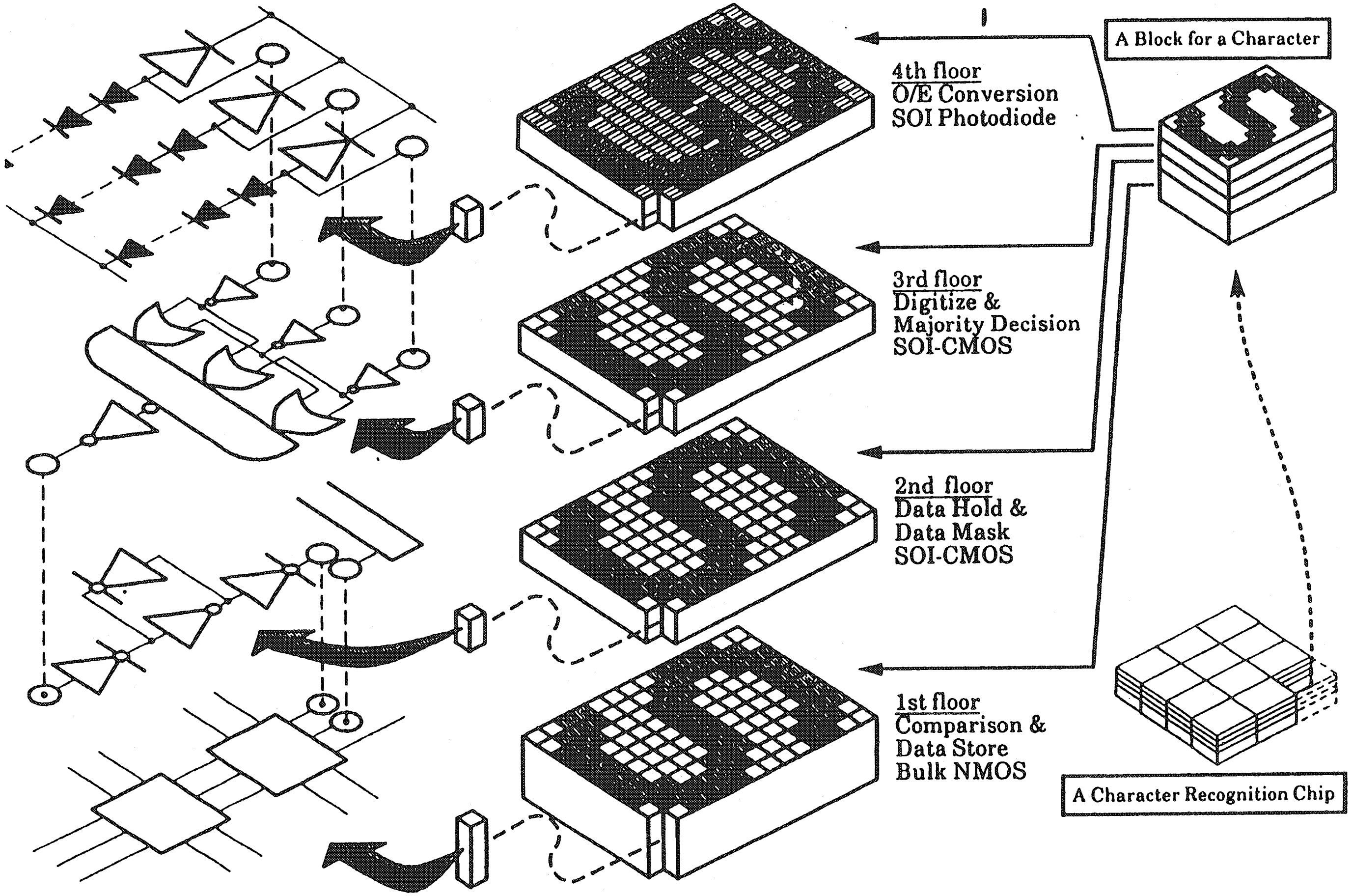

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Fig. 6