DESIGN AND PERFORMANCE OF THE READOUT ELECTRONICS CHAIN OF THE DELPHI FORWARD RING IMAGING CHERENKOV DETECTOR

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ABSTRACT

In this paper the front-end readout electronics chain of the Forward Ring Imaging CHerenkov (FRICH) detector used at the DELPHI experiment of the Large Electron Positron (LEP) collider is presented. The system incorporates a wideband low-noise preamplifier, mounted in the proximity of the MultiWire Proportional Chamber (MWPC), an Amplifying-Discriminating-Multiplexing (ADM) FASTBUS unit for further signal amplification, discrimination and channel reduction, and a LEP time digitizer FASTBUS unit for time digitization. The paper gives a general view of the detector and its electronics with particular emphasis on the novel characteristics and capabilities of the system.

Mac/Word/6008F/FF/gp

1. INTRODUCTION

The FRICH detector [1] is part of the particle identification system of the DELPHI experiment [2] at the CERN LEP collider. It is used to identify pions, kaons and protons in the forward and backward regions ($16° < \theta < 40°$) in most of the momentum range up to 20 GeV/c, using the ring imaging technique [3].

Charged particles traversing the detector emit UV photons by the Cherenkov effect in two different radiators: a liquid C_6F_{14} layer and a gaseous C_4F_{10} volume. The cones of light of the two radiators are focused onto the same planar photon detector where they form two ring images: a small one of ~ 3 cm radius for the gas radiator and another one of about ten times larger radius for the liquid radiator. Radiators and photon detectors are segmented into azimuthal sectors of $30°$. These 12 azimuthal sectors each contain a photo-sensitive Time Projection Chamber (TPC). The chosen photo-sensitive gas is tetrakis (dimethylamino)ethylene (TMAE) with the balance of the drift gas being ethane (C_2H_6). The windows on the front (liquid radiator) side and back (gas radiator) side of these TPCs are made of quartz. The wavelength dependence of the transmission of quartz and of the quantum efficiency for TMAE combine to permit the detection of photons in the range of 6–7.5 eV. Thus, photons in this energy range will convert to electrons by photoionization and will drift towards the two radial edges of the TPCs where the MWPc are located. The drift field is 1 kV/cm and the maximum drift length is 35 cm, resulting in a maximum drift time of ~ 9 μs.

Each of the 48 MWPCs contain 320 anode wires and 240 cathode strips, organized in 20 blocks of 16 wires and 12 perpendicular cathode strips (fig. 1). Special photon screens around the anode wires absorb most of the photons produced in the avalanche and prevent the photons from producing a feedback signal.

The particle separation power of the Ring Imaging CHerenkov (RICH) counter is directly linked to the granularity, i.e. the space resolution, of the detector. The geometrical uncertainty has to be better than the chromatic uncertainty of the detector. This plays a role not only in the readout granularity, but also in the choice of the detection gas.

We have achieved a fine granularity with few active elements in the whole Data AcQuisition (DAQ) system. The pick-up chambers of the detector provide anode and cathode signals; in addidon the drift time is recorded. This yields a final readout granularity of 0.5×2.6 mm^2 in the ring image plane, covering nearly 8 m^2 in total, and a depth granularity of 5 mm.

In addidon to the requirements of the granularity, the readout chain (i.e. chamber and electronics) has to maintain full detection efficiency for single photoelectrons in the presence of ionizing tracks which can generate ~ 600 primary electrons distributed over ~ 10 wires.

In order to achieve the required detection efficiency, the pick-up chamber operates in a saturated proportional mode (i.e. gas amplification $> 10^5$). Therefore, the ionizing tracks will have a truncated Landau-like pulse height distribution, while the single photoelectrons will show a broad Polya distribution near to the electronic noise limit.

Thus, the electronics must be able to detect the small single photon signals, while not being disturbed too much by the large signals from the ionizing tracks.

2. THE ELECTRONICS CHAIN

In this section, a general view of the electronics chain from the MWPC to the front-end buffers is presented. More details on each unit of the DAQ system are given in the following subsections.

The preamplifiers are housed in the chamber body. The signals are transferred via 40 m twisted-pair cables to the Amplifying Discriminating time MUltipleXing (ADMUX2) FASTBUS units and then to LEP Time Digitizer (LTD) FASTBUS units [4] (fig. 2). The needs of the whole detector are covered by 26 880 preamplifiers, 420 ADMUX2 and 70 LTD units.

The thresholds of the discriminators in the ADMUX2 are kept as low as possible to give a detection efficiency for the photoelectrons as high as possible. Even if the signal-to-noise ratio of the preamplifiers is good, additional noise hits will be recorded. These hits will be suppressed by a time matching of anode/cathode signals on the basis of their mutual coincidence which is set to $\pm$ 25 ns.

The time matching also opens the possibility to perform a 2:1 ORing of signals coming from different chambers as a first level of multiplexing. This can be done without any appreciable increase in the space point reconstruction ambiguity. An additional true time multiplexing following the ORing brings the multiplexing factor within one ADMUX2 to 4:1. At the system level, however, the total multiplexing factor is increased to 8:1 having the possibility of ORing together with the two outputs of two different ADMUX2 modules, as will be explained later.

The LTD module completes the readout chain. It provides the digitization of the time structure coming from the ADMUX2 units. Due to its internal zero suppression mechanism, along with an efficient use of its input memory, a fine time resolution on a wide dynamic range is made possible. In the "veto mode" it has the same resolution as the clock period on the overall time range up to 2^{12} clock pulses.

The ADMUX2 and the LTD units are synchronous devices. They run on the same 100 MHz timing FOFR unit. The FOFR unit produces up to 40 μs long clock bursts

which are synchronized by the local event supervisor, Pandora [5]. The Pandora relays all timing and trigger information in the DELPHI experiment.

2.1 The preamplifier

The preamplifier design has been optimized for cost, space and power requirements. It is based on a NE592 video amplifier (fig. 3) housed in the SO8 surface mount package. This 120 MHz unity gain bandwidth amplifier has differential inputs and differential outputs. It consists of two internal emitter-coupled stages plus an emitter-follower output stage. It provides the choice to trim its voltage gain by means of an external network, or to fix it at the maximum value of 400 without adding any external components. Its use is intended for magnetic memory systems, as well as for wideband pulse amplifiers in communication systems.

The MWPC preamplifier works as a voltage amplifier with a 4.7 kΩ resistor connected between one input and ground. The other input is tied directly to ground. The total gain is ~ 200 with a flat region for the frequencies between 600 kHz up to the NE592 high-frequency cut-off. The presence of a zero in the origin (i.e. for the DC component) of the preamplifier transfer characteristic causes the differentiation of the long $1/t$ tail of the input signal, reducing the dead time for a ionizing track signal to < 1 μs. There is practically no dead time for a single photoelectron and no appreciable pile-up for jet-like events.

The preamplifier outputs drive 40 m of twisted-pair cable which is terminated by the ADMUX2 line receiver. The negative output signal from the NE592 saturates earlier than the positive one due to the limited sink current of its emitter follower output stage. The asymmetric driving of the twisted pair cable gives rise to an unmatched termination of the signal and therefore a damped ringing for very large signals. Reducing this effect by increasing the supply voltages also increases power consumption, so an acceptable compromise has been reached between these two effects.

The preamplifiers for the anodes and for the cathodes are similar. Both assemblies consist of two printed-circuit boards (PCB) mounted one on top of the other, 2.5 mm apart and with the components on thc external sides. The anode assembly contains 16 channels, while the cathode has 12 channels. The 2.5 mm space between the two PCBs is used to accommodate the cooling tubes, which also provide a good bus bar for the common ground. The connections to the anodes and the cathodes are done by a Holtite™ connection system. This reduces the stray capacitance and pick-up problems.

2.2 The ADMUX2 unit

This FASTBUS unit performs a treshold adjustable discrimination of 64 differential analog inputs distributed on 4 input connectors, followed by an AND gating of every

single channel, two ORing of 16 + 16 signals belonging to adjacent input connectors, and finally a time multiplexing of the two sets of 16 + 16 channels coming from the previous ORing (fig. 4).

The full unit is composed of three modules: (a) the discriminator, (b) the FASTBUS mother board, and (c) the auxiliary card.

(a) **The discriminator module** is a four-channel double-sided 58×40 mm^2 daughter board which contains all the analog fast electronics. It is built in surface mount device (SMD) technology and consists of five stages (fig. 5):

(i) A line receiver/amplifier stage (NE592): its purpose is to amplify the input signal to a level where the discrimination can more easily be done. It has a typical gain of 26 and its differential inputs are a.c. coupled and terminated on 56 Ω.

(ii) A discriminator stage (1/3 of 10 116): it converts the analog information into digital by comparison with a threshold voltage (V_{th}). The input discrimination threshold range is linearly adjustable from 4 mV to 50 mV. The reference voltage (V_b) is set to the typical -1.29 V ECL threshold level (fig. 5). A dumping diode at its input improves the recovery time from exceptionally high input signals, while a capacitor can be put into the circuit to improve the noise characteristics of the input signal by limiting its bandwidth with an additional single pole.

(iii) A differentiator stage (1/3 of 10 116): it differentiates the output of the discriminator stage for a correct driving of the following monostable stage in the case of very long analog input pulses (i.e. it avoids multipulsing).

(iv) A monostable stage (1/3 of 10 116): it provides a well-defined output pulse of 50 ns duration when the discriminator is fired.

(v) An output gate stage (1/4 of 10 104): it allows one to disable the whole discriminator module when the common enable signal is turned OFF.

No detectable crosstalk at the minimum threshold of 4 mV has been seen on the ADMUX2 prototype. This feature has been achieved in the discriminator by choosing optimal ground "power" IN/OUT signal pin arrangement and by using a four-layer printed circuit board equipped with properly distributed bypass capacitors.

(b) **The FASTBUS mother board** carries the 16 discriminator daughter boards and all the additional digital and analog slow electronics.

After the discrimination, an AND stage allows one to enable/disable every single channel in order to reject those that have some problem such as preamplifier oscillation, excessive noise, or any other fault.

Then, an OR stage, composed of two 32-bit OR gates, mixes together the 16 + 16 signals coming from two adjacent input connectors in order to reduce by a factor of

two the total number of channels. This ORing is made by combining antipodal channels with respect to the beam axis (fig. 2).

The next multiplexing stage is a 1 k word shift register. It delays a group of 16 channels coming from the previous ORing by 10 μs compared to the other group of 16 channels. This shift register is implemented by means of fast ECL static memories sequentially addressed by a pointer for working in a circular configuration. The perfect synchronization of the memory input, output and control signals, as well as the adoption of an encoding scheme for the memory address lines, has permitted the use of cheap 10 ns access time memory that is clocked at 100 MHz.

Finally, after the time multiplexing stage, the two sets of 16 channels are mixed together and driven to the output on the FASTBUS auxiliary connector.

The dual power supplies for the detector preamplifiers, the FASTBUS interface and the digital-to-analog converters (DACs) for the remote adjustment of the discriminator thresholds are also located on the FASTBUS mother board. The discriminator thresholds are composed of 8 groups of 8 channels each. The preamplifier power supplies can be switched OFF by a FASTBUS command.

The FASTBUS interface is a pure slave interface addressable in both "random" and "broadcast" modes in Control Status Register (CSR) space. FASTBUS allows one to download the desired set-up, i.e. threshold levels and enabled/disabled channels, and to test the device without removing it from the experimental area. The test checks the integrity of any internal CSRs, the circular memory along with its address encoding logic, the whole data path taken by the data signals from the output of the discriminators up to the output drivers, as well as the FASTBUS interface itself.

(c) **The auxiliary card** is plugged into the rear side of the FASTBUS crate in the auxiliary area. It consists of two printed circuit boards (253 $\times$ 176 mm^2 and 53 $\times$ 176 mm^2) mounted one on top of the other and connected together by means of an internal connector.

This module will be plugged into two adjacent slots of the FASTBUS auxiliary area. It ORs bit-to-bit the single-ended signals coming from the outputs of two mother boards and convert, them into differential signals for driving a twisted pair flat cable.

2.3 The time multiplexing scheme

The time multiplexing is made in order to further reduce the number of channels without the loss of information and to optimize the use of the time measurement range of

the LTD unit (i.e. 41 μs at 100 MHz clock frequency) in comparison with the maximum detector drift time (i.e. ~ 9 μs).

The adopted scheme is that of the multiplexing four, which consists of multiplexing together four time slots of the same duration before presenting them to the LTD for time digitization. The time slot duration is set to 10 μs, but, if required by the user, it can also be tuned within 0 and 2^{12} clock counts just by changing some jumper positions in the ADMUX2. The LTD saturation probability caused by a high hit frequency is minimized by an appropriate choice of the multiplexed channels. As shown in fig. 2, these channels are taken from MWPCs belonging to sectors at 90° angle.

The ADMUX2 has two modes of operation, "low" and "high" modes, which allows one to implement the multiplexing four-scheme by only ORing the two outputs of two different low and high mode units. The selection of these two modes is made by means of a switch (fig. 4).

The low and high-mode units are hardware equivalent. They can be interchanged just by replacing the buffers in the low-mode units with an additional set of circular memories for the high-mode unit.

The low-mode unit performs the time multiplexing on the first two-time slots of 10 μs (fig. 6), i.e. in time slot 1, the first 32 input channels being directly driven to the output, while the second 32 channels are stored into the circular memories waiting for time slot 2 to be driven to the output. Then, the unit disables its output and waits for a reset condition.

The high-mode unit again performs the time multiplexing on two-time slots of 10 μs but shifting the output by 20 μs compared to the low-mode unit (fig. 6). That is, in time slot 1 all the 32 + 32 input channels are stored into the circular memories, while the ADMUX2 output is disabled. When time slot 3 arrives, the first set of 32 recorded input channels will be driven to the output, followed by the second set at time slot 4. Then again, the unit disables its output and waits for a reset condition.

2.4 The FOFR unit

The 100 MHz clock signal generated by this timing unit provides both the correct timing and the good synchronization mechanism (fig. 7). A series of fanout units distribute the clock to the whole system.

Two oscillators can be selected: a free running 100 MHz crystal oscillator or a start/stop RC oscillator which can be trimmed around 100 MHz frequency. The

synchronizing signal comes from the local trigger supervisor unit Pandora, which either gates the free running crystal oscillator onto the clock output or starts and stops the RC one.

Both oscillators generate a series of bursts which are started at the beam crossover time, with possibly some positive or negative fixed delay. It is stopped either by a negative first-level trigger (after ~ 3 μs) or a negative second-level trigger (after a maximum 39 μs). If the second-level trigger is positive, then the clock is left running up to the complete acquisition time (i.e. > 40 μs).

3. STATUS AND CONCLUSIONS

We have successfully designed and tested the analog and digital electronics for the DELPHI-FRICH Detector. The tests show that the system can detect with high efficiency photoelectrons in the presence of ionizing tracks. The new 10-layer ADMUX2 FASTBUS board used for the fast discrimination of the detector analog signals and the channel multiplexing is currently in its production phase.

One quarter of the detector will be installed by the end of 1991. The detector will be completed at the beginning of 1993.

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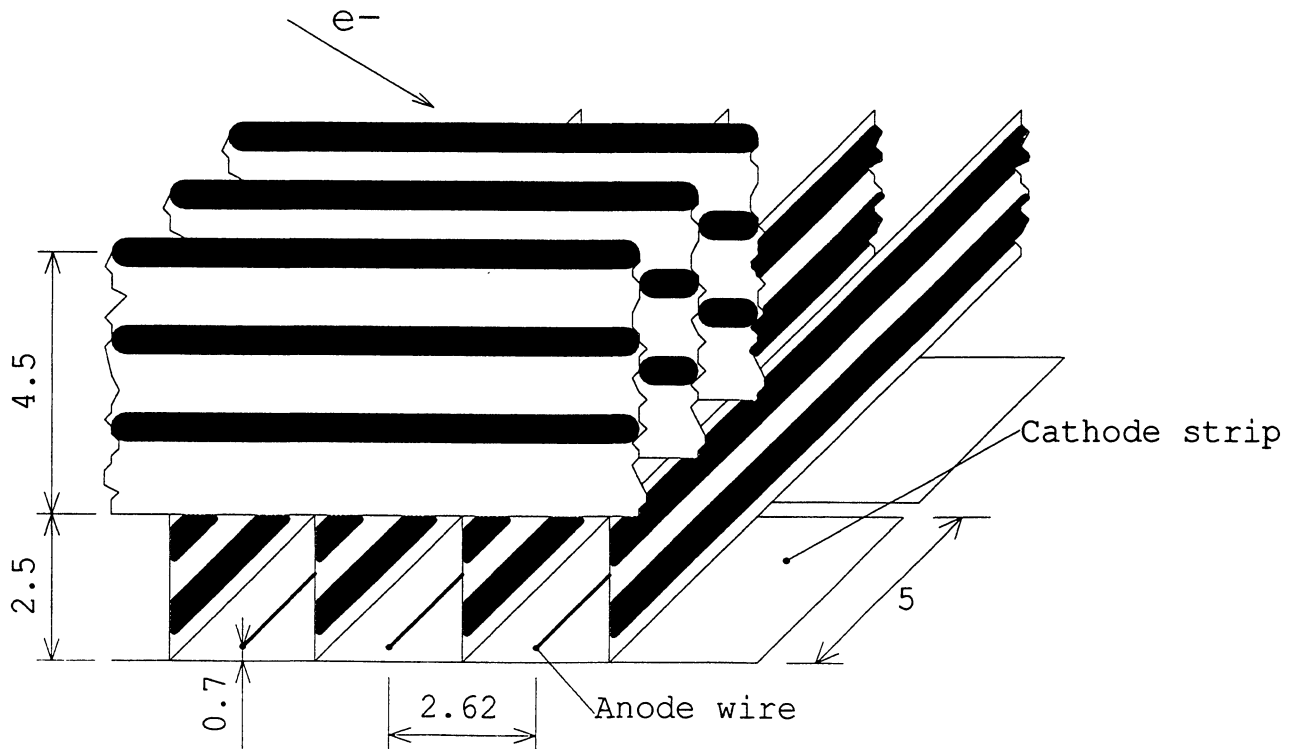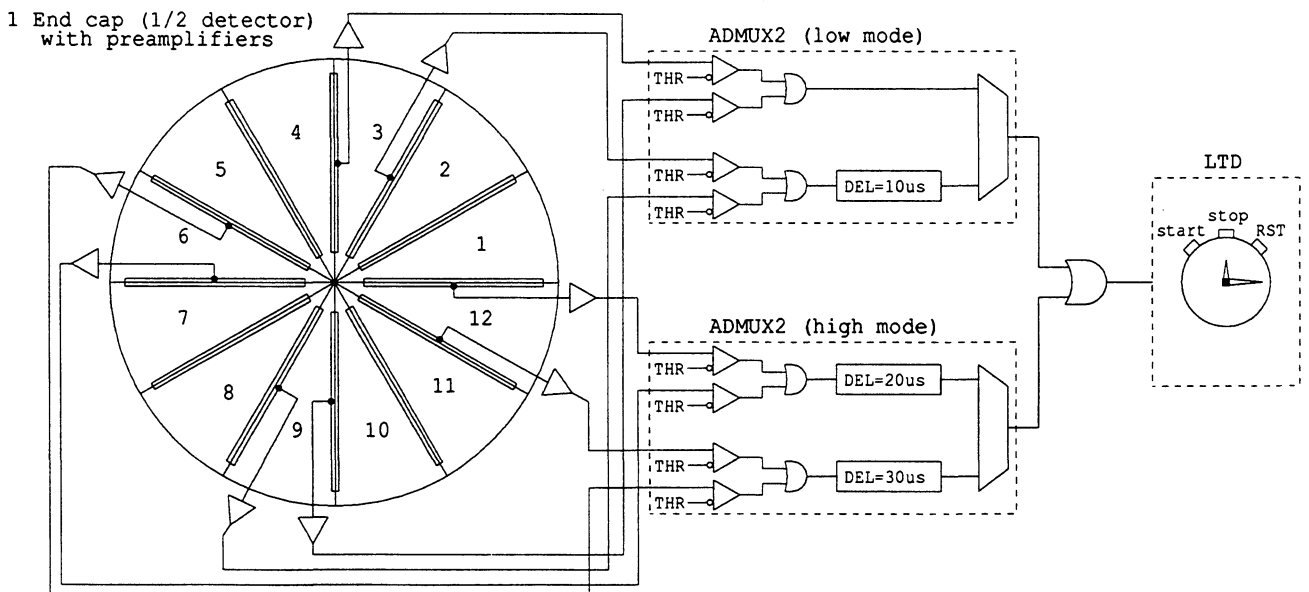Wuppertal Univ. Germany.

Fig. 1 Detail of the MWPC
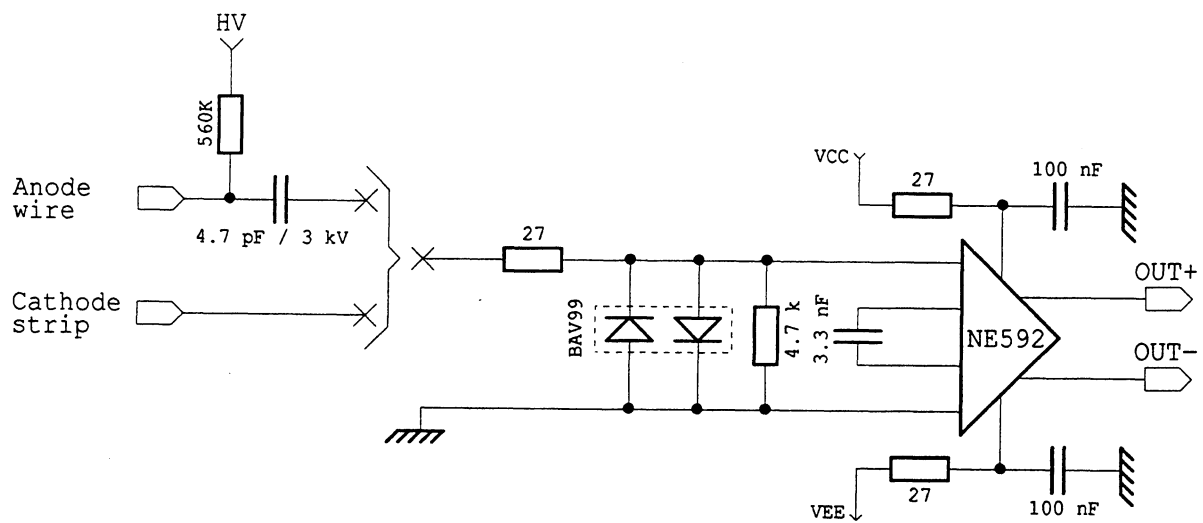

Fig. 2 Readout system block diagram

Fig. 3 Preamplifier circuit diagram
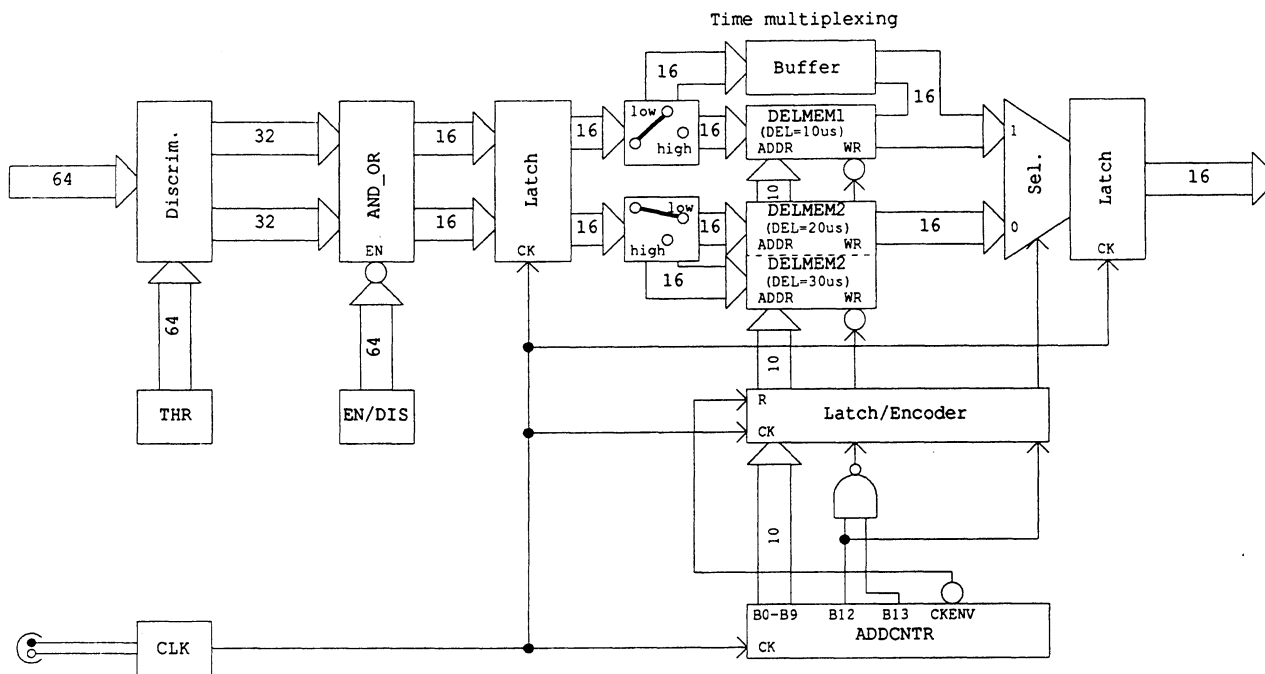
Fig. 4 The ADMUX2 block diagram
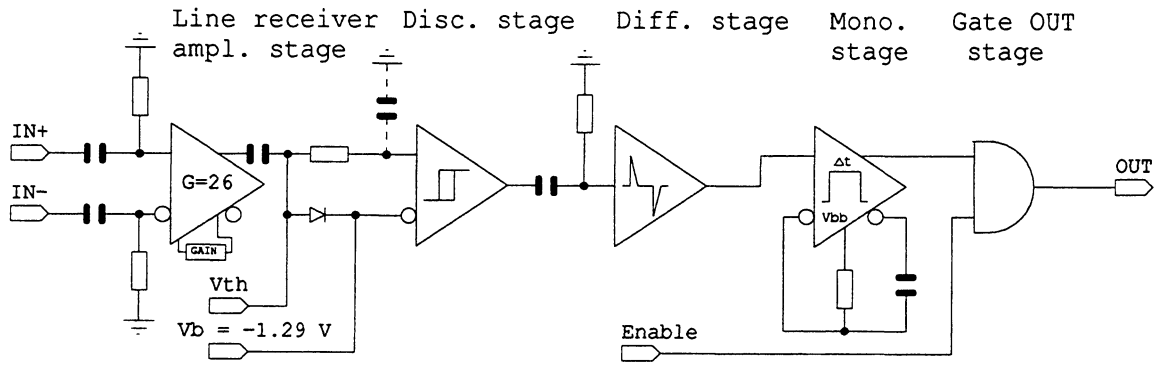
Fig. 5 Discriminator block diagram

	Time slot 1	Time slot 2	Time slot 3	Time slot 4
Acquis.	CH00-CH31 CH32-CH63			
Output	CH00-CH31	CH32-CH63	DISABLED	DISABLED

ADMUX2 low mode

	Time slot 1	Time slot 2	Time slot 3	Time slot 4
Acquis.	CH00-CH31 CH32-CH63			
Output	DISABLED	DISABLED	CH00-CH31	CH32-CH63

ADMUX2 high mode

Fig. 6 ADMUX2 low and high mode principle

Fig. 7 Clock signal