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CAcTμS: High-Voltage CMOS Monolithic Active Pixel Sensor for tracking and time tagging of charged particles

F. Guilloux[1,a], **F. Balli**[a], **Y. Degerli**[a], **M. Elhosni**[a], **C. Guyot**[a], **T. Hemperek**[b], **M. Lachkar**[a], **JP. Meyer**[a], **A. Ouraou**[a], **P. Schwemling**[a], **M. Vandenbroucke**[a]

[a] *IRFU, CEA, Université Paris-Saclay*
91191 Gif-sur-Yvette, France

[b] *University of Bonn,*
Nussallee 12, Bonn, Germany

E-mail: fabrice.guilloux@cea.fr

The increase of luminosity foreseen for the Phase-II HL-LHC upgrades calls for new solutions to fight against the expected pile-up effects. One approach is to measure very accurately the time of arrival of the particles with a resolution of a few tens of picoseconds. In addition, a spatial granularity better than a few millimeter will be needed to obtain a fake jet rejection rate acceptable for physics analysis. These goals could be achieved by using the intrinsic benefits of a standard High-Voltage CMOS technology – in conjunction with a high-resistivity detector material – leading to a fast, integrated, rad-hard, fully depleted monolithic active pixel sensor ASIC.

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[1]Speaker, corresponding author

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1. Introduction

The increase of luminosity foreseen for the Phase-II HL-LHC upgrades will lead to an unprecedented occupancy of the detectors. A solution proposed to fight against the resulting pile-up effect is to measure very accurately the time of arrival of the particles with a resolution of a few tens of picoseconds. This allows to reject by the time of flight technique the tracks associated with random pile-up vertices spread longitudinally along the protons bunches collisions. In addition, a spatial granularity better than a few millimeter will be needed to obtain a fake jet rejection rate that is acceptable for the physics analysis. Such performance should be obtained with a sensor also able to cope with the very important radiation levels expected at HL-LHC (up to 6×10^{15} 1 MeV equivalent n/cm² and 6.5 MGy).

These goals could be reached using the intrinsic benefits of the High-Voltage (HV) CMOS technology. The technology supports high-resistivity (HR) wafers leading to a complete depletion of the charge sensitive area (> 100 µm depth) of thinned sensors, enhancing the tolerance to neutron damages.

Proofs of the detection capability and radiation hardness have already been produced for HV-HR technology [1]. We will present here the architecture and simulation results of a 100 mm² pixel sensor, called CAcTµS (CMOS Active Timing µ Sensor), dedicated to timing measurements. Device (TCAD) simulations and electrical simulations studies based on the HV-HR CMOS LFoundry 150 nm technology design kit have been made to prepare a submission of the CAcTµS chip. These simulations have shown that a resolution of the order of 50 to 80 ps per MIP impact point can in principle be reached for a HV-CMOS monolithic active pixel sensor (MAPS) with 1 mm pixel pitch and 145 mW/cm² power budget.

2. TCAD simulations of HV-HR 150 nm process

CMOS Monolithic Active Pixel Sensor is a growing technology already used in several particle tracking detectors (EUDET telescope, STAR vertex detector [2], ALICE ITS & MFT [3]) which has shown its capability to detect efficiently MIPS into the CMOS wafer substrate. In addition to its tracking capability, the CMOS technology features options which could enhance the timing measurement resolution of sensors.

2.1 LFoundry technology

It has been shown that a 100 µm height thinned pixel sensor, developed in LFoundry 150 nm process technology with HR wafer ($R > 2\ k\Omega\cdot cm$), could be fully depleted for $HV = -80$ V. A fully depleted sensor guarantees a faster charge collection by drift with respect to charge collection by diffusion. It is also less sensitive to neutron and proton induced damage by minimizing the charge trapping effects in a damaged crystal [4]. Fast charge collection and minimized charge trapping are both an advantage for the design of a radiation-hard timing sensor.

This technology achieves in a standard process a high electric field by isolating the transistor devices – working with standard power supplies – into the collecting diodes. Thus the collecting diode fills the entire area of the pixel, excepted for the pixel guard-ring, leading to

100 % of detection efficiency between pixels and maximizing the electric field uniformity, especially for the case of backside polarized devices.

The in-diode electronics allows a first level signal processing but is a trade off between, electronics functionality, as signal amplification, which increases the signal to noise ratio and the additional input capacitance, proportional to the transistors surface, which decreases the signal to noise ratio if staying at a constant power budget.

2.2 TCAD simulations of pixels

A careful device level simulation of the LFoundry process has been done to optimize the charge collection time and the signal to noise ratio to target time measurement of MIP with less than 100 ps resolution. This study included a 3D validation of the pixel design in Sentaurus TCAD tools with the geometry imported from CADENCE software and later on electrical simulations in CADENCE.

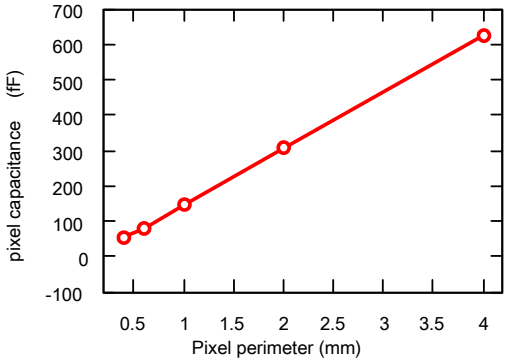

Figure 1: *Simulated pixel input diode capacitance. (100 µm thin sensor and HV = −80 V, backside polarization).*

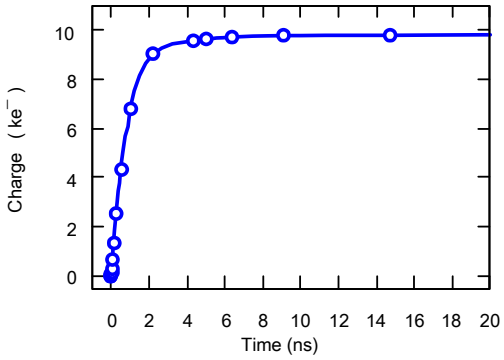

Figure 2: *Simulated charge collection of 1×1 mm² pixel. (100 µm thin sensor and HV = −80 V, backside polarization).*

Two major design parameters where confirmed by TCAD simulations: the expected pixel capacitance and the charge collection time profile (Figure 1 and Figure 2) with respectively 1.5 pF total capacitance for 1×1 mm² pixel (diode capacitance ≈ 0.65 pF + embedded electronics from CADENCE parasitic extraction in a worth case scenario) and about 8 ke⁻ collected within 1.8 ns.

3. CacTµS prototype

Results from the TCAD simulations were taken as inputs to Spice-like electronics simulations in CADENCE and has lead to the design of an ASIC prototype, named CAcTµS aiming to demonstrate the timing capabilities of the HV-HR CMOS technology.

3.1 ASIC architecture

The prototype architecture is based on the LF-CPIX ASIC [5] and designed in the same technology. It uses enhanced sensor layout with respect to LF-CPIX, which have been experimentally proven to support down to HV = −380 V.

The ASIC is composed of a 62 mm² sensitive area of 82 pixels divided equally between pixels with a surface of 1 mm² and pixel with a surface of 0.5 mm² (Figure 4). Each pixel embeds a fast readout chain featuring a charge sensitive amplifier followed by a leading edge discriminator with an in-pixel threshold trimming DAC. The digital output of the discriminator can be stored in an in-pixel memory or send out to the end-of-column digital circuit.

The end-of-column digital circuit concentrates all the pixel outputs into a fast digital OR sent out of the ASIC. In parallel, a dedicated circuit tags the address of hit pixels and sends the address out of the ASIC on a slow digital bus (Figure 3).

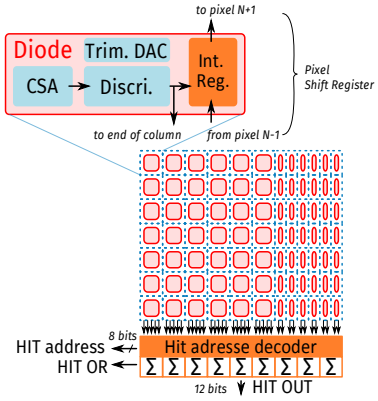

Figure 3: *CAcTµS schematic architecture.*

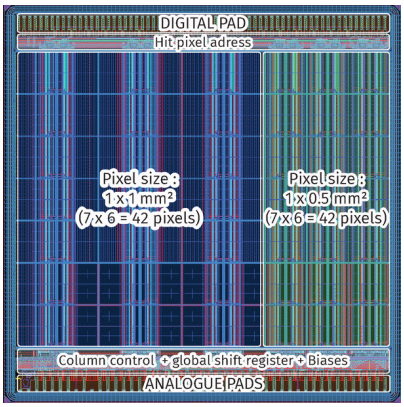

Figure 4: *CAcTµS layout view.*

3.2 Electronics simulations and expected performance

The in-pixel signal processing electronics has been designed to match with the transient response of the diode from TCAD simulations, leading to a fast rise time of 0.9 ns (Table 1) giving about 2 ns peaking time for a power consumption of 145 mW/cm² in case of 1 mm² pixel size.

Parameter	*C_{in} = 1.5 pF (1×1 mm²)*	*C_{in} = 1.0 pF (1×0.5 mm²)*
Rise time (10% - 90%)	0.9 ns	0.8 ns
Input Referred Noise	290 e^-	220 e^-
Jitter before comparator	67 ps	44 ps

Table 1: *Pixel charge sensitive amplifier performance estimated from AC simulation.*

Transient noise analysis have been performed to estimate the time resolution of the complete system at the ASIC output. The input of the signal processing is modeled by input charges following a Landau distribution (mean probable value expected MPV = 8000 e^- for 100 µm thin sensor, Figure 5). The individual digital output pulses are measured at the ASIC output and corrected from the time walk by the time over threshold (ToT) technique. Dispersion of the ToT is taken into account to calculate the final arrival time resolution (Figure 6).

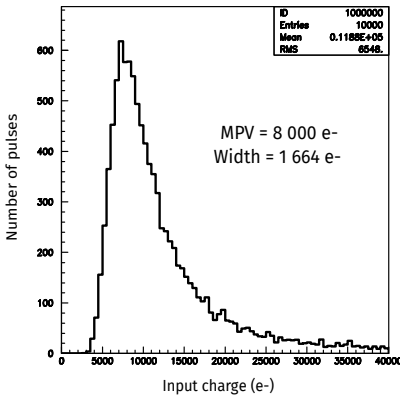

Figure 5: *Input signal charge distribution.*

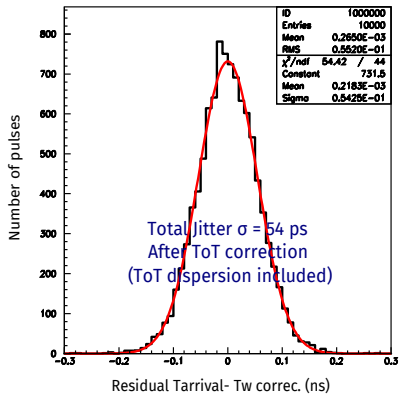

Figure 6: *Estimated arrival time resolution including time walk correction and time over threshold dispersion.*

The simulated time resolutions in theses conditions are respectively 60 ps and 80 ps for 8000 e^- and 4000 e^- Laudau charge distribution MPV.

4. Conclusion

A complete study of a timing sensor in HV-HR CMOS technology suitable for radiation-hard environment has been carried out. TCAD simulations have shown that a fully depleted substrate of 100 µm thin sensor paved with 1 mm² pixels should reach a time resolution better than 100 ps within the HV-HR CMOS LFoundry 150 nm process.

A sensor prototype named CAcTµS has been designed following the TCAD recommendations and aims to obtain 60 ps arrival time resolution. ASIC simulations and final optimizations have been done and the submission is expected for end 2017.

Acknowledgments

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