AIDA-2020-MS83

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Advanced European Infrastructures for Detectors at Accelerators

Milestone Report

Interfacing the FE chip VMM128, GEMROC, TIMEPIX3 to SRS

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MILESTONE REPORT

INTERFACING THE FE CHIP VMM128, GEMROC, TIMEPIX3 TO SRS

MILESTONE: MS83

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Abstract:

MS83 focuses on tools to facilitate gas (not exclusively) detector research and development. Carried on by three groups, our WP13 subtask exploits the interface of three different multichannel front-end ASICs for the Scalable Readout System, SRS [1], a common data acquisition system developed in the context of the RD51 collaboration.

Three ASICs has been selected, among the available ones, according to requirements coming from R&D and experiments needs: analog readout, self-triggering and high-rate capabilities (VMM128 and GEMROC), high granularity, analog, timing and pixelated readout (TimePix3).

The Advanced European Infrastructures for Detectors at Accelerators (AIDA-2020) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168. AIDA-2020 began in May 2015 and will run for 4 years.

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Executive summary

This milestone describes the status and the results achieved interfacing the RD51 Scalable Readout System (SRS) to three front-end ASICs suitable for gas detectors: VMM and GEMROC for high-rate, analog and self-triggering operation, timePix3 for highly pixelated, analog, amplitude and timing readout.

In the first part of the document, we will describe the VMM-SRS system where the interface has been completed. The activities have been carried on in synergy with ESS, ATLAS and RD51 groups. In the second part, the current status and future plans of the long-term activities (hardware, firmware, software) linked to TimePix3 and SRS will be shown. This implementation is following the successful previous experience with TimePix and SRS for the LC-TPC detector. In the last session, the adapter card for the GEMROC chip to be interfaced with the SRS will be described.

1. INTRODUCTION

The RD51 collaboration recognized, since the beginning of its activities, the importance of having a DAQ system and multichannel front-end chips to cope with the detector R&D phase. Because of this, part of the collaboration started, in the context of the electronics-working group, a project named the Scalable Readout System, SRS [1]. A few key points were simplicity of use, portability, scalability from small to large systems and software availability. It was moreover designed as a common interface that could be adapted to different front-end chips. This last feature is the one exploited in this AIDA WP13 subtask.

The SRS has nowadays a high impact in the community: more than 50 groups are using the system with more than 2000 APV25 chips (the first and most successful front-end ASIC adapted to the SRS). SRS Components are available on the CERN store and part of them are licenced to external companies. The AIDA-2020 support has been used to apply additional capabilities to the system. In this milestone we will report the activities linked to the interfacing of SRS to VMM128, TimePix3 and GEMROC FE ASICs.

2. SRS AND VMM128

In the context of the ATLAS NSW upgrade, a new front-end chip has been designed at BNL: VMM [2][3]. VMM has been selected in parallel as the future baseline solution for the RD51 SRS community. Several groups showed a strong interest in this and decided to support the development phase. The European Spallation Source (ESS) with the NMX neutron diffraction instruments is the most important example. Starting from the initial support of the ATLAS team (Iakovidis et al.), the CERN GDD/RD51 and ESS team (in particular H. Muller, M. Lupberger and D. Pfeiffer) successfully developed and built a complete readout chain. The work done is described in this document. A more detailed report will soon be available in [7].

2.1. HARDWARE

This section describes the hardware of the SRS/VMM system. Description of all the new components will be given while SRS standard components will not be treated. The introduction to the chip is taken from the ATLAS and BNL report and does not refer to any work done in this project.

2.1.1. VMM ASIC

"*The VMM is a custom Application Specific Integrated Circuit (ASIC). It is intended to be used in the front-end readout electronics of both the Micromegas and sTGC detectors of the New Small Wheels Phase I upgrade project of the ATLAS experiment. It is being developed at Brookhaven National Laboratory. It is fabricated in the 130 nm Global Foundries 8RF- DM process (former IBM 8RF-DM). The 64 channels with highly configurable parameters will meet the processing needs of signals from all sources of both detector types. Version 3, the first prototype having all the needed functionality for the ATLAS experiment, was submitted on May 2016 in a dedicated run. It has all the design features including Level-0 buffer logic and SEU mitigation circuitry for the configuration registers, the state machines, and the FIFO pointers. VMM3 is being tested since October 2016"* [4]

The VMM architecture is shown in Fig.1 and the main characteristics are shown in Fig. 2.

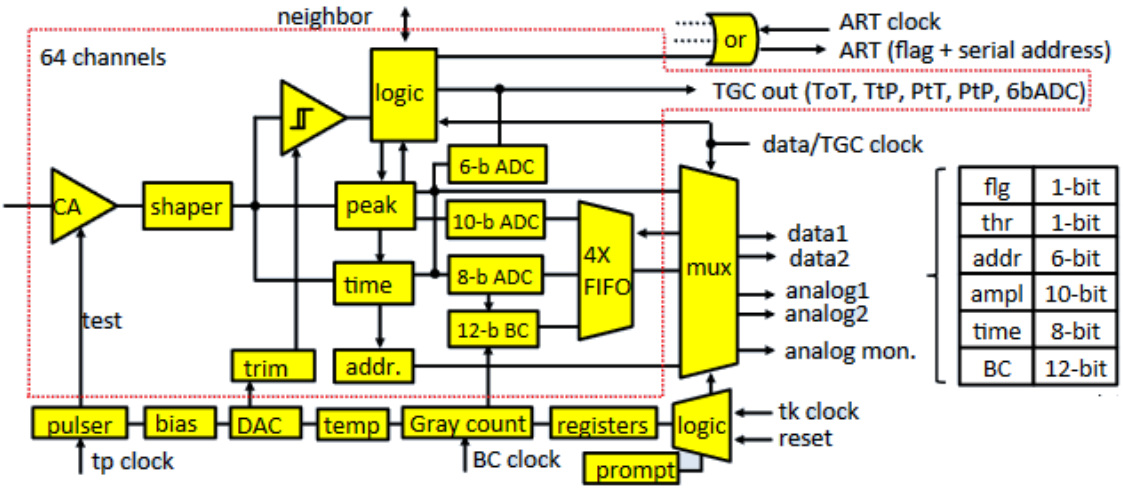


Fig. 1: Architecture of VMM [4].

Channels	64
Z_{in} [Ω]	50 - 75
Gain [mV/fC]	0.5 - 16
Sub-hysterisis	~20 mV
Charge linear range [pe]	250 - 8,000
Charge resolution [fC]	0.38 fC
Shaper	unipolar or bipolar
Shape order	3rd cc
Peaking time [ns]	25 - 200
TAC [ns]	60-650
Discrimination	yes (hysteris)
Readout buffers	up to 64 events
Threshold DAC	10-bits
Amplitude measurement	direct voltage
Timing measurement	TAC (peak or thr)
Time Walk [ns]	< 2
Timing resolution [ns]	< 1
Timing conversion	8-bits
Timing dynamic range	12 coarse + 8 fine
L1 buffer memory	64 deep / channel
Power/channel [mW]	< 10

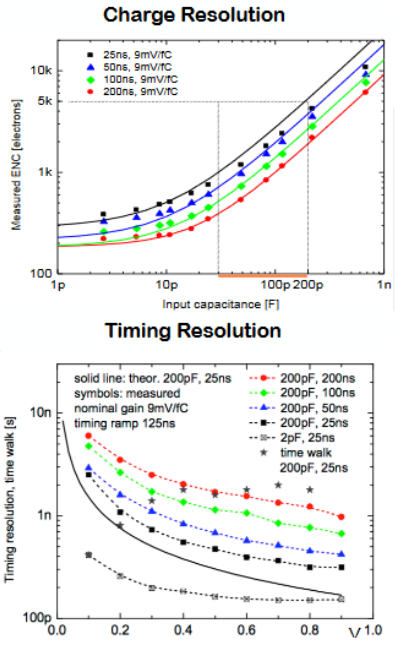


Fig. 2: Main Specification [4].

VMM can be operated in three different modes (literally from [6]):

- *Two-Phase Analog Mode (external ADC)*

In two-phase (analog) mode which is the mode originally implemented in the VMM1, the ASIC operates in two separate phases: acquisition and readout - During the acquisition phase the events are processed and stored in the analog memories of the peak and time detectors. As soon as a first event is processed, a flag is raised at the digital output. Once the process is complete the ASIC can be switched readout phase. The first set of amplitude and time voltages is made available at the analog outputs. The address of the channel is serialised and made available at the digital output using six data clocks.

- *Continuous (digital) Mode (internal ADCs)*

In this mode the peak and time detectors convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC respectively. The 10-bit ADC provides a high resolution A/D conversion of the peak amplitude in a conversion time of about 200 ns. The 8-bit ADC provides the A/D conversion of the timing (measured using the TAC) from the time of the peak or the threshold to a stop signal. The counter value at the TAC stop time is latched into a local 12-bit memory. In the continuous mode the 64 channel digital outputs are available as well providing time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), or a 10 ns pulse occurring at peak (PtP) or the 6-bit ADC. The channel self resets at the end of the timing pulse, thus providing continuous and independent operation of all 64-channels. Thus, in continuous (digital) mode a total of 38-bits are generated for each event.

- *L0 Mode (ATLAS Readout mode)*

The event processing is done in the same way but the readout is different. Each channel has a Level-0 Selector circuit which is connected to the output of the channel's latency FIFO. The selector finds

events within the BCID window (maximum size of 8 BCs) of a Level-0 Accept and copies them to the L0 Ch FIFO. The data are available in the output which is running on IDLE K28.5 in two data lines and can be readout DDR at a speed of 640Mbps (160MHz clock tested, effective bandwidth 560Mbps due to 8b/10b encoding).

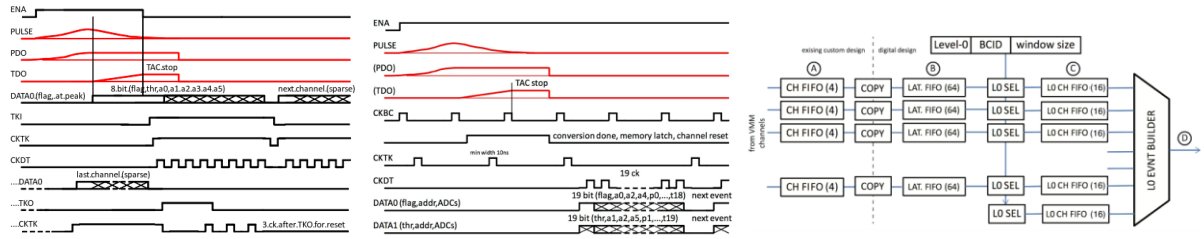


Fig. 3: VMM Operation Modes: Two-Phase Analog Mode – left, Continuous (digital) Mode – center, Lo Mode – right.

2.1.2. VMM 128 & SRS Interface

A schematic description of the SRS-VMM interface is sketched in Fig. 4. The full chain from the FE ASIC VMM (VMM RD51 hybrid) until the control and DAQ PC is shown.

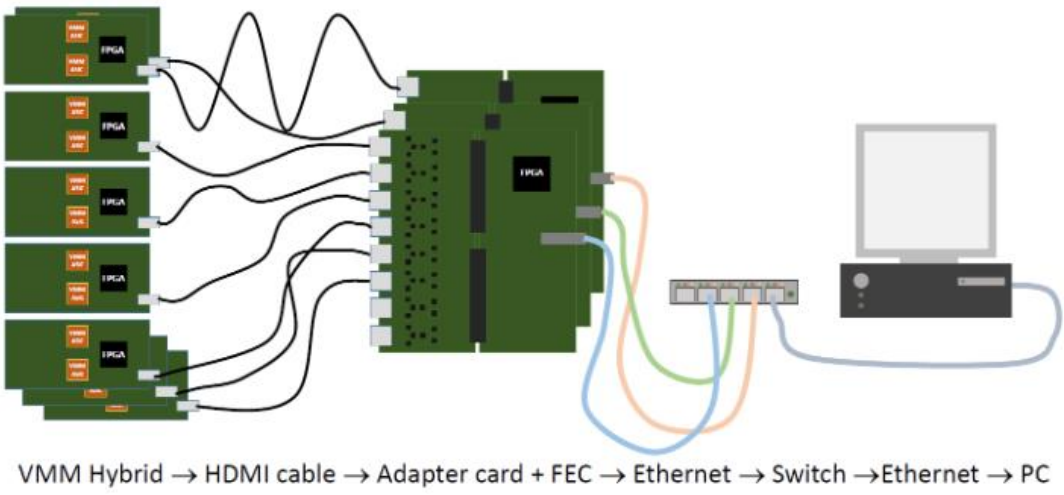


Fig. 4: Basic VMM and SRS system [5].

Specifically, the system is made of:

- **VMM Hybrid (RD51 VMM Hybrid):** the hybrid hosts two VMM chip. The total number of channel is 128. A proper input protection circuit is implemented on the hybrid to protect it in case of sparks. One FPGA is present to control the chip and organize the data transfer. ADC are present to read the analog test output of the VMM.
- **Adapter Card (DVM CARD):** SRS card specific to the reading of the VMM. In the case of the APV25, the interface card, namely called ADC Card, was digitizing analog signals from the APV25 itself. For VMM this card is "simply" routing the digital lines coming from the hybrid to the FEC. It provides power to the chip.
- **Front End Concentrator Card (FEC):** SRS common Front-End Concentrator. It takes care of the interface between the FE side and the PC side.
- **Network Switch:** necessary for systems with more than one FEC. For single FEC, direct connection to the PC is done.

- **Control & DAQ PC:** PC used for system control (FEC and Hybrids FPGA registers), data acquisition and online monitoring.

Connections and cables:

- **Hybrid-DVM CARD:** HDMI cables
- **FEC-SWITCH/PC:** Ethernet Cables

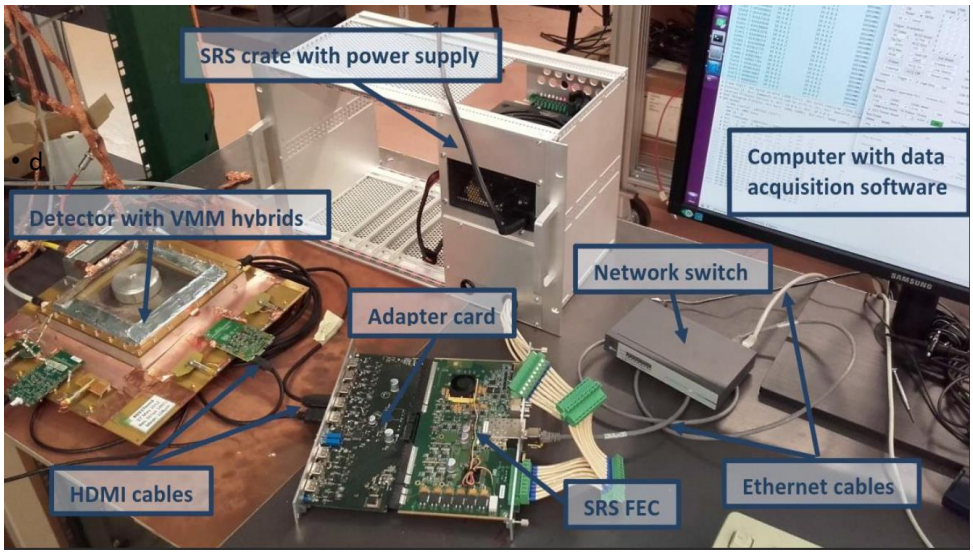


Fig. 5: SRS and VMM system mounted on a micromegas detector [5].

In Fig.5 a picture of a running system in the CERN GDD (154/R-007) laboratory is shown.
FEC and adapter card (DVM CARD) has been taken out of the SRS Crate for taking the picture.
The system is connected to a micromegas based detector.

2.1.3. VMM 128 RD51 Hybrid

The RD51 VMM hybrid (PCB that is carrying the VMM ASIC) is undoubtedly the major achievement of this project. Based on the previous experience gained with the APV25, the VMM hybrid proved to be successfully working since the beginning. The block diagram of the hybrid is shown in fig. 6 while a picture of the hybrid itself is shown in fig. 7 (left). In the right part of fig.7 the new HRS connector installed on the hybrid is shown. It represents an important difference compared to the existing APV25 where the 130pin Panasonic connector has been used. Adapter cards will be produced in order to preserve compatibility of both hybrids (APV25 and VMM) to old or new detectors.

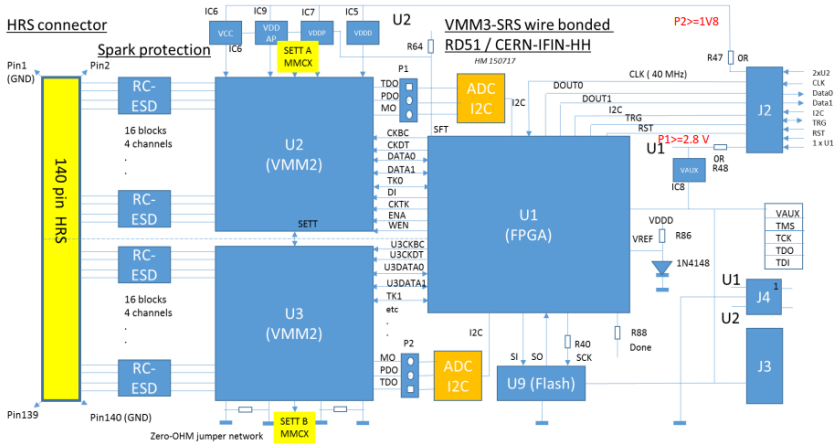


Fig. 6: RD51 VMM Hybrid Block Diagram [H. Muller].

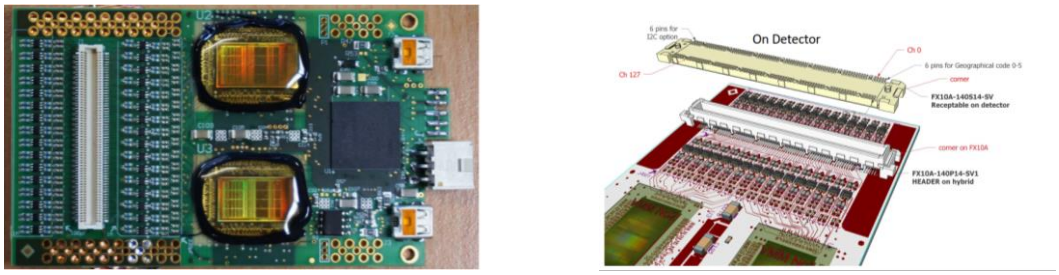


Fig. 7: Left: RD51 VMM Hybrid –VMM chips are wire bonded to the RD51 VMM hybrids. Right: 3d CAD and HRS connector.

The new connector should strongly improve the grounding of the chip, given the large number of ground pins and their distribution on the connector. Given the importance of grounding on noise reduction and spark protection, the proposed new solution should offer even better performances. The input protection circuit used with the APV25 has been modified for the new RD51 VMM hybrid. Fig. 8 and Fig. 9 show respectively the input circuit and the specification of the used TVS Diode.

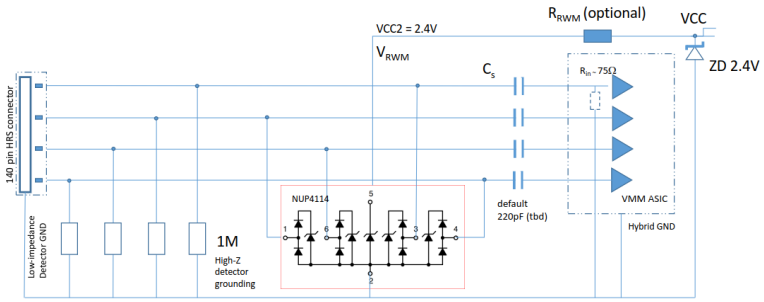
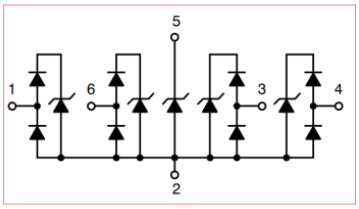


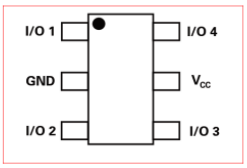
Fig. 8: AC coupling of the input and VMM protection circuit with TVS protection circuit NUP4114 [H. Muller].

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 1)			5.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, (Note 2)	5.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5.5 V			1.0	μA
Clamping Voltage	V_C	I_{PP} = 5 A (Note 3)			9.0	V
Clamping Voltage	V_C	I_{PP} = 8 A (Note 3)			10	V
Clamping Voltage	V_C	I_{PP} = 1 A (Note 4)		8.3	10	V
ESD Clamping Voltage	V_C	Per IEC61000−4−2 (Note 5)	See Figures 1 & 2			
Maximum Peak Pulse Current	I_{PP}	8x20 μs Waveform (Note 3)			12	A
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND			0.6	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins			0.3	pF



Key parameters
- Individual channels protected to GND only
- V_{RWM} = 2.5 V possible
- V_{clamp}(1A) = 8.3 -10V
- 0.6 pF per I/O
- Leakage current not specified below 1 uA
- air discharge safe +- 15 kV
- IEC 61000-4-4, 40A (5ns/50ns)



SC 88 package

footprint

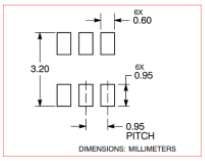


Fig. 9: TVS Diode array NUP4114 (same as APV25 RD51 hybrid with revised internal connection). [H. Muller].

2.1.4. DVM CARD

The DVM adapter card shown in fig. 10 is the SRS card specific to the VMM ASIC. It will interface Hybrid and FEC. The role played by the card is quite simple given the fact that the VMM outputs are already digitized. Its role in the powering system is instead crucial. Eight HDMI ports are available to power, control and read VMM hybrids (128 channels each). In the simplest configuration, a FEC/DVM system will be able to operate 8 VMM hybrids. This schema is sketched in fig. 11. For small setups, typically laboratory setups with a single detector tested (up to max 1k channels), the connection shown in fig. 11 will be enough and no additional hardware is needed. The simplest configuration is not suited instead for long (>5m) cables and larger number of channels. The Powerbox module that will be presented in the next section will be needed.

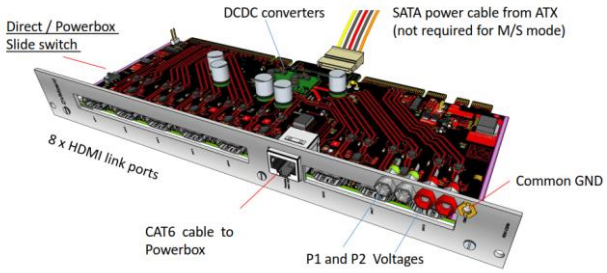


Fig. 10: Left: 3D CAD of the SRS DVM Card [H. Muller]. Right: A DVM card (card on the right) connected to the common SRS FEC(left card) [5].

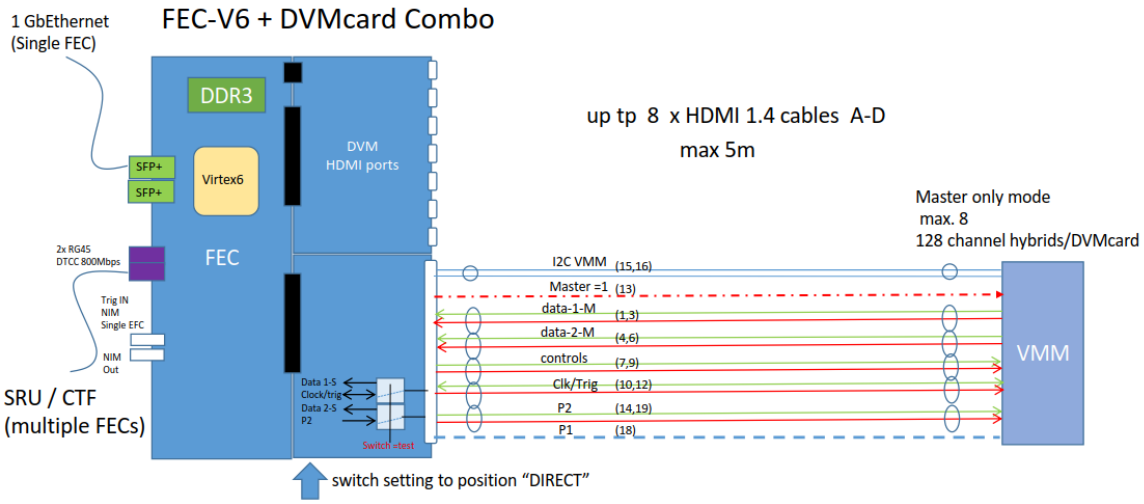


Fig. 11: Direct short VMM connection to the DVM card (master mode only). This configuration will allow the reading of 8VMMs per FEC at maximum 5m of distance.[H. Muller].

2.1.5. Powerbox

Limitations linked to the simplest system configuration (fig.11) come from the power consumption of the VMM. With the Powerbox it will be possible to supply the chips, without using the power line from the DVM through the HDMI cables. The schematics of this box are shown in fig.12. Fig.13 shows a sketch of the integration of the box in the system.

A first prototype of the Powerbox has been built and tested and it will soon be available together with all the rest of the hardware.

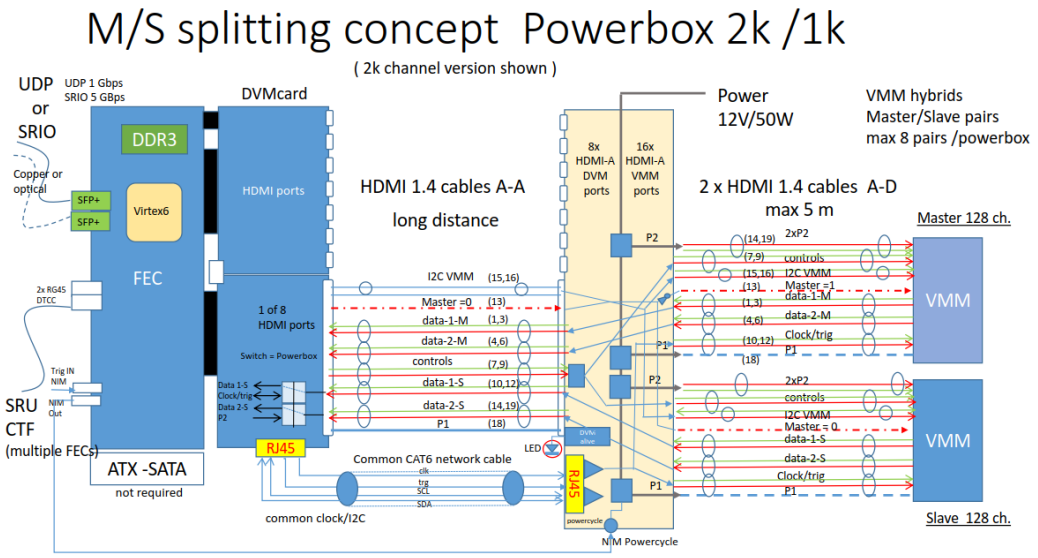


Fig. 12: Master/Slave splitting concept through the use of a Powerbox that will be used to supply power to the chips and to transfer signal and control lines.[H. Muller].

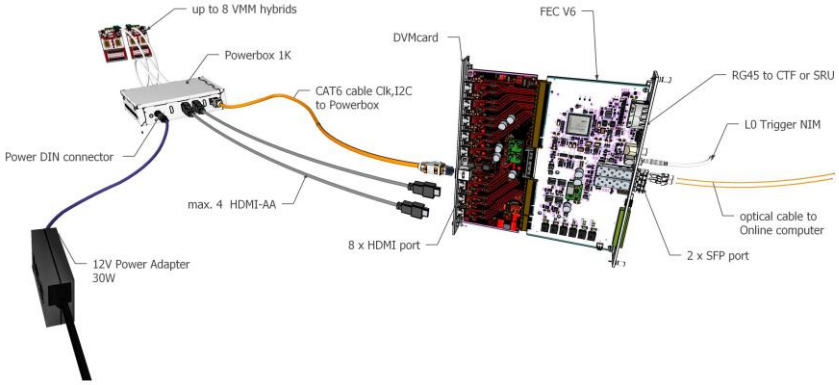


Fig. 13: Powerbox uplink to DVM-FEC Combo [H. Muller].

2.2. FIRMWARE AND SOFTWARE

In parallel with the hardware development, a large effort has been devoted to the firmware and software development. Important contributions came from different groups, in particular from ATLAS NSW (G. Iakovidis, S. Martiou), GDD/ESS (D. Pfeiffer, M. Lupberger) and ESS software development groups.

2.2.1. Firmware: status and future upgrades

The firmware development is done mostly at two levels: the FPGA on the hybrid and the FPGA on the FEC. S. Martiou has developed the core of the existing firmware for FEC and for VMM hybrid. With the existing version a standard test of the chip and real data taking is possible.

M. Lupberger and other collaborators took the original firmware and did several implementations to optimize certain aspects of the readout chain. One example is the optimization of the data transfer rate. Several applications need indeed to exploit the full readout speed capabilities of the VMM chip. Different hardware configurations are currently under evaluation to optimize the available bandwidth. All these developments will proceed in parallel with firmware upgrades.

All these developments are publically available.

2.2.2. Control and DAQ software

Control and data acquisition software have been developed starting from the work done by the ATLAS NSW team. Fig. 14 shows the main panel of the software developed by G. Iakovidis (BNL/ATLAS) used to control VMM chips and to control the data acquisition [8].

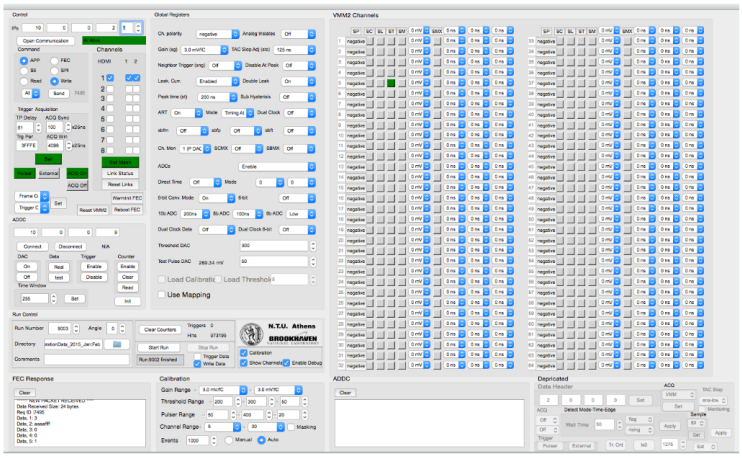


Fig. 14: Control and Data acquisition software developed by the ATLAS/BNL team [8].

2.2.2.1. Slow Control, Data Acquisition and online monitoring

Based on the ATLAS version, a new software has been developed. Preserving all the functionality of the original one, the new version has been designed in order to simplify the procedure linked to our specific use of the VMM chip. The operation of multiple chips and multiple FECs is for instance one of the additions made to the original version of the software.

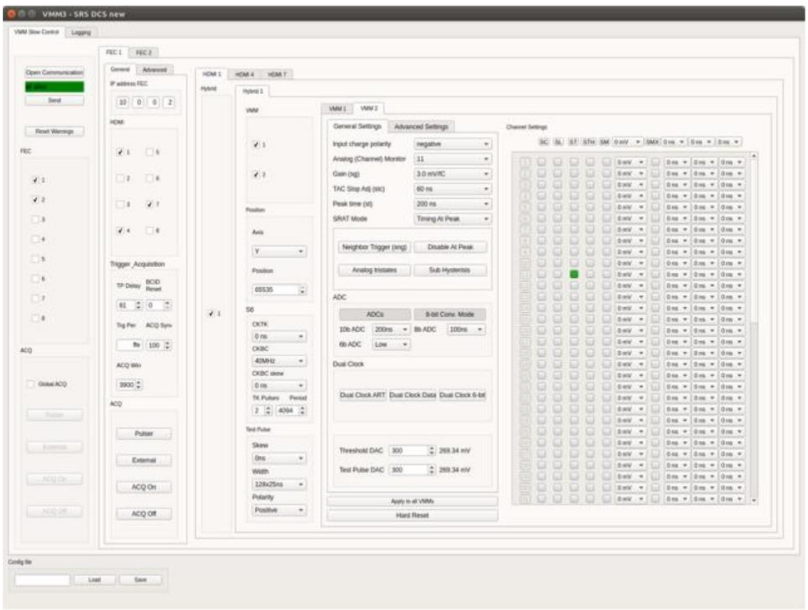


Fig. 15: VMM3 SRS DCS software. (2017 CERN Summer Student Project M. Guth) [5].

Data taking preserves the typical UDP package transmission of the SRS. Because of this all the previous software available in the SRS context can be used with minor changes. Tests with the ALICE DATE DAQ showed for instance full transparency of the SRS to the specific chip. Lighter DAQ software has been developed in addition to the existing one. ESS team did a Kafka based DAQ.

Concerning the monitoring tools, two codes coming from the ESS team are shown in fig.16: Wireshark plugin for Ethernet data monitoring and online data monitoring (detector geometry included).

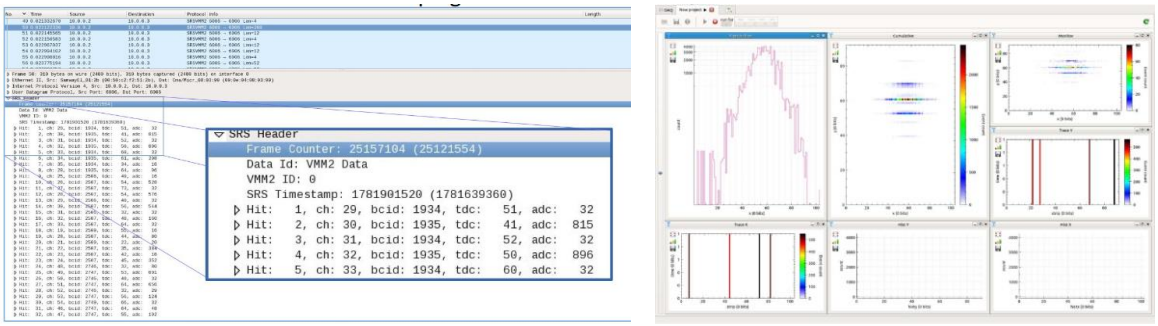


Fig. 16: Wireshark plugin (left) for online data check and online monitoring (right) from ESS software team [5].

2.2.3. Analysis Software

D. Pfeiffer of the GDD/ESS team and L. Bartels (2017 CERN summer student Project) developed several analysis routines and software that can retrieve all the information provided by the VMM and that link the chip readout to the detector geometry.

2.3. CONCLUSION AND FUTURE DEVELOPMENTS

Hardware-wise, prototypes of all the components have been developed, produced, interfaced and tested. A working setup is currently available at CERN (GDD/RD51 laboratory). RD51 VMM hybrid and DVM cards are at their final release and are ready for the first production. These components are available and covered via a not exclusive licence agreement between CERN and the CERN spin-off "*SRS Technology"*. Standard parts of SRS are available through the CERN store. Preparation of a few pilot systems is ongoing and they will be available for firmware and software developers and for interested users. On the firmware and software parts, we achieved good progress as well. All the different levels (firmware, slow control, DAQ, online/offline analysis) have been covered. Everything is open access and available to interested groups. The SRS VMM project will continue in the context of RD51 and in ESS. It will represent the main line in the development of a common readout system for detector R&D.

Procurement of the SRS/VMM system is accessible via:

- **CERN Store:** FEC, mini crate, SRS standard components.
- **SRS technology:** RD51V MM hybrid, DVM-Card, Power Box.
- **SAMWAY:** FEC

Groups without a CERN team account can access the hardware components available in the CERN store through KT.

3. TIMEPIX3 AND SRS

3.1. OBJECTIVES

The aim of this subtask is to support the activities focused on the interface of TIMEPIX3 with the SRS. The main goal is to develop an easy-to-use system to readout the TimePix3 ASIC within the SRS framework. In order to reach this goal, the following hardware and firmware components have to be specified and developed:

- TimePix3 Chip Carrier (CC)
- Intermediate Board (IB)
- Intermediate Board Firmware
- PC-based Control Software
- Cable connection between CC and IB

The CC should be easily adaptable to different detectors. Hence it needs to be simple and small with as few components on it as possible. The connection to the Intermediate Board (IB) will be made either by a high-density board-to-board connector, or via cable (e.g. DisplayPort) if non-radiation hard electronics need to be distanced from the detector itself. The IB itself shall contain a Zynq SoC with an integrated FPGA, meaning the slow control can be achieved at high speed by System-on-Chip (SoC) with an integrated FPGA. The IB then connects via DisplayPort or optical fiber to the FEC card, where the data and the slow control information are processed, timestamped and then sent to the PC via Ethernet.

On the PC side, a daemon is running which provides an Application Programming Interface (API) to interact with the IB. This API allows processes for different purposes to connect, e.g. a DAQ and / or slow control client, a live event display, online pre-analysis, etc. Following such a server / client model, provides cleaner software design for easier maintainability, compared to a single piece of software. This is especially important to support different detector designs and applications of the Timepix3, without the need to maintain potentially diverging branches of one software platform.

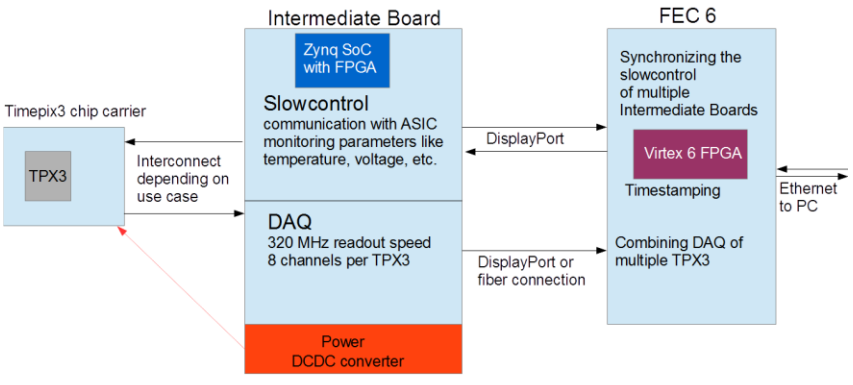


Fig. 17: Block diagram of the Timepix3 SRS readout.

3.2. STATUS

For the design of the IB the following items have been studied:

- For the Intermediate Board design, a System-on-Chip (SoC) with an integrated FPGA has been evaluated as Slow-Control processor, since Microcontrollers as previously used are not suitable due to IO-Speed restrictions.

For the IB firmware several design decisions have been taken:

- DAQ and Slow-Control parts to be separated. This results in less cables to interconnect between FEC6 and IB and makes it possible to check and send slow-control parameters independently of DAQ;
- The Ethernet core for the communication of the IB with the FEC is nearly finished.

For the PC-based control software the following items have been designed:

- DAQ / TPX3 control server running in background providing API which can be connected to a Command Line Interface (CLI) or a Graphical User Interface (GUI) for detector control;
- Data storage in HDF5 format;
- Purpose specific tools, e.g. live event display, on the fly data analysis etc. to be connected to the API.

Due to manpower limitations the project is proceeding slower than anticipated. An experienced electronics engineer has recently been assigned to the project. System design is expected to be finalized by Q2/2018. The production of the hardware components and the system test is expected to be finished by Q4/2018.

4. GEMROC AND SRS

Within the scope of gas detector (especially GEMs) readout, a dedicated ASIC for imaging application has been design in AGH [9]. In the context of the RD51 Collaboration, there is an interest to interface the GEMROC ASIC with the SRS system. The SRS system is widely used within the community therefore having the opportunity to use another ASIC is very appreciated. Moreover a new ASIC developed recently in AGH (e.g. GEMROC2) [10], which has a compatible interface with the GEMROC, can also benefit using the same connection system to the SRS. The AIDA-2020 support has been used within this perspective.

4.1. HARDWARE

This section describes the hardware of the SRS/GEMROC system. Description of the components needed to make the interface are given, as well as the introduction to the GEMROC ASIC will be provided. However, the AGH GEMROC report does not refer to work done in this project.

4.1.1. GEMROC ASIC

"The GEMROC ASIC consists of 32 independent channels, allowing for simultaneous recording of the amplitudes and time of incoming signals. Thanks to the implemented token-based read out of de-randomizing buffers, the ASIC also provides data sparsification and full zero suppression. Reconstruction of the hit positions is performed in an external FPGA based data acquisition system by matching the time stamps of signals recorded in X- and V-strips. The amplitude information is

used for finding centres of gravity for clusters of signals on neighbouring strips belonging to the same detection events. Such a readout architecture provides capability of working with high count rates up to $l0^6$ /s.

The circuit has been designed in O.35 um CMOS process. The basic functionality and parameters have been evaluated using the testability functions implemented in the ASIC design. A fully equipped GEM detector module has been built and tested with X-rays and electrons from radioactive sources." [9]

The GEMROC architecture is shown in Fig. 18 and the main characteristics are presented in Tab. 1.

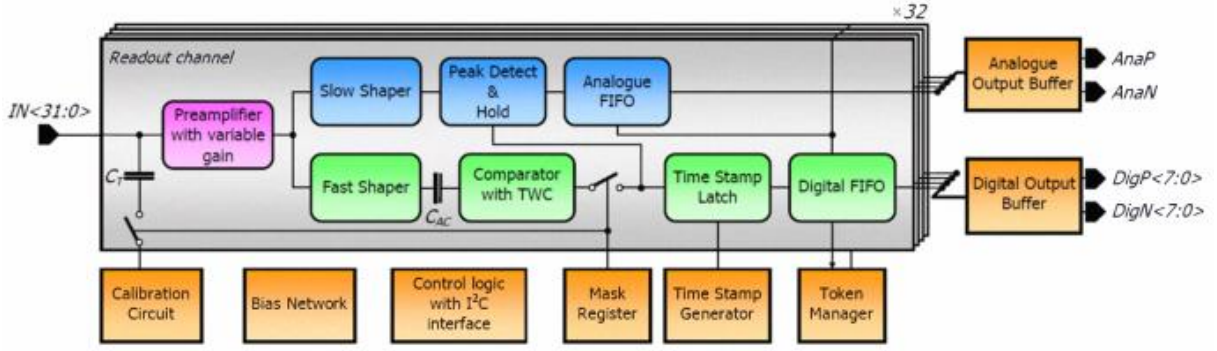


Fig. 18: Architecture of GEMROC ASIC [9].

Tab. 1. Main specification parameters of the GEMROC ASIC.

Input Signal Polarity:	Negative (electron collected) and positive.
Gain:	3 mV/fC (low gain) or 6 mV/fC (high gain)
Rise time:	20 ns in response to δ-like input charge signal
Crosstalk:	< 3% for detector inter-strip capacitance of 60 pF
Fast shaper (for time):	40 ns in response to δ-like input charge signal
Slow shaper (for amplitude):	40 ns in response to δ-like input charge signal
Input clock:	125 or 250 MHz
Slow control:	I2C

A block diagram of the GEMROC ASIC is shown in Fig. 18. Preamplifier output is split into two sub-channels, allowing separate signal-to-noise ratio optimization for time and amplitude measurement (see shaping times presented in Tab. 1.). The discriminator output signal from timing sub-channel is used to latch 12-bit time stamp of either 4 or 8 ns resolution (according to the input clock) and to enable the Peak Detect and Hold in the energy sub-channel. The digital information (time stamp) and analogue signal amplitude are stored inside dedicated FIFOs. The token-ring based readout schema is used in order to extract the data from the ASIC. The digital format of the data frame is shown in Fig. 19. This data frame is readout simultaneously with the analogue amplitude of the signal, which is sent to the external ADC for digitization [9], and then merged together in the FPGA.

Frame\Bit	7	6	5	4	3	2	1	0
0	DV	TS13	TS12	TS11	TS10	TS9	TS8	TS7
1	0	TS6	TS5	TS4	TS3	TS2	TS1	TS0
2	0	0	0	ID4	ID3	ID2	ID1	ID0
3	0	0	0	0	0	PU	OF	P

Fig. 19: GEMROC digital data frame format.

The ASIC is self-triggered, provides intrinsic sparsification and full zero suppression. It can work in two modes: “normal” when the measurement is performed and signals are recorded on the inputs and in the “test” mode. The test mode is used for testing and calibration of the ASIC. The internal calibration circuit allows, among other things, to trim the threshold levels of each channel making them equal.

4.1.2. GEMROC & SRS Interface

To make the GEMROC ASIC compatible with SRS a dedicated hybrid hosting the ASIC has to be used. The GEMROC hybrid has already been develop at AGH, together with a dedicated FGPA based readout system. The concept is working well as described in [11]. The two GEMROC ASICs sitting on a hybrid are readout by a FPGA. The timing and channel coordinates are readout directly, however the signal amplitude is digitized by the fast ADC and the data then is sent to the FPGA. Inside the FPGA the coordinates and amplitude informations are merged and then packed into UDP frame which is transferred to the PC using a Gbit Ethernet interface.

In order to separate the work in well-defined tasks, as a first step for development of the GEMROC & SRS interface an intermediate solution is proposed. The interface board which connects GEMROC hybrid and SRS was developed. The block diagram of the board is presented in Fig. 20.

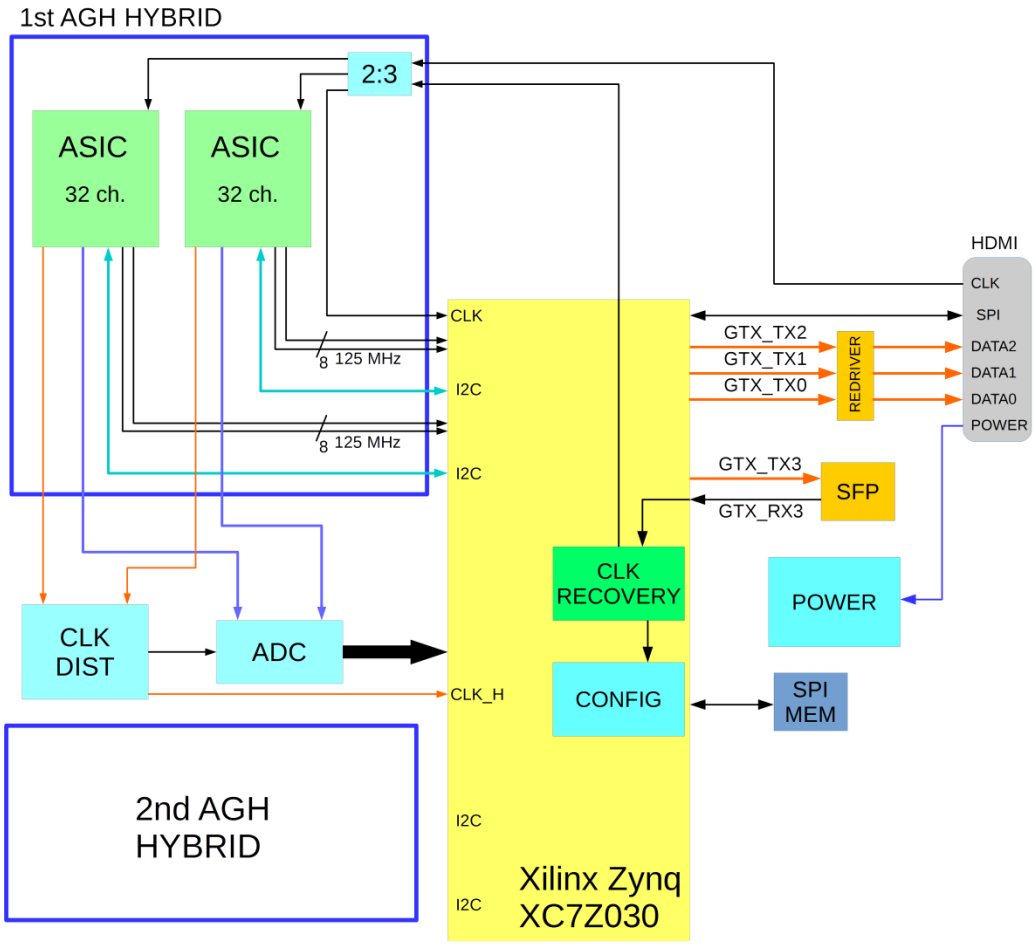


Fig. 20: Block diagram of the GEMROC & SRS adapter board.

The adapter boards can host up to two GEMROC hybrids. A configurable clock distribution to/from hybrids and to the FPGA is present. The clock distribution allows fine delay tuning. The board can use the clock provided by the ATCA blade via the HDMI connector or a recovered clock via small form-factor pluggable transceiver (SFP). The analog sampling of the signals coming from the hybrids is done with a 4-chanel, 12-bit ADC.

The idea of having the interface between the existing GEMROC hybrid and the SRS gives an opportunity of using the ASIC in a more efficient way. One has to remember that the number of produced GEMROC ASICs is only about a hundred, so saving as much GEMROCs as possible for later usage is a must. The GEMROC hybrids can be tested and verified within the existing readout system and after that used for testing with the interface board together with the SRS system. In this stage usage of the more expensive components (like FPGAs and ADCs) is also more efficient.

The handling of the digital data is done directly by a dedicated FPGA, which in addition makes a serialization of the data to be sent to STS. The FPGA is also responsible for the GEMROCs slow control configuration via I2C interface. The prototype interface board has been produced and is under test. The board is shown in Fig. 21.

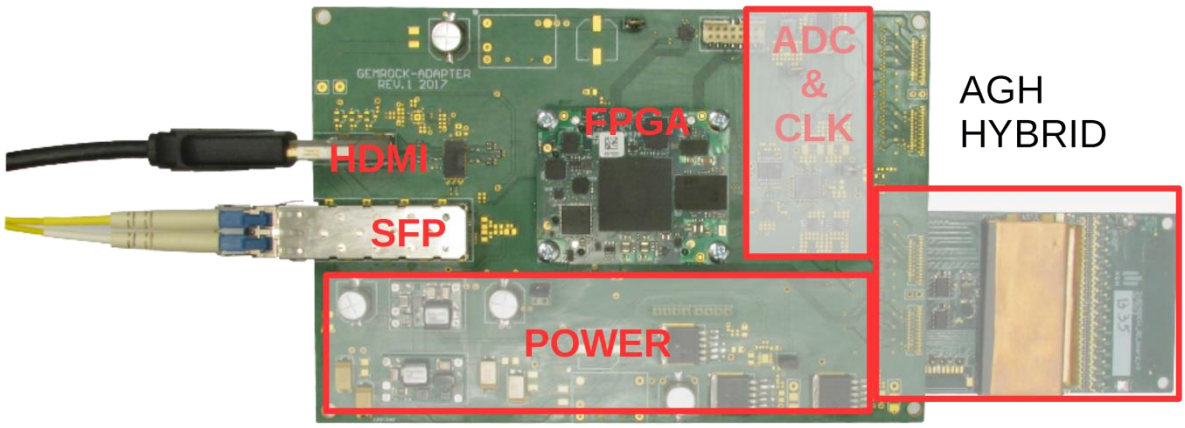


Fig. 21: Photograph of the GERMOC & SRS interface card.

The board design provides two readout channels:

- HDMI (3x MultiGigaBit link, only transmitter)
- SFP (1x optical link, transmitter and receiver)

Such a structure will allow to evaluate all possible interface types to SRS-ATCA, including:

- evaluation of total bandwidth, which can be achieved using HDMI cables
- evaluation of minimum bandwidth needed for efficient GEMROC readout

Single GEMROC chip generates:

- 1 Gbps digital data stream (8 bit bus x 125 MHz clock),
- 0.375 Gbps analogue data stream (12 bit ADC x 31.25 MHz clock)

This gives in total 5.5 Gbps required data stream from the test board (not taking into account zero-suppression and other data reduction modes) to the base system.

As previously mentioned, two readout schema are foreseen.

In the first schema, data can be fed in via HDMI connector at rates of ~2 Gbps. Integrated high-speed re-driver buffer are used to improve signal properties. This interface requires a special adapter board on the SRS-ATCA carrier blade. ATCA blade with this interface is shown in Fig. 22 with only 2 HDMI connectors and only 6 MultiGigaBit transceivers equipped.

In the second schema, an optical link is used. With a rate of ~6 Gbps to stream the data, a direct connection to one of the 10 Gbps interfaces on the SRS-ATCA ERTM-101 board is possible. With data suppression, ERTM-100 with 14 SFP interfaces can be used.

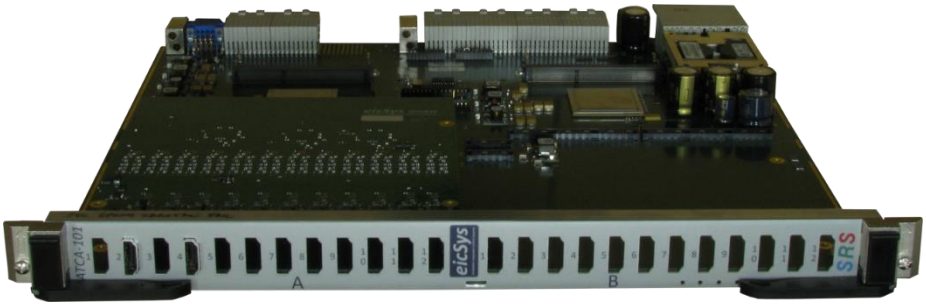


Fig. 22: Photograph of the ATCA blade with 2 HDMI connectors connected to MultiGigaBit receivers.

With SFP interface, the data stream will contain:

- commands to hybrids,
- board configuration (clock selection, delays, reset, etc.)
- a clock signal coded into incoming data stream

Fig.23 shows the tested hardware configurations. GEMROC adapter board connected via HDMI cable to EATCA-101 blade and via SFP to ERTM-100. In the first case, a simple adapter HDMI to MGT has been used in the mezzanine module. Data are sent via HDMI and via fiber to the same ATCA blade. FPGAs on the ATCA blades process incoming data and send the data over Ethernet to the host PC. Data is processed in 2 stages:

1) Xilinx Zynq combines on the adapter board digitized analog data and digital data into one stream when the SFP is used. When the HDMI is used, Zynq produces 3 data streams.
2) Virtex6 on the ATCA blade receives data stream(s) and builds UDP frames, compatible with ALICE DATE DAQ – from that point onwards the standard, known DAQ software is used

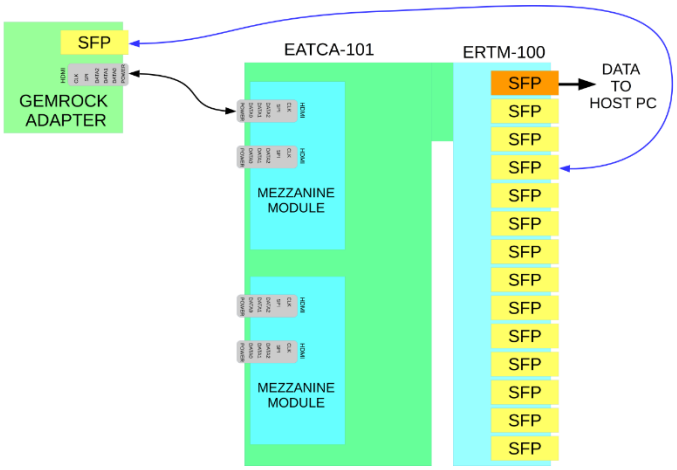


Fig. 23: Photograph of the GERMOC & SRS interface card.

4.1.3. GEMROC ASICs based readout system

Currently a few fully featured readout systems employing the GEMROCs are available in AGH Kraków for testing and measuring their performances. A sample result obtained with one of the system can be seen in Fig. 24, where a screenshot of the readout software main application window with the actual reconstructed data in a 2D histogram form is depicted. Moreover, very many results have already been presented in publications (e.g. [12]) and during the RD51 Collaboration meetings. Tests with the SRS readout system have started and first results prove that it is possible to adapt the GEMROC readout to the ALICE DATE DAQ.

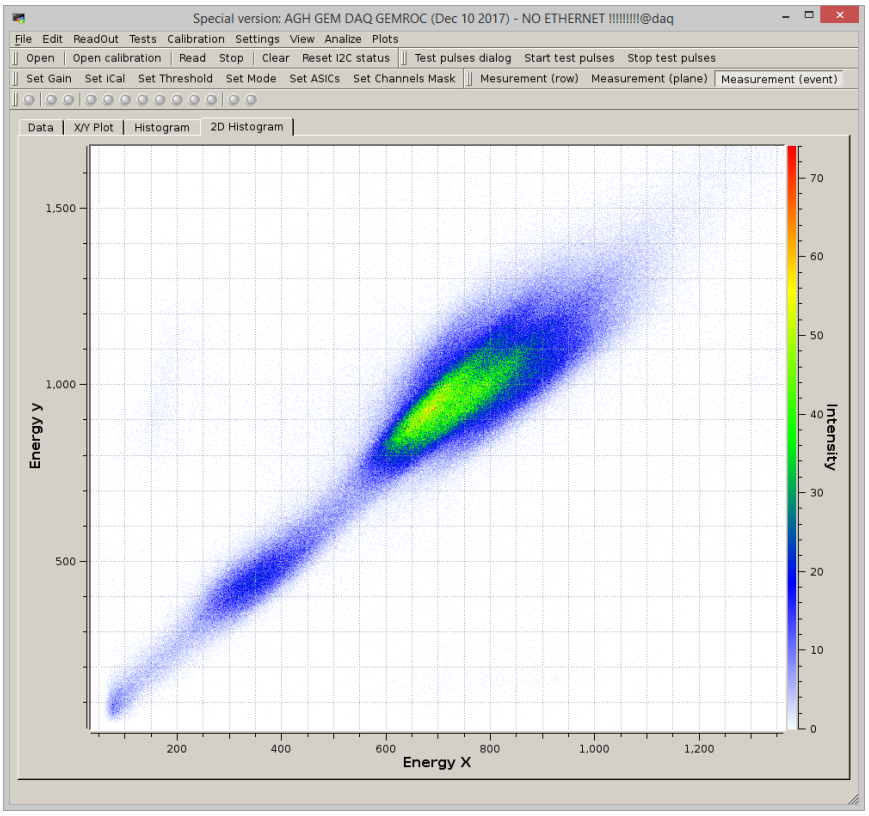


Fig. 24: Screenshot of the GEMROC readout system control software.

4.1.4. Conclusions

Firmware and software developments are ongoing. Quite a few firmware and software components will be taken from the existing readout system to speed up the development process. The originally planned HDMI connector (interface between SRS and GEMROC) limits the number of hybrids that can be connected to one ATCA blade. Discussion on future options is needed.

4.2. FUTURE PLANS AND INTERESTED COMMUNITY

The GEMROC-based readout system is available in AGH Kraków and the GEMROC & SRS interface board is ready for evaluation. Further developments (design and build a dedicated GEMROC hybrid which can be directly readout by the SRS system) can be done if there is explicit interest in the community. The GEMROC FE ASICs, hybrids and interface board are publically accessible to the community.

A new improved version of the ASIC called GEMROC2 has been developed in AGH. A key feature of the GEMROC2 is having 64 channels (instead of 32 for GEMROC) which allows to directly connect each detector readout strip to the ASIC's input channel (without grouping the channels into pairs). Having in mind that the GEMROC2 has a similar back-end interface to the GEMROC one eventually will be able to use it with the SRS system directly.

The firmware for the GEMROC-SRS readout is still under development, in particular to be used via the ALICE DATE DAQ software. Either integration or a separate software code has to be developed. Given the fact that the RD51 community is planning a migration to new DAQ software, these developments are not considered crucial in the context of the project.

5. CONCLUSION AND ACKNOWLEDGMENTS

Milestone MS83 describes the activities carried on interfacing the SRS DAQ system with different FE ASICs. Three different front-end ASICs have been covered: VMM, TIMEPIX3 and GEMROC. In the case of the VMM, being this ASICs the future FE readout baseline for the MPGD/RD51 community, the goal was to complete a full integration. The results are more than satisfactory and the system will soon be available to the community. In the case of TIMEPIX3, the activity is following the successful results with SRS & TIMEPIX for LC-TPC. The AIDA-2020 support was meant to be used as support for the ongoing process of integration. Final integration is expected in the coming years. In the case of GEMROC, the main goal was to achieve the proof of concept for the system compatibility. Proper adapter cards have been developed. The current GEMROC interface has been developed for the ATCA version of the SRS, currently produced in eicSys. Future developments are possible (migrating eventually to a new version of the GEMROC ASIC) if users show an explicit interest in the chip.

In the context of the VMM128 interface to SRS, we acknowledge all the precious support received from the ATLAS NSW micromegas group and from the ESS European Spallation Source teams.

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ANNEX: GLOSSARY

Acronym	Definition
SRS	Scalable Readout System
FEC	Front End Concentrator
DVM	Digital VMM Module