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Pixel detector bias supply and control using embedded multicore processors

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Abstract

The aim of the project is to create a software controlled, open source, low footprint and low power high voltage bias supply and current monitor for a pixelated radiation sensor. The solution is based on the LT3905 integrated circuit and the multi-core XMOS xCore 200 microcontroller and it is intended to be used in a battery powered, mobile platform for educational settings.

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1 Introduction

1.1 Context

Since the properties of silicon with respect to the interaction with radiation are favourable and well known, many silicon based detector schemes were developed over the second half of the last century (Rossi et al. 2006, 13). The development of silicon based electronics lead to the appearance of silicon pixel sensors and corresponding readout electronics.

Bump bonding (Rossi et al. 2006, 203) a pixelated silicon sensor with readout electronics is called a hybrid pixel detector. Such detectors were developed by the CERN/Medipix collaboration. Timepix3 is the latest edition of the ASIC readout electronics for a pixelated silicon sensor, which is bond together with a silicon sensor.

These hybrid pixel detectors were developed mainly for medical and particle physics applications with high data rates and high power consumption. The Timepix3 readout is capable of measuring time of arrival and time over threshold for each pixel (Poikela et al. 2014), thereby allowing the fast pixel by pixel evaluation of the energy deposited by the radiation hitting the reverse biased silicon sensor allowing it to be deployed in radiation imaging applications.

One pixel of a reverse biased silicon sensor is similar to a reverse biased diode (Poikela 2015, 5) requiring a controlled high voltage supply.

The aim of this project was to aid the implementation of such a sensor in a mobile application by developing a software driven low footprint and low power high voltage supply

controlled from the multi-core microcontroller used for the pixel data readout to bias the silicon sensor.

1.2 Importance of the project - portability

While FPGA based electronics typically using an off the shelf high voltage supply to be connected to a hybrid pixel detector such as the Timepix3 exist (Visser et al. 2015) and (Turecek et al. 2016), these are suited to high data rate applications to be used in high radiation environments, for instance in medical applications and particle accelerators and detectors.

The project of which this masters is a part of is to create an educational purpose low speed, open source, low cost and low power readout to enable portability and battery powered operation in laboratory and outdoor settings.

1.3 Novelty

Such a low footprint and low power consumption detector could be used for in mobile applications, for instance in visualizing radioactivity in an augmented reality application such as in the iPadPix project (Keller et al. 2016).

Adding low power control electronics enables more power to be used in the hardware acceleration for the data processing required by the application, which could be achieved by using the parallel processing features of the XMOS xCore 200 multi-core microcontroller (XMOS 2015), thereby allowing faster response times and ultimately contributing to better user experience.

Using the XC based XMOS programming environment has the advantage of relatively easy extension of the project with readily available mostly BSD style licensed libraries, which allow the source code of the project to be publicly published (XMOS n.d.).

The high voltage supply is implemented to comply with the safety requirements of the IEC 61010-1 (IEC 2010) standard having an accessible pixel sensor in a mobile application see figure 3. In order to keep the power consumption as low as possible while still keeping the uncertainty of the current monitoring within the advertised figures of the LT3905[1] even in the sub

[1] 2% within the whole temperature range.(LTCorp. n.d.)

μA range, a low footprint, software driven RC current measurement scheme is implemented to monitor the sensor current, which eliminates the need of using an external operational amplifier, provided the scheme is used for slow monitoring.

Furthermore the footprint of the proposed solution for the high voltage bias circuit is less than $2\,\mathrm{cm}^2$, therefore it can be implemented on a credit card sized board requiring less than 4.4% of the area of a single side of the board.

1.4 Summary

Implementing and evaluating a software driven, low power and low footprint high voltage supply for a pixelated silicon radiation sensor with an optionally dynamic range, multi-core microcontroller based current monitor is described in this report. The proposed circuit uses the LT3905 switched mode DC-DC converter and an XMOS xCore200 microcontroller. The high voltage supply is to be used with a mobile, education purpose application, for instance an augmented reality radiation visualizing device, such as the iPadPix (Keller et al. 2016).

2 Hybrid pixel detector and supporting electronics

2.1 A comparison of silicon pixel detector readout schemes

This section compares existing and proposed readout structures. One of the early readouts that could be compared to our design was developed for the Medipix detector chip that achieves a similar end, but the structure of the chip is significantly different to Timepix3 that has more features, namely time over threshold and time of arrival measurements and a much better time resolution (Poikela 2015). However, in terms of the slow control electronics around the detector chip: the high voltage bias supply and the control electronics requirement is very similar, therefore it is worth comparing the different solutions despite the difference in the integrated detector circuits.

Given that the requirements to bias a silicon pixel detector are similar to the requirements of biasing avalanche photodiodes for optical transceivers requiring a low noise high voltage

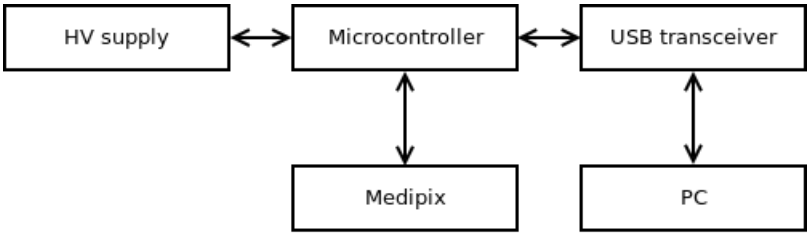

Figure 1: Functional block diagram of a USB readout for the Medipix chip - based on (Vykydal et al. 2006).

supply. Therefore, relevant building blocks of circuits are going to be studied briefly in this section.

The schematic for a prototype readout (Vykydal 2005) shows that this detector uses an amended reference design of the MAX1932 bias supply as a high voltage supply and has an USB transceiver to be connected to a PC. To complement the discrete circuitry and achieve software control, a separate microcontroller was added. This also served as the main device to read the data from the pixels of the detector chip. The functional block diagram can be seen in figure 1.

If adapted to be a board without an enclosure on which the components could be accessed, certain MAX1932-based solutions would not meet the safety requirements of the IEC 61010 standard (see the MAX1932 part in section 3.2.1). Moreover, the LT3905 IC is half the price of the MAX1932, while the less external components are needed for a better current measurement.

Moreover an Ethernet interface is desired over USB, which would mean that the device could be connected to the network without the need of an additional PC. Besides the mobile application, there are more possibilities for the graphical user interface, too. Finally, using Ethernet means that it would be easier to develop and debug the data transfer from the Timepix3 readout electronics.

Replicating the typical structure of a performance chip readout (Turecek et al. 2016) and (Visser et al. 2015), an FPGA could have been chosen as our platform which could meet the requirements, except for perhaps the low power consumption and and low footprint requirement. An FPGA architecture would be the fastest and could utilise the theoretical maximum bandwidth of $5.12\,\mathrm{Gbps}$ of the Timepix3 chip. This scheme would offering flexibility without the need of connecting the detector locally to a PC. The first published prototype architecture

to test the chip used this structure (Poikela et al. 2014).

The main reason why this architecture was not chosen is that using commercial IPs on an FPGA would make the solution closed source as well as it would add complexity to operating the detector. In contrast, XMOS offers libraries with BSD style licences (XMOS n.d.). It is much easier to extend the XMOS system with existing C-based libraries for data encapsulation and on board cluster processing. Furthermore, given the needs of a typical educational application, high data rates are not needed, since the expected number of events from commercially widely available radioactive sources for education and natural background are low (Patrigiani et al 2016, 260) and (Patrigiani et al 2016, 291).

Our chosen architecture is closest to the FPGA solution, but the main difference is that it operates at a lower readout frequency of $40\,\mathrm{MHz}$ or $80\,\mathrm{MHz}$ (Poikela et al. 2014). However, since an integrated solution was preferred, a more powerful microcontroller with 16 logical cores would enable the required parallel processing for the data readout and chip control, while keeping the BOM costs low.

2.2 Bias power supply overview

Although there is the possibility of building a high voltage supply entirely from discrete components, the fact that sufficient low cost integrated circuits exist for this purpose rules out this option.

One alternative would be to use the MAX1932 DC-DC converter to create the high voltage bias and use external monitoring for the current consumption and the high voltage.

A solution similar to this is presented by Vykydal (Vykydal et al. 2006) and (Vykydal 2005). In order to measure the very low bias current (typically in the tens of nA range) an operational amplifier with a shunt resistor in a bridge measurement configuration is used and a differential measurement is made. The high voltage is divided down so the operational amplifier could be operated from a lower power rail, which is usually desired to avoid using high voltage operational amplifiers. Optionally the gain of the amplifier is set through a passive network to achieve a desired output voltage range. The voltage signal from this current monitor circuit is then sampled with an ADC.

However, as Williams points out (Williams 2002), this type of differential measurement puts an additional strain on the tolerance of the resistors required that increases the cost and in essence makes the design impractical using discrete components. Williams proposes several solutions to successfully overcome this problem including high side current and voltage measurements, however these solutions are complex and require many discreet components and extra operational amplifiers and converters.

Therefore a new approach to biasing a silicon radiation sensor is proposed, since the requirement that the solution should fit on an as small as possible area, preferably around $1\,\mathrm{cm}^2$-$2\,\mathrm{cm}^2$ on the board. This restricts the use of performance operational amplifiers. In addition, every added operational amplifier increases the power consumption, too.

An alternative would be to use a pre-packaged PCB mount high voltage supply such as the Iseg APS 200 PCB mount HV solution (Iseg n.d.). However, a lower ripple solution than this is needed for a lower voltage range see table 1. Despite the relatively small size, the device will have a much larger footprint: $8\,\mathrm{cm}^2$ than the proposed approximately $1\,\mathrm{cm}^2$-$2\,\mathrm{cm}^2$ LT3905 solution. The power consumption and the power output is much higher for such a device, which is not needed for our application.

The LT3905 offers a fully integrated solution with current monitoring capabilities, yet it offers flexibility to adapt the design to the needs of a hybrid pixel detector. This would fit on a lower board area and the bias noise characteristics are excellent, too. It would meet the demanding safety requirements of an accessible pixel sensor: see section 3.2.1. However, the design has to be adapted to our needs. Much of this report will concentrate on achieving this goal and integrating the solution with the XMOS controller used.

One challenge of this implementation is to lower the current monitoring capabilities of the LT chip down to the nA ranges, since the default range is $3\,\mu\mathrm{A}$ - $3\,\mathrm{mA}$, using a few external components only in order to limit the board area occupied (LTCorp. n.d.).

2.3 XMOS architecture

The XMOS xCore200 device is the chosen microcontroller to achieve the data transfer and control the high voltage bias. A block diagram of the XMOS architecture can be seen in figure

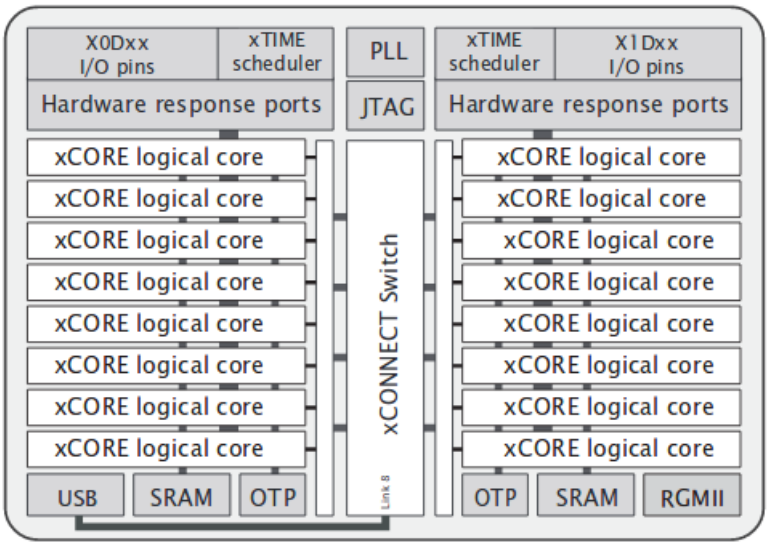

Figure 2: The two tiles having access to hardware ports are the actual physical processing cores on the XMOS microcontroller. These tiles are then divided into eight logical cores in this diagram. These cores are threads scheduled in a round-robin fashion with a predictable worst case performance. Figure 1 from (XMOS 2015, 2).

2.

The threads communicating using typed channels in this microcontroller are called logical cores (XMOS 2014). This scheduling is supported by hardware, therefore there is no need to run a separate RTOS. There is a minimum performance requirement that each thread has to abide by. Each thread is scheduled to execute with a virtual clock cycle of 1/nth of the actual clock cycle, where n is the number of the threads running with an upper limit per logical core.

This is the worst case execution time, since if one thread is blocked because, for instance, it is waiting for input data, then another one is executed earlier. Our chosen microcontroller (XMOS 2015) running at a clock of $500\,\mathrm{MHz}$ could be scaled from $100\,\mathrm{MHz}$ processing cores down to 16, $63\,\mathrm{MHz}$ cores. In our measurement setup (see section 5.2.1) 2 logical cores were used, which then would correspond to two conventional $100\,\mathrm{MHz}$ microcontrollers.

3 Specifications

3.1 Overall requirements

- To be deployed with a Timepix3-based pixel detector platform for education.

- Voltage range up to at least $50\,\mathrm{V}$.
- Compliance with IEC 61010-1.
- Small footprint area of 1-2 cm^2.
- Low power consumption in the mW range.
- Output ripple as low as possible in the low mV range.
- Monitoring and control using an XMOS processor.
- Current monitoring resolution such that differences between sensors are observable in $10\,\mathrm{nA}$ range.

3.2 Requirements for the HV supply

3.2.1 Safety

The IEC 61010-1 standard was applied. This is an electrical safety standard regarding instruments with accessible parts having a voltage (IEC 2010, 39), see figure 3. The requirements for the voltage of accessible parts is set in this standard. The D.C. level is deemed to be hazardous live in dry locations if it is above $70\,\mathrm{V}$ and either one of the following three statements is true. The D.C. current exceeds $2\,\mathrm{mA}$ for low frequency applications or $45\,\mu\mathrm{C}$ charge for up to $15\,\mathrm{kV}$ or $350\,\mathrm{mJ}$ stored energy above $15\,\mathrm{kV}$. This is implicitly suggested in the LT3905 datasheet (LTCorp. n.d.), too, in the form of limiting the size of the output filtering capacitor at $0.22\,\mu\mathrm{F}$ for applications above $25\,\mathrm{V}$, below that the datasheet recommends a $1\,\mu\mathrm{F}$ capacitor. (LTCorp. n.d., 10). In comparison it can be seen that one of the recommended MAX1932 solutions (Maxim 2015, 14) does not meet this requirement, since it uses a $1\,\mu\mathrm{F}$ capacitor at $90\,\mathrm{V}$ to filter the ripple, which would store a charge of $90\,\mu\mathrm{C}$ at nominal value. This is twice the allowed charge for the equipment not to be classified as hazardous live by the IEC 61010-1 standard, provided the parts are accessible. Should this be the case, the output ripple performance in the MAX1932's case should probably be sacrificed if the IEC 61010-1 standard is to be met by lowering the capacitance of the output filter capacitor. See table 1.

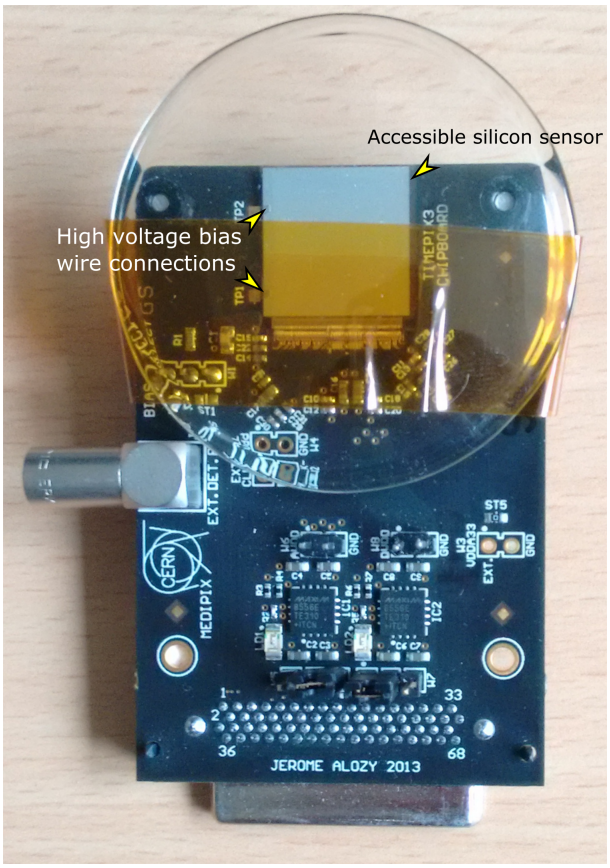

Figure 3: Timepix 3 chipboard designed by J. Alozy and provided by the CERN Medipix collaboration. The silicon bias is accessible, because it is supplied via wire bonding on the top of the sensor. Therefore the limitations of the IEC 61010-1 standard were adhered to.

Solution	Max. ripple (mV)
Keithley 2400 (200 V max)	5
Keithley 2410 (1000 V max)	20
Iseg APS, 0.5 W, 200 V max.	10
MAX1932 90 V max.	$<$ 1 - with $1\,\mu\mathrm{F}$

Table 1: Comparison of voltage ripple of different high voltage bias circuits used to reverse bias silicon detector chips.

A second condition was applied, which can in certain cases lower the production cost. The circuit does not require to be made on material of at least V-1 classified flammability rating if it is a limited energy circuit (IEC 2010, 100). Since in our application there was no real value in raising the voltage above $60\,\mathrm{V}$, the requirements were lowered to a maximum of $60\,\mathrm{V}$ output voltage and less than $2.5\,\mathrm{A}$ current which was met by the previous condition.

3.2.2 Ripple

Besides the safety aspect of the ripple, which means that the A.C. root mean square value is not advised to be more than $33\,\mathrm{V}$, with the maximum current rating of $2\,\mathrm{mA}$, this would also create a very poor D.C. bias. The requirements of biasing an avalanche photodiode require much lower ripple (Williams 2002).

As low ripple as possible was desired to meet or even exceed the performance of the existing solutions. See table 1. Our aim was to produce a ripple at least as low as the Keithley 2410 at our much lower output voltage, but on a much lower footprint. Therefore the minimum aim was to achieve a noise figure from the switching less than $5\,\mathrm{mV}$, but if possible we wanted to meet the ultra low ripple performance of $1\,\mathrm{mV}$ of the MAX1932.

3.2.3 Power consumption

Since the Timepix3's power consumption when designing a lower frequency readout should be well below the rated $2\,\mathrm{W}$, the bias supply should contribute to power consumption as little as possible, well below $0.2\,\mathrm{W}$. The output power of the supply is going to be low, since the silicon sensor is expected to draw less than $1\,\mu\mathrm{A}$. Which would mean a maximum output power of $60\,\mu\mathrm{W}$ at the maximum $60\,\mathrm{V}$. However, conversions in the low power output region are expected to be more inefficient due to the low duty cycles involved (Rogers 1999). This is

confirmed by the slope of the graph in the LT datasheet (LTCorp. n.d., 1) indicating 17% power conversion in the low current ranges and 36% in the higher current ranges.

3.2.4 Current monitoring and limiting

The current monitoring is required to establish the current consumption of the detector chip and to protect the device. As an addition it is useful to gain more insight into the power consumption of the sensor in different conditions. Although the Timepix can dissipate $2\,\mathrm{W}$ of power, therefore it can tolerate a fair amounts of current in a radiation environment our typical background or very low radiation type application would require much lower currents than the maximum rating. The currents are typically well below $1\,\mu\mathrm{A}$, in the $100\,\mathrm{nA/cm^2}$ range when operated at the full depletion voltage. The Timepix3 has an active area of $2\,\mathrm{cm}^2$, therefore a modern $300\,\mu\mathrm{m}$ thick silicon sensor should draw a current around below $200\,\mathrm{nA}$ (Kalliopuska et al. 2013).

3.2.5 Footprint

The final design is imagined for on a board that is compatible with a C.H.I.P. Computer compatible module (*CHIP (computer)* n.d.) to host an embedded linux processor and battery-based power management in addition. This restricts the final design to a size of a credit card for a mobile, pixel detector platform for education. Applications such as iPadPix (Keller et al. 2016), where a Timepix detector is attached to the back of an iPad mini, are intended to be upgraded with the final design. Therefore the HV supply should occupy as little as possible area. The prototype does not have this strict restrictions, because it is to be connected to a ready made board for the Timepix3 chip designed by J. Alozy and provided by CERN/Medipix Collaboration see figure 3. Nevertheless these factors played a significant role in the selection of the components.

4 Implementation: simulations and models

4.1 High voltage bias power supply

The chosen device to satisfy the requirements of small footprint and low ripple voltage was the LT3905 power supply made for avalanche photodiodes. This section elaborates on the configuration of the device to be suitable for biasing a hybrid pixel detector chip.

4.1.1 LT3905 general description and configuration

The LT3905 is designed to bias avalanche photodiodes in optical receivers. Our application is not optical, but the general structure for one pixel of a hybrid pixel detector could be modelled as an avalanche photodiode in reverse bias (Poikela 2015, 5). The LT3905 is a switch mode DC-DC converter having a $3\,\mu\mathrm{A}$ to $3\,\mathrm{mA}$ output range with 2% accuracy APD monitoring over this range, having a maximum safe output voltage of $65\,\mathrm{V}$. Therefore although the diagram in (LTCorp. n.d., 5) suggests that it could be used in lower current ranges, our application would use it outside its specifications.

In order to calculate the values of the external components required for this integrated circuit, the internal operation has to be understood. A block diagram was created based on the block diagram in the LT datasheet. Certain parts of in the diagram were simplified, net names and external components were added to aid the understanding of the operations. See figure 4.

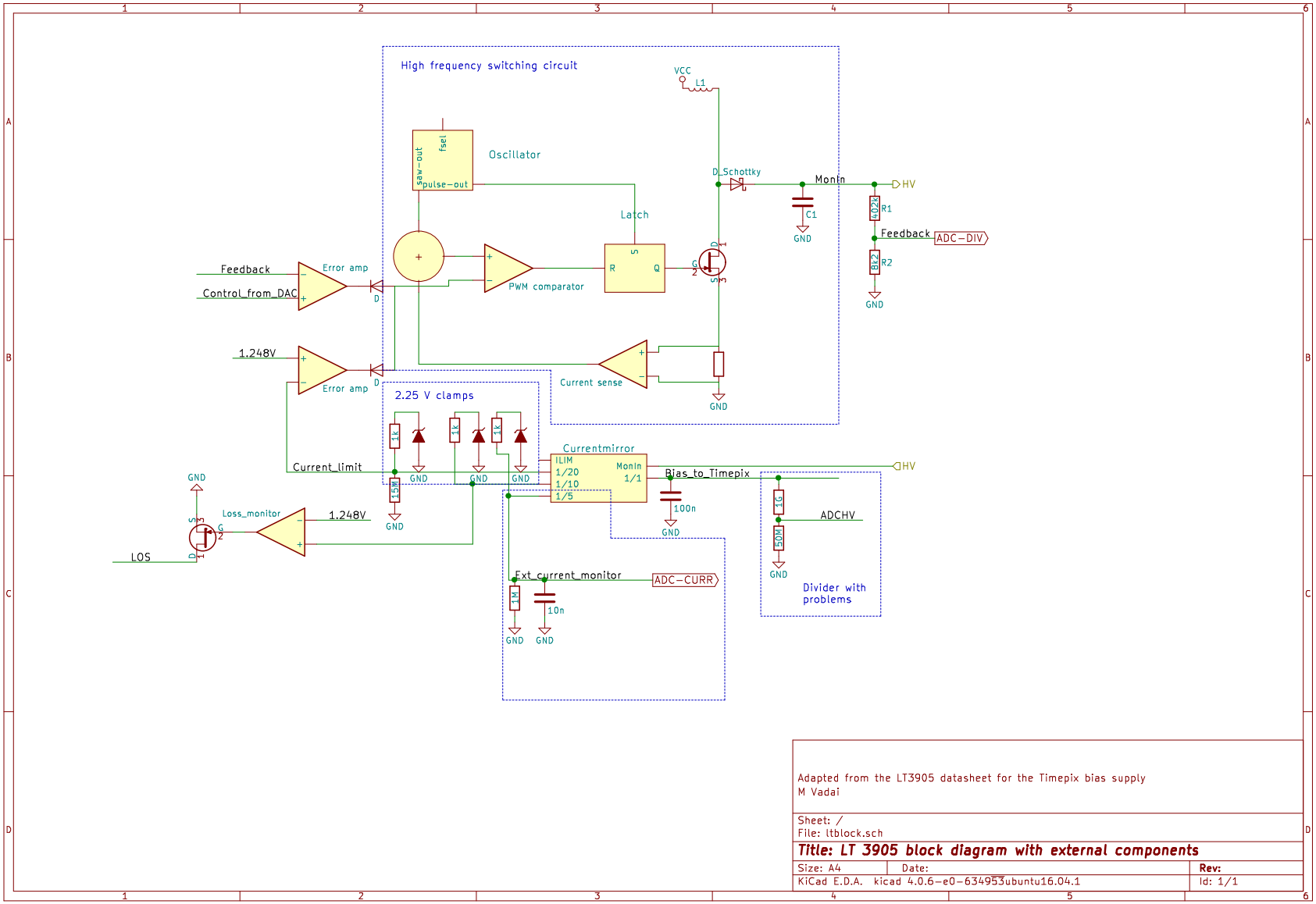

Figure 4: LT3905 adapted block diagram showing the chip's internal and some external components. The main measurement and control options are shown, too.

The oscillator turns on the latch at the beginning of the cycle by outputting a high pulse. The high output from the latch turns on the DMOS transistor switch and the current on the external inductor, L_1 rises. The output of the current sense amplifier is added to the saw-tooth or ramp output of the oscillator. This signal is fed into the positive input of the PWM comparator. If the voltage level of this pin is higher than the signal from the error amplifier, the latch is reset. This then turns off the power switch which creates a voltage pulse, since the magnetic field in the inductor collapses. Then current flows through the internal Schottky diode and the charge accumulated raises the voltage on the output capacitor. The feedback from the current sense amplifier is added to the ramp output from the oscillator, this stabilizes the positive input of the PWM comparator.

A feedback signal is created by an output voltage divider, which is then fed to the negative input of the error amplifier. The potential divider is calculated in such a way that the maximum of level of this feedback signal is $1.248\,\mathrm{V}$. This was the first value that we had to calculate to set the maximum $60\,\mathrm{V}$ output. The actual output for the prototype was set somewhat lower to $59\,\mathrm{V}$, because of the constraints of the available resistors and available footprints on the evaluation board the achievement of this value was simulated first as it can be seen in figures 7 and 27.

$$R_1 = R_2 \left(\frac{V_{MonIn}}{V_{ref}} - 1 \right) \tag{1}$$

Taking into consideration the current limiting feature discussed in section 4.1.4, this voltage was set higher since the high priority control path is not the net labelled feedback, but the path through the internal current mirror detailed in sections 4.1.3 and 4.1.4. The reason is that there is 1-3 V voltage drop on the current mirror in the low $\mu\mathrm{A}$ ranges compared to the MONIN pin (LTCorp. n.d., 6).

4.1.2 Noise and transient response simulations

The circuit was simulated in LTSpice to observe the desired output characteristics. The silicon sensor was simulated as a reverse biased diode with a set DC leakage current see figure 5. This simplified model was chosen based on the fact that this is the typical electrical characteristic of a silicon pixel detector (Rossi et al. 2006). The ripple, however was much higher than

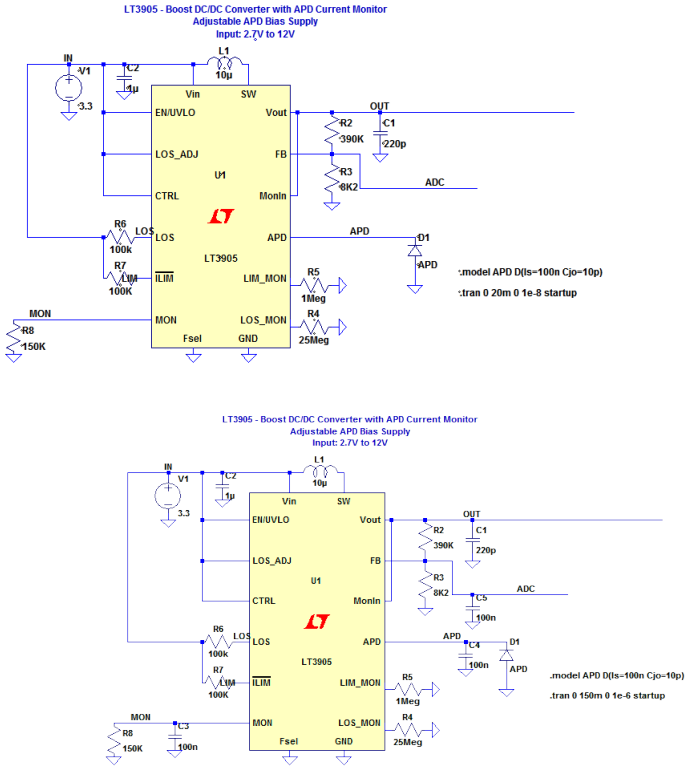

Figure 5: The proposed bias supply circuit was simulated in LTSpice without (left) and with (right) external filtering capacitors to observe the noise characteristics and basic transient behaviour of the circuit.

expected, see figure 7. Therefore filtering capacitors were included in the design as suggested by the datasheet. However, the transient response would be worse as a result as it can be seen in the timings to a step input response in figures 27 in contrast to the quick response seen in figure 7.

The transient response of the circuit to a mixed ramp and step signal was simulated with the setup seen in figure 8, where the csv file contained the PWL control information. As it can be seen in figure 27, adding the filtering capacitors greatly influenced the noise characteristics for the better and the transient response to the worse. Figure 9 provides a simulation to observe the capping of the control voltage at $1.248\,\mathrm{V}$ when the internal error amplifier limits the control signal as it was mentioned in section 4.1. The lag in the response can be seen in figures 9 and 10 due to the filtering capacitors. In contrast the fast response which was simulated without the capacitors with much more noise can be seen in figure 11.

The capacitor on the feedback pin was omitted in the final design since the accurate feed-

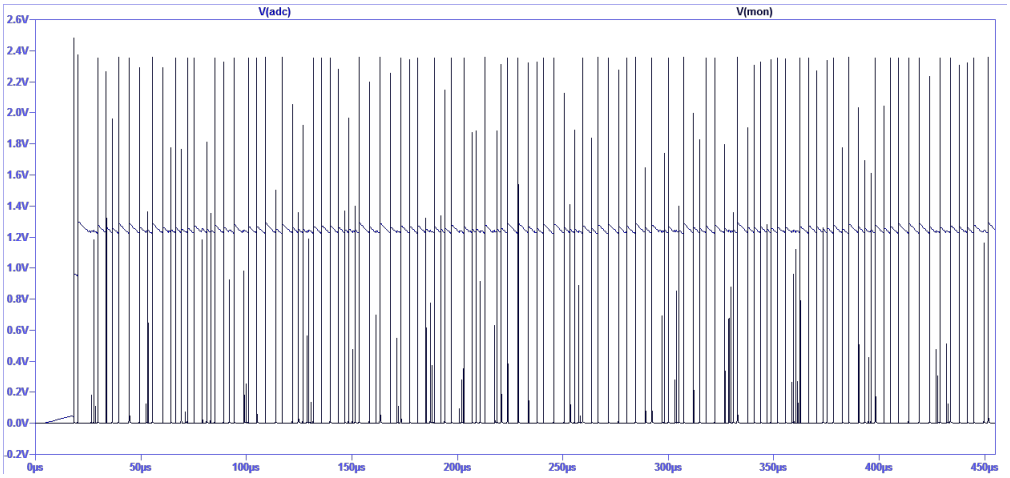

Figure 6: The result for the simulation without added external filtering capacitors on the feedback divider used for voltage monitoring and the MON pin used for current monitoring. We can see a noise in the magnitudes of several tens of millivolts in the case of the feedback potential divider noted as V(adc) and in the range of volts on the monitoring pin. The clamping voltage was hit several times on the MON pin.

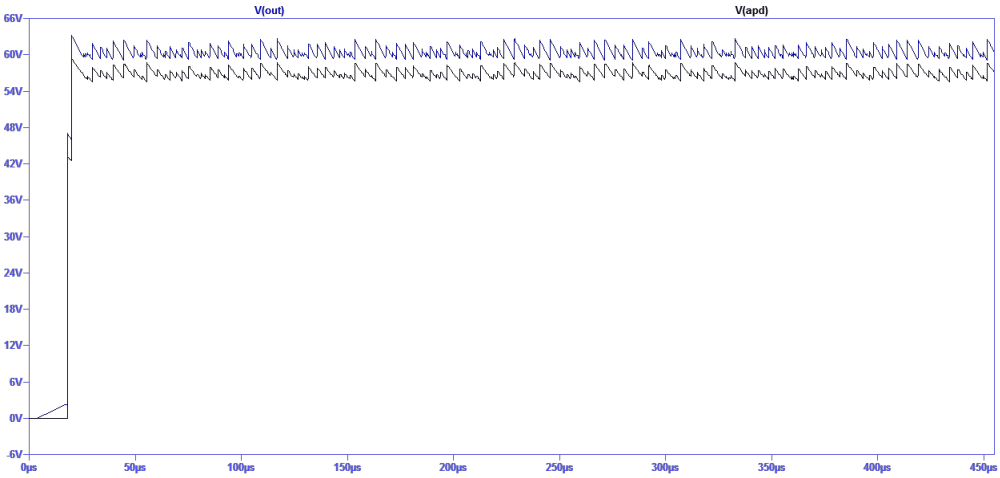

Figure 7: The result for the simulation without added external filtering capacitors on the APD output used as the output for biasing the silicon sensor and the OUT pin used for the feedback. We can see a noise in the magnitudes of several hundred millivolts on both pins. The noise on the OUT pin is scaled down to the ADC output in figure 6.

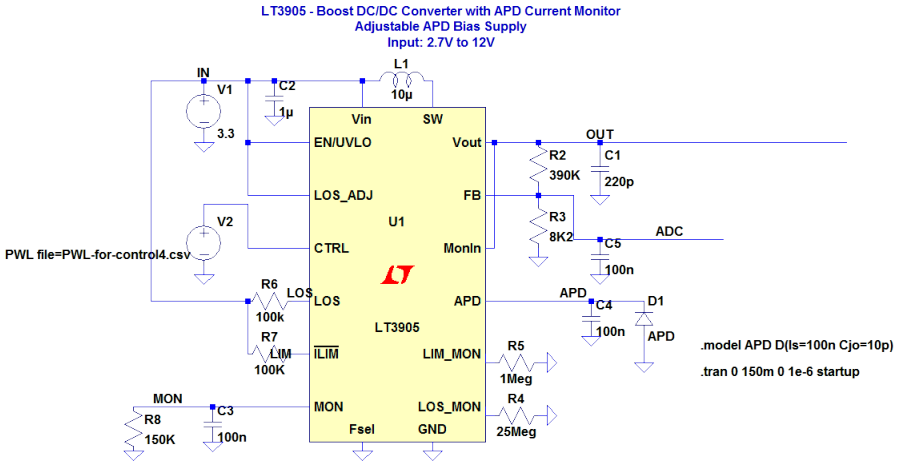

Figure 8: The control signal was added as a PWL file to the simulation to observe the differences in the transient behaviour of the circuit with or without filtering capacitors.

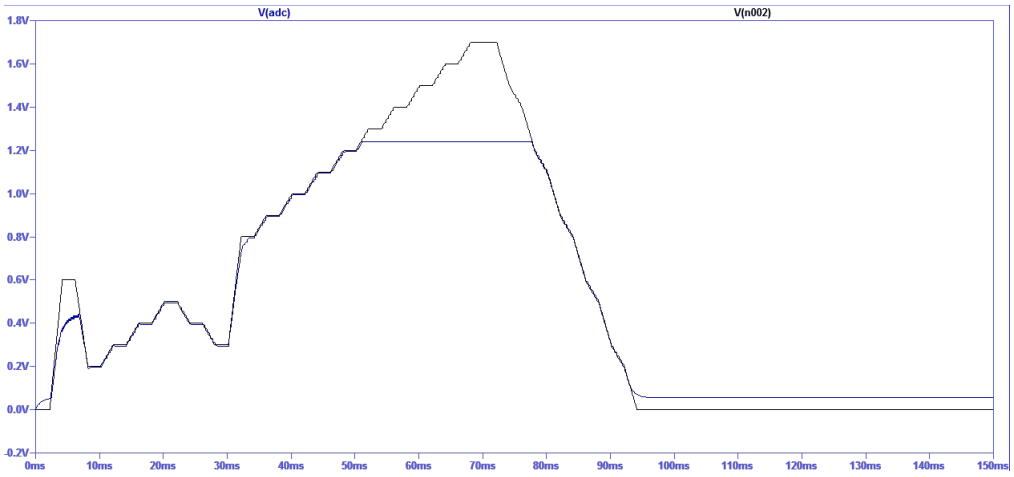

Figure 9: The capacitor added to the ADC input does remove the noise from the feedback signal. The control voltage is capped at $1.248\,\mathrm{V}$ despite the higher voltage on the control pin. It can be seen in figure 10 that the output of the circuit does not respond to the elevated control signal level above $1.248\,\mathrm{V}$ as expected.

back is more important than suppressing the noise on the ADC. digital filtering was used instead on the ADC output.

4.1.3 Current monitor: workings, noise, transients and quiescent current

The LT3905 has an internal current mirror that provides four different outputs. The main, 1/1 output is connected to the silicon sensor and there are three other outputs that provide a fraction of the APD current at 1/5, 1/10 and 1/20 of the actual current on the MON, LOS_MON and ILIM_MON pins respectively. Since the expected current in our application is lower than the

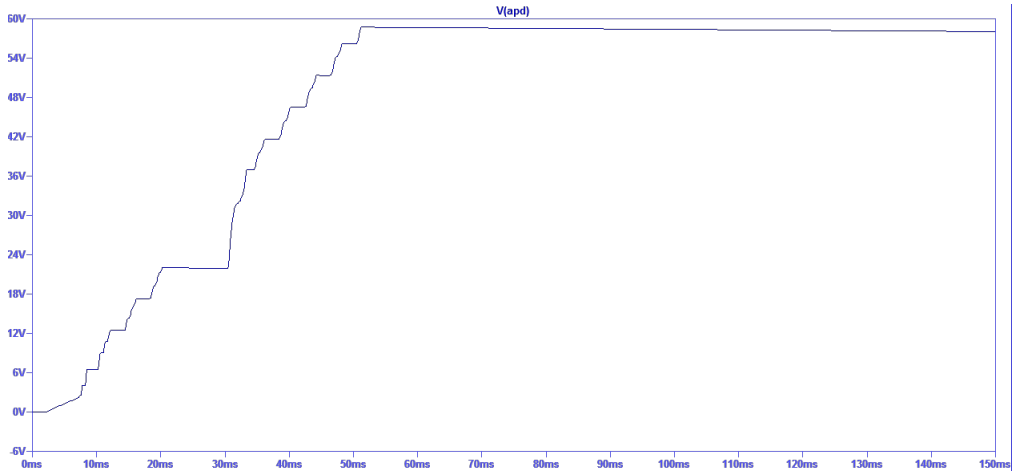

Figure 10: The sensor can not sink the current from the output filtering capacitor at a fast enough rate, the circuit can not respond as fast to lowering the voltage as to raising the voltage. This lag has to be taken into account when developing the software for the slow control circuit.

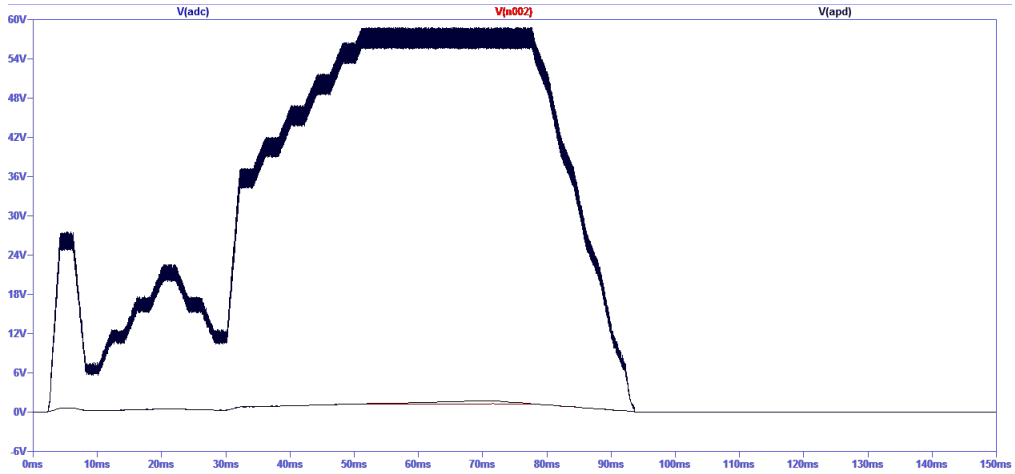

Figure 11: The response to the control signal is visibly faster in either increasing or decreasing the voltage without the external capacitors, but the noise is much higher, too. The V(n002) signal is the control signal defined by the PWL file and the V(ADC) is the signal of the feedback divider. The two lines overlap except for when the control signal is above $1.248\,\mathrm{V}$, which is due to the absence of the capacitor on the ADC pin.

minimum load current of the chip, the highest MON output is thought to be amplified[2] and used to monitor the APD current.

The brief explanation of this feedback path could be followed in figure 4. The current mirror provides an output of fractions of the actual output current to the sensor and this is fed back to an error amplifier which controls the negative input of the PWM comparator. The lower error amplifier in figure 4 takes over the control from the feedback path once it is above the $1.248\,\mathrm{V}$ threshold. The feedback and external control options are only available when the output current is within the set limits.

To program the default measurement range of the current monitor, an external resistor can be connected to the output of the MON pin tied to ground as the application note suggests. The current supplied from the current mirror would flow through this resistor which would determine the voltage measured. This would set the reference for the internal error amplifier. The datasheet (LTCorp. n.d.) sets an upper voltage limit of $2.1\,\mathrm{V}$, above which the accuracy of the measurement would be compromised. The voltages above $2.25\,\mathrm{V}$ would be clamped through the internal diodes, see figure 4. Initially a $1\,\mathrm{M\Omega}$ resistor was chosen in order to provide a sufficiently high range measurement while achieving a sufficient resolution in the 10s of nA range. This was modified to a $5\,\mathrm{M\Omega}$ resistor with a $10\,\mathrm{nF}$ capacitor to allow for a more flexible current measurement scheme. See section 4.5.2.

First simulations with the calculated values did not lead to a conclusive evidence that the nA resolution in the current measurement could be achieved without extensive external circuitry. The reason for this is threefold. First, the quiescent current on the MON pin when operating the device near or beyond its lower limits is large causing an unknown offset, to which the datasheet does not refer (see label Q in figure 12). This offset is comparable with a $500\,\mathrm{nA}$ current increase, therefore if this has a high uncertainty, then our measured value could be meaningless. Second, when the voltage changes on the output pin the MON pin saturates (see label T in figure 12), therefore a measurement in the steady state is needed. Third, appropriate noise cancelling could not be simulated within the available time for the simulation. The reason is that when using larger capacitors to achieve noise filtering in a wider band, the rise time

[2]The final design did not need external amplification at the end see figure 25.

increases, which naturally increases the response time of the circuit, therefore the steady state can only be achieved later and this increases the simulation time to an extent where simulations become unpractical.

However, provided that the noise levels observed earlier (see figures 26 and 27) could be achieved in the monitoring setup, and that the offset - even if it is voltage dependent - could be calibrated for, a nA measurement would still be possible without adding precision measurement circuitry (Williams 2002) to the design. These phenomena alongside with the noise were illustrated in with varying load and control settings in figure 12. The simulation settings can be seen in figure 13. Note that the filter capacitor (C_3 and C_4) values are much smaller in this setting than the conceived values for the design, due to time-related limitations of the simulations, but the expected behaviour can be seen alongside with the noise.

To sum up the findings of the simulation the following is true of the sum of the currents.

$$I_{mon}(t) = I_{1/5}(t) + I_{transient}(t) + I_{quiescent}(t) \tag{2}$$

Where I_{mon} is the current measured on the mon pin. $I_{1/5}$ is the 1/5-th of the bias current, which is the ideal output of the current mirror. $I_{transient}$ is the contribution of the voltage increase on the bias supply. $I_{quiescent}$ is the intrinsic leakage current of the internal current mirror. In the steady state $I_{transient}(t) = 0$.

4.1.4 Current limiting

We can distinguish between two overcurrent scenarios. The first one considers the peak current that happens when the internal DMOS switch closes and the current starts to ramp up on the inductor L_1, see figure 4. This is called the peak inrush current (LTCorp. n.d., 9) and can be calculated with the formula given by the datasheet:

$$I_p = \frac{V_{in} - 0.9}{\sqrt{\frac{L}{C} - 1}} e^{\frac{-\pi}{2 \cdot \sqrt{\frac{L}{C} - 1}}} \tag{3}$$

V_{in} is the supply voltage, L is the external inductor marked as L_1 in figure 4 and C is the capacitor connected to the voltage output marked as C_1 in figure 4. This inrush current should

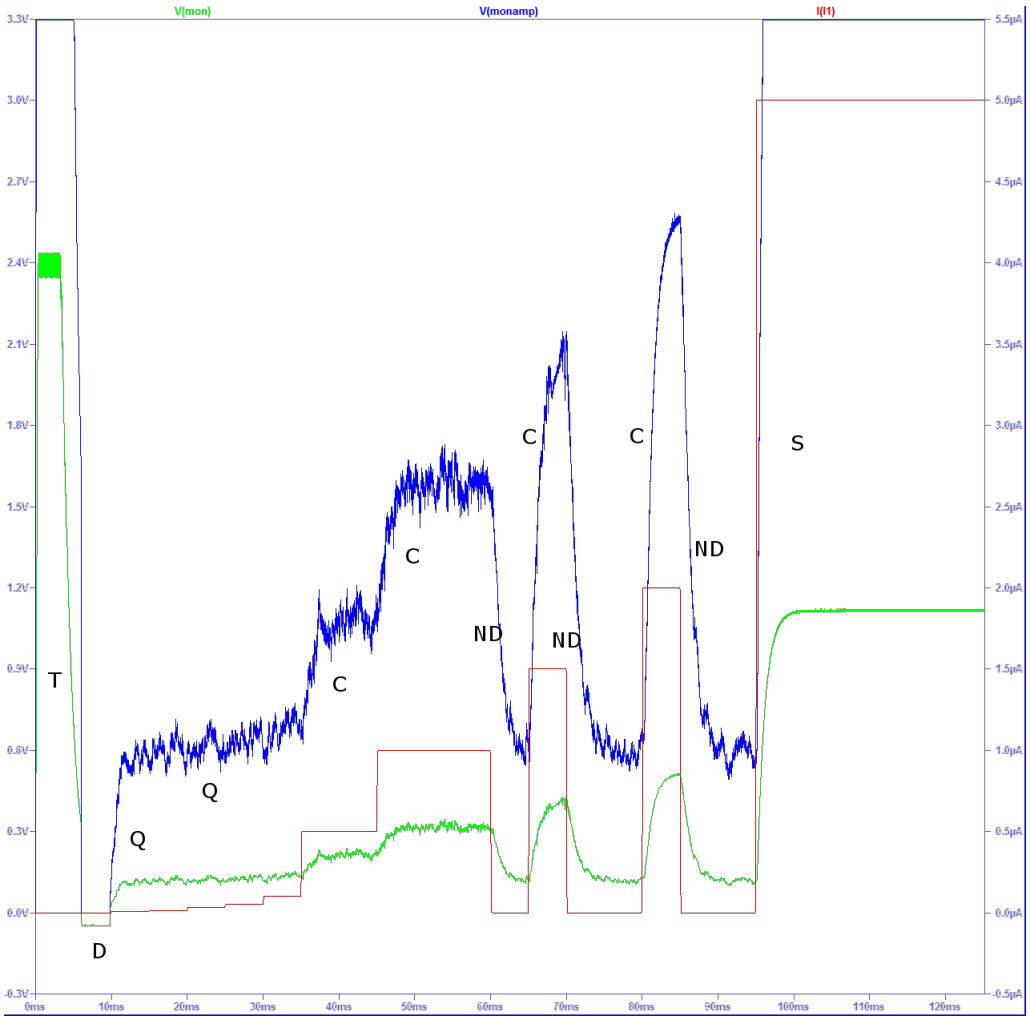

Figure 12: The red $I(I1)$ represents the load, $V(mon)$ is the MON pin output and $V(monamp)$ is the amplified output. The following regions were identified on the graph. T: Transients. While the output voltage was rising the current mirror is in saturation. D: First I_2 discharges the measurement capacitor tied to the MON pin, and since I_2 (see figure 13) loaded the MON pin the voltage on it went slightly negative. Q: With no load conditions the quiescent current through the MON pin is added to the output. The effect of the nA increases on I_1 are buried in the noise. C: Only when the current was raised by at least $500\,\mathrm{nA}$ the MON output starts to show this. ND: C_3 is naturally discharging through R_8 under no load conditions. S: the amplified monitoring output is in saturation due to too high loading.

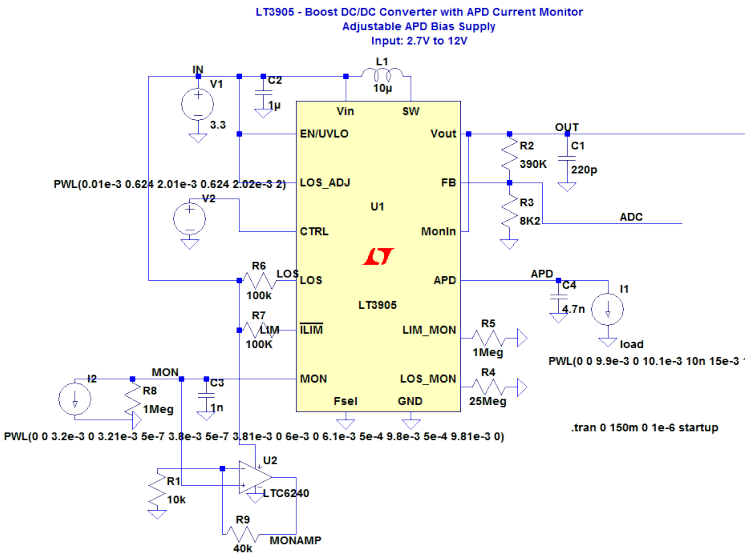

Figure 13: I_1 represents the silicon sensor with varied loads and timings. I_2 was added to discharge C_3 tied to the MON pin in stage D (see figure 12) after the transients stage, otherwise it can be taken as open line. A 1:5 non inverting amplifier was added using the LTC6240 operational amplifier to provide a better range for the ADC and buffer the MON output.

be kept below a peak of $1\,\mathrm{A}$ to protect the internal DMOS switch. In our application $C_1 = 220\,\mathrm{nF}$ and $L_1 = 10\,\mu\mathrm{H}$, therefore the peak inrush current calculated is $0.284\,\mathrm{A}$ therefore our application should not overload the internal DMOS switch.

The other overcurrent that can be controlled internally is the output current through the APD pin, which is the current delivered to the load. The APD current limit could be set by connecting just one resistor on the ILIM_MON pin which was calculated using the given formula (LTCorp. n.d., 12):

$$R = \frac{20 \cdot 1.248}{I_{APD}} \tag{4}$$

This current was set first at $700\,\mathrm{nA}$, but later discovering that the sensor on the prototype board draws more current than expected due to a missing metal layer on the top of the silicon which made the sensor sensitive to visible light. The current limit therefore was increased to be $1.67\,\mu\mathrm{A}$. This later option was tested in section 5.1.

4.2 Passive components selection

The capacitors were selected to provide as small voltage ripple as possible over a wide range of temperatures. Since the capacitance value of multilayer ceramic capacitors depend on the

package size and the temperature (Fortunato 2012), a 1206 package X7R type was selected to retain as much capacitance as possible over a wide range of temperatures.

The low voltage sampling capacitor tied to the MON pin was selected to have the C0G dielectric which has excellent properties over the temperature and frequency ranges.(AVX n.d.).

We were using the inductor in continuous conduction mode, which means that the current on the inductor is never zero during the switching cycle. This ensures higher efficiency during the DC-DC boost or up conversion. (Rogers 1999). The inductor was selected based on LT's recommendations (LTCorp. n.d., 10) observing the saturation rating and inductance requirement based on our $3.3\,\mathrm{V}$ input voltage. This was calculated using the following formula based on the manufacturer's recommendations:

$$L = \frac{V_{out} + 1 - V_{in}}{V_{out} + 1} \frac{V_{in}}{f \cdot 80\,\mathrm{mA}} \tag{5}$$

4.3 Loss of signal monitor

A low threshold for the current monitor could serve as a loss of signal monitor on the chip. Should the current drawn by the load be below a given threshold, a loss of signal condition would be asserted on the LOS pin of the device. The loss of signal condition occurs when the 1/10-th of the current drops below the internal threshold of the loss monitor comparator in figure 4. The formula to calculate the value for this resistor was the following based on the datasheet (LTCorp. n.d.).

$$R_{LOS\_MON} = \frac{10 \cdot 1.248\,\mathrm{V}}{I_{APD\_LOS}} \tag{6}$$

The loss of signal monitor was programmed to signal drop out at $500\,\mathrm{nA}$, which corresponded to a resistor value of $25\,\mathrm{M\Omega}$. However, since this threshold is well below the minimum load of $3\,\mu\mathrm{A}$ correct circuit behaviour of the loss of signal monitor was in question at this design stage[3], but the graph in (LTCorp. n.d., 5) in the lower right corner suggests that the supply covers currents down to $300\,\mathrm{nA}$. The final calculated values for the passive components can be found in the schematic in figure 30.

[3] In the end software monitoring is suggested through the current mirror, because that is found to be more accurate.

4.4 PCB layout

Since the LT chip is a switching regulator with a selectable (1 or 2 MHz) high frequency oscillator, it will introduce noise related to the high frequency switching in the circuit. The PCB layout should make the attempt of minimizing this noise. Since the changing magnetic field in the inductor can cause coupling especially in the area under the inductor, traces should be kept out of this area and a ground plane should be used below the switching part to minimize coupling with other traces nearby. The traces with respect to the high frequency circulating path which includes the output capacitor, the switch and the diode should be kept to a minimum.

4.5 Voltage and nA range current measurement

4.5.1 High voltage measurement

A direct HV measurement was not mandatory for this project, since the LT bias chip we are using has a built in current limiter which protects the sensor and user sufficiently. Rather it was an option to be explored could it be implemented with reasonable accuracy in a space and cost saving fashion. These requirements mean that, if at all, then we could only use a very few, possibly small form factor components for the high voltage measurement. The simple operational amplifier circuit options were not considered due to problems mentioned by (Williams 2002). The complex, accurate solutions were not implemented, because of footprint and power consumption concerns.

The requirements for the measurement were that the (1) voltage measurement affects the current drawn by the silicon sensor as little and as (2) predictably as possible. Therefore three options were explored. One was to use an operational amplifier with a low input current in a voltage follower configuration to buffer the voltage and step down the voltage in a second stage. The second option was to use the operational amplifier in an inverting amplifier configuration to step down the voltage. The third option was simply use a potential divider with a large resistor. Due to the low output current of the LT, a high voltage operational amplifier would draw too much current, therefore a separate supply would be needed for it which makes the solution not practical to implement, therefore the options are still the ones that (Williams 2002)

has mentioned. On top of that, it is desirable to not have an additional offset in the current measurements due to the high voltage operational amplifier that would be magnitudes higher than the current across the sensor.

Furthermore, it was desirable to include as little number of external components as possible, therefore the options of a solution without an external operational amplifier were explored. As a result simply the feedback potential divider was sampled, see figure 4 with the option of loading the APD line with a divider.

4.5.2 Analytical modelling of the current measurement

The main challenge of the current measurement is that the currents drawn by a $2\,\mathrm{cm}^2$ large and $300\,\mu\mathrm{m}$ thick silicon sensor are very low, in the hundreds of nA range (Kalliopuska et al. 2013), but sub $100\,\mathrm{nA}$ measurement results are also interesting to determine whether full depletion has occurred (Rossi et al. 2006). The LT3905 provides a current mirror to supply different proportions of the load current as explained in section 4.1.3. However, this requirement means that the LT chip is to be operated below the $3\,\mu\mathrm{A}$ lower limit provided by the datasheet (LTCorp. n.d.).

The datasheet suggests to tie a resistor from the MON pin to ground and measure the voltage on this, optionally adding a capacitor to filter the noise on the output. The transient response of the suggested RC circuit tied to the monitor pin was modelled separately in the time domain with the relevant system parameters for the expected constant current input to account for the deviations from the ideal behaviour.

A schematic seen in figure 30 was used, but only the RC part was analytically modelled, since the rest of the circuit[4] should not interfere with this when in an off state. The model is constant current charging the capacitor that has a resistive leakage optionally controlled by an external resistor essentially forming an RC network. The insulation resistance of the capacitor, the PCB and the off resistance of the transistor and the ADC in off state was modelled as resistors in parallel connected from the measured V to ground. Therefore the total leakage

[4]The ADC in particular.

resistance is

$$R_{leak} = \frac{RR_FR_C}{3RR_C + RR_F + R_CR_F} \tag{7}$$

Where R is the installed resistor in the RC circuit, R_F is the off resistance of a MOSFET transistor, which is taken to be the same as the off resistance of the ADC and the PCB in our simplified model (see section 6.2 for more details). R_C is the insulation resistance of the capacitor typically $1\,\mathrm{M\Omega/nF}$ (AVX n.d.), but it was found much higher in practice.

Provided the mentioned resistances do not change with the measured voltage, this simple model can be used. In practice this can be achieved with good accuracy if the current through R is dominant over the current through the active components in off state, therefore $R << R_F$. R can be omitted if R_C is constant. However, choosing a larger R decreases precision per least significant bit in the ADC in a linear way, this can be seen from equation 11.

Since the constant current charging is to be verified only, a direct time domain solution is provided for this first order system. During an infinitesimal dt period, the charge dQ accumulated on the capacitor is

$$(I_{mon} - I_{leak})dt = dQ = CdV. \tag{8}$$

Since $I_{leak} = \frac{V}{R_{leak}}$ provided that the resistance does not change, the following differential equation can be written for the voltage V on the capacitor C306 in figure 30:

$$\frac{dV}{dt} = \frac{I_{mon}}{C} - \frac{V}{R_{leak}C}. \tag{9}$$

The general solution of this first order non-homogeneous differential equation is

$$V(t) = Ae^{-\frac{t}{R_{leak}C}} + I_{mon}R_{leak} \tag{10}$$

Using the boundary condition $V(0) = 0$ at the beginning of the sampling period the solution is

$$V(t) = I_{mon}R_{leak}(1 - e^{-\frac{t}{R_{leak}C}}) \tag{11}$$

If I_{mon} is in the nA range and R_{leak} in the $M\Omega$ range, the steady state output will be in the mV range. R was chosen to be $5\,\mathrm{M\Omega}$, then $1\,\mathrm{nA}$ load from the silicon sensor would equal to a $1mV$

output on the current monitor pin (see the results verifying this ohmic behaviour in figure 25).

Taking the linear Taylor series approximation of this equation, with $I_{mon} = kI$, where k is the fraction[5] of the current I drawn by the sensor:

$$V(t) = \frac{kI}{C}t \tag{12}$$

Which is the constant current charging $V(0) = 0$, time domain equation of a capacitor. It can be seen that R_{leak} cancels in the linear approximation. The difference between the two models is more apparent when the charge collection time on the capacitor is in the range of $R_{leak}C$ see section 6.1.2.

Figure 14 summarizes the opportunities for current measurement on the current monitor pin. The nA precision measurement would ideally take place in the steady state and higher constant current measurements in the linear region or even using exponential curve fitting.

[5] $k = 1/5$ in case of the MON pin.

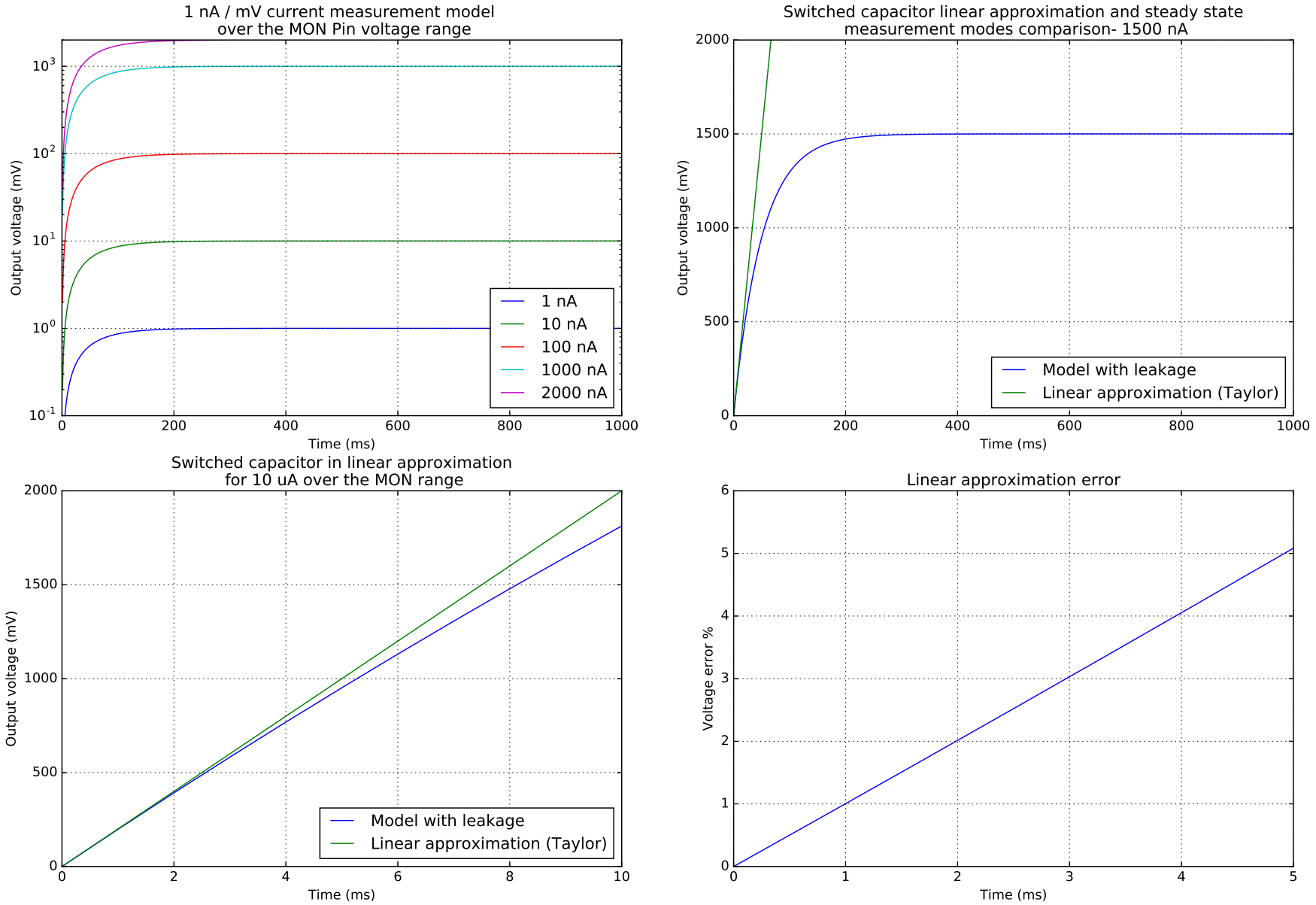

Figure 14: Graphs showing the different current measurement regions and the dependence of these on the leakage current. The error plot is based on equation 17 in section 6.1.2. The error is dependent on the time it takes for the capacitor to charge, therefore it is smaller for higher currents in the input range of the ADC.

4.5.3 Linear range current measurement simulation with switching

In this measurement the slope of the voltage on the capacitor C tied to the MON pin is measured. This slope in the linear region equals to I_{mon}/C (see equation 12 and figure 14), where C is the capacitance of the capacitor connected to the MON pin of the LT3905.

A more realistic transistor switching scheme was substituted[6] by periodically discharging the sampling capacitor C_3 using a pulse driven current source, I_2. The schematic used for the simulation can be seen in figure 15. The results of the simulation including a quiescent current measurement can be seen in figure 29. The current source I_1 was programmed to step the current on the APD pin.

The dynamic range is determined by the charging time of the capacitor and the clamping on the MON pin. Therefore the maximum current to be measured can be calculated as

$$I_{max} = \frac{CV_{max}}{kt} \tag{13}$$

Where k is the proportion of the current mirrored, in our case $k = 1/5$. In turn for a given I_{max}, t can be determined by simply rearranging the equation 13:

$$t = \frac{CV_{max}}{kI_{max}} \tag{14}$$

Given our setup with a $2.20\,\mathrm{nF}$ sampling capacitor and $V_{max} = 2.1\,\mathrm{V}$, equation 13 simplifies to $I_{max\ nA} = \frac{23.1}{t}$ and to set a sampling time in seconds given the current range to $t = \frac{23.1}{I_{max\ nA}}$. provided that the linear approximation is valid, see sections 4.5.2, 6.1.2 and figure 14.

The non-linearities caused by active devices even in an off state when added to the RC network were measured with the prototype setup later, but this switching scheme was not prototyped or modelled further, since the resistive scheme is successful enough in the given current range.

[6] Due to time constraints of the simulation.

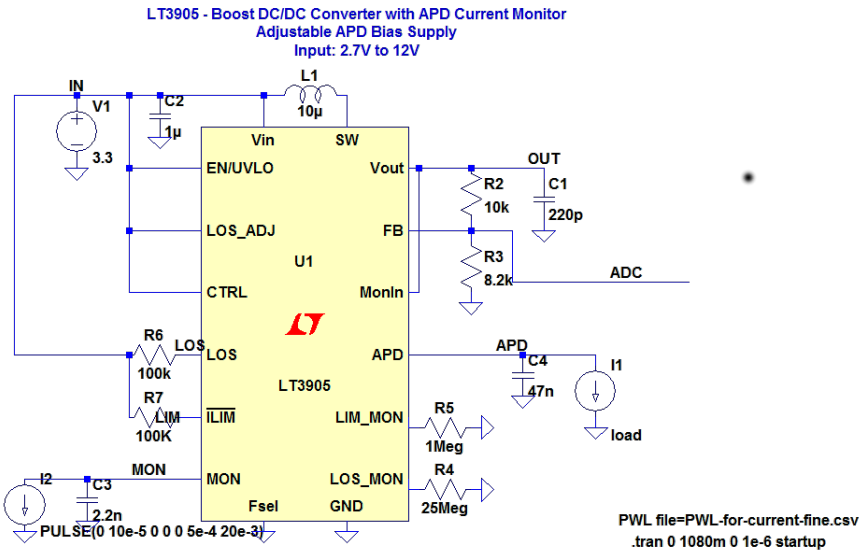

Figure 15: A $2.2\,\mathrm{nF}$ sampling capacitor was used to shorten the simulation times, but the scheme would work the same way with a bigger capacitor.

4.6 ADC and DAC settings

XC driver code to interface the TI ADS1015 ADC and the MCP47FEB DAC was developed for the XMOS controller.

The $10\,\mathrm{bit}$ DAC had the role of setting the output voltage. This could be achieved with less than $0.1\,\mathrm{V}$ precision over the $60\,\mathrm{V}$ range.

The ADC was used to monitor the feedback divider to detect then the steady state in terms of the output voltage and to measure this voltage indirectly. This means a measurement range of 0-$1248\,\mathrm{mV}$.

On a different channel the ADC measures the output of 0-$2000\,\mathrm{mV}$ from the current monitor, therefore the internal programmable gain amplifier of the ADC was set to a gain corresponding to the maximum of $2048\,\mathrm{mV}$ measurement range in order to get as close to the $12\,\mathrm{bit}$ precision as possible. Unfortunately, the ADC ranges are defined in differential mode, therefore to cover a range of $0\,\mathrm{mV} - 2000\,\mathrm{mV}$, either two ADC channels and a differential measurement in the range $\pm 1024\,\mathrm{mV}$ can be used, or one single range of $\pm 2048\,\mathrm{mV}$. The differential measurement was ruled out, since a single wire connection was preferred, therefore the $\pm 2048\,\mathrm{mV}$ range was used to cover the 0-$2000\,\mathrm{mV}$ measurement interval. This means that in practice the

$12\,\mathrm{bit}$ measurement is only a $11\,\mathrm{bit}$ measurement given that the negative half of the range is not used. This is enough for our purpose, since a $1\,\mathrm{nA/mV}$ current measurement scheme was used. The resolution of the ADC in the $\pm 2048\,\mathrm{mV}$ range is $1\,\mathrm{mV/LSB}$ which is enough to measure the current with much better than the required accuracy of $10\,\mathrm{nA}$.

In order to reduce the power consumption and to reduce the current drawn from the current monitor setup the ADC was programmed for single shot measurements as opposed to the continuous conversion mode. See section 6.1.4 on the discussion of the errors this might cause.

5 Testing and evaluation

5.1 Testing the high voltage bias supply

5.1.1 Current limiting and hysteresis

The current limiting feature was tested using an automated measurement using the Keithley 2410 SourceMeter. The measurement script used the pymeasure library which is based on the underlying NI Visa interface. A current sweep algorithm was designed to load and then unload the circuit to observe the hysteresis in the current limiting feature. Two sweeps were performed: one with a step of $1\,\mathrm{nA}$ and the second with a step of $0.1\,\mathrm{nA}$. The results can be seen in figure 16. These limits were modified later in the development, since it was found the actual sensor on the Timepix3 development board we had access to for testing consumed much more current than expected. Both measurements confirmed that the circuit limits the current in the desired range in a predictable, but not accurate way. However, the current monitoring scheme is much more accurate see figure 25, therefore this hardware solution can be substituted by software.

5.1.2 Power consumption

Since after initial tests it became apparent that the sensor consumes more power that what we expected, the current limiting feature of the prototype was set to the default $2\,\mathrm{mA}$ setting, which is the safety limit for such voltages. With the current limiting removed, power measurements were taken to establish the behaviour of the circuit.

First, coarse voltage sweep measurements were performed with four different loads: $1\,\mu\mathrm{A}$, $10\,\mu\mathrm{A}$, $100\,\mu\mathrm{A}$ and $1000\,\mu\mathrm{A}$. The results can be seen in figure 17. The main source of error of this measurement was the resolution of the power supply with which the measurements were carried out. The error bars on the y axis represent this constant error. The error of the voltage measurement was negligible compared to this.

We can see that at the $1\,\mu\mathrm{A}$ and $10\,\mu\mathrm{A}$ loads expected from a production device the current consumption stays below $30\,\mathrm{mA}$. The two sets of results can not be distinguished from one another, therefore in the expected range of operation we can say that the current consumption of the device is independent of the load with a $1\,\mathrm{mA}$ precision. This would mean a maximum power consumption of $92 \pm 2\,\mathrm{mW}$.

Second, a current sweep measurement was performed alongside a maximum voltage measurement to establish the maximum current consumption at different loads and identify how the loading affects the maximum bias voltage. The main error in this measurement was still the same as before, therefore the error coming from the resolution of our coarse current meter. However, this precision was enough for this measurement.

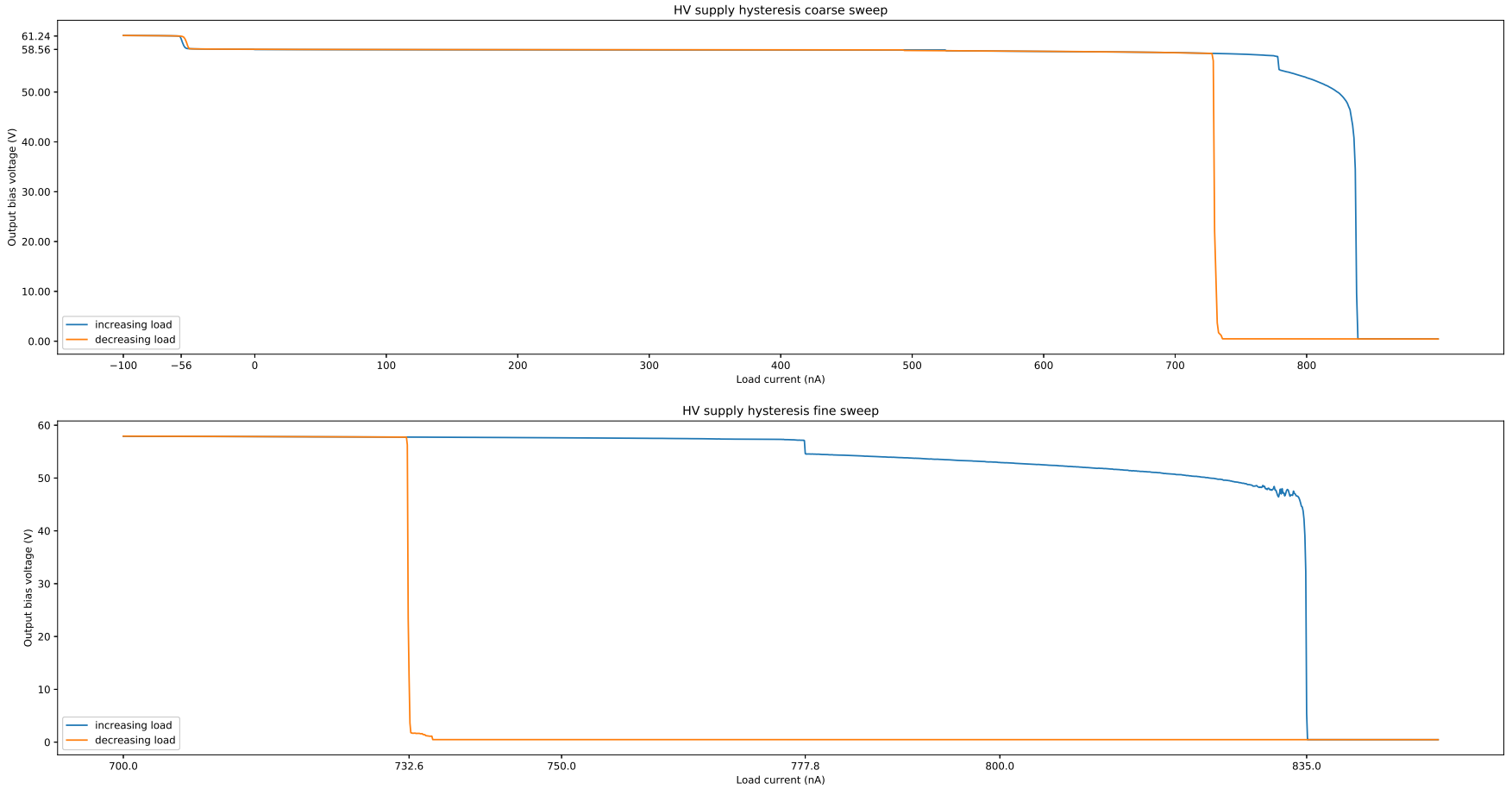

Figure 16: Coarse and fine current limiting measurement using automated Python measurement scripts. The top graph shows a full operating scale measurements using a $1\,\mathrm{nA}$ step including a negative load whereby the initial jump in voltage for the unloaded circuit can be observed. The bottom graph shows the measurement for the current limiting region performed with a $0.1\,\mathrm{nA}$ step.

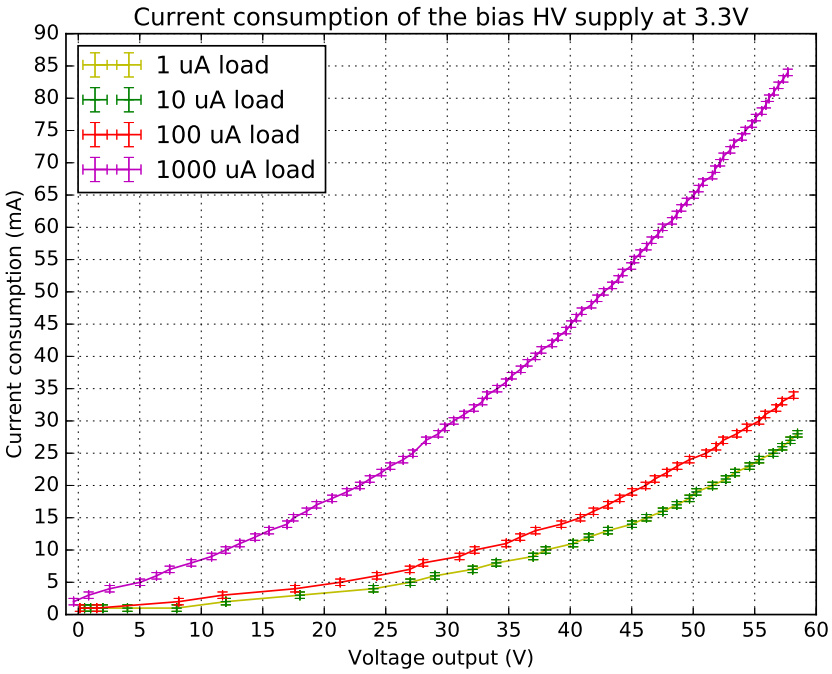

Figure 17: Current measurements with the sense input of the power supply. The resolution of the current measurement was $1\,\mathrm{mA}$.

5.1.3 Output ripple and safety

Two measurements were carried out. One measurement without the output filter capacitor, the other measurement with the filter cap. In the first case the output voltage ripple was measured in different operating conditions to establish how two parameters, the output voltage and the current load affects the noise in the operating range of our instrument. It was found that the ripple is high, but very consistent across the range, see table 2. These measurements were taken with a Tektronix MSO 2024 Oscilloscope using the factory passive probes supplied with the scope. The AC coupled measurements were taken at the lowest $20\,\mathrm{mV/div}$ setting.

The output filter capacitor was added to the circuit. The charge stored in this capacitor in order to comply with the IEC 61010-1 standard for lab equipment to be used in an educational setting has to be lower then $45\,\mu\mathrm{C}$, and the filter should attenuate the main source of the noise, the $1\,\mathrm{MHz}$ switching frequency. To meet both requirements a $100\,\mathrm{nF}$ capacitor was added. Because the measured noise was buried in the noise of the passive probes supplied with the oscilloscope, the ripple measurement was repeated with the TAP1500 Active probe using the Tektronix MSO 2024 as before. The output voltage ripple when using the external filter capac-

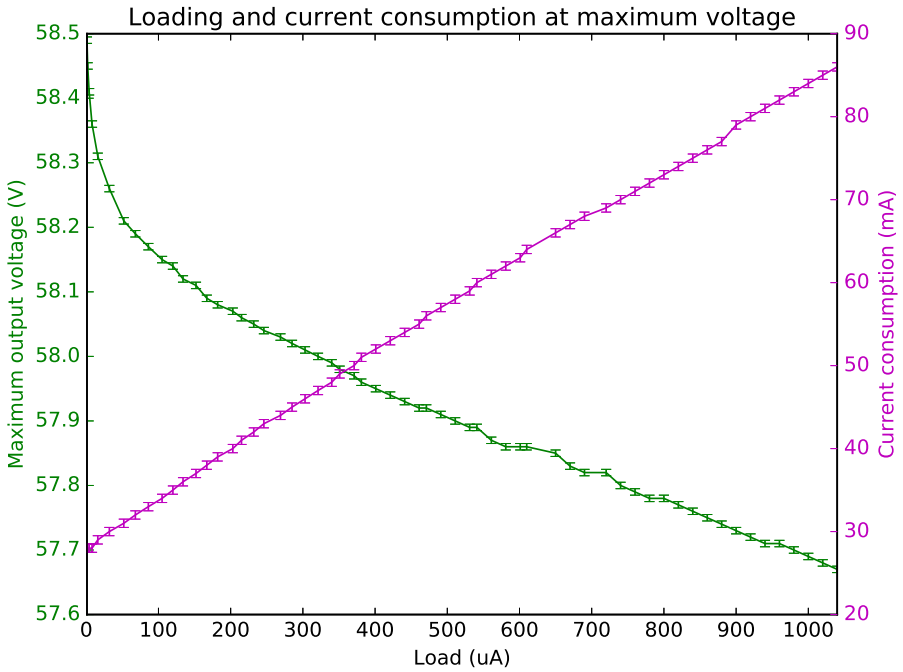

Figure 18: Loading effects and current consumption at maximum output voltage. The resolution of the voltage measurement was $0.01\,\mathrm{V}$ and the resolution of the current measurement $1\,\mathrm{mA}$.

itor was less than $1\,\mathrm{mV}$. This measurement was only conducted at $6\,\mathrm{V}$ output voltage, since the active probe had a $15\,\mathrm{V}$ limit for AC and DC measurements. However, this result is consistent with the reference result from the datasheet (LTCorp. n.d., 14).

To gain further evidence that there are no other frequency components in the output signal, a Fast Fourier Transform was performed on the high voltage supply output. We did this with an oscilloscope that has a low input noise (Rohde & Schwarz HMO1002), to identify the $1\,\mathrm{MHz}$ switching frequency and its harmonics. First an FFT was performed on the DC coupled signal to look at the ratio of the DC component compared to the noise. Second, the AC coupled signal was investigated to look at the fine details of the harmonics present in the signal. The signal was investigated in the time domain to identify periodic components. See figure 19.

After searching the frequency domain spectrum it was established that the strongest source of noise is not the expected $1\,\mathrm{MHz}$ switching frequency, but the $50\,\mathrm{Hz}$ noise. The magnitude of this could not be established in the time domain, since even this signal was buried in the rest of the noise, therefore an FFT measurement was performed. Since the smallest Δf setting on the scope was $63.58\,\mathrm{Hz}$, the $50\,\mathrm{Hz}$ component could not be distinguished form the DC component

Figure 19: Fast Fourier Transforms performed on the high voltage supply output to identify sources of noise unaccounted for. The DC coupled measurement is on the left at $20\,\mathrm{V/div}$ setting. The AC measurement is on the right with $10\,\mathrm{mV/div}$ setting. We can see that the noise is very low in both cases and the $1\,\mathrm{MHz}$ component could not be distinguished in a meaningful way from the rest of the frequency components.

when analysing the DC coupled signal using FFT on the oscilloscope. However, when we were comparing the DC coupled result with the AC coupled result, which blocks the $0\,\mathrm{Hz}$ component, the difference in the attenuation gives the relative strength of the $50\,\mathrm{Hz}$ component to the DC component, despite both of them falling in to the first $63.58\,\mathrm{Hz}$ frequency interval. Since the DC coupled measurement gives $A_{0Hz} + A_{50Hz}$ in the first $63.58\,\mathrm{Hz}$ interval and the AC coupled measurement gives only A_{50Hz} in dB terms. The result is that the in our experimental setup the noise component of the highest amplitude is $35\,\mathrm{dBV} - -48\,\mathrm{dBV} = 83\,\mathrm{dBV}$ below the signal, which is the DC output in our case. Therefore our $SNR = 83\,\mathrm{dB}$ considering the highest amplitude component in the noise. See figure 20. The rest of the frequency components were approximately $20\,\mathrm{dBV}$ lower than the $50\,\mathrm{Hz}$ component.

Translating this to relative and absolute amplitudes at MAX1932 equivalent output for a fair comparison we arrive at the following figures. $\delta V_{50\,\mathrm{Hz}}\% = 0.0071\%$, $\Delta V_{50\,\mathrm{Hz}} = 6.4\,\mathrm{mV}$. The noise level due to the $1\,\mathrm{MHz}$ switching is a magnitude lower, therefore $\delta V_{1\,\mathrm{MHz}}\% = 0.00071\%$ and $\Delta V_{1\,\mathrm{MHz}} = 0.64\,\mathrm{mV}$. The actual absolute values are lower, since these were calculated at $90\,\mathrm{V}$ output for comparison.

This means that we achieved to keep the ripple due to the $1\,\mathrm{MHz}$ switching at less than $1\,\mathrm{mV}$ while also staying well below the limit of the equipment to be classified as hazardous

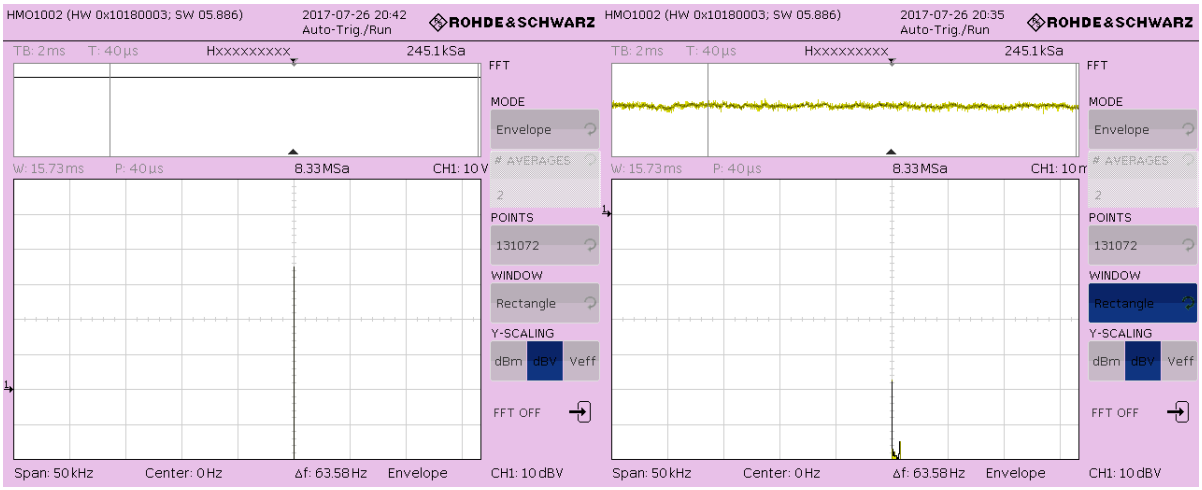

Figure 20: The dBV values of the first Δf FFT interval were compared in DC coupling (left) and AC coupling (right) modes by setting the centre frequency to $0\,\mathrm{Hz}$. The snapshot of the time domain signal can be seen on the top. The aim was to distinguish between the $50\,\mathrm{Hz}$ and the $0\,\mathrm{Hz}$ components. The oscilloscope did not support lower resolution and in the time domain the $50\,\mathrm{Hz}$ component could not be successfully measured. After evaluating several options, the envelope FFT mode was used since this was most suitable to visualize the $50\,\mathrm{Hz}$ noise. However, other methods gave the same result on the oscilloscope screen, too. This was only chosen, because the lines appeared to be thicker on the printed graph.

live. The nominal value of the charge stored in the high voltage capacitor in the circuit is $6\,\mu\mathrm{C}$, when the standard allows for $45\,\mu\mathrm{C}$. This means that the stored charge value does not exceed the requirements even when the capacitance value tolerances are taken into account.

5.2 Current measurement and optional voltage measurement

5.2.1 Measurement setup

All of these measurements below were done with the XMOS controller with the ADC and DAC connected. Test programs were developed in XC to set the voltage on the DAC and measure the voltage on the ADC. To avoid blocking and to take as much control as possible over the timing, the DAC and the ADC control codes were running on two separate cores, see figure 21. A picture of the setup can be seen in 31.

The measurement of the output voltage and the setting of the load currents were done externally with the Keithley 2410 SourceMeter.

Output voltage (V), $I = 0.3\,\mu\mathrm{A}$	Ripple (mV)	Load (µA), $V = 58.6\,\mathrm{V}$	Ripple (mV)
0.61	104	-0.1	114
2.08	106	0.0	96
7.18	113	0.1	96
14.91	117	0.2	110
25.01	102	0.3	107
35.03	102	0.4	112
40.02	106	0.5	106
45.14	108	1.0	102
50.11	114	2.0	103
55.07	110	5.0	115
58.57	106	10.0	106

Table 2: Output voltage ripple without an external filter capacitor. This is clearly bigger than acceptable. The ripple was found to be consistent across voltage and current ranges. However, the ripple was consistently less than $1\,\mathrm{mV}$, when a filter capacitor had been added to the output.

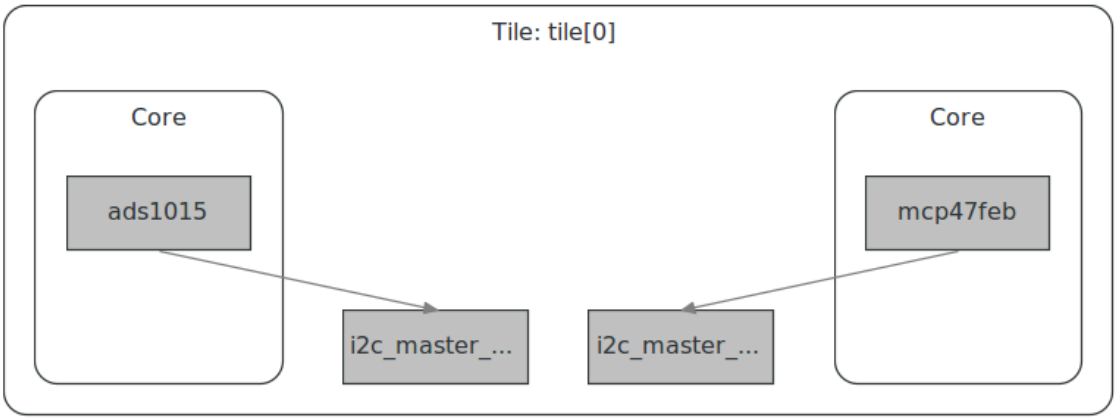

Figure 21: The test programs for the ADC and the DAC were running on separate logical cores, as displayed by xTimeComposer. Both processes were running on tile 0 on separate cores to operate the two I2C master interfaces independently.

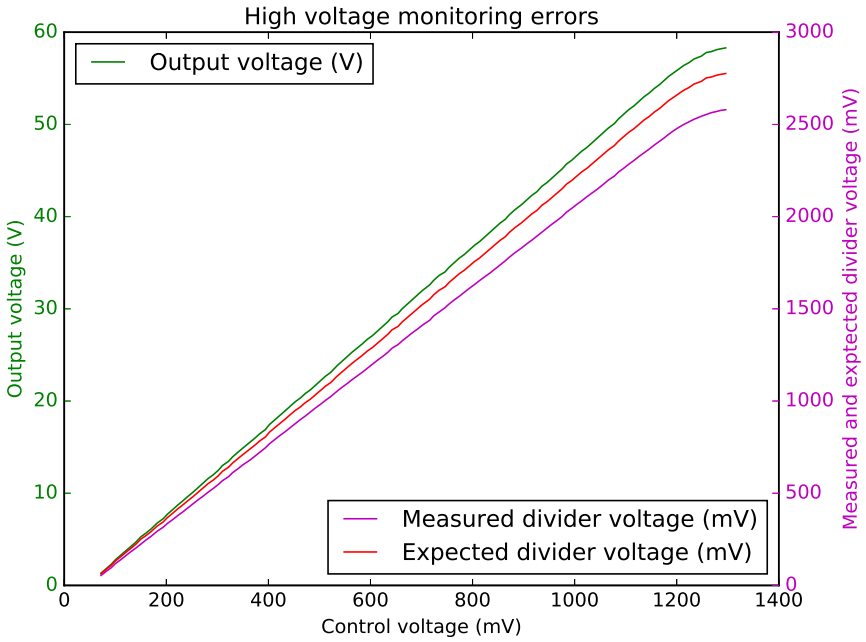

Figure 22: A high voltage measurement without buffering was attempted with a simple potential divider with an added stabilizing capacitor.

5.2.2 High voltage measurement - load characteristics

There are two alternatives to this measurement: one is to measure the feedback potential divider tied to the VOUT pin and the internal comparator alongside with the CTRL pin, or to attempt an external high voltage measurement.

A simple potential divider was attached directly to the ADC pin in an attempt of drawing a very small, calculable extra current from the pin and try to measure the voltage directly. It can be seen that even when filtering the noise with a capacitor, without buffering, this technique introduces errors in the measurement. See figure 23. The voltage measured is systematically lower than expected. The main source of this systematic error is the voltage drop that happens when the ADC samples, therefore the sampled value is systematically lower than the measured value, see 24.

The main source of the error is that the divider limits the currents in the nA range, because a 1 GΩ resistor was used as the high side resistor to limit the current on the APD pin, and this little current is not enough to drive the ADC. Namely the charge of the internal input capacitor can not be successfully achieved, while the ADC is sampling due to the high time constant of

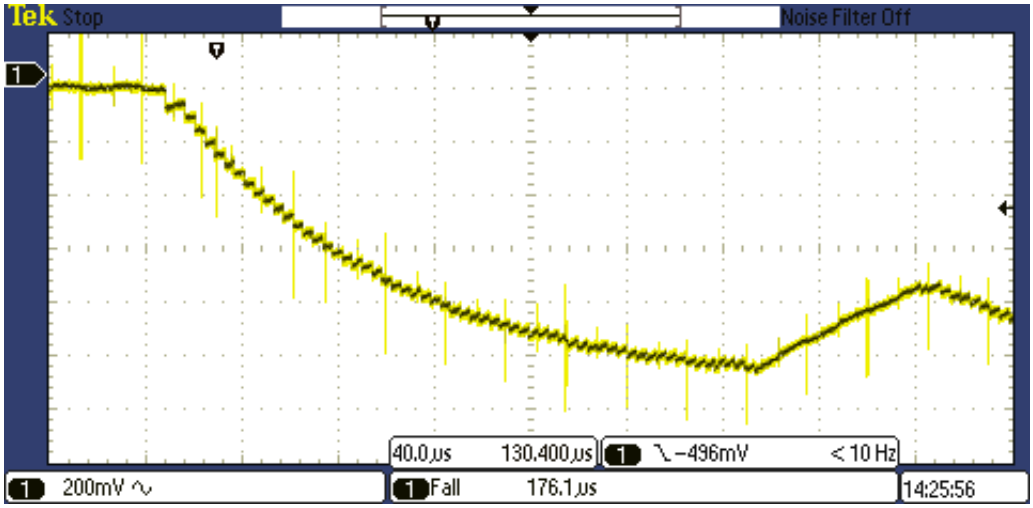

Figure 23: ADC input capacitance and sampling when tied to a high impedance source. The effects of the sampling can be seen as the internal capacitor is charged. An inversion occurs when the voltage reaches 0 V. The internal sampling frequency of the ADC is $250\,\mathrm{kHz}$, which can also be confirmed from the diagram above. There is approximately 10 steps in one time division. Which would correspond to $4\,\mu\mathrm{s}$, which in return corresponds to $250\,\mathrm{kHz}$ sampling frequency.

the input RC network. This phenomenon is most apparent when a stabilizing capacitor is not used on the ADC input and can be seen in figure 23.

Therefore the potential divider on the APD pin was omitted and the feedback signal was used to measure the high voltage indirectly.

5.2.3 Current measurement in the 0-2000 nA range without an op-amp

To verify the workings of the current monitor, a test connecting a current sink to the output of the bias supply was conducted. The voltage output of the monitor was measured with the ADC from the XMOS controller. The setup can be seen in figure 31. Four tests were performed with the results shown in figure 25. Control data was produced with only connecting the passive RC components to the system (see section 4.5.2) and the operation was verified in the steady state of the current measurement system. The schematic can be seen in figure 30. Here the steady state output is expected to be increase linearly with the increase of the constant current at a rate of $1\,\mathrm{mV/nA}$ as per equation 11. Then to verify the workings different tests with the switching measurement setup in off state were performed to see how the off resistance of the transistors affect the result (see section 6.2.4). First using a MOSFET transistor (BS170), then

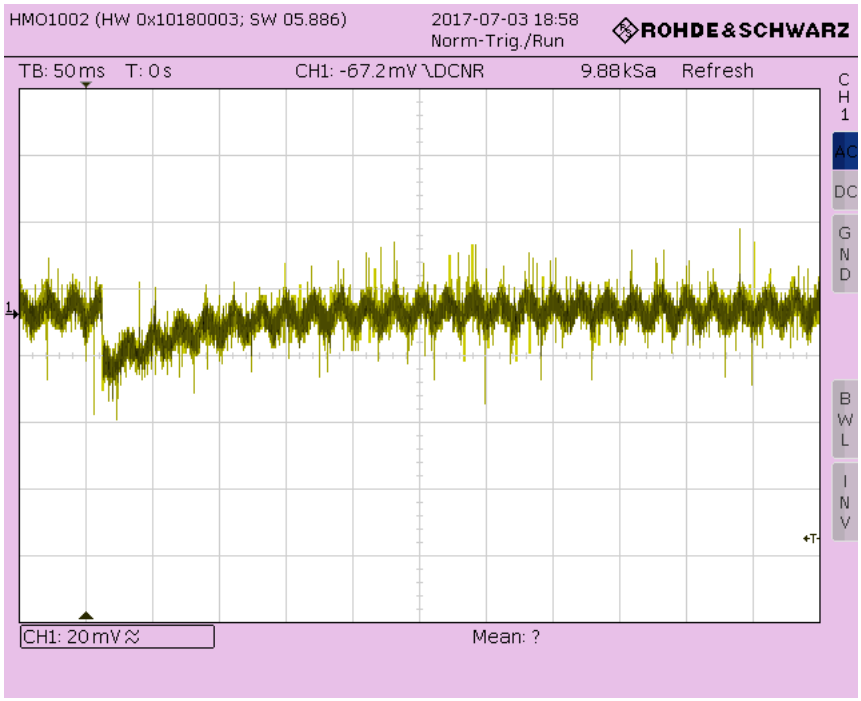

Figure 24: After adding a $10\,\mathrm{nF}$ buffering capacitor instead of an operational amplifier we can still see a drop in the voltage during the measurement and the $50\,\mathrm{Hz}$ noise the prototype circuit picked up, partly because of the large resistors in the divider. This noise was successfully attenuated to a much lower level, see figure 20.

two of them connected in series, then a bipolar junction transistor (PN2222A) and a capacitor (10nF C0G) alone with leakage. $R = 5\,5\mathrm{M}\Omega$, $C = 10\,\mathrm{nF}$. Figure 25 shows the difference of the effects of off resistances of the BS170 MOSFET and the PN2222A transistor compared with the reference data measured on the RC network.

6 Discussion

The uncertainties of the two current measurement schemes are compared in this section.

6.1 Uncertainties and improvements of the current measurement in linear approximation

The current measurement depends on a voltage measurement by the ADC, therefore the main source of the uncertainties could be identified from the linear approximation of the charging. The advantage offered by this scheme is a dynamic range current measurement, but it has more

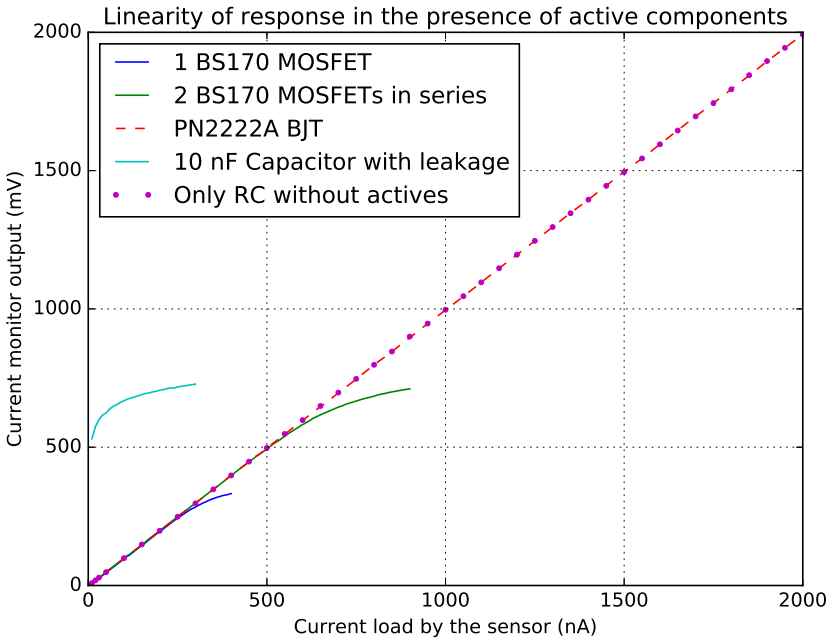

Figure 25: Verifying the expected $1\,\mathrm{mV/nA}$ linear behaviour and testing active components in the circuit. Since the current range to be measured is very low, some of the active components when switched off introduce non linearity to the system deviating from the expected $1\,\mathrm{mV/nA}$ response. The capacitor is measured to establish the region where its insulation resistance behaves like an external resistor. This in this present form is not useful in our application.

sources of uncertainties and errors than the pure resistive measurement.

6.1.1 V is not constant during sampling

The first inherent problem of this linear charging measurement scheme is that the voltage is changing during a single sampling period of $303\,\mu s$, therefore this introduces an error of

$$\Delta V = \frac{kI}{C} t_s \tag{15}$$

Where t_s is the sampling time of the ADC and C is the capacitance of the external sampling capacitor and I the current through the sensor assuming linear charging during the sampling period (see section 4.5.2).

By using the formula rearranged for C developed for the charge period of the capacitor in equation 14 in section 4.5.2, ΔV could be expressed in other relevant terms of the sampling scheme, too:

$$\Delta V = \frac{kI}{\frac{kt_c I_{maxr}}{V_{max}}} t_s = V_{max} \frac{I}{I_{maxr}} \frac{t_s}{t_c} \tag{16}$$

Where t_c is the charging time of the capacitor. It can be seen from equation 16 that ΔV scales with three factors linearly: V_{max}, $\frac{I}{I_{maxr}}$ and $\frac{t_s}{t_c}$.

I_{maxr} and t_c are dependent on each other as per equation 14. Equation 16 was only shown to provide a different angle in understanding this error. Otherwise equation 15 is equivalent to equation 16.

6.1.2 V(t) is not linear during charging

The percentage error due to this calculated by dividing equation 12 by equation 11 at the end of the charging period t_c is

$$\Delta V\% = \left(\frac{\frac{kI}{C} t_c}{kIR_{leak}\left(1 - e^{\frac{-t_c}{R_{leak}C}}\right)} - 1 \right) \cdot 100 = \left(\frac{t_c}{R_{leak}C} \frac{1}{\left(1 - e^{\frac{-t_c}{R_{leak}C}}\right)} - 1 \right) \cdot 100 \tag{17}$$

Where t_c is the charging period and the rest of the symbols are defined in section 4.5.2.

This error is 1% when the charging time of the capacitor is 1/50 of the time constant and scales according to the function above (see figure 14).

This can be used to measure higher currents, because for those the charging times are low. However, a fast sampling ADC is needed.

6.1.3 Offset and peak value uncertainty

If only the peaks of the voltage are used for the measurement, as in the illustrative calculation of the simulated output in figure 29, then the result does depend on the peak value and offset. However, if the slope of the curve is calculated, then the peak value and offset errors do not affect the result, provided the linear waveform does not change during the charging of the capacitor. Otherwise the model shown in section 4.5.2 has to be used.

6.1.4 ADC timing uncertainty

The uncertainty in the slope of the voltage *with respect to the uncertainty of the timing* of the ADC measurement in the constant current charging scenario is zero. In other words the uncertainty in the ADC measurement timing (i.e. sampling period) does not contribute to the overall uncertainty in the linear charging case. This is because the voltage in this approximation on the sampling capacitor is linear with time. This can be proven in the continuous time domain by saying that $\dot{V} = m$, which is the slope of the line is constant. This does not depend on t. This is true in the discrete sampling case, too, therefore it can be implemented on the microcontroller easily, because starting at $t = t_0$

$$\frac{\Delta V}{\Delta t + \delta t} = \frac{m(t_0 + \Delta t + \delta t) - mt_0}{\Delta t + \delta t} = m \tag{18}$$

even without infinitesimal calculus, because there is only one time interval measurement involved which has one and the same δt. Where Δt is the time between two ADC measurements (i.e. sampling period), δt is the uncertainty of the sampling period and m is the slope to be measured.

6.1.5 Capacitance uncertainty

This consists of five main parts. First, the uncertainty of the capacitance value of the chosen material (C0G) due to the temperature is $30\,\mathrm{ppm}/^{\circ}\mathrm{C}$, a total of $\pm 0.3\%$ from $-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$, but since this detector is aimed at lab use, the actual variation in the capacitance due to temperature change is much smaller than this. Second, the uncertainty due aging is $\pm 0.1\%$. Third, the uncertainty due to charge and discharge hysteresis is $\pm 0.05\%$. Fourth, the variance of the absolute value is $\pm 1\%$, which can be addressed with calibration. Fifth, the uncertainty the due to the frequency is negligible according to the datasheet (AVX n.d.).

Altogether the uncalibrated value can vary about $\pm 1.45\%$ and the calibrated value by $\pm 0.3\% + 0.1\% + 0.05\% = 0.45\%$ in the worst case. Assuming a $50\,^{\circ}\mathrm{C}$ temperature change in a lab, the uncertainty due to the temperature change is $30\,\mathrm{ppm}/^{\circ}\mathrm{C} \cdot 50 = \pm 0.15\%$, and adding the hysteresis since that is a dynamic property which can not be calibrated for and assuming one calibration, therefore the aging has to be taken into account, too, the total uncertainty in the capacitance in the calibrated lab case is $\pm 0.15\% + 0.05\% + 0.1\% = \pm 0.3\%$. Should the calibration be done on a regular basis, this can be as little as $\pm 0.3\% - 0.1\% = \pm 0.2\%$.

6.2 Errors and uncertainties in the current through the MON pin

In order to evaluate the error with respect to the current consumed by the chip, the errors in the LT chip and in the measurement hardware have to be evaluated.

6.2.1 Quiescent current

This current was simulated and then measured under zero load conditions. This current is supplied by the output of the internal current mirror of the LT chip and it is a significant part of the current monitor output according to simulations. See figure 12 label Q. This current was found to be linearly dependent on the output or control voltages when a simulation was done, see figure 28. The average value could be compensated for, but the value of the quiescent current was found to have an approximately $\pm 3.5\%$. However, this current does not affect the measurement noticeably when the measurement is performed in the steady state see figure 25. Further tests have to be performed to establish the true contribution of this error.

6.2.2 Transient current and output ripple

Referring to figure 12 label T, it is clear that current measurements should not be taken place at all when the voltage increases, this error completely jeopardizes the measurement. Therefore it is essential that the current measurements take place when the steady output voltage is reached in order to achieve the desired accuracy. The noise on the APD pin should be kept to a minimum, so it does not cause the system to deviate from the steady state. This is achieved in our implementation.

6.2.3 Capacitor leakage

The current leaking through the capacitor is determined by the insulation resistance of the capacitor. This values is given for the C0G material as $1000\,\mathrm{M}\cdot\mathrm{C}(\mu\mathrm{F})$ (AVX n.d.). Therefore if a $100\,\mathrm{nF}$ capacitor is used this resistance would be in the $100\,\mathrm{M}\Omega$ range. This is comparable with our measurement range in the more sensitive region and could be compensated for. The smaller the capacitance, the higher this leakage. This leakage does not affect the measurement in our setup noticeably.

6.2.4 ADC off leakage current

The typical MOSFET off resistance has a typical value of above $10\,\mathrm{G}\Omega$ (Horowitz & Hill 2015). The ADC off resistance was approximated with the leakage of a FET (R_{off}) given that the input multiplexers in the ADC are implemented using CMOS technology. A single FET leakage was found to be lower than this as per figure 25, however the presence of the ADC was not noticeable.

6.2.5 PCB solder mask and solder paste surface insulation resistance

Reports have been found the board surface insulation resistance and the solder paste resistance to be in the $10\,\mathrm{G}\Omega$ range (Michalkiewicz et al. n.d.) and the same is true of the overall surface insulation resistance (Customer 2010), therefore the surface insulation resistance was taken to be as an additional FET. This effect is found not to be noticeable even in our test setup, which consisted many PCBs connected with wires and even a breadboard see figure 31.

6.3 Uncertainties of the resistive measurements

The uncertainty of this measurement comes from the uncertainty of the current through the MON pin and the uncertainty of the external components. However it does not suffer from the uncertainties mentioned in section 6.1. Since the behaviour of the RC measurement circuit is resistive in the steady state. Therefore the uncertainty is only affected by the uncertainty of the resistor tied to the MON pin and the uncertainties related to insulation resistances of the ADC in off state and the PCB.

Since the resistance of the $5\,\mathrm{M\Omega}$ resistor is much lower than the typical insulation resistances, it is assumed that this measurement uncertainty is dominated by the uncertainty of the resistance of the resistor. Provided that the resistance value is calibrated at $2\,\mathrm{V}$, the uncertainty of the measurement will be due to the uncertainty of the resistance changing with temperature at a typical rate of $100\,\mathrm{ppm/^\circ C}$ (Vishay 2017), which would be an uncertainty of $\pm 0.5\%$ over an $50\,^\circ\mathrm{C}$ assumed laboratory temperature change and $\pm 2.1\%$ from $-55\,^\circ\mathrm{C}$ to $155\,^\circ\mathrm{C}$.

6.4 Conclusion

The requirements for the bias supply stated in section 3.1 are all met. An output voltage of nearly $60\,\mathrm{V}$ is reached and the charge stored is compliant with IEC61010-1 while the ripple is found to be lower than $1\,\mathrm{mV}$. The footprint requirement of 1-2 cm^2 is met, too. The resolution of the current limiting scheme is $1\,\mathrm{mV/nA}$, with the uncertainty being dependent on the resistor tolerances only according to the measurements. In order to make a comment on the overall uncertainty, tests under different temperatures have to be performed. The XMOS drivers for the ADC and DAC are implemented and the monitoring parameters are verified using the microcontroller.

The quiescent current is not measurable as predicted by the simulations in the 0-$2000\,\mathrm{nA}$ range when measuring in the steady state. The voltage measured at the monitor output is directly proportional with the current drawn by the Keithley at the bias output, no measurable offsets were found with $1\,\mathrm{mV}$ precision.

The leakage resistance of the ADC, the charge drawn during sampling and the leakages even in the test setup do not affect the results measurably. However, the presence of MOSFETs even

in an off state do affect the linearity of the current measurement, whereas a bipolar junction transistor do not.

Overall, improvements can include including a current measurement scheme that works with higher currents, too, if needed. The quiescent current as predicted by the simulations can be investigated further, but no effect of this has been found so far.

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7 Appendix

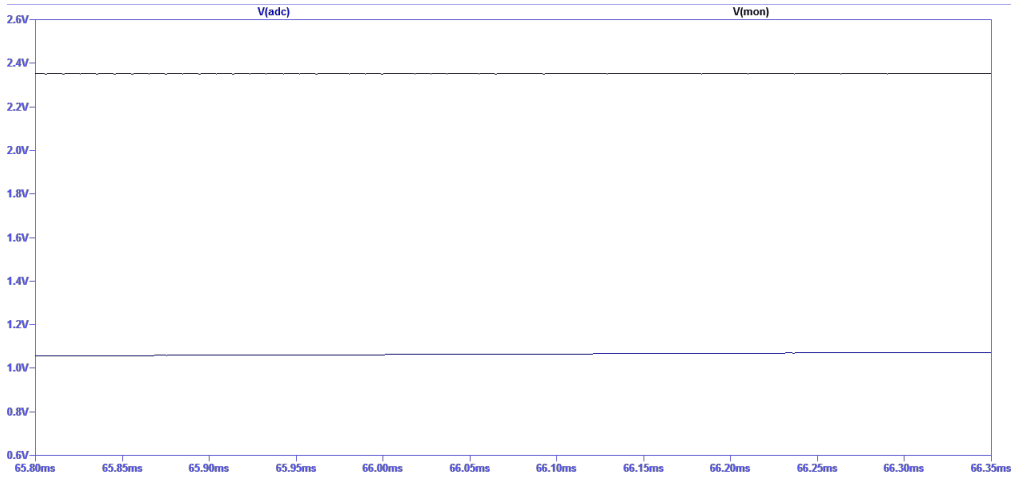

Figure 26: The figure shows the result of the simulation with added external filtering capacitors on the feedback divider and the MON pin. We could see that the magnitude of the noise was greatly reduced as a result of adding the capacitors. The time interval of the graph is the same as in figures 6 and 7.

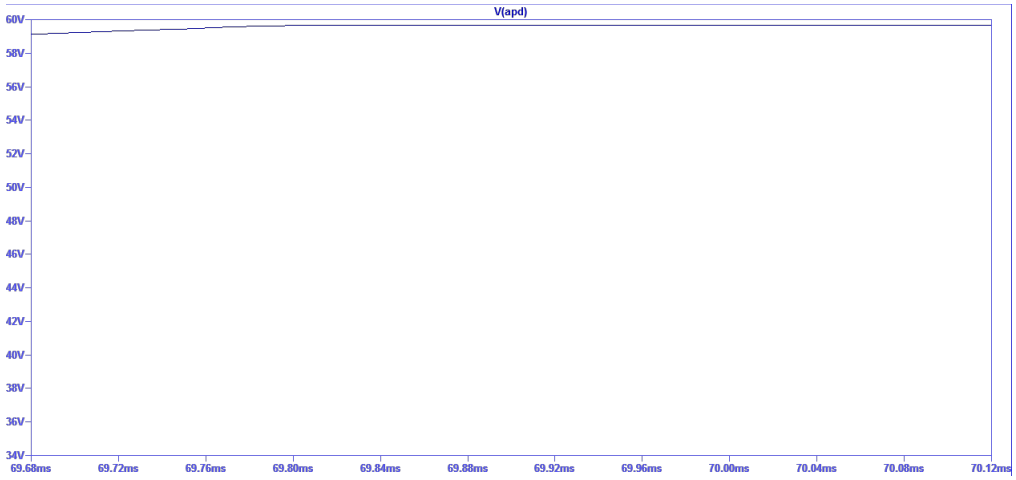

Figure 27: Adding a filtering capacitor on the APD pin greatly improves the noise performance of the circuit in the presence of noise at the expense of the much slower transient response.

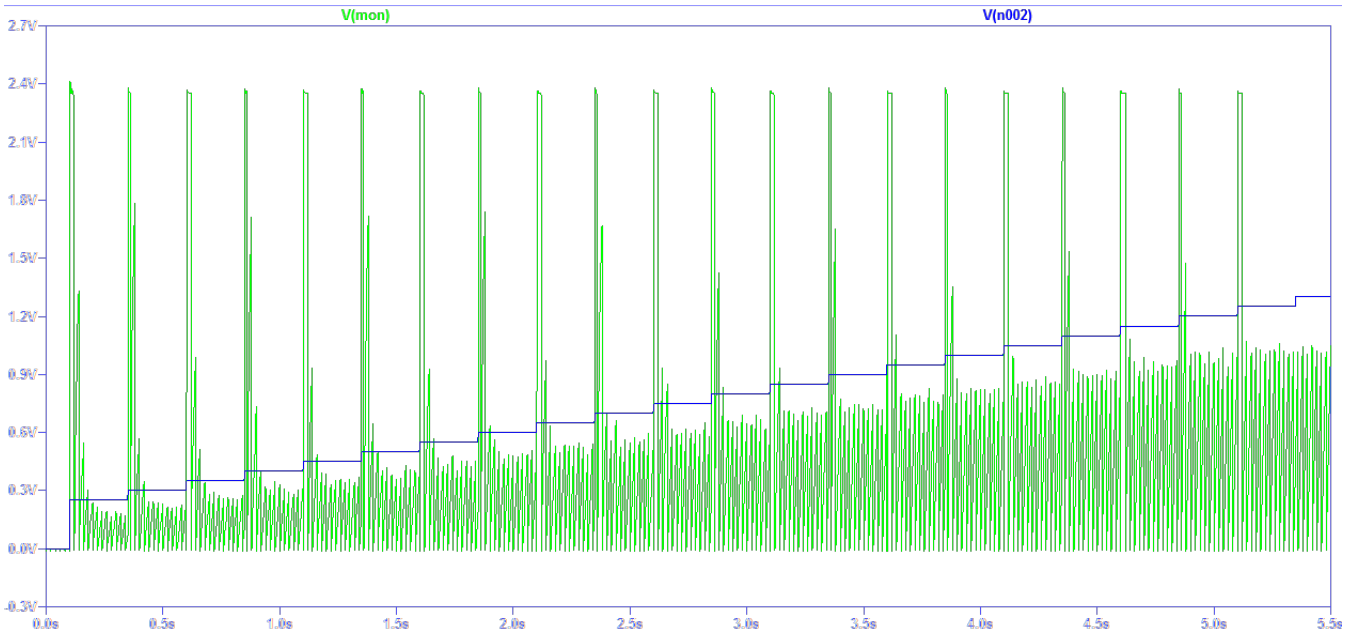

Figure 28: The simulation shows that the quiescent current (green) depends on the control voltage (blue). The current was calculated based on the slopes of the capacitor voltages when charged through the constant current supply and the steady state was reached as explained in section 4.5.3. It was found to be linearly changing with the control voltage, according to the measured data $I_{quiescent}(nA) = 0.0953 \cdot V_{control}(mV) - 2.09$ with $R^2 = 0.9988$. The control voltage is capped at $1.248V$. The average percentage uncertainty in the quiescent current calculated from the slopes is found to be $\pm 3.5\%$. This had to be simulated, since the datasheet does not have information on the quiescent current of the current mirror.

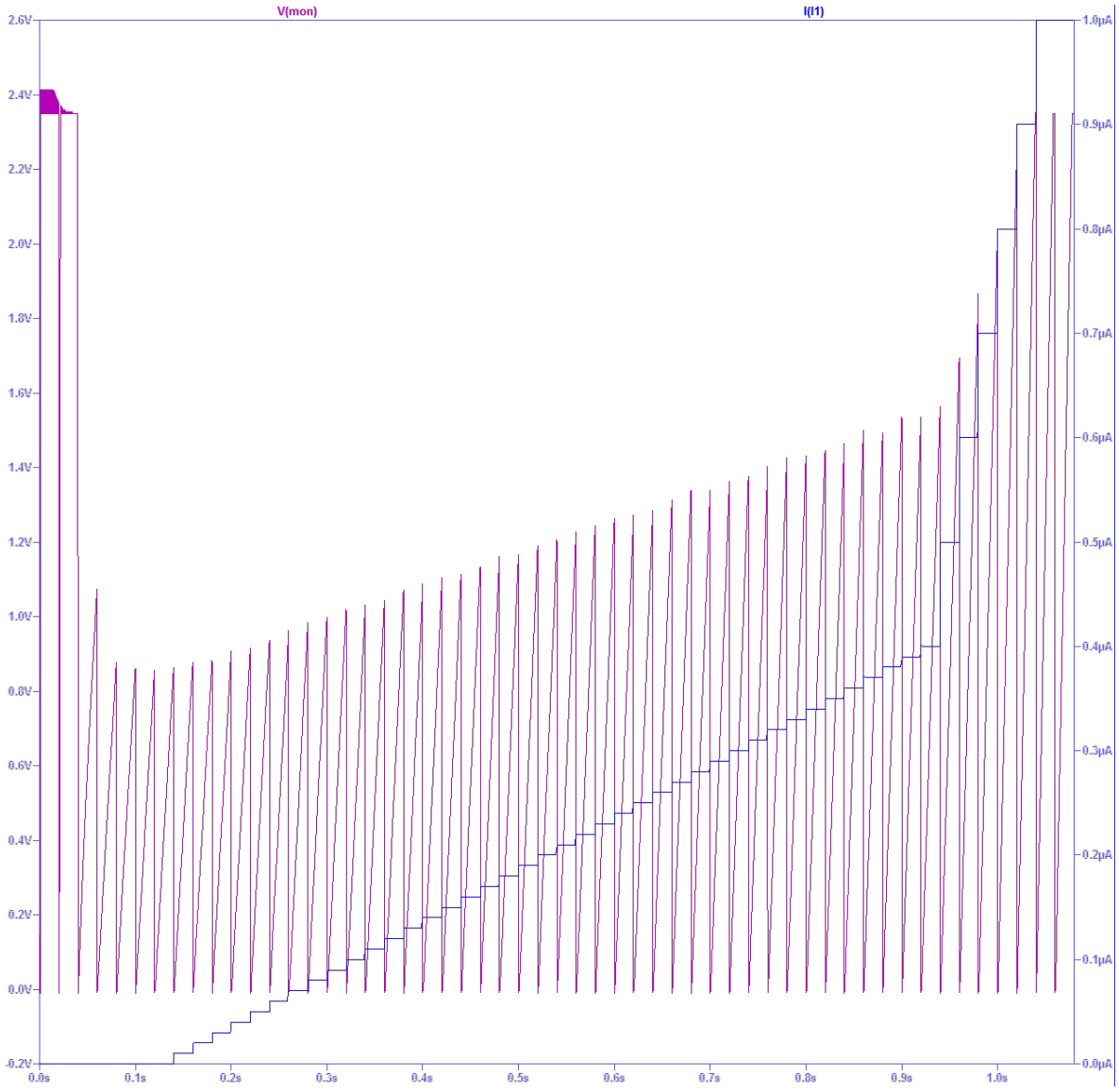

Figure 29: After the voltage has settled on the APD output, the I_1 current source provided a stepped output first with $10nA$ steps then from $400nA$ with $100nA$ steps. The current waveform was defined in an external .csv file. As an illustration a linear curve was fitted on the peaks in the data. It was found that the resolution of the measurement is $0.57nA/mV$ for this model data set with $R^2 = 0.9991$. In the end, the resistive measurement was implemented for low currents (see figure 25).

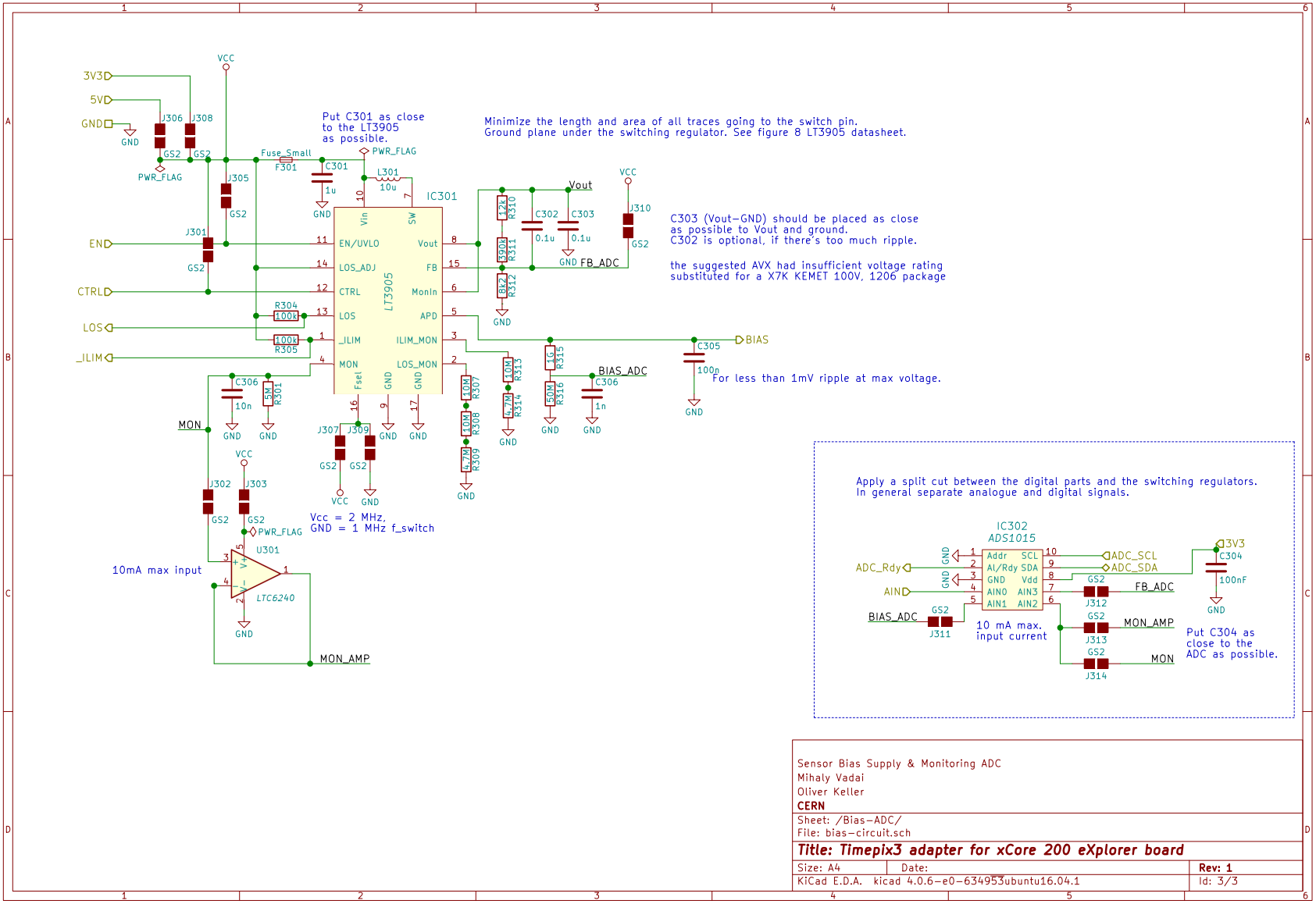

Figure 30: Prototype bias circuit schematic. Jumper pads were included to enable and disable options in the prototype. The comments are based on layout recommendations with the aim of isolating the high frequency switching path.

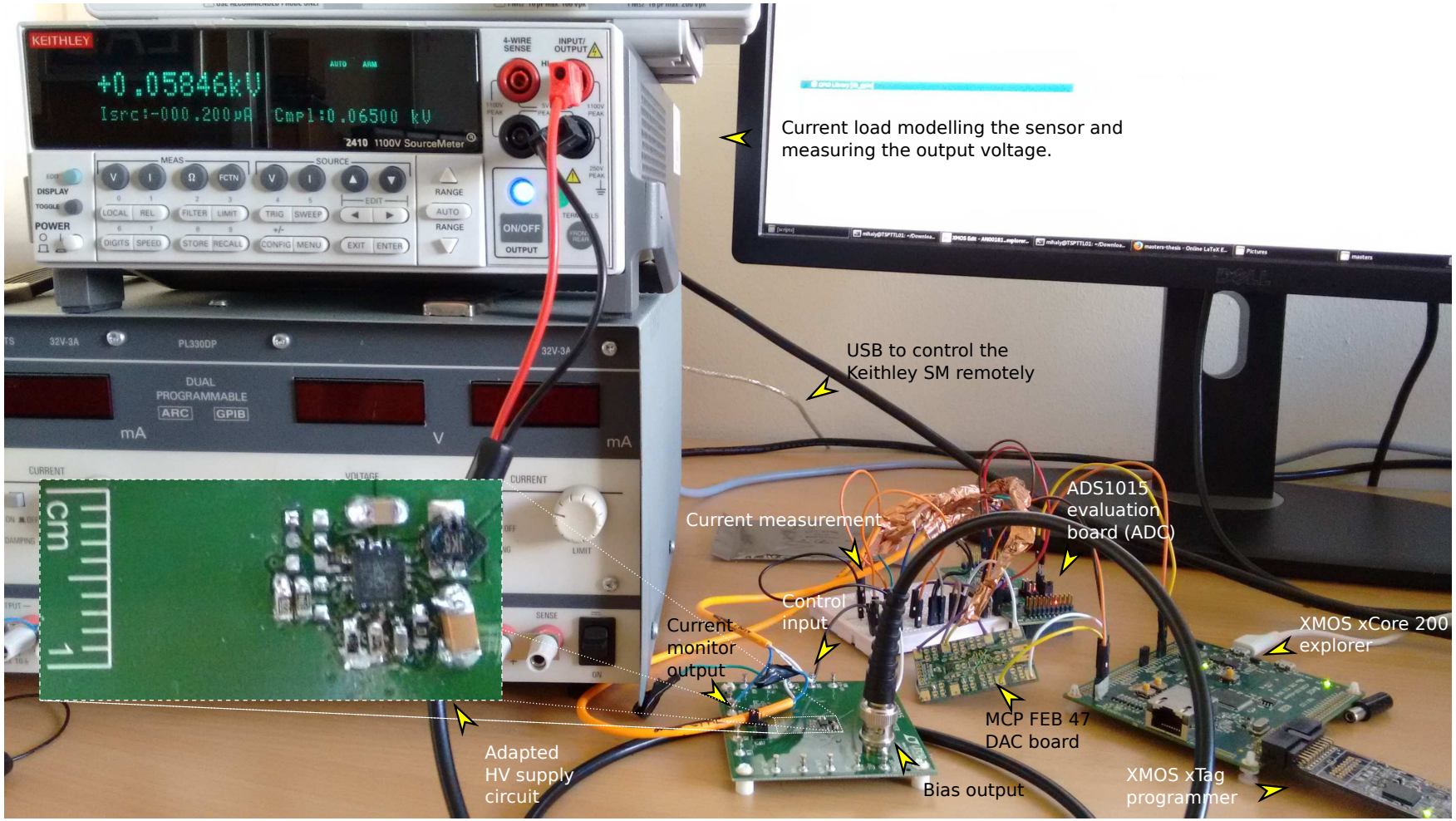

Figure 31: Picture of the working setup. The bias supply is connected to the Keithley SourceMeter drawing $200nA$ with the supply output being $58.46V$. The ADC is measuring the output voltage of the current monitoring circuit and DAC is controlling the HV output voltage from the XMOS microcontroller. It is at its maximum setting in the picture.