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A 2.5V Step-Down DC-DC Converter for Two-Stages Power Distribution Systems

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A prototype second-stage buck DC-DC converter has been designed in 130 nm CMOS and fully characterized. This circuit provides up to 3 A at an adjustable output voltage of 0.6-1.5 V from an intermediate bus voltage of 2.5 V. Hardening-by-design techniques have been systematically used, and the prototype successfully passed TID irradiation up to 200 Mrad (SiO_2) and Single Event Effects tests with a heavy ion beam. Safe integration on-board requires an optimized PCB design and bump-bonding assembly to reduce parasitic inductances along the input current path.

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1. Introduction

The High-Luminosity-LHC experiment upgrades require more power-hungry front-end circuits, while the material used must be minimized. In such context, an efficient power distribution system is required to limit the size of the power cables and the thermal load for the cooling system. Therefore, a power distribution scheme that employs point-of-load DC-DC converters was proposed [1]: a 12 V line runs up to close proximity to the sensors and is fed into DC-DC converters, which provide the required low voltage to power the front-end circuits. These converters use an ASIC and a few discrete components. The environment in which such DC-DC converters are placed requires them to be radiation and magnetic field tolerant.

Some detector systems in the upgraded LHC experiments need multiple voltage domains on a single compact module. In particular, optoelectronics circuits, front-end analog and digital circuits require respectively a power supply voltage of 2.5 V, 1.2 V and 1 V. In such cases, a highly-efficient and light power distribution scheme can use two stages of conversion: a first-stage converter steps down the voltage from 12 V to 2.5 V, powering the optoelectronics components and feeding two second-stage converters. The two second-stage ASICs can be identical, while their output voltage can be adjusted by means of an external component to provide the 1.2 V and the 1 V voltages.

This work focuses on the second-stage converter: the main features of its design are presented in Section 2, while the characterization results of the first prototype are shown in Section 3. Section 4 is devoted to the main improvements included in the second prototype.

2. Design

The second-stage converter must be able to step down from 2.0 ÷ 2.5 V to 0.6 ÷ 1.5 V, providing a maximum output current of 3 A. The high magnetic field in the LHC experiments (up to 4 T) requires the use of bulky air-core inductors. The architecture of choice is the buck configuration: it employs a single inductor, whose size can be made sufficiently small (<150 nH according to the specifications) by using switching frequencies in the MHz range. The first prototype converter features a programmable switching frequency between 4 and 8 MHz, using inductors of 47 to 100 nH. A conventional voltage-mode control is used (see Figure 1).

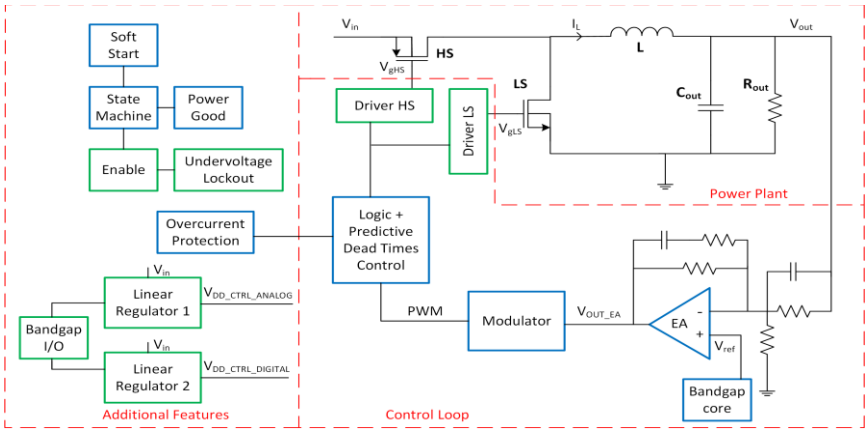

Figure 1. Block diagram of the second-stage DC-DC converter.

Radiation tolerance specifications include 150 Mrad of Total Ionizing Dose (TID), a fluence of $4 \cdot 10^{15}$ n/cm^2 for Displacement Damage, and no Single-Event-Effects-induced destructive events and output power interruptions up to a Linear Energy Transfer (LET) of 40 MeV·cm^2/mg. The ASIC is developed in a 130 nm technology, and the radiation tolerance specifications have been addressed by using hardening-by-design techniques. In particular, Enclosed Layout Transistors (ELTs) and p+ guard rings are used to suppress the TID-induced leakage currents [2]. Overly-sized logic gates, logic triplication, and a novel architecture for the modulator exhibiting a fast recovery time from a particle hit were used to make the circuit Single-Event-Upset-tolerant. Abundant and regularly distributed n+ and p+ contacts have been employed to prevent Single-Event-Latch-Up. Displacement Damage is not an issue for MOS transistors, therefore the two on-chip reference voltage generator use Dynamic-Threshold-NMOS transistors (DTNMOS) rather than more conventional diodes or bipolar devices [3].

2.5 V-rated transistors have been employed in any circuit block powered by the input voltage, in particular the power train, while the 1.2 V supply for the control circuitry is provided by two embedded linear regulators, one for the analog and one for the digital domain. Because of that, the delicate control circuits can take advantage of the improved radiation tolerance of the 1.2 V-rated transistors. The action of linear regulators also suppresses the noise coming from the output ripple of the first-stage converter, allowing looser specifications in terms of Power Supply Rejection Ratio for the control circuitry.

Substrate parasitic devices such as bipolar transistors and thyristors can lead to enhanced substrate noise disturbing the control circuitry, they can degrade the efficiency and even cause the failure of the converter by latch-up. Dedicated test structures to evaluate such effects and to allow the choice of the optimal floor-plan have been included in the first prototype. The results of this study are presented in details in [4].

The large switching input currents that are inherent to the functionality of the buck converter can raise reliability concerns: large dI/dt are experienced by the bonding and PCB parasitic inductors placed along the input current path, and this causes over-voltages that challenge the reliability of the used 2.5 V-rated devices. It is therefore crucial to have the circuit bump bonded rather than wire bonded to minimize the parasitic inductance of the bonding. In addition, the slew rate in the commutation of the power transistors has been reduced to decrease the value of dI/dt experienced by the parasitic inductors. This latter measure is nevertheless detrimental for the converter efficiency, since it leads to increased switching losses. An on-chip Track & Hold circuit has been designed to allow the direct measurement of the switching voltage peaks, and verify that they do not exceed the technology safe operating area.

3. Measurement results

3.1 Electrical characterization

The regulation performances of the first prototype are depicted in Figure 2a: the converter exhibits a line regulation $\Delta Vout/\Delta Vin < 7$ mV/V, and a load regulation $\Delta Vout/\Delta Iout < 3$ mV/A.

The peak efficiency obtainable using a 100 nH inductor and setting Vin = 2.5 V is 89.1% for Vout = 1.2 V and 85.6% for Vout = 1 V (see Figure 2b). These figures become respectively 86.6% and 82.3% if the inductor size is lowered to 47 nH: in such conditions, the switching frequency

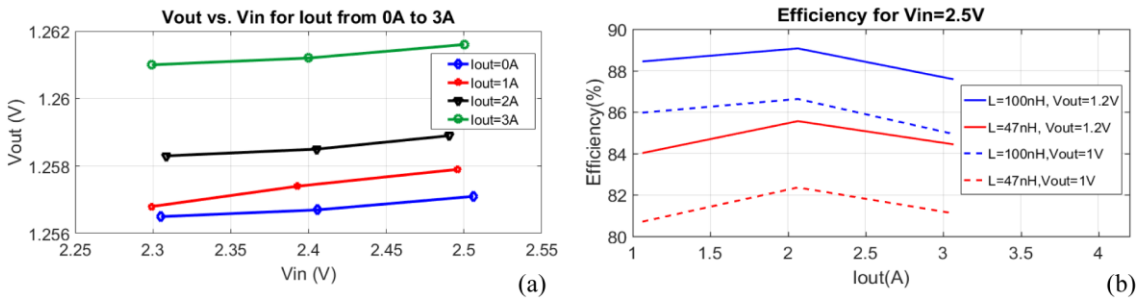

Figure 2. Measured regulation performance (a) and efficiency (b) of the designed prototype.

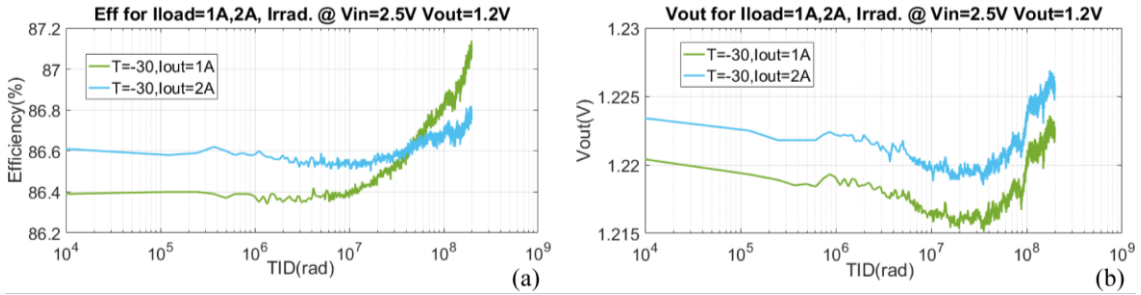

Figure 3. Evolution with TID of the converter efficiency (a) and of its output voltage (b) at -30°C.

must be increased from 4 Mhz to 8 MHz to keep the same peak-to-peak inductor current, not to compromise the reliability of the circuit. Therefore, the lower efficiency arises from the larger switching losses linked to the higher switching frequency.

3.2 Radiation characterization

An X-ray system has been used to irradiate the circuit up to 200 Mrad (TID). Figures 3a and 3b respectively show the evolution of the efficiency and of the output voltage with TID at -30°C (which is the expected temperature in the final application). The efficiency slightly increases with TID. Considering the larger increase at lower load currents, such variation suggests that a radiation-induced reduction in the switching losses occurs. The output voltage changes only by few tens of mV up to 200 Mrad, and reflects the TID-induced changes in the reference voltage generators. The circuit appears to be compliant with TID specifications.

Irradiation with heavy ions up to a LET of 54 MeVcm^2/mg excluded the presence of destructive SEEs or undesired resets in the LHC environment, where the maximum LET of recoils from nuclear interaction in Si or SiO_2 is below 15 MeVcm^2/mg [5]. Extending the test to higher LETs (above 40 MeVcm2/mg) also covers the more unlikely event where a fission recoil from nuclear interaction in the tungsten used in the metallization layers reaches the sensitive region of the device.

3.3 Over-voltages

The on-chip peak values of V_{in}-V_{ss} have been measured by the Track & Hold circuit introduced in Section 2. Figure 4 shows the measured voltages peaks reached at the two commutation instants. Such peak values do not raise concern for the reliability of the circuit.
Nevertheless, premature failures occur in case the converter is rapidly switched on and off multiple times due to the action of the Undervoltage-Lockout (UVLO) protection. A sudden decrease in the converter efficiency has been found when this occurs. A plausible explanation of such failures is linked to the instant in which the circuit is switched on again after the UVLO

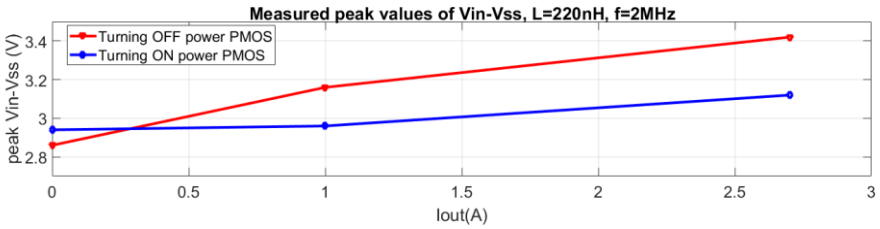

Figure 4. Measured on-chip V_{in}-V_{ss} peaks at the two commutation instants for different values of I_{out}.

circuit is released: it may occur that the DC-DC converter is turned on before the output voltage has dropped to 0, and this causes a large negative current to flow through the inductor during the start-up phase. Turning off the power NMOS while such negative current is flowing leads to large over-voltages on its V_{ds}, causing the failure of the device.

4. Improvements in the second prototype

A second prototype has been designed, with the main goal to make the circuit immune to the early failures described in Section 3.3 and to introduce additional features (such as the over-current protection). The commutation speed of the NMOS power transistor during the start-up phase has been significantly reduced, in order to lower the peak voltages reached at large negative inductor currents. In parallel, an optimized PCB layout has been developed that reduces the Vin-to-gnd parasitic inductance from 450 pH to 212 pH. Thus, a further reduction in the amplitude of the over-voltage peaks is expected.

5. Conclusion

A first prototype of the second-stage converter has been designed and fully characterized. The circuit shows good regulation performance and a peak efficiency of 89.1%. The irradiation campaign has highlighted no significant performance degradation up to a TID of 200 Mrad and tolerance to the expected values of LET for Single Event Effects. Early failures occur when the UVLO protection rapidly turns on and off the converter multiple times. Such failures have been linked to over-voltages that have been addressed by design modifications.

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