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A 2.56 GHz Radiation Hard Phase Locked Loop ASIC for High Speed Serial Communication Links

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This works presents the design and experimental study of a radiation hardened Phase Locked Loop (PLL) for high speed serial-communication links. These research results are used for the LpGBT (Low Power Gigabit Transceiver) chip which will be widely used for optical data-links between the detectors and the counting rooms in the HL LHC experiments. The PLL features a novel LC-oscillator architecture which is not sensitive to single-event transients. Additionally, the circuit uses triple-modular redundancy and is designed in a 65 nm CMOS technology.

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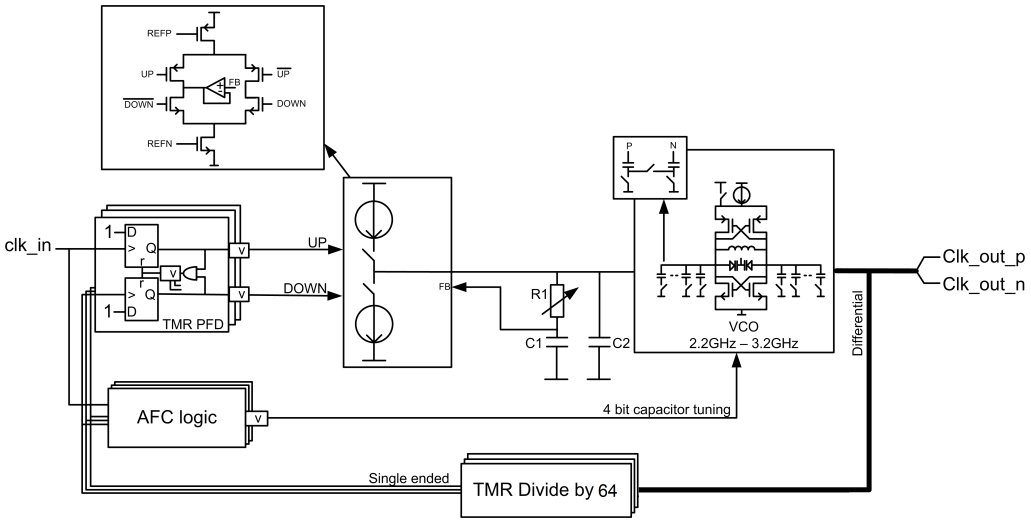

Figure 1: PLL block diagram.

1. Introduction

Future upgrades to the HL-LHC at CERN will demand ever-increasing data-rates from the detector modules to the counting rooms without an increase of the overall power consumption of the links. The LpGBT (Low Power Gigabit Transceiver), which is currently being developed, will make this speed available to the experiments with an up link data-rate of 10.24 Gbps and a down link data-rate of 2.56 Gbps which will be widely used in the different experiments around the LHC like ATLAS, ALICE, CMS and LHCb. This work presents the design of a radiation hardened Phase Locked Loop (PLL) that will be incorporated in the PLL/CDR of the LpGBT. To ensure the stability of the link, a small single-event upset (SEU) cross section is required and a Total Ionizing Dose (TID) resistance of 200 Mrad is targeted for the overall SoC. Furthermore, radiation hardened PLLs are mandatory in most timing systems in high-energy physics experiments like time-to-digital converters [1].

Many attempts were done before to harden PLLs [2][3]. However, it has been shown that deep sub micron CMOS technologies have an increased sensitivity to single-event effects [4].

2. PLL architecture

The architecture of the PLL which is used in this work is shown in Fig. 1. It includes an integrated LC-tank oscillator that is optimized for a low phase noise. This analog PLL is controlled by a radiation hardened phase-frequency detector (PFD) and triplicated divider to mitigate single-event upsets in the digital logic. The divider is synthesized using an enclosed layout transistor (ELT) standard cell library which has shown a degradation of less than 10 % across the targeted dose. The charge-pump produces up- and down current corrections to the loop filter which are proportional to the phase differences, detected by the PFD. It is essential for the PLL that the up- and down currents are closely matched to prevent additional spurious tones and static phase offsets. The output resistance of the current sources is further boosted with source degeneration

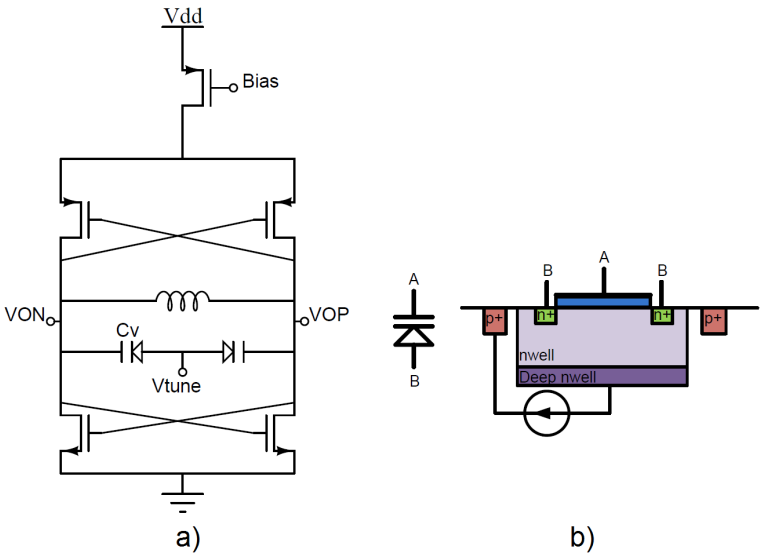

Figure 2: Commonly used oscillator architecture with direct varactor tuning.

to improve the current equality. An automated, all-digital frequency calibration algorithm uses a binary search after power-up to select the correct band of the oscillator such that the narrow tuning band aligns with the operation frequency of the PLL. This is essential since the center frequency of the oscillator is not constant across different process corners and needs an initial calibration with digitally controlled capacitors that are connected to the tank.

3. Radiation effects in CMOS LC-tank oscillators

Commonly, VCO circuits are based on the circuit that is shown in Fig. 2a. From an electrical point of view, this circuit has several advantages. Firstly, its tuning range is relatively large. At one node, the varactors are biased at the common mode voltages of the VCO and at the other node, they are biased at the PLL control voltage. This means that the voltage across the varactor can be tuned approximately from -Vdd/2 up to Vdd/2 which maximizes the capacitance variation across its tuning range since the sensitivity is maximal when the voltage across the varactor is zero.

Secondly, the PMOS tail current source limits the current consumption of the tank. However, this current source exhibits low frequency 1/f noise that can be upconverted to $1/f^3$ phase noise. Two mechanisms are present here. In the first case, due to an asymmetrical switching waveform, this noise gets upconverted around the oscillation frequency, similar to a mixer in RF systems. In the second case, the noise can also be upconverted through frequency modulation (FM) due to the varactors. As is the case in this circuit, the varactors are directly connected to the output node and any common mode voltage noise at the VCO output modulates the varactors which integrates this 1/f noise to phase noise. A PMOS is employed in this design since these devices induce significantly less 1/f noise compared to NMOS devices.

Previous work on this circuit has shown that this architecture exhibits a large sensitivity to single-event upsets due to the varactors' topology [5]. This can be explained from Fig. 2b. One node is connected to an nwell and the other node is connected to a gate terminal. The gate ter-

minal does not introduce any difficulties. However, the nwell is a p-n junction in the p-substrate which can capture charges due to ionizing particles. In particular, only currents from the nwell to the substrate. This problem was experimentally verified with heavy ions and two-photon laser experiments. These results showed a deviation to only one direction which can be explained from the currents, originating in the nwell junction. The nwell was in this case connected to the tuning voltage of the PLL such that the injected charges disturb the control voltage of the PLL. This results in frequency steps which are compensated by the PLL. However, the transient highly depends on the loop dynamics of the PLL.

4. Radiation hardened oscillator core

To mitigate the single-event transients in the varactors, a different tuning topology was presented. This circuit is shown in Fig. 3. In this implementation, the nwell of the varactor is biased to the ground potential (substrate potential) such that any remaining charges which are captured in the nwell junction are shorted through the ground terminal. In this case, the nwell cannot contribute to charge injection anymore. To tune the tank, an AC coupling is now required such that the DC bias voltage of the varactor can be set, independently from the common mode voltage of the LC-oscillator. In the proposed circuit, two coupling capacitors Cc are used to couple the varactors to the tank and a bias resistor Rb is added to bias the varactor at the control voltage of the PLL.

The addition of the coupling capacitors and the biasing resistors requires some special attention. Firstly the capacitors should be sufficiently large to ensure that the coupling factor between the varactors and the tank is enough. If these capacitors are too small, the effect of the varactor to the tank is reduced and the tuning range of the oscillator will reduce. However, care should be taken while sizing the capacitors. In practice, these capacitors also have a bottom-plate capacitance which is parallel to the varactor and also limits the tuning range. The optimal capacitor for this design was found to be between 6 to 10 times the varactors' capacitance in this technology. Secondly, the biasing resistor should not load the tank too much since it can reduce the quality factor of the tank resulting in a worse phase noise and a higher power consumption. On the other hand, a larger resistance adds noise through FM modulation of the varactors. Therefore, an optimal resistance exists that optimizes the phase noise and power consumption of the design. In this design, the resistance was 600 ohms but this number highly depends on de sizing of the tank and the oscillation frequency.

Heavy ion experiments were performed with an LET from 3.3 Mev.cm^2/mg up to 62.5 MeV.cm^2/mg. These experiments have shown that this architecture is insensitive to single-event effects which were again confirmed with laser charge injection. The cross section of the heavy ion experiments is shown in Fig. 4. This shows the measured cross section for the traditional LC-oscillator, a ring oscillator as a reference design and the improved LC-oscillator. For the improved oscillator, a shaded area is shown since no errors were measured. Therefore, we estimate that the real cross section is below this shaded area. The different values for the estimations are due to the different fluences that were measured for each ion. For our experiments, the ions around 10 MeV.cm^2/mg were most interesting and had the highest fluence. The estimated cross section is in this case 600 times smaller than the original design proving that this topology is a significant improvement for such RF integrated circuits.

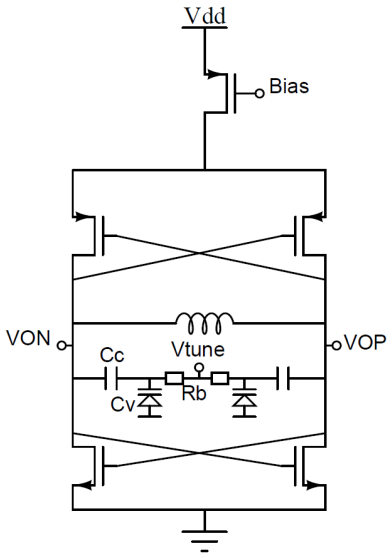

Figure 3: Radiation hard LC-tank oscillator.

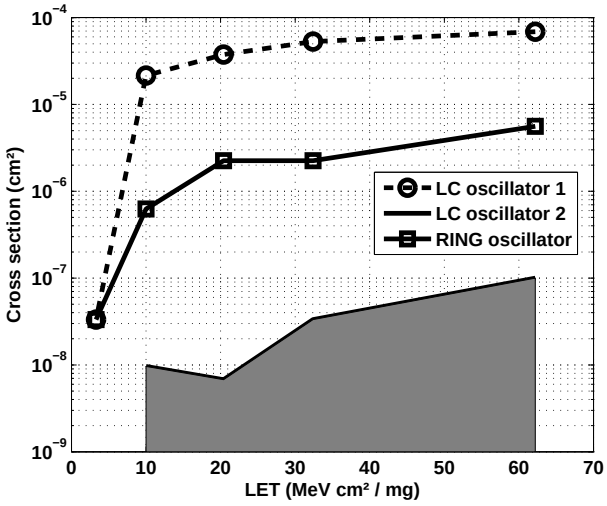

Figure 4: Cross section of the oscillator: a) Traditional LC-tuning topology, b) Ring oscillator with the same power consumption and c) Improved LC-tuning topology.

5. Measurements

The PLL was measured using a phase noise analyzer, both in open loop and closed loop. Since both the conventional oscillator and the improved architecture was processed, the noise measurements can be compared. In Fig. 5a, the open loop phase noise measurements of both oscillators is shown. It can be seen that no significant loss of performance is observed. The oscillator has a phase noise of -118 dBc/Hz at a 1 MHz offset frequency for a 2.56 GHz oscillation frequency. The closed loop PLL measurements are shown in Fig. 5b with a -110 dBc/Hz in-band phase noise. The total integrated jitter of the PLL with the improved oscillator is less than 0.5 ps rms.

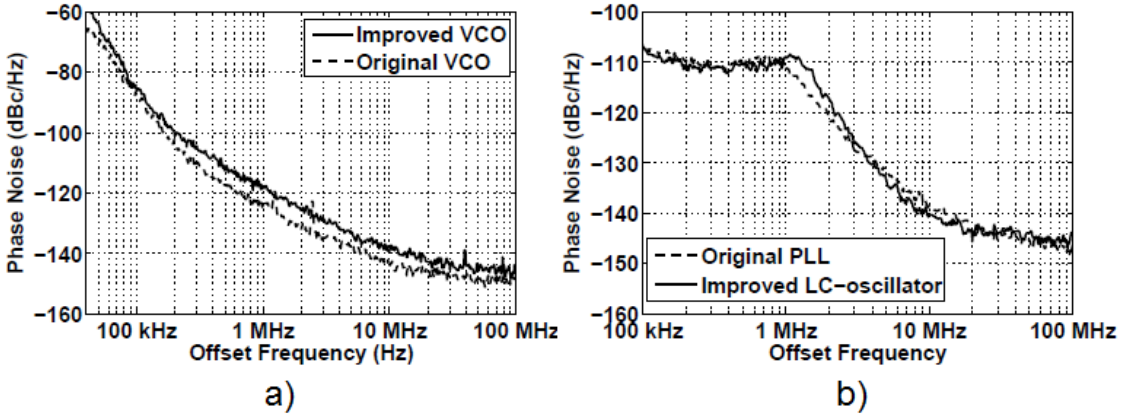

Figure 5: a) VCO open loop phase noise measurements. b) Closed l

6. Conclusion

This paper introduced a low noise and radiation hardened phase locked loop for high-speed serial data-links. The PLL uses triple-modular redundancy in the multi-GHz digital circuits to mitigate single-event upsets in the logic. It was shown that a conventional LC-tank oscillator experiences a high sensitivity to ionizing particles due to the varactors' nwell junction to the substrate. A radiation hardened by design oscillator was presented which is insensitive to single-event transients by using an innovative varactor topology. This mitigates the transient currents that originate in the nwell junctions by biasing them to the ground. The PLL was experimentally tested with heavy ions and two-photon laser experiments to verify the circuit techniques that are discussed in this work. The performance of the PLL was measured to have an integrated jitter of less than 0.5 ps at a power consumption of only 11.7 mW.

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