INTRA-TRAIN POSITION AND ANGLE STABILISATION AT ATF BASED ON SUB-MICRON RESOLUTION STRIPLINE BEAM POSITION MONITORS

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Abstract

A low-latency, sub-micron resolution stripline beam position monitoring (BPM) system has been developed and tested with beam at the KEK Accelerator Test Facility (ATF2), where it has been used to drive a beam stabilisation system. The fast analogue front-end signal processor is based on a single-stage radio-frequency down-mixer, with a measured latency of 16 ns and a demonstrated single-pass beam position resolution of below 300 nm using a beam with a bunch charge of approximately 1 nC. The BPM position data are digitised on a digital feedback board which is used to drive a pair of kickers local to the BPMs and nominally orthogonal in phase in closed-loop feedback mode, thus achieving both beam position and angle stabilisation. We report the reduction in jitter as measured at a witness stripline BPM located 30 metres downstream of the feedback system and its propagation to the ATF interaction point.

INTRODUCTION

The designs for the International Linear Collider (ILC) [1] and the Compact Linear Collider (CLIC) [2] require beams stable at the nanometre level at the interaction point (IP). In support of this, one of the goals of the Accelerator Test Facility (ATF2) at KEK, Japan, is to achieve position stability at the IP of approximately 2 nm. To this end, the Feedback On Nanosecond Timescales (FONT) project [3] operates a position and angle feedback system in the ATF2 extraction line [4]. In order to achieve the required level of position stability at the IP, the FONT feedback system needs to stabilise the beam to 1 μm at the entrance to the final focus system; this requires a BPM processing scheme capable of delivering position signals accurate to the sub-micron level on a timescale of the order of 10 ns.

The FONT beam position monitoring system makes use of three 12 cm stripline BPMs (P1, P2 and P3), which are located in the diagnostics section of the ATF2 extraction line and are placed on individual x, y movers (Fig. 1), and a witness stripline BPM (MFB1FF) located ~30 m downstream (Fig. 2). The BPMs are connected to specially developed analogue processing electronics [6] in order to deliver appropriate position signals to a digital hardware module [7] that digitises the signals and returns the sampled data to a computer where they are logged. The BPM system has achieved a demonstrated resolution of ~300 nm at a charge of $\sim 0.5 \times 10^{10}$ electrons/bunch [6].

BPM PROCESSOR DESIGN

A schematic of the processor module is shown in Fig. 3 and a photograph of a partially disassembled module is shown in Fig. 6. The operation is as follows: the top (V_T) and bottom (V_B) stripline BPM signals are subtracted using a 180° hybrid to form a difference (Δ) signal and are added using a resistive coupler to form a sum signal. The resulting signals are then band-pass filtered and down-mixed with a 714 MHz local oscillator (LO) signal phase-locked to the beam before being low-pass filtered

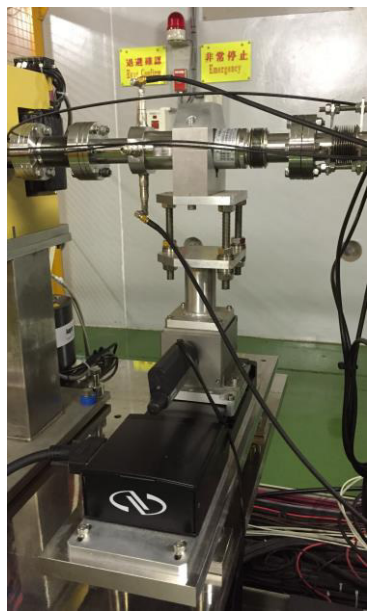

Figure 1: Photograph of the stripline BPM P3 and its mover.

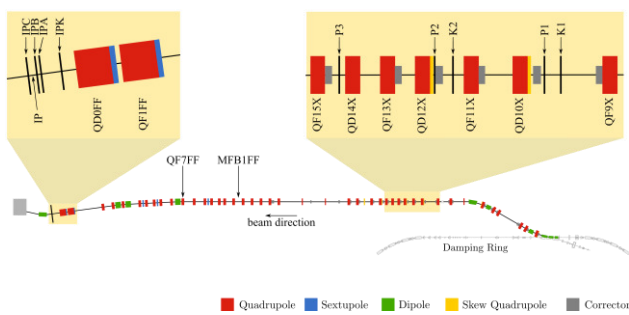

Figure 2: Layout [5] of the ATF2 extraction and final focus beamline with the FONT regions shown in detail.

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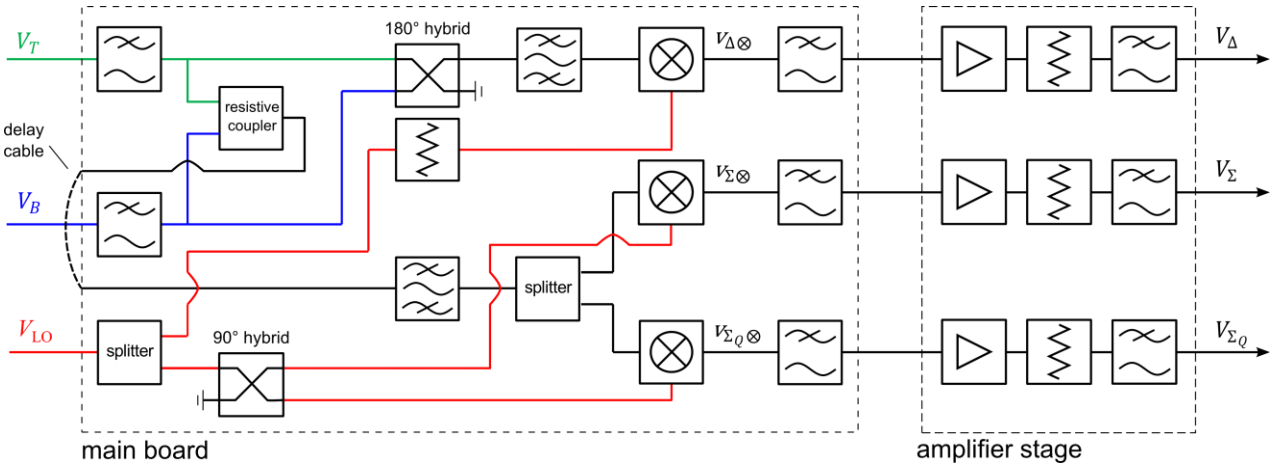

Figure 3: Schematic diagram illustrating the structure of the BPM analogue processor.

and amplified using 16 dB low-noise amplifiers. The hybrid, filters, and mixer were selected to have latencies of the order of a few nanoseconds in order to minimise the overall processor latency.

The phasing of the LO with respect to the beam signal is maintained using an adjustable phase shifter on the LO input to the processor (Fig. 4). In the sum channel, a 90° hybrid is used to downmix the raw sum signal with two orthogonal phases of the LO, producing an in-phase sum signal (Σ) and quadrature-phase sum signal (Σ_Q). The phase of the difference channel is accurately matched to that of the in-phase sum signal via a custom loopback cable in the sum channel. Hence the optimal phasing of both the Δ and Σ signals is achieved by minimising the Σ_Q signal.

The latency of the processor, that is the time interval between the arrival of the stripline signals at the inputs and the peak of the signals at the outputs, has been measured by using a test bench to provide realistic beam proxy input signals and observing on an oscilloscope the arrival time of the processed output signal. Subtracting from this the time of arrival at the oscilloscope of the input when the processor is bypassed, the processor latency before the amplifier stage was found to be 10.4 ± 0.1 ns, and 15.6 ± 0.1 ns including the amplifier stage (Fig. 5).

The three output signals (Δ, Σ, Σ_Q) from the BPM processor are digitized using analogue-to-digital converters (ADCs) on the FONT5 digital board, capable of converting at up to 400 MHz with 14-bit resolution. Low-noise amplifiers, with a gain of 16 dB, built into the processor modules are used to boost the input levels to just above the digitiser noise floor, and hence maximise the dynamic range of the measurement system. The ADCs, and sampling logic of the FONT5 board's Field Programmable Gate Array (FPGA), are clocked in a system-synchronous mode at 357 MHz, this being a convenient frequency derived from the machine RF. The ADC clock may be delayed in increments of 70 ps to allow sampling at the exact time the bunch arrives. There are nine ADCs in total and so a single board is able to fully record the data from three BPMs.

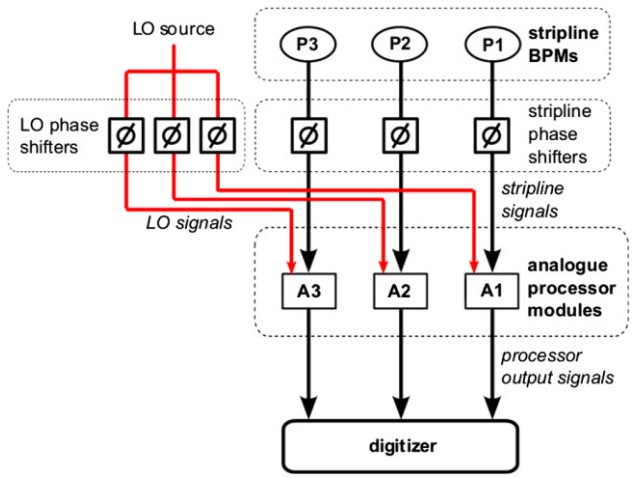

Figure 4: Schematic of the BPM system. For each BPM, a phase shifter is used on one of the stripline signals to adjust the relative path lengths of the two input signals at the BPM processor, and another phase shifter is used to adjust the phase of the LO signal at each processor.

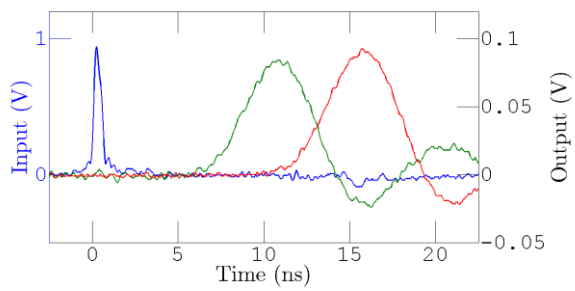

Figure 5: Input beam proxy V_T signal (blue, left-hand scale) and processor output V_Δ signal before the amplifier stage (green, right-hand scale, with factor 5 multiplication), and after the amplifier stage (red, right-hand scale), vs time.

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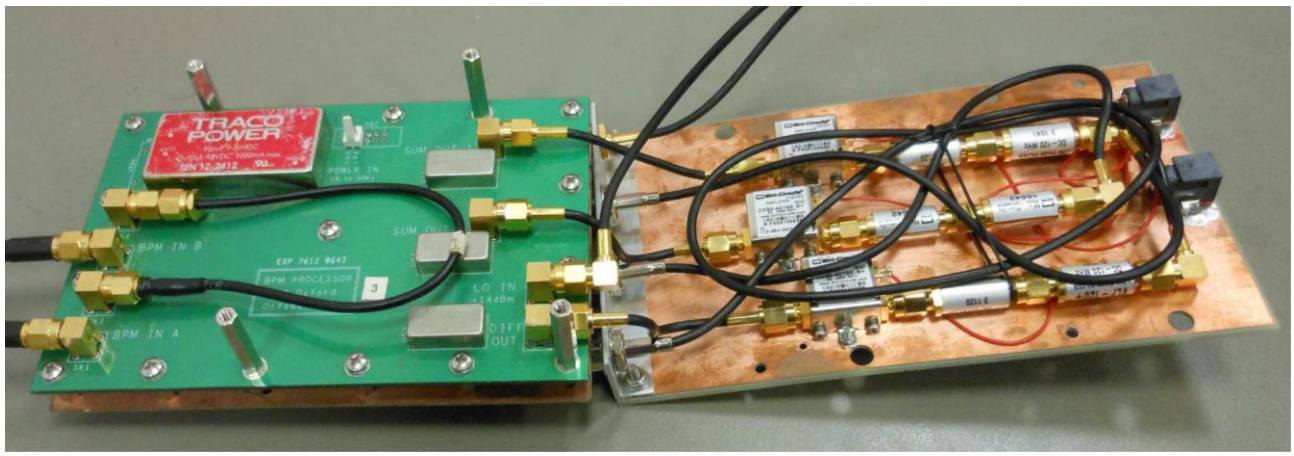

Figure 6: Photograph of the BPM analogue processor. The unit is partially disassembled for viewing purposes.

FEEDBACK RESULTS

Two stripline BPMs (P2 and P3) have been used to drive a pair of kickers (K1 and K2) local to the BPMs (Fig. 7) and nominally orthogonal in betatron phase, to form a two-phase closed-loop feedback system to stabilise the position and angle of the beam at the entrance to the final focus [8].

For these demonstrations, a beam consisting of two bunches separated by 182 ns was used. The feedback tests therefore involve measuring the vertical position of bunch one and correcting the vertical position of bunch two. The system was typically operated in an 'interleaved' mode, whereby the feedback correction was toggled on and off on alternate machine pulses; the feedback 'off' pulses thereby provide a continual 'pedestal' measure of the uncorrected beam position. The feedback correction of the beam was witnessed at MFB1FF.

Figure 8 shows the result of the feedback operation as measured at P2, P3 and MFB1FF. The position jitter is reduced from 1.6 µm to 610 nm at P2, and from 1.8 µm to 520 nm at P3. This factor of ~3 reduction in jitter is successfully preserved out to MFB1FF, with the beam jitter being stabilised from 30 µm to below 10 µm.

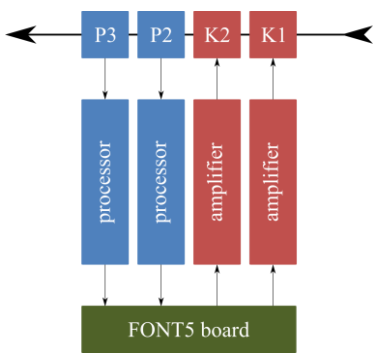

Figure 7: Block diagram of the feedback system.

Figure 10 shows the measured feedback performance at P2, P3 and MFB1FF as a function of bunch charge. Also shown is the expected jitter [9] that can be attained on operating the feedback (σ_{Y_2}) given the feedback off values for the position jitter of the two bunches (σ_{y_1}, σ_{y_2}) and the bunch-to-bunch position correlation ($\rho_{y_1 y_2}$):

$$\sigma_{Y_2}^2 = \sigma_{y_1}^2 + \sigma_{y_2}^2 - 2\sigma_{y_1}\sigma_{y_2}\rho_{y_1 y_2}. \quad (1)$$

The results show that the feedback successfully reduces the position jitter to the expected level given the measured incoming beam conditions.

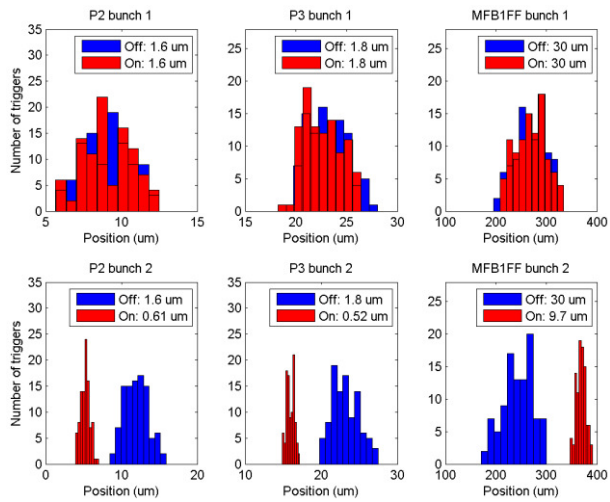

Figure 8: Distribution of the vertical position of bunches 1 and 2 in P2, P3 and MFB1FF with (red) and without (blue) application of the feedback correction. Values of the position jitter are quoted for each BPM.

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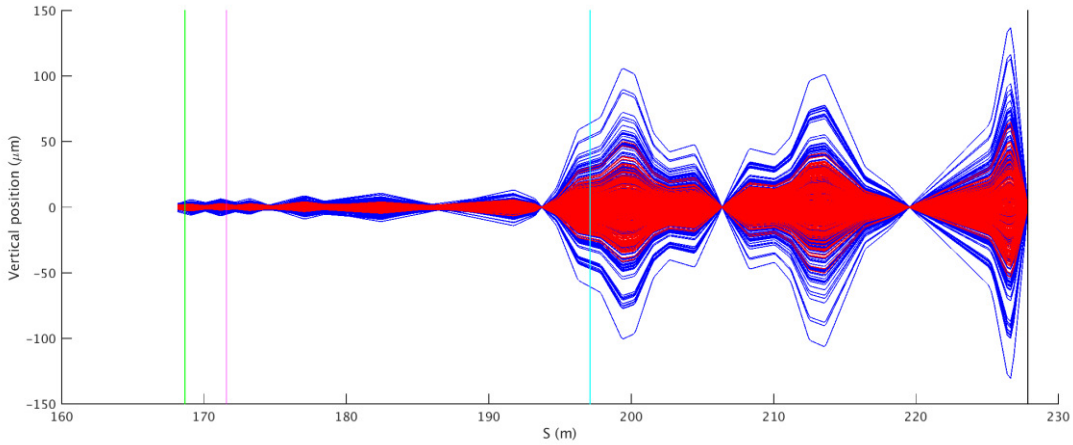

Figure 9: Vertical bunch position versus longitudinal distance S in the lattice, for an ensemble of triggers, propagated from measured positions at P2 and P3 for data with (red) and without (blue) application of the feedback correction. The vertical lines indicate the location of P2 (green), P3 (magenta), MFB1FF (cyan) and the IP (black).

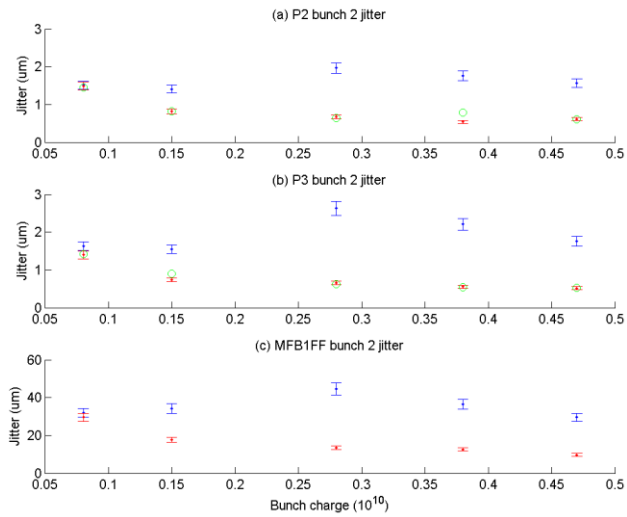

Figure 10: Bunch 2 position jitter measured in (a) P2, (b) P3 and (c) MFB1FF for a range of bunch charges with (red) and without (blue) application of the feedback correction. Expected jitter with feedback is shown in green.

The results at P2 and P3 have been propagated using vertical position and angle (y, y') transfer matrices through the ATF2 line to the IP. Figure 9 shows the result of propagating the measured vertical positions at P2 and P3 to the IP, illustrating the reduction in position jitter throughout the lattice on operating the feedback system.

CONCLUSIONS

Beam position and angle stabilisation has been demonstrated using a coupled-loop system consisting of two stripline BPMs and the two kickers in the ATF2 extraction line. Vertical beam stabilisation has been achieved at the 600 nm level locally at the feedback BPMs, and the propagation of the correction has been demonstrated in simulation and confirmed using a witness stripline BPM located approximately half way along the ATF2 line.

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