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LAPA, a 5 Gb/s modular pseudo-LVDS driver in 180 nm CMOS with capacitively coupled pre-emphasis

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A pseudo-LVDS driver has been designed in a 180 nm technology for operation up to 5 Gb/s. It contains parallel main driver units based on an H-bridge circuit steering a current on an external load. The number of active units is adjustable, to reduce switching capacitance and static current, and hence power consumption, if a smaller current swing can be tolerated. Pre-emphasis is applied with a capacitively coupled charge-injection circuit. In the nominal condition with a steering current of 4 mA over a 100 Ω termination resistor, it consumes 30 mW from a 1.8 V supply.

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1. Introduction

The HL-LHC upgrade will see the first collisions in mid-2026, bringing the maximum instantaneous luminosity from the current value of $\sim 1 \times 10^{34}\ cm^{-2}s^{-1}$ to $\sim 7.5 \times 10^{34}\ cm^{-2}s^{-1}$. The High-Luminosity LHC upgrade will also require an upgrade of several subsystems of the ATLAS experiment [1]. The new Inner Tracker (ITk) [2] will substitute the actual Inner Detector (ID) and will be made entirely of silicon detectors. One possible technology under study is CMOS monolithic silicon pixel detector. After the ALPIDE monolithic sensor was successfully implemented in the TowerJazz 180nm CMOS imager technology [3], and promising irradiation results [4] were obtained modifying this process [5], an ATLAS-specific development in this modified process was started. As part of the development, a 5GB/s pseudo-LVDS driver has been designed. The pseudo-LVDS for ATLAS Pixel Apparatus (LAPA) is made of parallel H-bridge units that steer a current on an external load.

2. The LAPA pseudo-LVDS driver

The output driver is based on the LVDS standard transmission protocol TIA/EIA 644 [6], with a modification of the common mode voltage V_{CM}, equal to 0.8 V instead of 1.2 V of the standard. The power supply of 1.8 V combined with a reduced V_{CM} allows optimizing the PMOS size in respect of speed performances and power consumption.
LAPA can drive up to 6 mA, in the nominal condition with a steering current of 4 mA over a 100 Ω termination resistor, it consumes 30 mW from a 1.8 V supply with an input clock of 2.5 GHz. 40 drivers have been embedded in the MALTA (Monolithic from ALICE to ATLAS) chip and 10 in a dedicated test chip, both submitted in September 2017. The pseudo-LVDS contains a main driver, a pre-emphasis circuit and the common mode voltage can be internally held to the nominal value via a feedback regulation.

2.1 Main driver

The main driver is based on an H-bridge scheme that steers the current on the external output load, with a different approach in respect of the most common LVDS schemas using switchable current sources [7]. Each half branch of the H-Bridge has a three transistor circuit that acts as a switchable current source, as shown in Fig. 1. The transistor defining the OFF current I_{off} is in series with the transistor defining the ON current I_{on}. Another transistor, operated as a switch, is in parallel with the transistor defining the OFF current. When the switch is in the OFF state, the half branch output current is limited to I_{off}, and when it is ON, the output current is limited to I_{on}. I_{off} allow the circuit to switch faster and define the operating point in the OFF status of each branch. This scheme avoids a current source in series with the H-bridge, resulting in a larger operating margin above saturation, allowing a reduction in transistor size (width) and hence dynamic power consumption. Referring to the schematic in Fig. 1, the OFF current I_{off} is defined by the voltage reference VpH and VnL, for the PMOS and the NMOS transistors respectively; the ON current I_{on} instead is defined by the voltage references VpL and VnH. The total current over the load will be $I_L = I_{on} - I_{off}$ and the direction will be steered when switching.

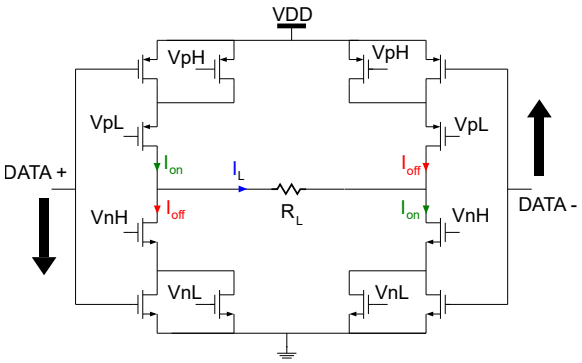

Figure 1: *Schematic of the main driver.*

The main driver consists of seven driving units operating in parallel. The number of active units can be varied to drive the required static current, hence optimizing the dynamic power consumption. Each driving units can drive up to 0.85 mA.

2.2 Capacitively coupled pre-emphasis circuit

Speed performance can be improved applying pre-emphasis with a capacitively-coupled charge injection circuit [8]. A similar approach as been developed in the VeloPix chip for the LHCb experiment upgrade [9]. LAPA integrates 16 independent capacitively-coupled charge injection circuits, which can be activated or not. Each circuit consists of a CMOS buffering stage that drives a coupling capacitance of 25 fF. The pre-emphasis strength is so tunable to optimize the performance in terms of speed and dynamic power consumption, depending on the external load of the driver. The pre-emphasis schema is summarized in Fig. 2. The layout is carefully optimized to reduce the parasitic capacitance of the buffering driving node and the overall output pad capacitance.

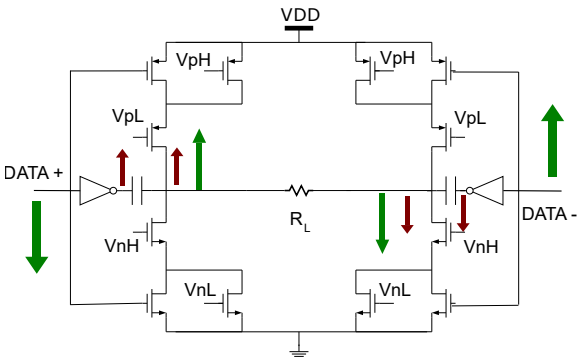

Figure 2: *Schema of the pre-emphasis. An inverting stage driven by the same data that drives the main driver is directly capacitively coupled to out pads. The effect of the pre-emphasis on the output is represented in red.*

2.3 Common mode feedback

The driver is optimized to operate with a 400mV differential output voltage, with a nominal

I/O	SPEC	Min	Max	Nom
LVDS IN	V_{CM}	0.8 V	1 V	0.8 V
LVDS IN	V_{diff}	0.3 V	-	0.4 V
LVDS IN	T Res	-	-	100 Ω
LVDS IN	bit rate	-	-	5 GBit/s
CMOS IN	bit rate	-	-	5 GBit/s
CMOS OUT	bit rate	-	-	2 GBit/s (0.5pF parasitic load)
LVDS OUT	V_{CM}	-	-	0.8 V
LVDS OUT	V_{diff}	-	-	0.4 V
LVDS OUT	Iout	0.8 mA	6 mA	4 mA
LVDS OUT	T Res	-	-	100Ω
LVDS OUT	bit rate	-	-	5 GBit/s (1pF parasitic load)

Table 1: Expected specifications for each component of the chip.

common mode voltage V_{CM} equal to 0.8 V. The ON current I_{on} of the PMOS can be regulated in an arbitrary number of main driver units using a feedback amplifier that locks the V_{CM} at the nominal value.

3. Chip implementation

The pseudo-LVDS has been developed to fit the ATLAS ITk requirements [10]. The innermost layer will require an average data rate of 1 GB/s, with peaks of 5 GB/s.
The MALTA chip integrates 40 LAPA drivers, and the maximum output data rate is limited by MALTA at 1 GB/s per channel. In the MALTA chip, the configuration of the output buffer is given by a slow control digital block with five separated four-bits DACs that regulate the biases of LAPA. To test the performance of the driver, that has been designed work up to 5 GB/s, a test chip has been submitted together with MALTA. In the test chip ten data transmission channels are implemented, with LVDS/CMOS input and pseudo-LVDS/CMOS output. The specifications of the test chip are summarized in Tab. 3. The chip works as a repeater, an input signal can be applied to the LVDS or CMOS input to characterize the pseudo-LVDS buffer measuring the output.

3.1 Simulation results

The performance have been simulated as a stand-alone circuit as well as integrated into the MALTA chip and the test chip. Fig. 3 shows the eye diagram of a post-layout simulated response of one of the differential channel of the test chip.

4. Conclusion and future plans

LAPA is a pseudo-LVDS output buffer that has been designed in 0.18 μm CMOS technology, following the requirement for the ATLAS inner tracker detector upgrade. The simulations of the driver have to be confirmed by measurements on a test chip that will be back from the foundry at the beginning of 2018. The measurement aims to confirm the performance of the driver in terms

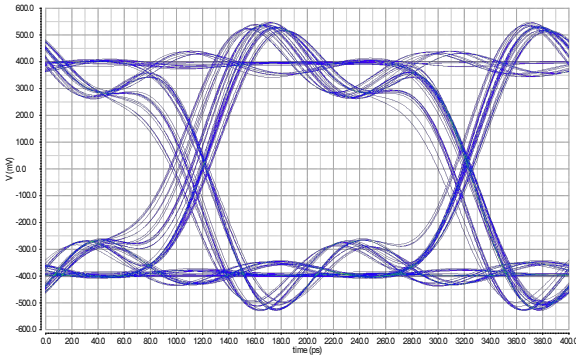

Figure 3: *Eye diagram of the simulated response of the LAPA pseudo-LVDS driver integrated in a channel of the test chip. The input is a 2.5 GHz differential signal of 400 mV, with 50 ps of rising/falling time, V_{CM} of 0.8 V. The simulated peak to peak jitter is 45 ps.*

of speed, 5 GB/s, and power consumption, 30 mW with an input clock of 2.5 GHz. The design of a next iteration of the driver has already started, to allow the driver to work with AC coupling, as required by the upgrade of the ATLAS pixel system.

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