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Development of Telescope Readout System based on FELIX for Testbeam Experiments

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The High Voltage CMOS (HV-CMOS) sensors are extensively investigated by the ATLAS collaboration in the High-Luminosity LHC (HL-LHC) upgrade of the Inner Tracker (ITk) detector. A testbeam telescope, based on the ATLAS IBL (Insertable B-Layer) silicon pixel modules, has been built to characterize the HV-CMOS sensor prototypes. The Front-End LInk eXchange (FELIX) system is a new approach to function as the gateway between front-ends and the commodity switched network in the different detectors of the ATLAS upgrade. A FELIX based readout system has been developed for the readout of the testbeam telescope, which includes a Telescope Readout FMC Card as interface between the IBL DC (double-chip) modules and a Xilinx ZC706 evaluation board. The test results show that the FELIX based telescope readout system is capable of sensor calibration and readout of a high-density pixel detector in test beam experiments in an effective way.

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1. Introduction

The ATLAS experiment is planning to build a new all-silicon Inner Tracker (ITk) for the High-Luminosity LHC (HL-LHC) [1]. The High Voltage CMOS (HV-CMOS) sensors are extensively investigated for multiple advantages compared to the traditional planar pixel detectors [2]. A IBL (Insertable B-Layer) DC (double-chip) module based testbeam telescope has been built to test HV-CMOS sensor prototypes [3, 4]. The Front-End LInk eXchange (FELIX) is a system to interface the front-end electronics and trigger electronics for several detectors in the ATLAS Phase-I and HL-LHC upgrade [5, 6, 7]. A new FELIX based readout system has been developed for the testbeam telescope sensors.

2. Readout System Overview

This FELIX based readout system includes a Xilinx ZC706 evaluation board and an interface board of Telescope Readout FMC Card in the front end. The block diagram of test setup is shown in the Figure 1. The Telescope Readout FMC Card is connected to the ZC706 through FMC connectors. And RJ45 Cat6 cables are used for connecting six IBL DC modules and the Telescope Readout FMC Card. There are two GBT links between the front end and the FELIX in the back end: one is used to distribute the clock signal for synchronization, and the other is for data transmission [8] [9]. The FE-I4B output data from the IBL modules are mapped to the 4-bit Elinks directly in the GBT frame. The FELIX is configured of direct mode for the from-host data direction, and 8b10b mode for the to-host direction. The received FE-I4B data will be 8b10b decoded in the FELIX firmware, before sending to the PC through PCIe express [10]. The FELIX low-level software is responsible for issuing all the control commands and continuously storing all the pixel data from the front end for off-line analysis.

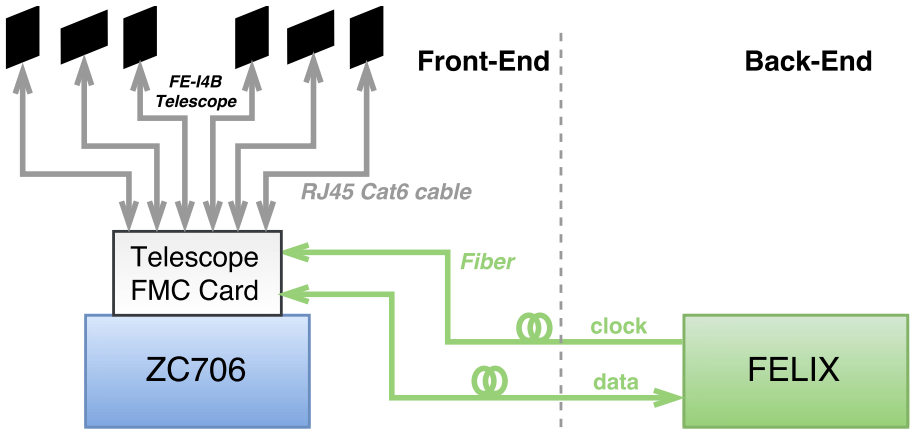

Figure 1: Test Setup of Telescope Readout with the FELIX

3. Telescope Readout FMC Card

The interface Telescope Readout FMC Card, as shown in the Figure 2, is placed between IBL DC modules in the testbeam Telescope and the ZC706 board. This board is connected to the ZC706

through FMC connectors and receives power from a single external 12 Volt power supply. There are 12 RJ45 ports for connecting to all of the six IBL DC modules. A clock chip of Si5345 is implemented on board in order to improve the quality of recovered clock from the FELIX GBT link. This clock chip can be configured by the FELIX low-level software through the GBT links. The Telescope Readout FMC Card also consists 4 SFP connectors for GBT link. There is no error in the Xilinx IBERT test in the data rate of 9.6 Gb/s. The I2C bus on the Telescope Readout FMC and the ZC706 can be accessed by the FELIX GBT links. The hardware design of the Telescope Readout FMC Card has been verified, including the power rails, I2C bus, Si5345, SFP connectors, LVDS repeaters, etc.

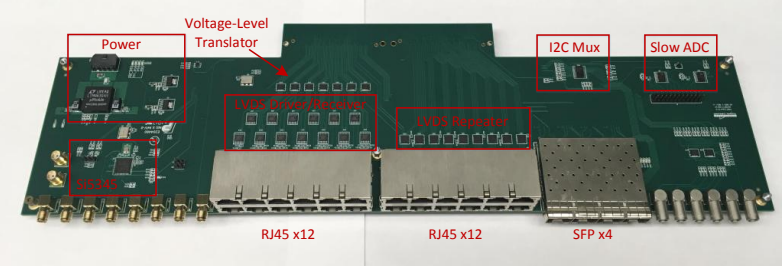

Figure 2: Telescope Readout FMC Card

4. Test Results

4.1 FE-I4B Tuning

The FELIX based DAQ system can control and readout the FE-I4B chip in the IBL DC modules effectively. The ZC706 firmware is 'transparent' for the FE-I4B input command and output data, which are connected to the GBT frame directly. The Idelay in the ZC706 FPGA is configured in order to guarantee a good phase relationship between the FE-I4B serial output data and the reference clock. The FE-I4B global registers, shift registers and in-pixel registers can be read and written by the FELIX low level software.

Since each FE-I4B pixel has an independent, free running amplification stage with adjustable shaping, followed by a discriminator with adjustable threshold, the tuning test should be carried out to eliminate the threshold and feedback current variance between pixels before using it to read out the signals from the sensor.

The tuning procedure includes global threshold scan, TDAC scan, FDAC scan and TDAC-rescan [10]. In all these scan tests, binary search is applied in order to optimize the tuning speed. The time needed for the whole tuning test is less than 2 minutes. The tuning results of threshold distribution is showed in Figure 3. The effective threshold deviation after tuning is around 77 electrons which is consistent to the specification of the FE-I4B [10].

4.2 Testbeam Results

The FELIX based DAQ system has been deployed in testbeam at the H8 beamline of the CERN Super Proton Synchrotron (SPS) during August 2017. It was used to control and readout all of the

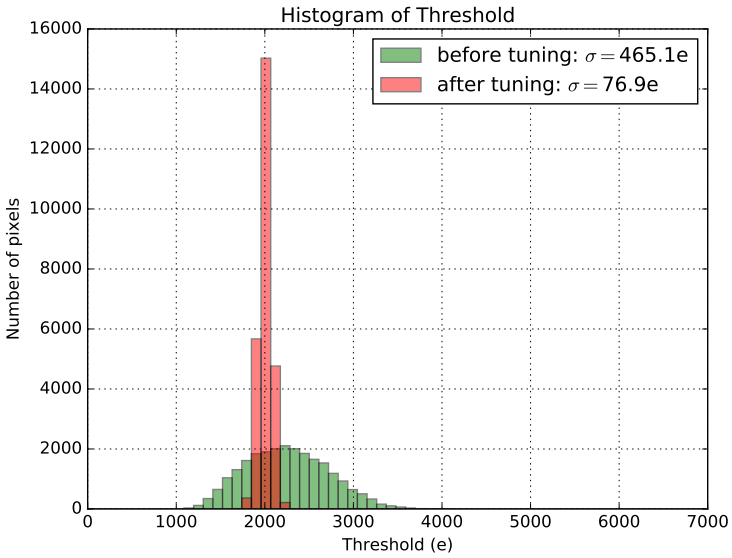

Figure 3: FE-I4B Threshold Distribution

six IBL DC modules in the testbeam Telescope. A logic AND signal of the Hitor signals from the front and bottom IBL DC modules was generated in the ZC706 firmware, which was sent to the FELIX. The FELIX generated the trigger command when receiving the Hitor AND signal from the front end. A photograph of the testbeam setup is shown in the Figure 4. The hit map of the testbeam data is shown in the Figure 5. The FE-I4B chip hosts a pixel matrix of 336 rows by 80 columns. Each pixel size is 250 μm x 50 μm. The spot area shown in the Figure 5 are pixels fired by the beam.

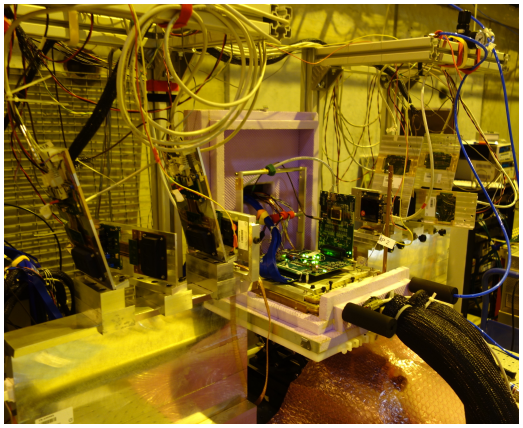

Figure 4: Testbeam Setup

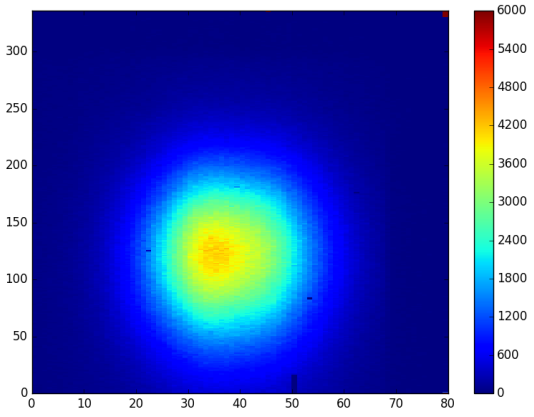

Figure 5: Hit Map of Testbeam Data

5. Conclusion

The FELIX based DAQ system has been developed for control and readout of the IBL DC

modules in the testbeam Telescope. An interface board of the Telescope Readout FMC Card has been designed for communication between the testbeam Telescope and the ZC706 board. The test results show that this DAQ system can carry out the FE-I4B tuning test efficiently. This DAQ system was employed successfully in testbeam at the CERN SPS during August 2017. It has been proved to be effective to readout the testbeam data with high trigger rate.

References

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