The Development of the Global Feature eXtractor (gFEX) for ATLAS Level 1 Calorimeter Trigger at the LHC

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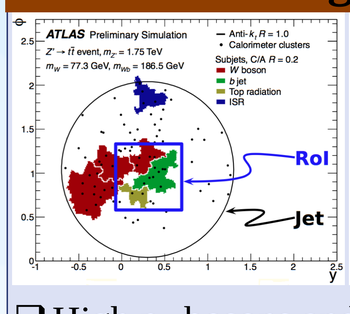
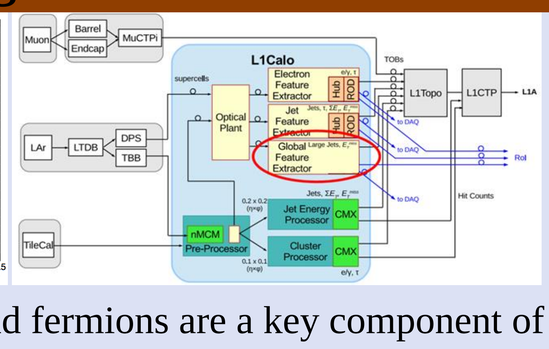
Abstract

As part of ATLAS Phase-I Upgrade, the gFEX is designed to help maintain the ATLAS Level-1 trigger acceptance rate with the increasing LHC luminosity. The gFEX identifies patterns of energy associated with the hadronic decays of high momentum Higgs, W, & Z bosons, top quarks, and exotic particles in real time at the 40MHz LHC bunch crossing rate. The prototype v1 and v2 were designed and fully tested in 2015 and 2016 respectively. A pre-production gFEX board has been manufactured, which is an ATCA module consisting of three UltraScale+ FPGAs and one ZYNQ UltraScale+, and 35 MiniPODs are implemented in an ATCA module. This board receives coarse-granularity (0.2x0.2) information from the entire ATLAS calorimeters on up to 300 optical fibers and 96 links to the L1Topo at the speed up to 12.8 Gb/s.

Motivation of gFEX

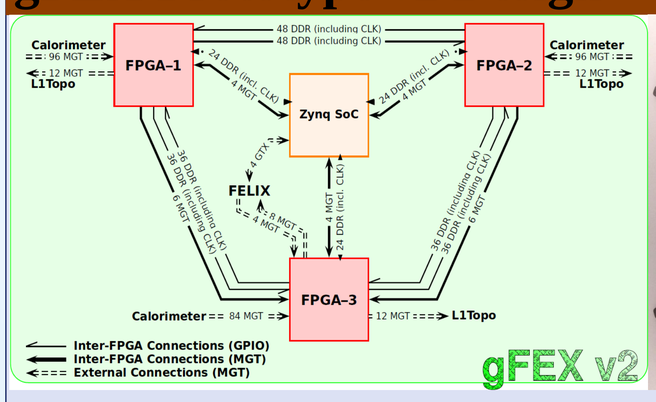


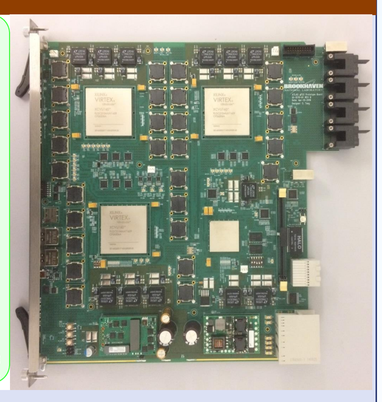


gFEX will be installed during the Phase-I upgrade (2019 – 2020), and will be used for triggering from 2021 onwards.

- ❑ High p_T bosons and fermions are a key component of ATLAS physics.
  - -- W, Z and H bosons, top quarks and exotic particles
  - -- Many analyses with boosted objects
- ❑ Analyses that addresses this physics use large R jets with R > 1
- ❑ Adding the gFEX, we can accept the boosted objects.

gFEX Prototype v2 Design

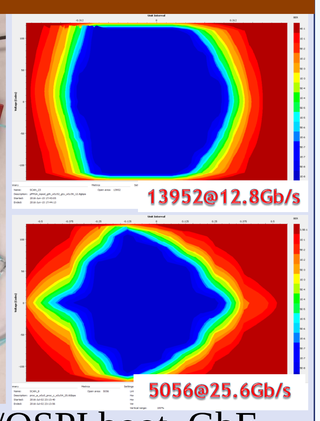




FEX v2 is a full function prototype with three Virtex UltraScale FPGA and one ZYNQ FPGA.

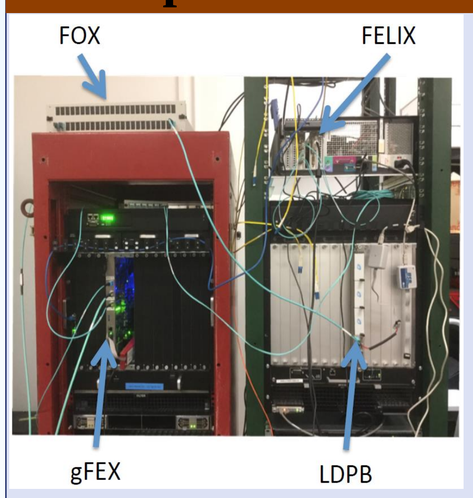
- ✓ Optical links interface with LAr LDPS and L1Topo are implemented
- ✓ MGT links and GPIOs for inter-FPGA communications
- ✓ 26-layer PCB with low loss material (Megtron-6) and back-drill for improved signal integrity

Evaluation Test at BNL



- ❑ All functions (JTAG, SD/QSPI boot, GbE, I2C, and Clock, etc.) are verified successfully
- ❑ MGTs speed test - All optical links are stable at 12.8Gb/s and all onboard electrical link are stable up to 25.6 Gb/s
- ❑ Nine groups of GPIOs are running at 1.12 Gb/s with good margin (>60%)

Link Speed Test at CERN

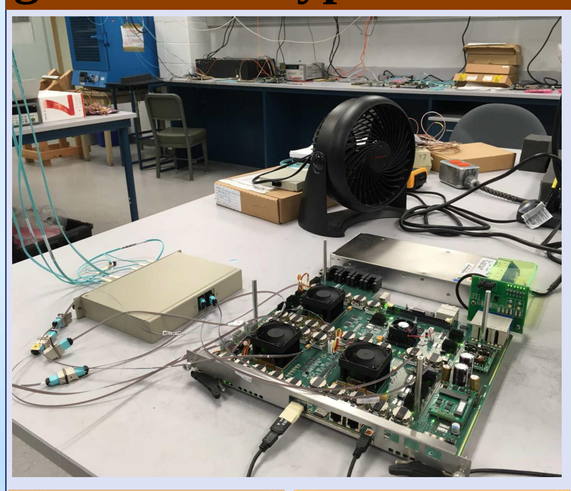


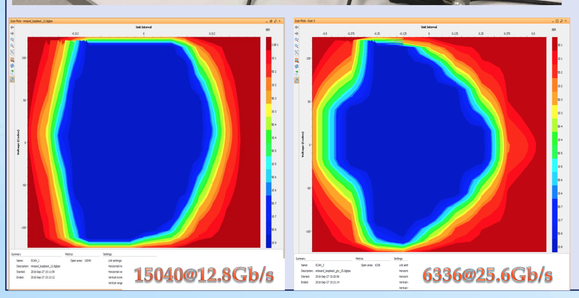
FOX: Fiber-Optic eXchange
FELIX: Front-End LInk eXchange (Readout Link)
LDPB: LAr Digital Processing Blade
TTC: Timing, Trigger and Control

48 links between LDPB and gFEX are successfully tested simultaneously at following conditions.

a. Link speeds at 6.4/9.6/11.2 Gb/s
b. One or two stages of FOX
c. TTC clock from FELIX

gFEX Prototype v2 and FELIX Integration Test

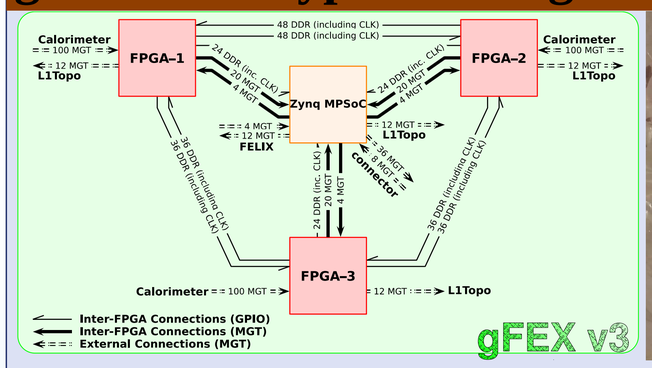


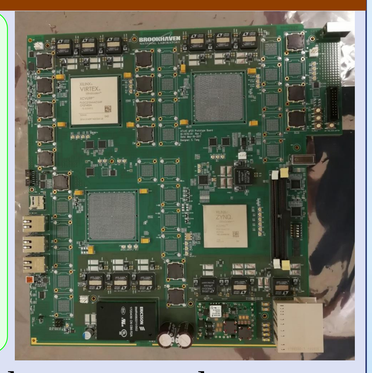


The gFEX and FELIX integration test was carried out before the final design review.

- ❑ gFEX uses the recovered TTC clock from FELIX link as its system clock. Jitter cleaner (Si5345) is used to improve the clock quality.
- ❑ 4 links between gFEX ZYNQ FPGA and FELIX
  RX Links: fixed low latency GBT mode (4.8Gb/s)
  TX Links: FULL mode
- ❑ The links from FELIX to gFEX can work well in latency-fixed GBT mode. The latency is 87.3 ns for FEC mode, and 79 ns for Wide-Bus mode.
- ❑ The links from gFEX to FELIX can work well in FULL mode.
- ❑ With the recovered TTC clock, the GTH can work well at link speed of 12.8 Gbps, and the GTY work well at 25.6 Gbps.

gFEX Prototype v3 Design

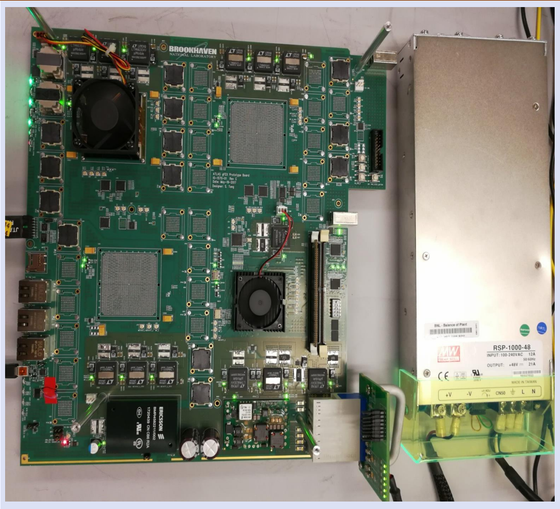


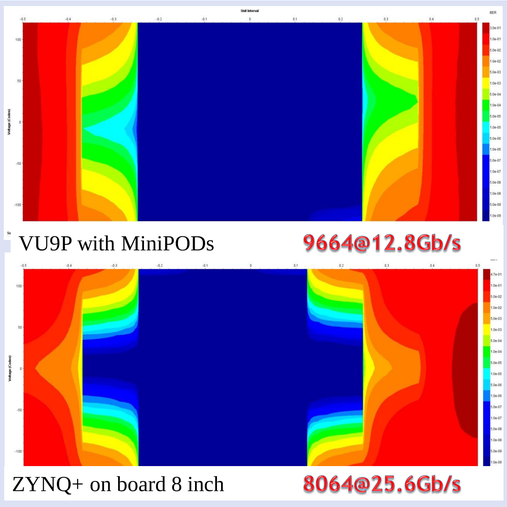


Comparing to the v2 board, the major changes are shown as below.

- ❑ ZYNQ →ZYNQ Ultrascale+;
- ❑ 8 Gb DDR3 DRAM → 16GB DDR4 DIMM
- ❑ XCVU160 → Vertex Ultrascale+ FPGA XCVU9P
- ❑ Add 5 more TX MiniPODs and 2 RX MiniPODs
- ❑ Only ZYNQ Ultrascale+ FPGA interface to FELIX, while all four FPGAs will interface to L1Topo
- ❑ DC/DC converter from 400W → 500W version.
- ❑ Stack up 26 layers → 30 Layers.

gFEX Prototype v3 function test at BNL





Evaluation test of gFEX prototype v3 has been carried out at BNL. For the first assembly, two FPGAs are installed for verification.

- ❑ Basic functionalities of 2 FPGAs have been verified successfully, such as ZYNQ Ultrascale+ interfaces, DDR4, GbE, UART and I2C monitoring.
- ❑ Link speed test for two FPGAs. All the optical links are stable at 12.8Gb/s and the onboard electrical GTY links are stable at 25.6 Gb/s.
- ❑ Parallel data buses are running up to 1.12Gb/s with good margin (>60%).

Summary and Conclusion

- ❑ The gFEX prototype v2 has been used to test all the challenging hardware technology successfully, such as 12.8 Gb/s optical links, 25.6 Gb/s on board electrical links, and 1.12Gb/s on board parallel data buses.
- ❑ The gFEX prototype v2 has been used in the link speed test, FELIX integration test, and gFEX firmware development.
- ❑ The partial assembled gFEX prototype v3 board has been tested successfully with all the functionalities and performance.
- ❑ Another fully assembled v3 board will be tested and used for the integration test at USA-15 at CERN in 2018.