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Peric, Ivan (KIT) *et al*

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Status of HVCMOS Developments for ATLAS

I. Perić[a]*, Roberto Blanco[a], Raimon Casanova Mohr[b], Felix Ehrler[a], Fadoua Guezzi Messaoud[c], Christian Krämer[a], Richard Leys[a], Mridula Prathapan[a], Rudolf Schimassek[d], André Schöning[e], Eva Vilella Figueras[f], Alena Weber[a], Hui Zhang[a]

[a] *IPE, Karlsruher Institut für Technologie, Karlsruhe, Germany*
[b] *IFAE, Barcelona, Spain*
[c] *University of Geneve, Geneva, Switzerland*
[d] *IEKP, Karlsruher Institut für Technologie, Karlsruhe, Germany*
[e] *University of Heidelberg, Heidelberg, Germany*
[f] *University of Liverpool, Liverpool, UK*

ABSTRACT: This paper describes the status of the developments made by ATLAS HVCMOS and HVMAPS collaborations. We have proposed two HVCMOS sensor concepts for ATLAS pixels - the capacitive coupled pixel detector (CCPD) and the monolithic detector. The sensors have been implemented in three semiconductor processes AMS H18, AMS H35 and LFoundry LFA15.
Efficiency of 99.7% after neutron irradiation to 10^{15} n_{eq}/cm^2 has been measured with the small area CCPD prototype in AMS H18 technology. About 84% of the particles are detected with a time resolution better than 25 ns. The sensor has been implemented on a low resistivity substrate.
The large area demonstrator sensor in AMS H35 process has been designed, produced and successfully tested. The sensor has been produced on different high resistivity substrates ranging from 80 Ωcm to more than 1 kΩcm. Monolithic- and hybrid readout are both possible.
In August 2016, six different monolithic pixel matrices for ATLAS with a total area of 1 cm^2 have been submitted in LFoundry LFA15 process. The matrices implement column drain and triggered readout as well as waveform sampling capability on pixel level. Design details are presented.

KEYWORDS: high-voltage pixel detector; HVCMOS detector; high-voltage CMOS technology; capacitive coupled pixel detector; CCPD; ATLAS.

*Corresponding author.

Contents

1. Introduction

In this paper, we discuss the developments made by ATLAS HVCMOS and HVMAPS collaborations of Universities of Bern, Geneva, Heidelberg, Karlsruhe (KIT), Liverpool, Tsukuba, Brookhaven National Laboratory and IFAE Barcelona. Beside these, there are several other groups developing sensors for ATLAS. Some of them are: Universities of Bonn, Stanford (SLAC), CPPM Marseille, CERN, HVR_CCPD and HVSTRIP collaborations and others. For an overview of all ATLAS CMOS activities please refer to [1].

Our group is developing HVCMOS sensors for ATLAS Phase-II upgrade since 2011 [2]. There are several motivations that drove this project. The present ATLAS pixel detector is based on two technologies which are developed mostly for the high energy physics applications: a sensor produced on a high resistivity substrate in a double sided process and a bump bonding technology with a pitch of $50\,\mu$m. Our goal is to produce a sensor that can be used for ATLAS in a commercial integrated-circuit process, i.e. in a process that is developed for commercial devices and applications like microprocessors, electronics in cars, mobile phones. One example of such a process is the high-voltage (HV-) CMOS. The use of a commercial process would lead to cost reduction would allow faster construction of large area detectors.

The use of CMOS technology could also help to improve the performance of particle detectors. One example is spatial resolution. Presently the pixel size is limited by bump bond pitch. CMOS sensors do not require bump bonding, since monolithic readout or capacitive coupling can be used, and smaller pixels are in principle possible. Further advantages are reduced amount of material and lower bias voltage. This also helps to broaden the area of application ranging from high energy physics, x-ray detection, electron microscopy to medicine.

HVCMOS detectors [3] are depleted active pixel detectors implemented in standard HVCMOS processes. The sensor element is the deep n-well/p-substrate diode. High voltage is used to deplete the part of the substrate around the n-well. The main charge collection mechanism is drift of the charge generated within the depleted region. Pixel electronics is usually implemented inside the deep n-well, although there are variants with the electronics near the sensor electrode. Fig. 1 illustrates the standard HVCMOS sensor structure.

At the beginning of HVCMOS sensor development for ATLAS the decision has been made to use the existing ASICs for the readout of the HVCMOS sensors. In this way a HVCMOS sensor is the replacement for a standard passive sensor. There are several advantages of the hybrid detectors based on HVCMOS versus the standard hybrid detectors. First, it is the possibility to transmit the signals from sensor to electronics by means of capacitive coupling. Further, there is the possibility to connect many sensor pixels to one readout channel and in this way improve spatial resolution. Finally, the cost of the sensors is reduced thanks to the large scale CMOS production. Since the beginning of the project two families of capacitively coupled pixel detectors (CCPD) [4] based on HVCMOS sensors have been developed by our collaboration. One family is implemented in the commercial semiconductor process AMS H18 (180 nm transistor gate length), the other in AMS H35 (350 nm).

Since 2015, we are also developing monolithic HVCMOS sensors for ATLAS experiment. Monolithic sensors have an obvious advantage over the hybrid sensors that they require only one part. Readout circuits are placed on the same substrate as the sensors. However, there are several drawbacks - the space for the readout electronics is limited in comparison with the hybrid detectors, the readout electronics may influence sensor by crosstalk. Nevertheless, prototypes in AMS H35, H18 and LFoundry LFA15 (150 nm) processes have been designed.

The paper is organized as follows: Section 2 lists the specifications of CMOS sensors for ATLAS. Section 3 deals with CCPD in AMS H18 technology. Section 4 describes monolithic CMOS sensors for ATLAS. Finally, after the description of readout architectures, two monolithic sensors are introduced: H35DEMO designed in AMS H35 process and LF_ATLASPIX implemented in LFoundry LFA15 technology.

2. Specifications of CMOS Sensors for ATLAS Phase II Upgrade

HVCMOS sensors are proposed within ATLAS Phase-II upgrade both for pixel [5] and for strip layers [6]. This paper will concentrate on HVCMOS pixels. The use in the outer pixel regions, like layer 5 with radius 30 cm, seems to be the most probable option. Moreover, it is investigated whether a CMOS pixel sensor can be used in the inner pixel layers and at the place of the strip layers.

In this section we will summarize the specifications for the ATLAS Phase-II upgrade (CMOS) pixel detectors.

Particle Hit Rate: The particle hit rate in different regions is still subject for simulations: The particle hit rate, or more precisely the number of hit-signals per pixel-sensor area, depends on R- and Eta position in the detector, the size of pixel detection volume (pixel area and the depletion layer thickness) and the rate of photon conversion in the detector material. The numbers are in the range from 50 hits/cm^2/25 ns for layer 1 (4 cm), about 5 hits/cm^2/25 ns for layer 3 (14 cm) down to

about 1 hit/cm^2/25 ns for layer 5 (30 cm). More detailed numbers are given in [7]. The hit-signal rate depends almost linearly on the depletion layer thickness. The numbers indicated above assume about 100 μm and the forward detector regions. The hit-signal rate depends on the pixel area since smaller pixels lead to a higher hit multiplicity, i.e. one particle usually produces signals in many neighbor pixels.

Pixel Size: The pixel size is determined by the required spatial resolution in φ direction and the number of hits per pixel and unit time referred to as occupancy. The pixel size in the present ATLAS pixel detector is 50 μm $\times$ 250 μm. Our goal is a pixel size of 50 μm $\times$ 50 μm, however for outer pixel layers larger pixels may be more efficient choice.

Time Resolution, Efficiency and Radiation Tolerance: Our preliminary goal is 99% in-time efficiency within 50 ns which means that 99% of the hits must be detected with timing better than 50 ns. The final goal is 99% in-time efficiency within 25 ns. The sensor should be radiation tolerant in terms of nonionizing damage to fluence from 0.7 to 2 $\times 10^{15}$ n_{eq}/cm^2 and in terms of ionizing damage to dose from 30 to 100 Mrad assuming the application in pixel layers 5 and 3 respectively.

Noise Level: The noise rate per pixel should be less than 10^{-4}/BC, where BC stands for bunch crossing period of 25 ns.

Power Consumption: The power consumption of a CMOS pixel detector should be less than 500 mW/cm^2. A smaller power consumption is highly desirable. It could allow the use of pixel sensors in the tracker regions where presently strips are used, it would simplify the module design and reduce the amount of material needed to bring power in and take heat out.

3. CCPD in AMS H18 process

This section presents shortly the status of the CCPD development in AMS H18 process. The first sensor chip - CCPDv1 has been submitted in November 2011 [5]. It is a small HVCMOS test sensor that can be glued to the FEI4 ASIC [8] and readout capacitively. Since then we have designed seven CCPD versions. The following list summarizes the properties of every version.

- CCPDv1: Basic design - pixel size 33 μm $\times$ 125 μm, readout with FEI4 pixel readout ASIC [8]
- CCPDv2: Improved radiation tolerance, linear transistors replaced with enclosed ones
- CCPDv3: Large matrix with 25 μm $\times$ 25 μm pixels implemented, readout with CLICPIX pixel readout ASIC [9]
- CCPDv4: Pixel position encoded as pulse length
- CCPDv5: Comparator with time walk compensation
- CCPDv6: Chip version in AMS aH18 process, a new version of H18 process that offers more flexibility such as the use of high resistivity substrates
- CCPDv7: Chip version with a new guard ring geometry that allows higher bias voltage of up to 150V

The CCPD chips are implemented in the standard HVCMOS process on the standard substrate of 10 - 20 Ωcm resistivity. The PMOS transistors are not isolated from the deep n-well. It is a triple well process that includes p-well, n-well, and a deep n-well. Therefore PMOS may produce crosstalk to sensor. By careful design, such as the use of NMOS-only current mode logic gates, the crosstalk has been eliminated. The pixel contains a charge sensitive amplifier, a comparator with threshold tune circuits and an output stage. The signals of three pixels are multiplexed to one signal pad. The signal is transmitted capacitively to a FEI4 chip. The pixel position is encoded as signal amplitude or signal width.

CCPD sensors in AMS H18 process have been extensively tested. The most recent measurements have been presented in [10]. The sample irradiated to a fluence of 10^{15} n_{eq}/cm^2 (TRIGA reactor of the JSI, Ljubljana, Slovenia) - a relevant value for pixel layer 5 - exhibited 99.7% average hit efficiency. This measurement has been performed at CERN at Super Proton Synchrotron (SpS) with 180 GeV pions using a pixel matrix capacitively coupled to FEI4. About 84% of the tracks have been detected with a time resolution better than 25 ns and 99% with a time resolution better than 50 ns. The bias voltage used in these measurements was up to 85 V. The samples irradiated to 1.3 $\times 10^{14}$ n_{eq}/cm^2, 5 $\times 10^{14}$ n_{eq}/cm^2, (irradiations with 18 MeV protons at the Bern Cyclotron Laboratory, Switzerland) and 5 $\times 10^{15}$ n_{eq}/cm^2 (TRIGA) had the efficiencies of 98.1%, 99.7% and 97.6%, respectively. Notice that the efficiency for samples irradiated to 5 $\times 10^{14}$ n_{eq}/cm^2 with protons and to 10^{15} n_{eq}/cm^2 with neutrons is higher than for samples irradiated to 10^{14} n_{eq}/cm^2 with protons. This can be explained by the acceptor removal effect [11]. Irradiation leads to an effective decrease of the shallow acceptor concentration and therefore an increase of the depletion region thickness. Signal amplitude gets increased, which may lead to a better efficiency. On the other hand, for fluences significantly above 10^{15} n_{eq}/cm^2, neutron irradiation introduces deep acceptors, which leads to reductions of the depleted region and efficiency [11].

4. Monolithic Sensors for ATLAS

A monolithic sensor contains both the sensor and the readout circuits on one substrate.

We are investigating two readout architectures.

In the case of *store-readout-filter* architecture (referred also to as "column drain"), every pixel has one hit-buffer. After particle hit, the information containing time stamp, pixel address and signal amplitude is stored temporarily until it can be transferred from the hit-buffer to the periphery where some sort of data filtering is done. In the ATLAS baseline design the filtering is based on a trigger signal. There are also ideas to implement the filter electronics on dedicated chips that would receive data from several detector layers. In this case, simple track fitting could be done on chip and track information could be used to trigger the readout.

The main source of inefficiency in the case of store-readout-filter scheme is a limited buffer readout rate. Notice that all the hit data need to be transferred from the hit-buffers to the periphery and this takes time. It may happen that a pixel is hit by a particle for the second time before its buffer, that contains the information of the first hit, is emptied. A higher particle-hit rate leads to a longer transfer time, which additionally worsens the efficiency because it takes longer until a buffer is emptied. Column drain architecture is used in FEI3 readout ASIC [12].

In the case of *store-filter-readout* architecture, a group of pixels share some number of trigger-buffers. The hit information (pixel address) is stored in the first empty trigger buffer. The information is kept for a defined time. At the end of the storage time, a trigger signal is expected that is initiated by the particular collision the hit is originating from. The hit information is readout only if the trigger signal arrives. If there is a new hit in the pixel group, while the old hit is still in the buffer, the new hit information will be stored in the next empty buffer cell. Inefficiency occurs if a new hit happens while all the buffer cells are occupied. Store-filter-readout architecture can be relatively easily adapted to a higher hit rate by adding more buffers. This architecture is implemented in FEI4 readout ASIC [8].

4.1 H35DEMO

H35DEMO, shown in Fig. 2, is a large ATLAS sensor that is implemented on four different substrates in AMS H35 technology. Sensor design is based on MuPix [13] [14] [15] and CCPD detectors. The project has been performed in collaboration between Universities of Bern, Geneva, Karlsruhe (KIT), Liverpool, CERN and IFAE Barcelona [16].

H35DEMO can be used as a monolithic detector and as a CCPD. The total chip area is about $1.9\,\text{cm} \times 2.4\,\text{cm}$. About half of the sensor area can be readout in "monolithic" way using on chip readout circuits that do zero suppression and generation of hit data packets: time stamp and address. The entire sensor area can be also readout by FEI4 readout chip that can be mounted onto H35DEMO. Signal transmission can be established capacitively or through bumps. Pixel size is $50\,\mu\text{m} \times 250\,\mu\text{m}$. The design is radiation hard i.e. enclosed transistors have been used. Radiation tolerance at least to 100 Mrad has been shown on smaller prototypes in AMS H35 technology [17]. Analog power consumption is about 200 mW/cm^2. H35DEMO implements three matrix types, two combined (monolithic and CCPD) and one only CCPD. The combined matrices are based on pixels with or without comparators. The pixels are connected to the readout cells placed on periphery. CCPD matrices use pixels without comparators. The readout cells have one or two thresholds for rejection of small hits. The pixel comparators have time walk correction. The readout type is store-readout-filter where the filtering part is still not implemented. The sensor is implemented on four different substrates of the resistivity 20, 80, 200 and $1000\,\Omega\text{cm}$. The bias voltage used in measurements was up to 180 V.

The testing of the sensor has started in early 2016. Both the monolithic readout and the CCPD readout with FEI4 have been successfully tested. The first beam test measurement has been done. Detection efficiency of more than 99% and a good time resolution have been measured. The results will be published soon.

Fig. 3 shows the monolithic readout test. The sensor has been exposed to ^{90}Sr radioactive source, hit data have been taken. The figure shows the difference between the time stamps generated by H35DEMO and the scintillator trigger point. This sensor is implemented on the $80\,\Omega\text{cm}$ substrate. Measured minimum ionizing particle (MIP) signal is about $3700\,\text{e}^-$ for a sensor on $80\,\Omega\text{cm}$ substrate (100 V bias voltage) and $5000\,\text{e}^-$ for a sensor on $200\,\Omega\text{cm}$ substrate (140 V bias). Fig. 4 shows the result of a threshold tuning. The number of tune bits per pixel is two.

4.2 LF_ATLASPIX

AMS H35 technology is interesting for the outer tracking layers. However, a large transistor size in

this technology leads to a large chip periphery and a rather high supply voltage of 3.3 V to a higher power consumption in the digital part compared with the designs in smaller technologies. From these reasons, we have started developments of monolithic sensors for ATLAS in smaller feature size technologies. We have chosen two technologies AMS H18 (180nm) and LFoundry LFA15 (150nm).

In August 2016 the collaboration of Universities of Bern, Geneva, Heidelberg, Karlsruhe (KIT), Liverpool and IFAE Barcelona has submitted six matrices in LFoundry LFA15 process. These designs are referred to as LF_ATLASPIX. The total reticle size is $1\,\mathrm{cm} \times 1\,\mathrm{cm}$. The sensors are implemented on four different substrates with the resistivities 100, 500-1100, 1900 and 3800 Ωcm. The nominal bias voltage is up to 120 V. One matrix is a CCPD with small pixels ($27.5\,\mu\mathrm{m} \times 27.5\,\mu\mathrm{m}$) that can be readout by TimePix ASIC [18]. A version for the new RD53 ASIC [19] is planned. The remaining five matrices have monolithic readout. They can be distinguished by the readout type (store-readout-filter and store-filter-readout), the pixel type ("smart"- and small n-well diode) and the pixel addressing (lossy and lossless).

Readout and Addressing Types

In all monolithic matrices pixels contain charge sensitive amplifier (CSA), comparator, edge detector, pulse stretcher and 4-bit threshold tune digital to analog converter (DAC).

One out of five monolithic matrices uses the store-readout architecture. The filtering part is not implemented. Pixel size is $40\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$. Hit information contains 8-bit time stamp and pixel address.

Three monolithic matrices use a new version of the store-filter-readout architecture. This readout architecture supports trigger delays of up to $25\,\mu\mathrm{s}$. Pixel matrix is divided in pixel groups called superpixels. Depending of matrix variant, one superpixel contains either eight or sixteen pixels. Every superpixel is connected to a dedicated readout block. This block contains four trigger buffers. After a particle hit, the address coming from the superpixel is stored into the first empty trigger buffer. After the trigger delay the buffer is either emptied (if no trigger arrived) or marked for readout (if trigger is received). Presently implemented scheme should cope with hit rate of 5 hits/cm^2/25 ns which corresponds to pixel layer 3 in the Phase II ATLAS upgrade. A trigger delay of $10\,\mu\mathrm{s}$ is assumed. The size of the readout block with four buffers is only $40\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$. As mentioned, the number of pixels in the superpixel is eight or sixteen depending of matrix variant. In the first case every pixel has one address bit assigned. The pixel size is $40\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$. In the case of sixteen pixels per superpixel, the pixel size is $40\,\mu\mathrm{m} \times 60\,\mu\mathrm{m}$ and 16 to 8 "lossy" addressing is used which works as follows: Sixteen pixels are grouped into four groups each containing four pixels. Every group corresponds to one group-address bit and every of four pixel positions within a group to one pixel-address bit. If, for instance, the first pixel in the second group is hit by a particle, the pixel-address bit 1, and the group-address bit 2 are high and all other bits are low. Such addressing has been chosen because it introduces a reduction of address-width with respect to the trivial addressing where every pixel has its address bit. Further, 16 to 8 addressing scheme does not lead to corrupted addresses in the case of clusters or multiple hits - the actual hit coordinates can be extracted from the stored address.

The fifth monolithic matrix uses a variant of the store-readout architecture with the waveform sampling capability. The analog waveform is sampled with eight-bit resolution, six times close to the threshold crossing moment. The time position of the samples can be either six before the

threshold crossing or three samples before and three samples after the threshold crossing. The sampled voltages are immediately digitized by six single-slope analog to digital converters (single-slope ADCs) and the digital values are stored. Every pixel has its own sampling block, in total six ADCs per pixel. The pixel size is $40\,\mu$m $\times$ $250\,\mu$m. The sampling capability may improve time resolution of the sensor since particle hit time can be determined by fitting a curve to the measured sample points.

Pixel Types

There are two pixel types. All but one matrix use the standard HVCMOS pixel, referred to as the "smart" diode. The electronics is placed in a large deep n-well. Fig. 5 shows the layout of this pixel type. Since LFoundry offers the deep p-well implant which allows isolation of PMOS transistors from the deep n-well and in this way a crosstalk reduction, we have used CMOS logic gates in the pixel.

One matrix uses the small-diode pixel type. The pixel size is $40\,\mu$m $\times$ $60\,\mu$m. Two sensor diodes implemented as n-wells are placed near the readout electronics. The readout electronics is embedded in a deep p-well. Both diodes are shorted and belong to the same pixel. The use of two diodes may improve charge collection efficiency, especially in the cases when the signal charge is generated underneath the deep p-well. The connection between the diodes and the pixel amplifier is established by AC coupling. High voltage capacitors are used and the sensor diodes can be biased with a positive voltage of about 50 V. The small-diode pixel has, according to preliminary simulations, a smaller detector capacitance and therefore a better time resolution than the smart-diode pixel for the same power consumption. However, it is still unknown whether the radiation tolerance is equally good. Fig. 6 shows the layout of the pixel with small diodes. Both pixel types, the small diode- and the smart diode pixel, use the same electronics that include CSA, comparator, edge detector, pulse stretcher and threshold-tune DAC.

Similar designs will be realized in AMS aH18 technology on different high resistivity substrates and submitted in December 2016. The reticle size will be 2.1 cm $\times$ 2.3 cm.

5. Summary

This paper gives an insight on the status of the developments made by ATLAS HVCMOS and HVMAPS collaborations. We have proposed two HVCMOS sensor concepts for ATLAS pixel detector - the capacitive coupled pixel detector (CCPD) and the monolithic detector.

Efficiency of 99.7% after neutron irradiation to 10^{15} n_{eq}/cm^2 has been measured with a CCPD prototype implemented in AMS H18 process (180 nm gate size). About 84% of the tracks are within 25 ns bin. The measured sensor is implemented on a low resistivity wafer of 10-20 Ωcm.

The first large area (5 cm^2) HVCMOS ATLAS demonstrator (H35DEMO) sensor in AMS H35 350 nm process has been designed, produced and successfully tested. The sensor has been produced on wafers with resistivity ranging from 80 Ωcm to more than 1 kΩcm. Both monolithic- and CCPD-readout with FEI4 as the readout chip are possible. First beam tests have been performed showing good results. Efficiency of more than 99.7% has been measured. Different laboratory tests with radioactive sources and electric signals have been performed.

In August 2016, six sensor matrices for ATLAS with a total area of 1 cm^2 have been submitted in the LFoundry LFA15 150 nm process on different high resistivity wafers (LF_ATLASPIX). One

matrix has the FEI3-like readout. Three matrices have a triggered readout that is based on similar architecture as in FEI4. One matrix has the waveform sampling capability at pixel level. Pixel sizes are from 40 μm $\times$ 250 μm (waveform sampling matrix) to 40 μm $\times$ 60 μm (FEI4-like readout). Beside the monolithic matrices, a small-pixel CCPD matrix is implemented. The pixel size is 27.5 μm $\times$ 27.5 μm and the pixels can be readout by TimePix ASIC [18]. Similar designs will be realized in AMS aH18 technology and submitted in December 2016. The reticle size will be 2.1 cm $\times$ 2.3 cm.

6. Acknowledgement

The production of H35DEMO and LF_ATLASPIX was a joint effort of the Universities of Bern, Geneva, Heidelberg, Karlsruhe (KIT), Liverpool, CERN, Brookhaven National Laboratory and IFAE Barcelona. The project has been partially supported by EU and BMBF within H2020 project AIDA-2020 (GA no. 654168) and "HV-MAPS Pixel Detectors for high-rate Experiments with Hadrons (HL-LHC)" project respectively.

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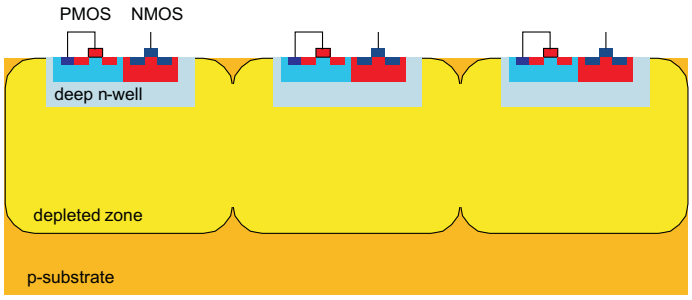

Figure 1. HVCMOS sensor structure.

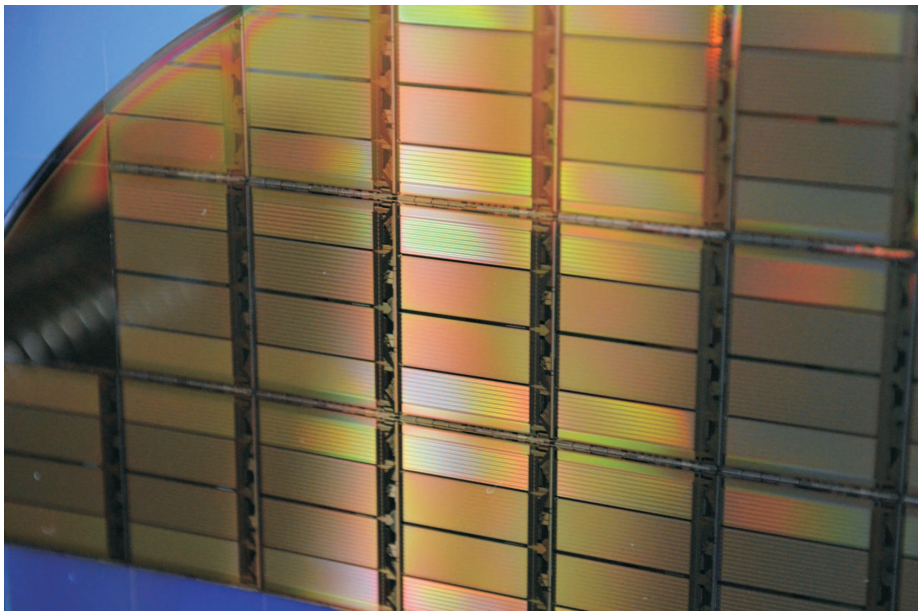

Figure 2. Photograph of H35DEMO wafer.

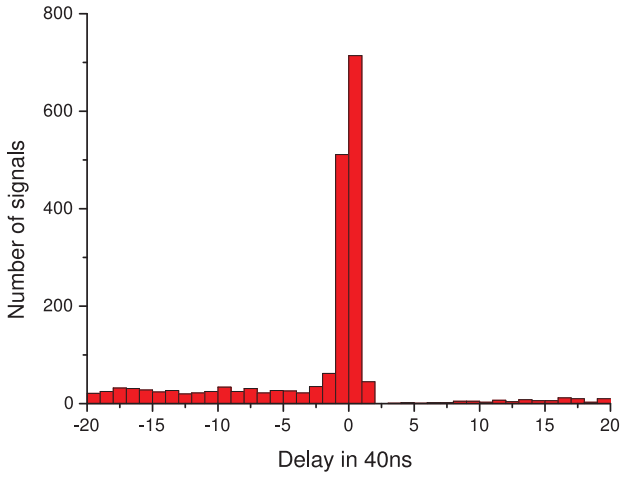

Figure 3. Monolithic readout test: The difference between the time stamps generated by H35DEMO and the scintillator trigger point is shown. Each bin is of 40 ns.

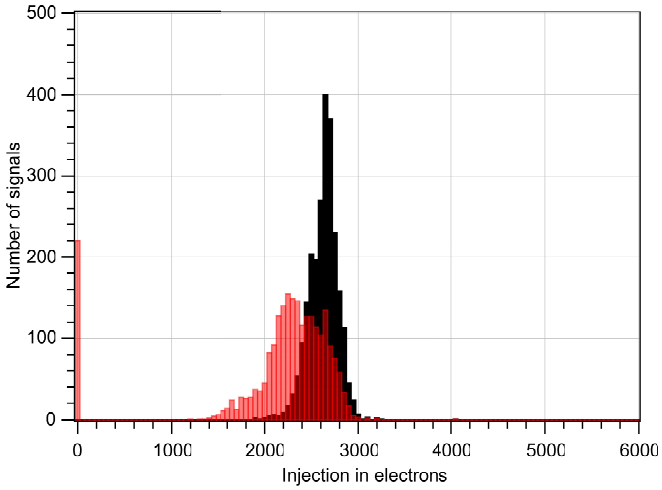

Figure 4. Monolithic readout test: Input referred thresholds have been measured before and after tuning.

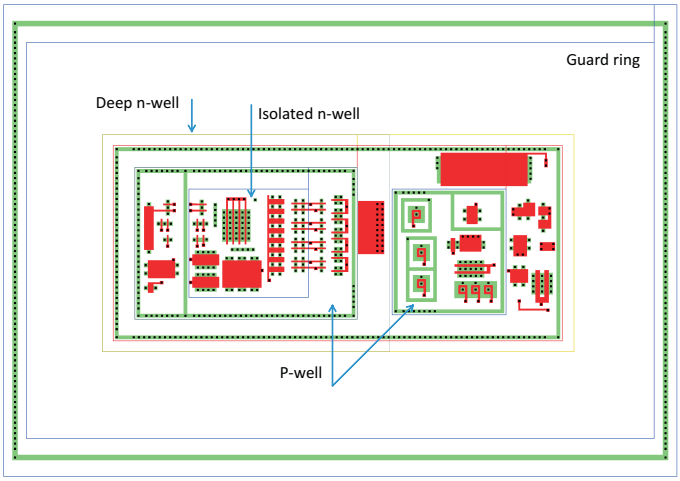

Figure 5. Layout of the standard HVCMOS, with pixel electronics implemented inside the n-well that acts as the sensor electrode.

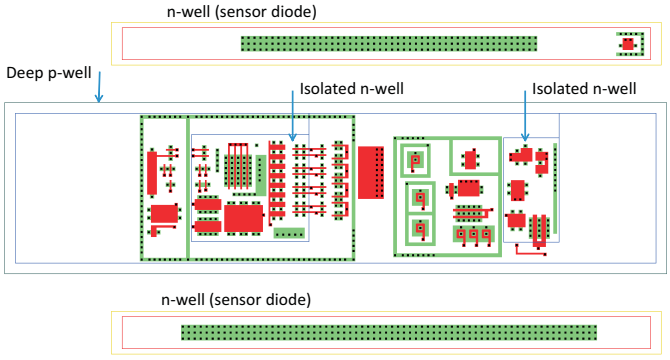

Figure 6. Layout of the pixel with external diodes. The pixel electronics is embedded in a deep p-well and placed between the sensor diodes.