Operational Experience of ATLAS SCT and Pixel Detector

Vertex 2017

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for the ATLAS Collaboration

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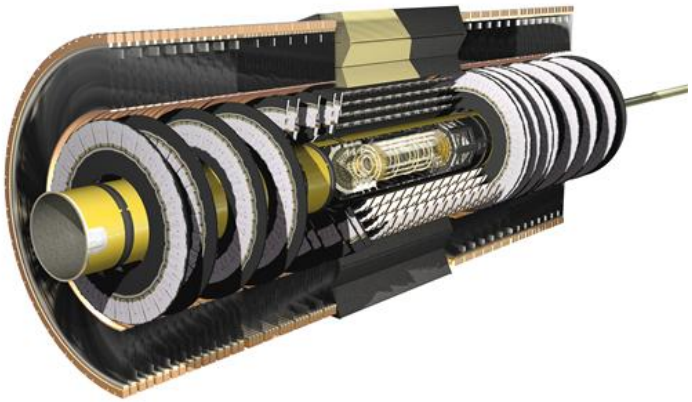
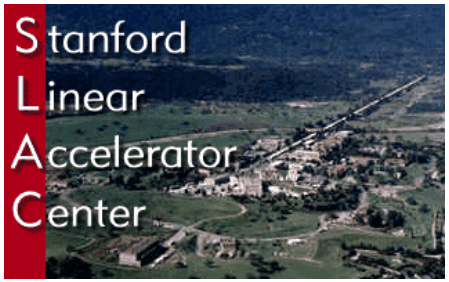
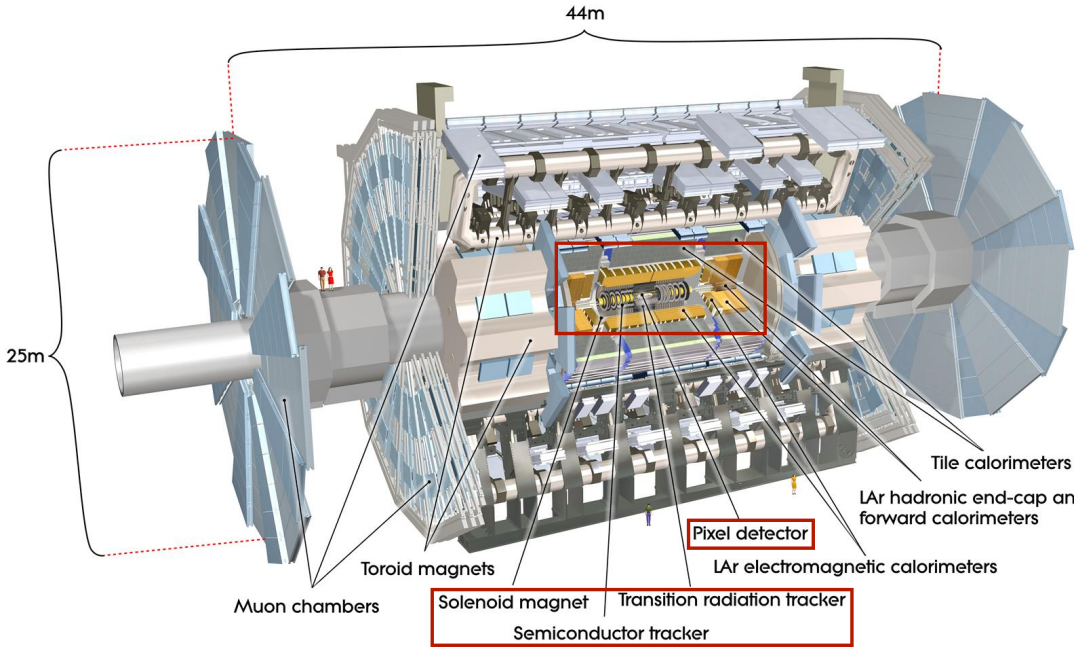


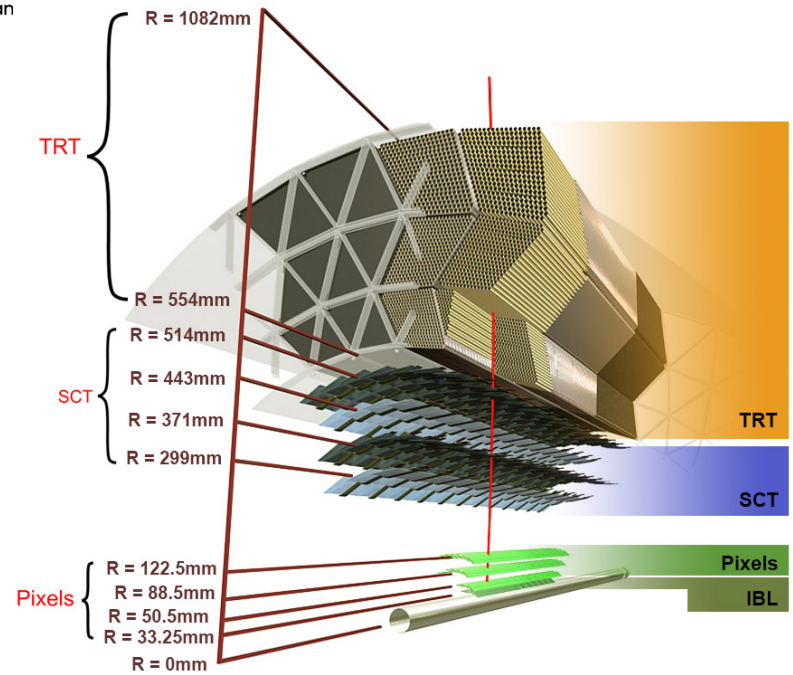


ATLAS Silicon Tracking Detectors



The ATLAS Tracker:

1. Pixel Detector.
2. Silicon strip detector (SCT).
3. Transition Radiation Tracker (not Silicon).



Pixel:

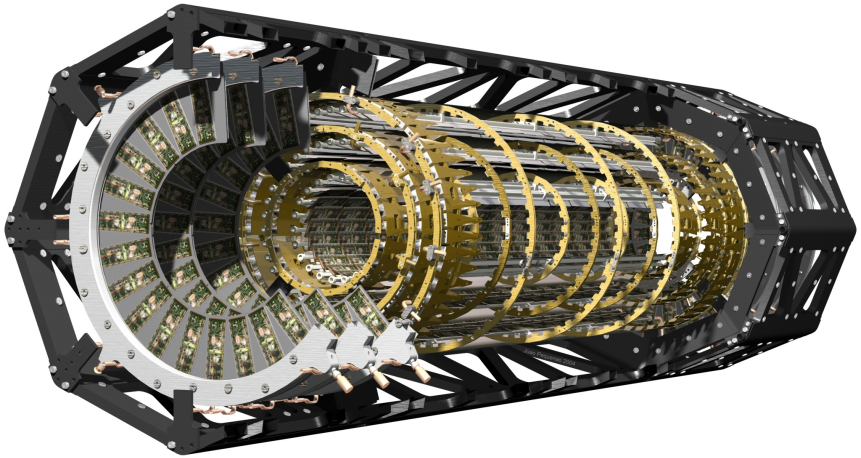
- 92 million channels.
- 1968 modules.
- 1.9 m^2 of silicon.
- More than 40 institutes.

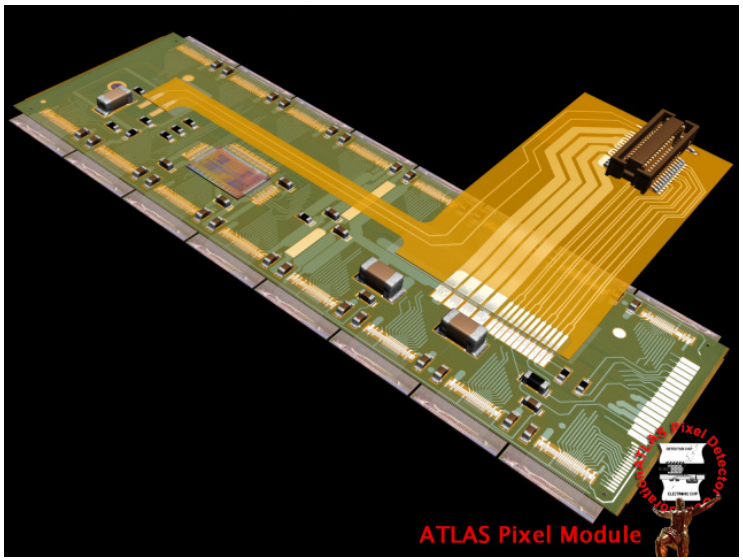
SCT:

- 6 million channels.
- 4088 modules.
- 60 m^2 of silicon.
- More than 40 institutes.

The Pixel Detector

- Originally 3 barrel layers and 2 x 3 endcap disks.
- A 4th barrel layer was added in 2014 (next slide).
- Angular Coverage: $|\eta| < 2.5$
- Barrel radii: 5.05 cm, 8.85 cm, 12.25 cm.



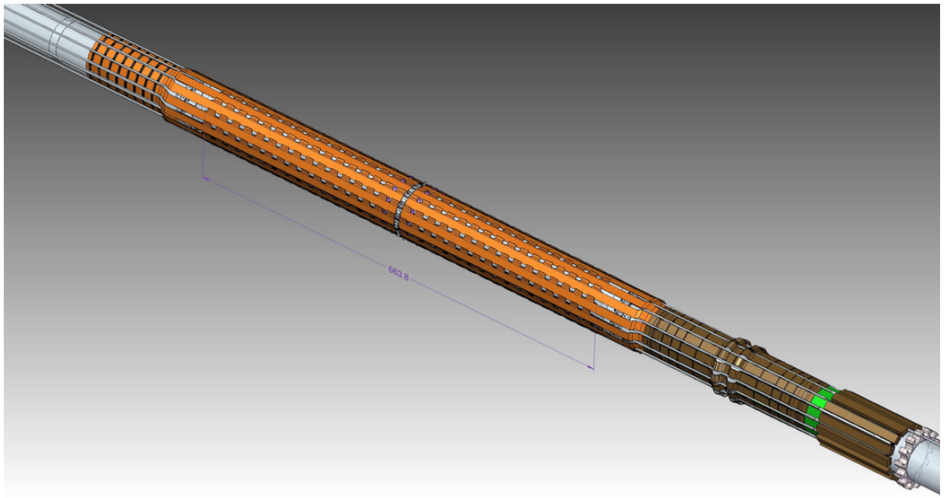


Each pixel module consists of

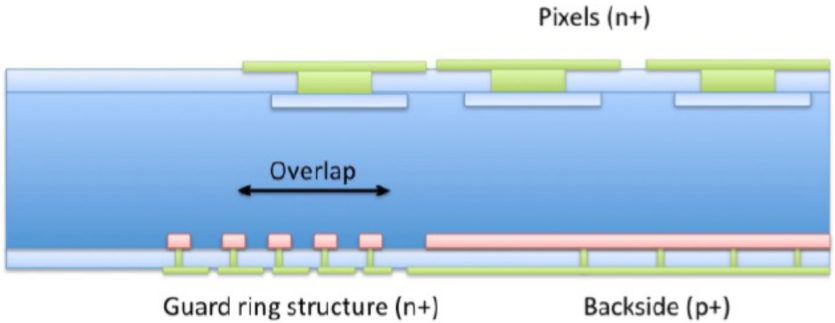
- 1 planar n-on-n sensor 62.4 mm x 21.4 mm in size, 250 μm thick.
- 16 FEI3 frontend chips plus one controller (0.25 μm CMOS).
- 1 flex that provides the electrical connections.

The frontends are bump-bonded to the sensor.
46080 pixels, size 50 μm x 400 μm.
The data rate per module is 40/80/160 Mbps.

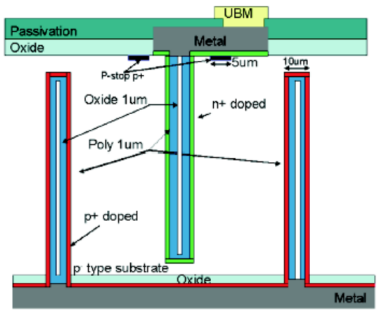
IBL



- IBL stands for “Insertable B-Layer”.
- New innermost layer of the Pixel Detector.
- Added in the 2013-2014 LHC shutdown (aka LS1).
- 14 staves.
- Radius 3.2 cm



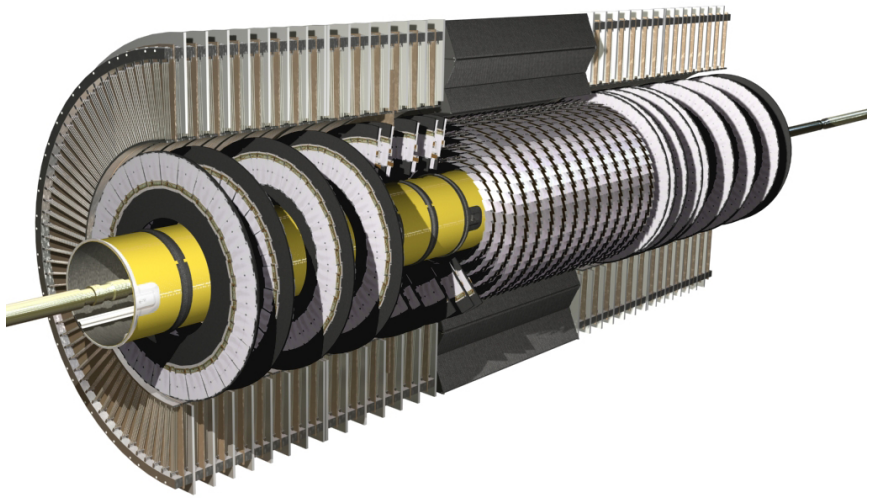
- 2 sensor technologies:
  - Planar slim edge n-on-n, 200 μm
  - 3D with 2 electrodes per pixel, 230 μm.
- Planar sensors in the central region, 3D on the outside.
- FEI4 2 cm x 1.8 cm frontend chips in 130 nm CMOS, data rate 160 Mbps.
- 26880 pixels per FEI4, size 50 x 250 μm^2.
- Sensors bump bonded to frontends.

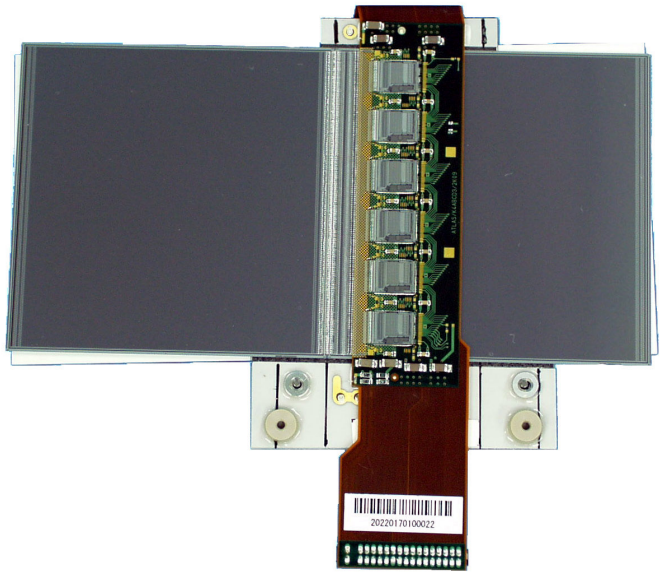


With the 3D sensors, CO_2 cooling, and local support IBL is a step towards ITK.

The SCT (Semiconductor Tracker)

- Microstrip detector.
- 4 barrel layers and 2 x 9 endcap disks.
- Angular Coverage: $|\eta| < 2.5$
- Barrel radii between 30 cm and 52 cm.

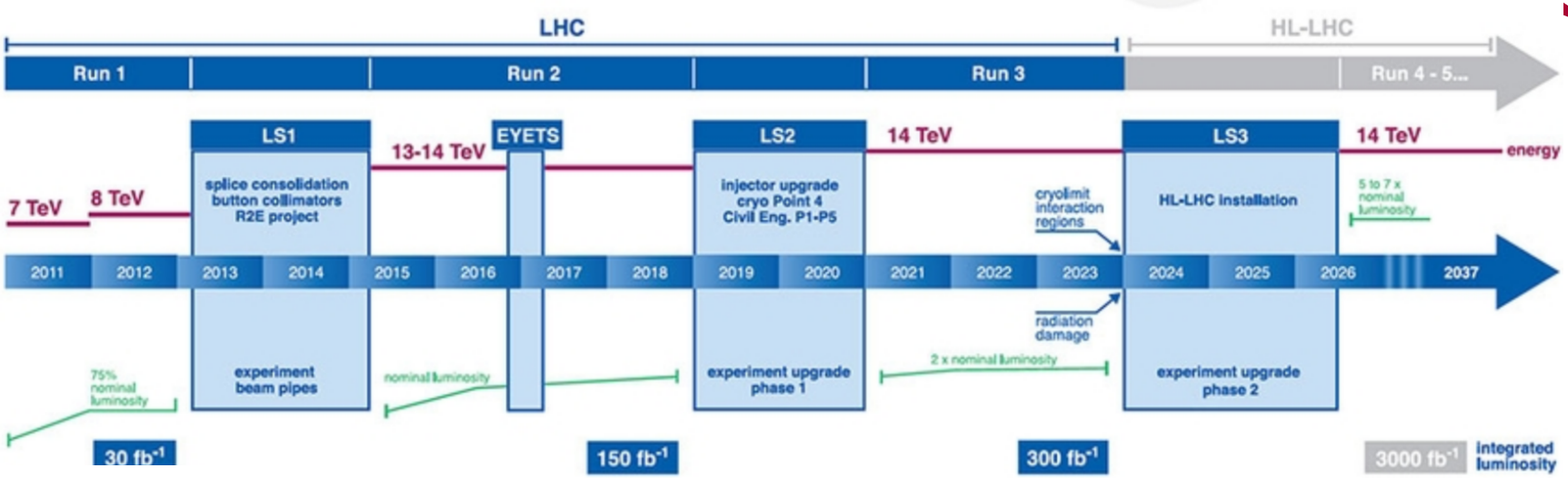


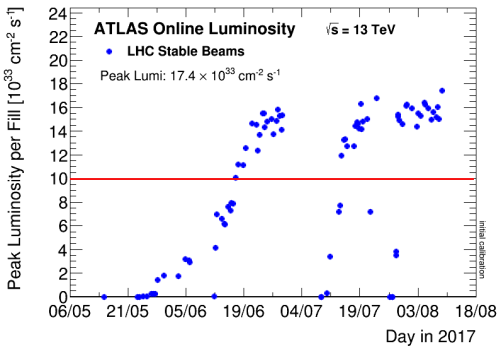


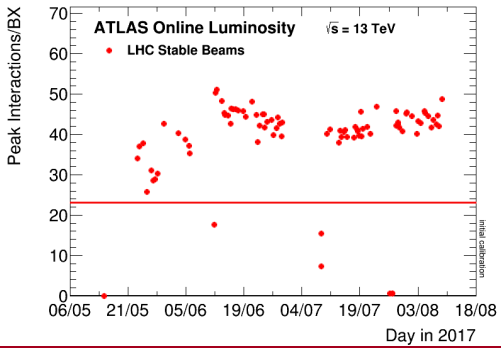
SCT Modules:

- Double sided modules, 12.8 x 6.4 cm^2.
- Sensor thickness 285 μm.
- Stereo angle of 40 mrad between sides.
- 768 strips per side, pitch 80 μm.
- 12 ABCD readout chips, readout at 40 Mbps.

LHC Roadmap



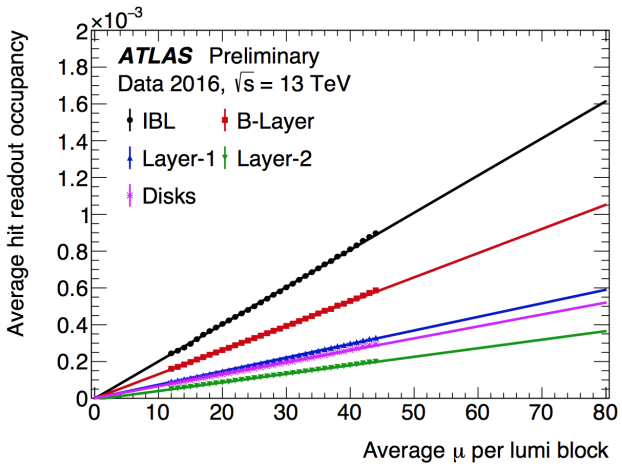




- Original target: $1 \cdot 10^{34}$ cm^{-2}s^{-1} with an average of **23** interactions per bunch crossing (also called pile-up or μ).
- Now already exceeded $1.7 \cdot 10^{34}$ cm^{-2}s^{-1} with $\mu = \mathbf{48}$.
- Until the end of run 2 we expect up to $2 \cdot 10^{34}$ cm^{-2}s^{-1}, $\mu = \mathbf{58}$.
- For run 3 we expect up to $3 \cdot 10^{34}$ cm^{-2}s^{-1} and $\mu = \mathbf{80}$, though inner triplet cooling constraints in place today suggest a limit of $2.2 \cdot 10^{34}$ cm^{-2}s^{-1}, $\mu = \mathbf{61.5}$.
- SCT and Pixel will take data until the end of run 3.

The performance of the LHC far beyond the original specs poses a substantial challenge to the detectors in terms of bandwidth and radiation dose.

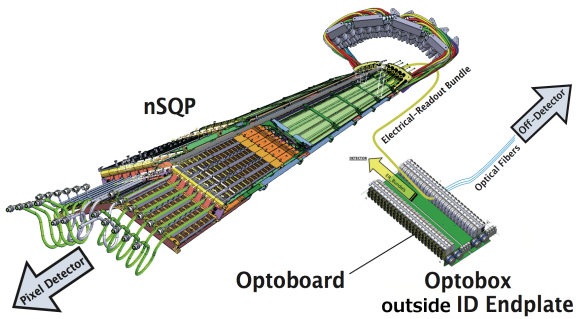
Pixel Readout Hardware Upgrade

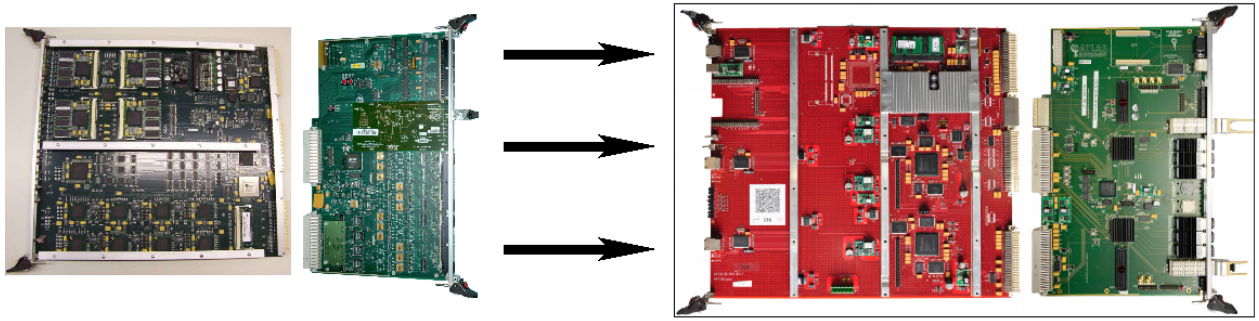


Module Link Occupancy at 100kHz L1					
	μ	B-Layer 160Mbps	Layer-1 160Mbps	Layer-2 80Mbps	Disks 80Mbps
25ns 13 TeV (Estimation based on Run2)	30	50%	33%	49%	62%
	50	71%	92%* → 46%	139%* → 69%	86%
	80	101%	125%* → 63%	188%* → 94%	115%

* Assuming bandwidths before the upgrade

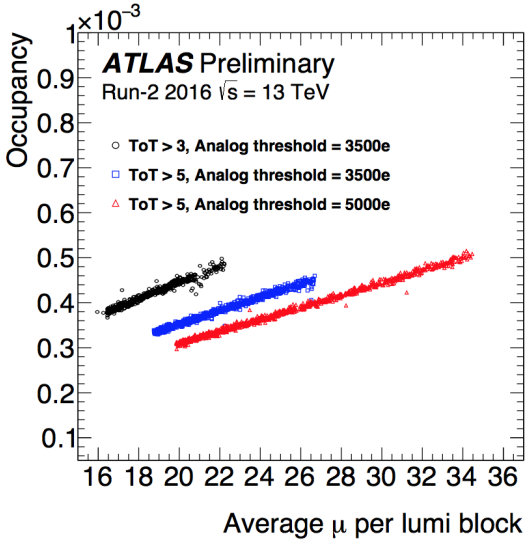
- The two outer layers would have hit the bandwidth limit by now.
- **2016:** Layer 2 was most critical. The readout rate of 40 Mbps was doubled to 80 Mbps. Replaced readout boards (ROD/BOC) with IBL boards for higher density.
- **2017**: Second most critical was layer 1, running at 80 Mbps previously. In the shutdown of 2013/14 new service quarter panels, new optoboards, and 2 fibers per layer-1 module were installed. This allowed for a doubling of the rate (160 Mbps). ROD/BOC $\Longrightarrow$ IBL.

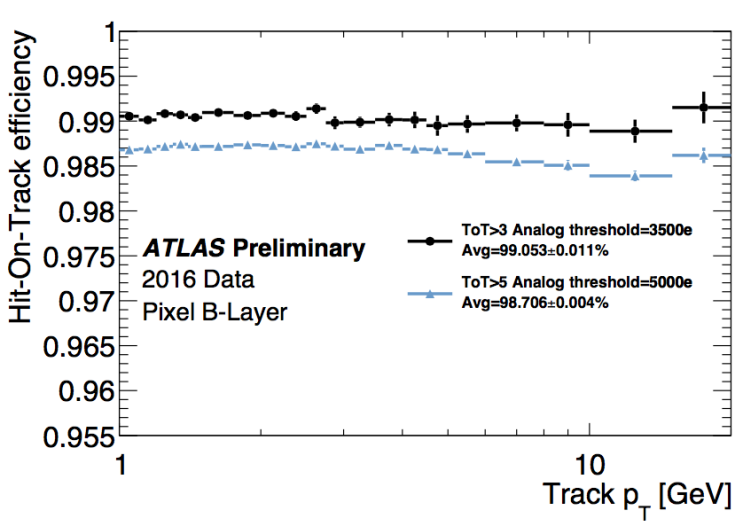


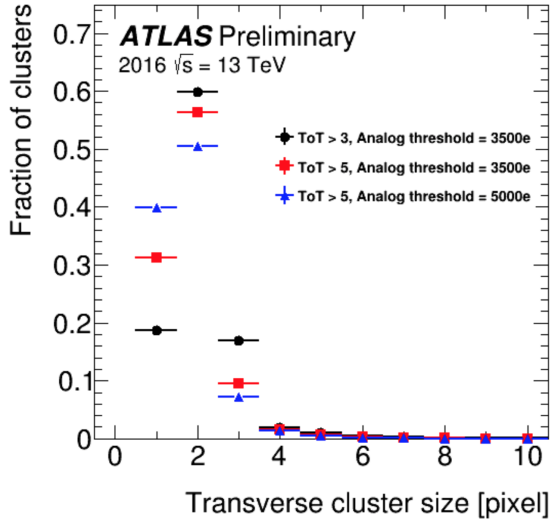


Pixel Threshold Adjustments

- For B-Layer (already at 160 Mbps) and disks D1 and D3 (no second readout line installed) no increase of the readout speed is possible.
- Reduce data volume by increasing the threshold, thereby decreasing the number of hits.
- Increased B-layer time-over-threshold (ToT) cut from 3 to 5 in the frontends.
- Increased B-layer threshold from 3500 e^- to 5000 e^- and to 4500 e^- for disks.
- Reduces the occupancy by about 30 %.
- Tracking efficiency only affected at the sub-percent level.
- Cluster shapes are affected (see plots below).
- In addition the latency in the B-layer was reduced from 255 to 150 bunch crossings in order to free up buffer space inside the frontend chips. Retuned (MIP=18 BC instead of 30 BC) to preserve the ability to record large signals.
- The plots below show results for the B-layer.

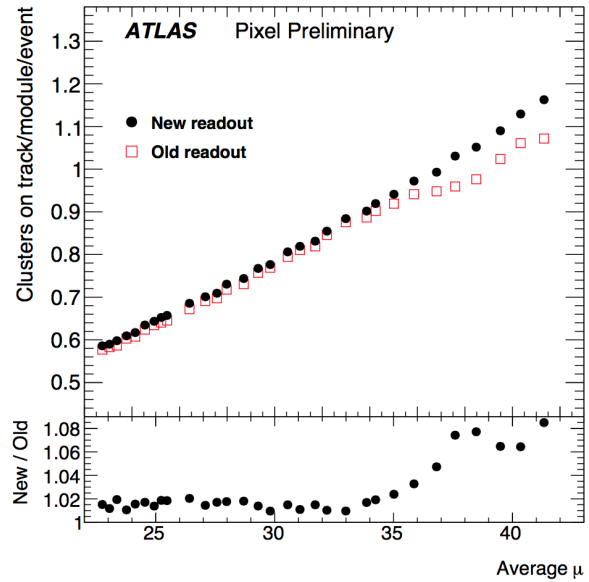


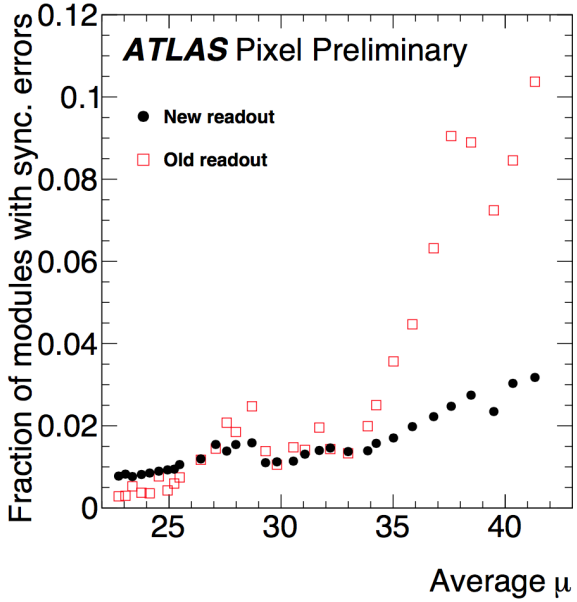




Pixel Desynchronization

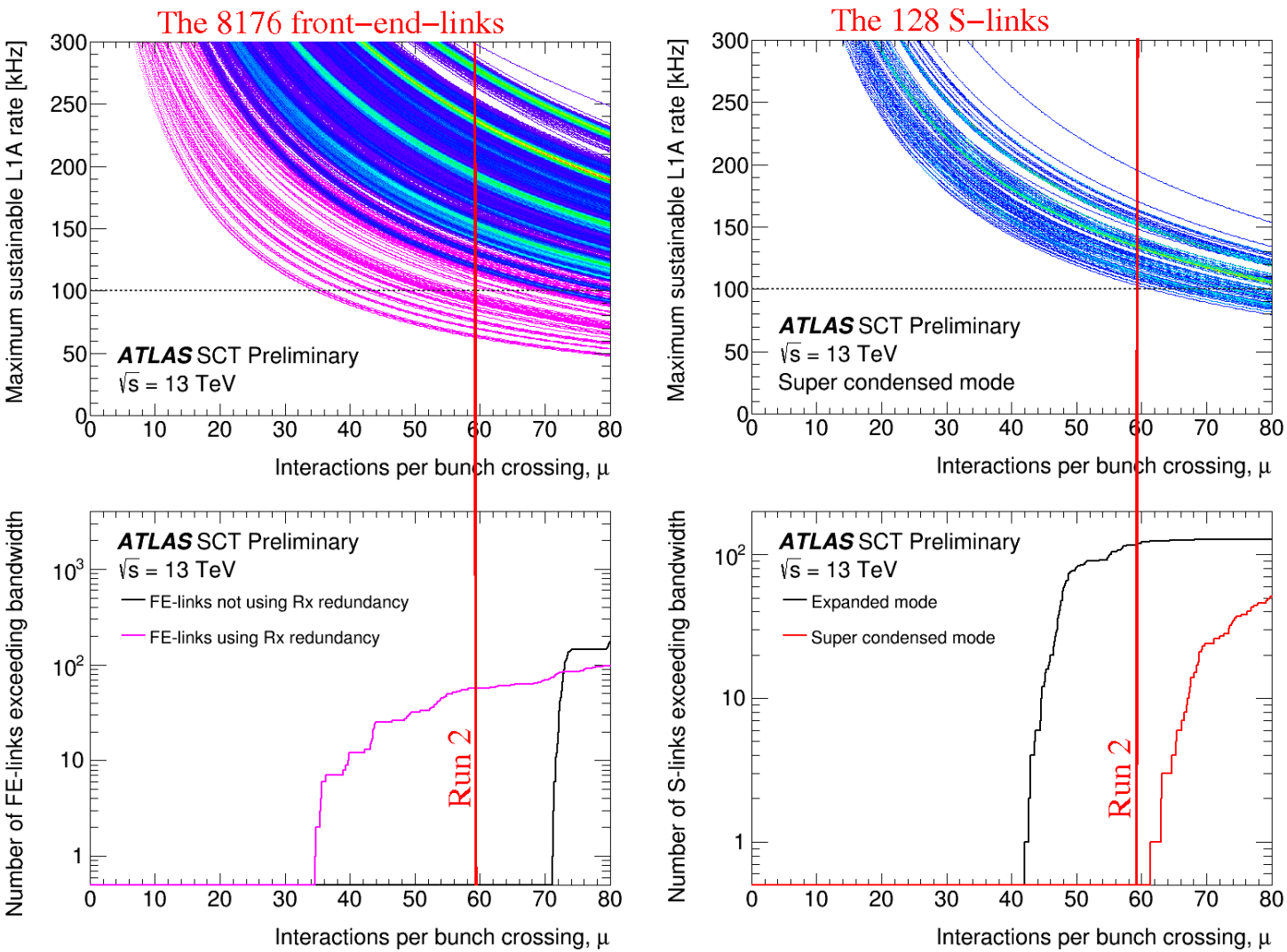
- Data that is being assembled into an event fragment from multiple sources can go out of synch when individual contributions belong to different events.
- Desynchronization can happen at the module level (between frontends) or at the readout level (between modules).
- Every 5 s the ATLAS Central Trigger Processor (CTP) sends an Event Counter Reset signal (ECR) inside a 2 ms window without triggers.
- The Pixel Detector uses this time to resynchronize:
  - Sends a frontend sync command to the modules.
  - Resets the firmware in the RODs.
- In the plots the new readout has the ECR firmware reset, the old readout doesn't.





Substantial improvement in data quality.

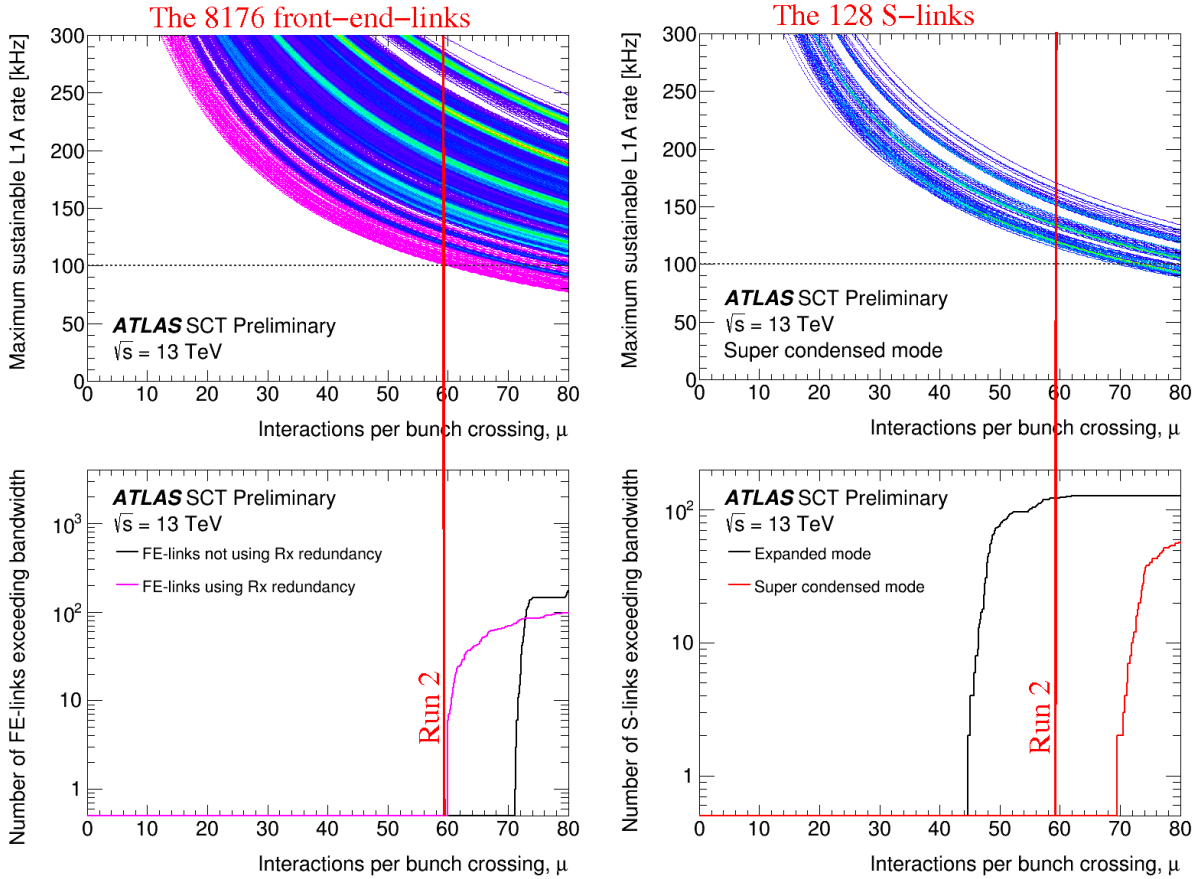
SCT Bandwidth



- Frontend links are the optical links between detector and counting house (ROD).
- S-Link is the downstream link from the ROD (event fragments).

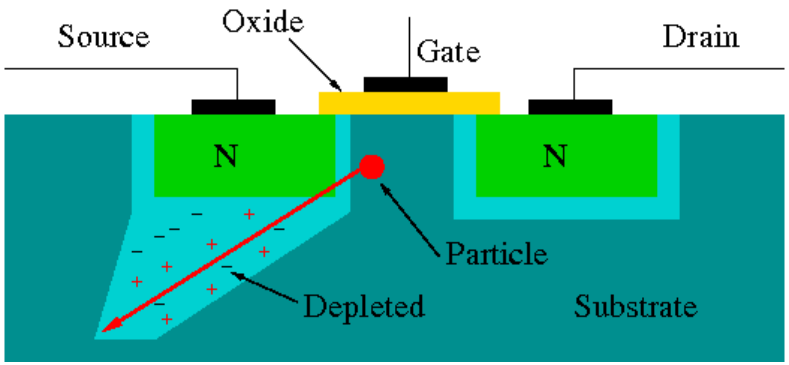
SCT Bandwidth Strategy

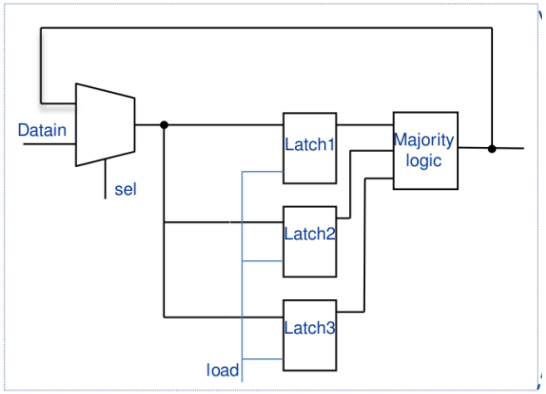
- **Frontend links:** Dynamic masking of chips depending on instantaneous luminosity during the run to reduce data volume.
- Up to a maximum of 163 masked chips in total (0.3 %).
- Efficiency loss below 1 %.
- **S-Link:** Remapped 23 frontend links onto S-links to optimize bandwidth usage.



SCT is fine at a L1 trigger rate of 100 kHz and a pile-up of 60.

Pixel Single Event Upsets



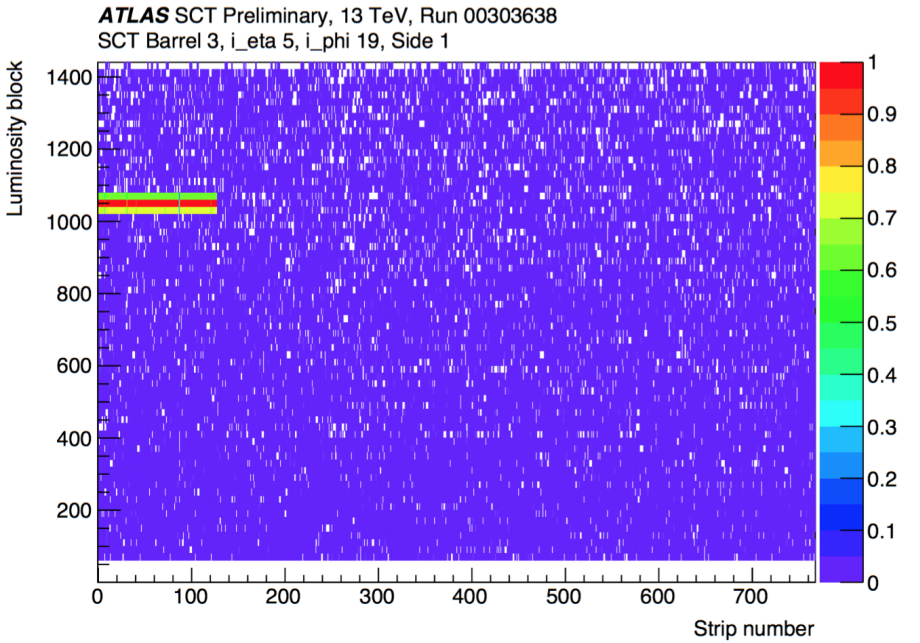


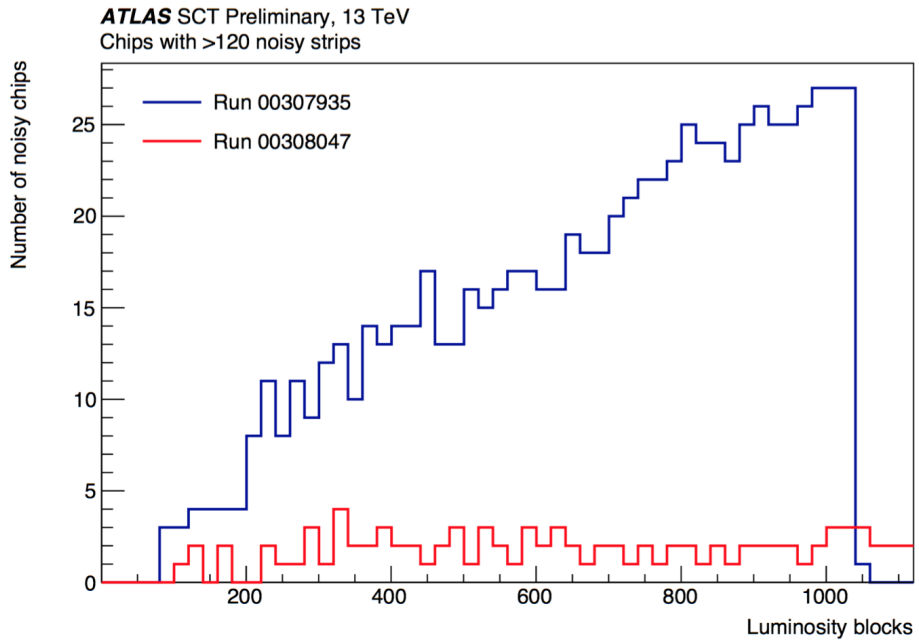
- The registers in Pixel/IBL have triple redundancy and majority logic to make them resilient against single event upsets.
- Nonetheless we do observe a number of SEUs per run.
- Symptoms are mostly a change in frontend current and a decrease in occupancy.
- Occurs particularly in IBL.

Countermeasures:

- *Reconfiguration at ECR:* The global registers for all IBL modules are now reconfigured every 5 s. This happens during the 2 ms ECR-busy window from ATLAS so no data taking efficiency is sacrificed.
- *"Quick Status":* Constant monitoring of occupancy and status counters from the firmware. Automated response by reconfiguration of a module.

SCT Single Event Upsets





Two types of SEUs:

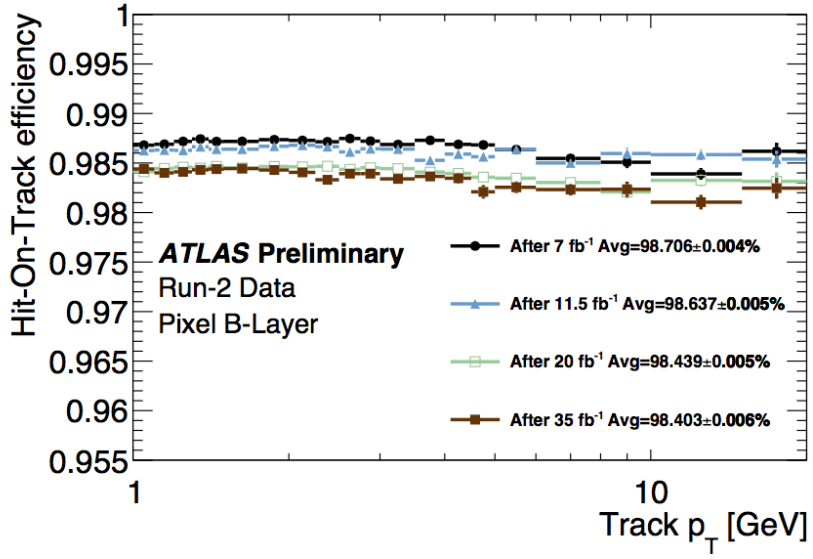
- Desynchronization of modules due to energy deposition in the pin diode (opto-link).
- Change in occupancy due to corruption in the frontend registers.

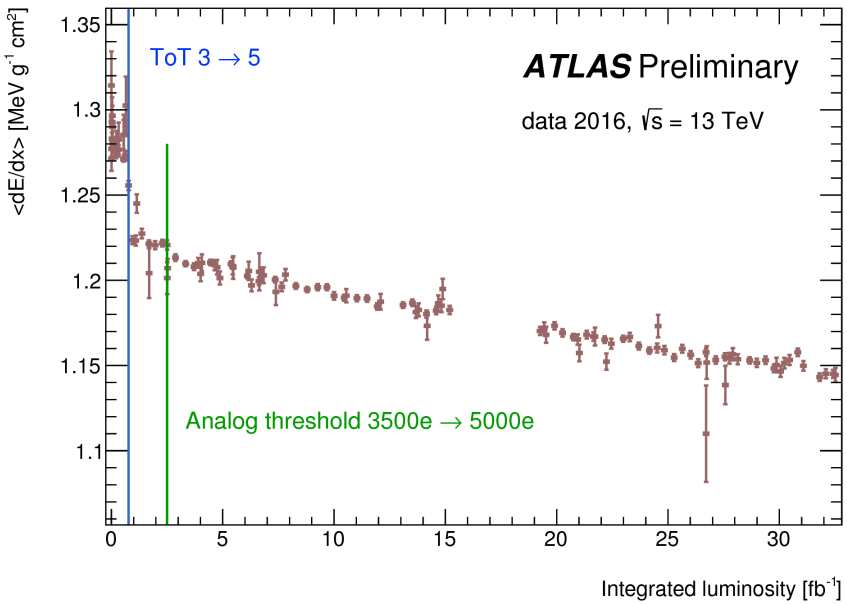
Countermeasures:

- Desynchronization is detected and recovered within one minute.
- The entire SCT detector is reconfigured every 30 minutes to remove corruption in the register settings. The feature was enabled in run 308047 (plot).

Pixel Total Integrated Dose Effects

- The charge collection efficiency in the sensors decreases with radiation dose.
- This affects the tracking efficiency.
- About 0.3 % efficiency loss during 2016.
- The dE/dx measurements is also affected by radiation damage. Steps in the dE/dx plot are due to the new ToT cut and threshold settings (loss of low-ToT pixels in the clusters).

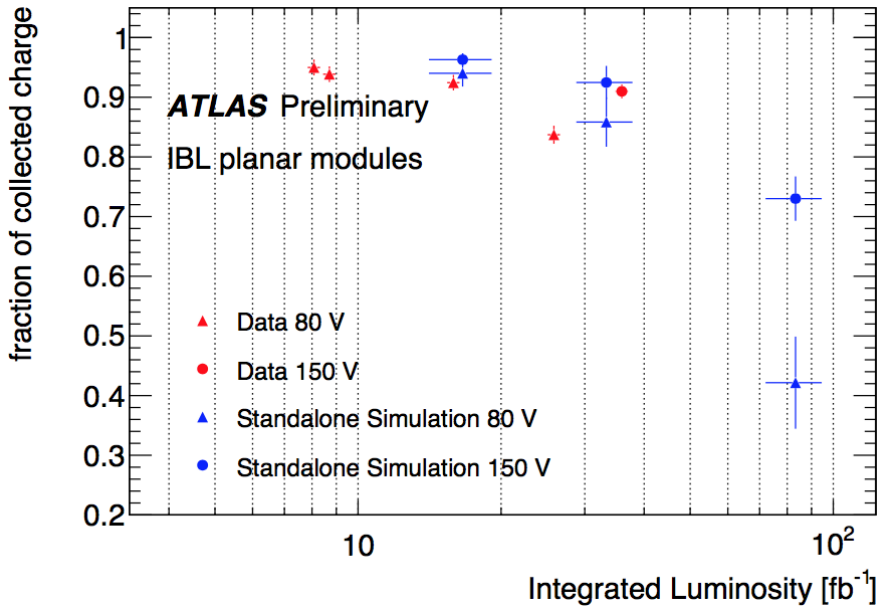


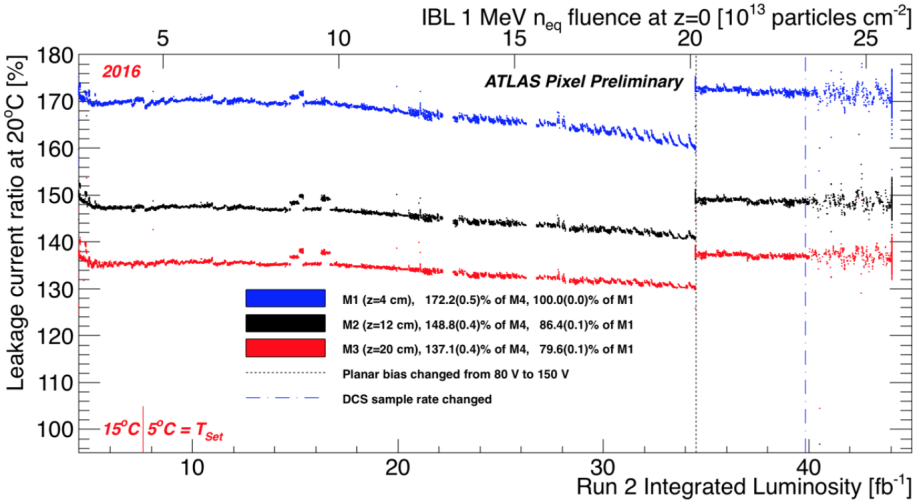


IBL Charge Collection Efficiency

- Simulation of charge collection efficiency.
- Geant 4, field maps from TCAD with Chiochia model.
- Central IBL: $|\eta| < 0.2$
- Comparison with 2016 data.
- Extrapolation at 2 bias voltages.

$\Longrightarrow$ *Ongoing effort to model the evolution of the efficiency with dose.*





- Increased the bias voltage for the planar sensors in IBL from 80 V to 150 V during 2016 (3D sensors still fully depleted at 20 V).
- The leakage current ratio between planar and 3D sensors went back to a constant level $\Longrightarrow$ back to full depletion.

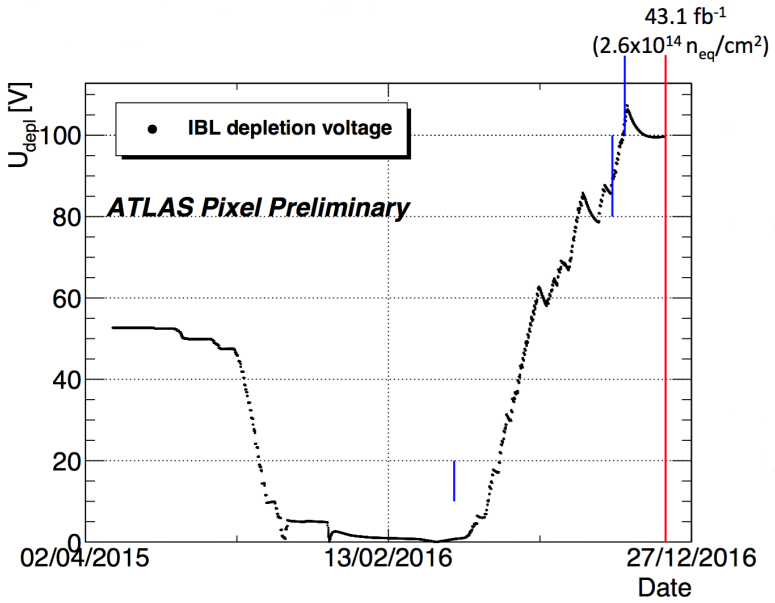
Pixel Depletion Voltage

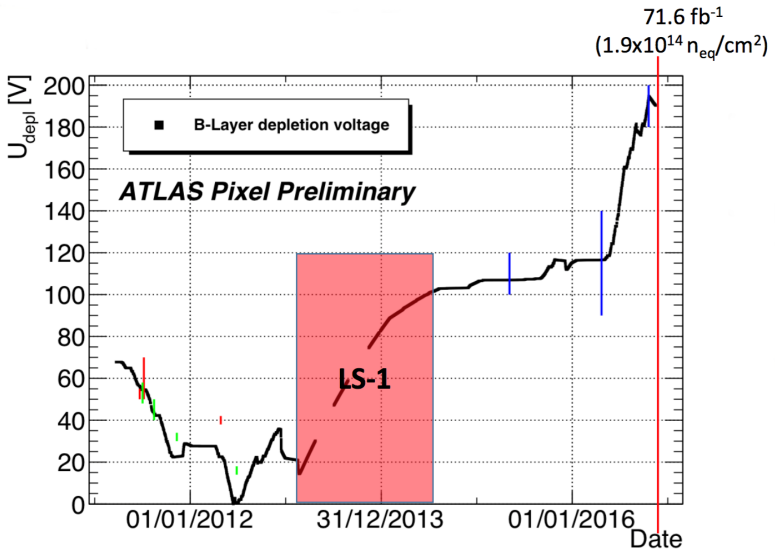
- Using the Hamburg model to predict the increase of the depletion voltages for pixel/IBL.
- HV-scans are performed regularly to monitor the actual depletion voltage.
- Data points in the plots are from the HV-scans.
- LS1 is “long shutdown 1”.

Simulation extended to 2017:

- **IBL:** Expecting increase to 350 V.
- **B-Layer:** Expecting increase to 300 V.

$\Longrightarrow$ IBL bias voltage adjusted accordingly.

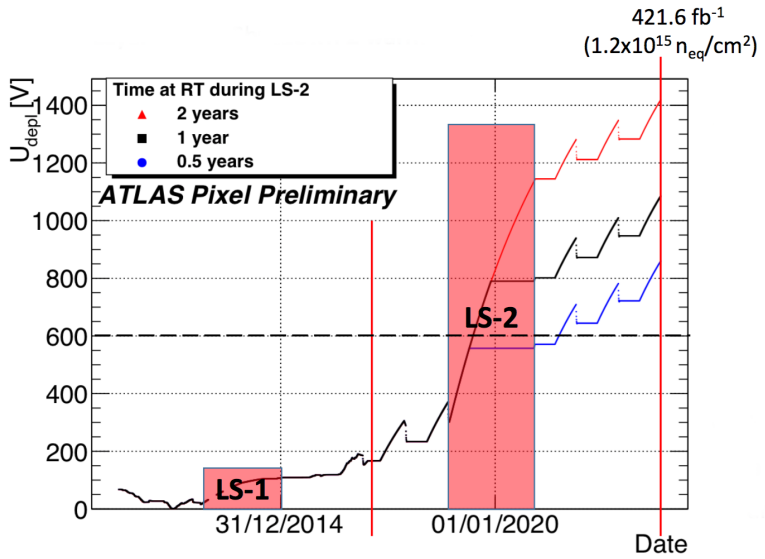


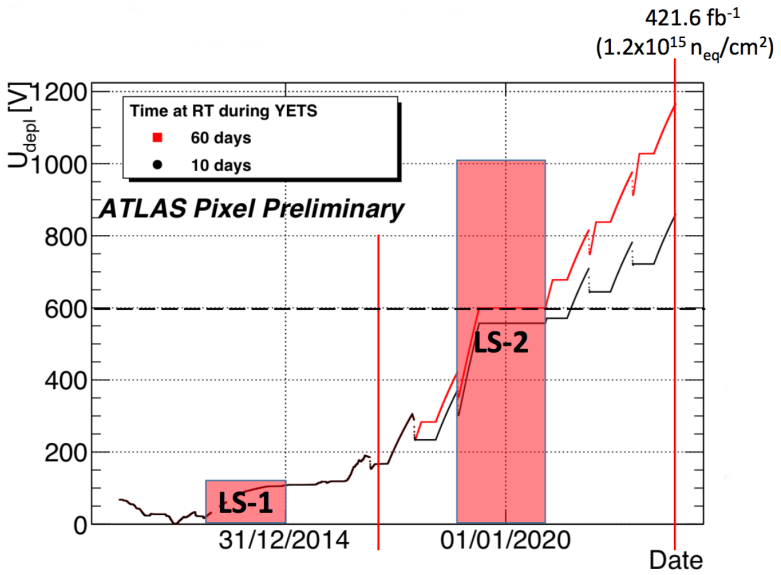


Pixel Reverse Annealing

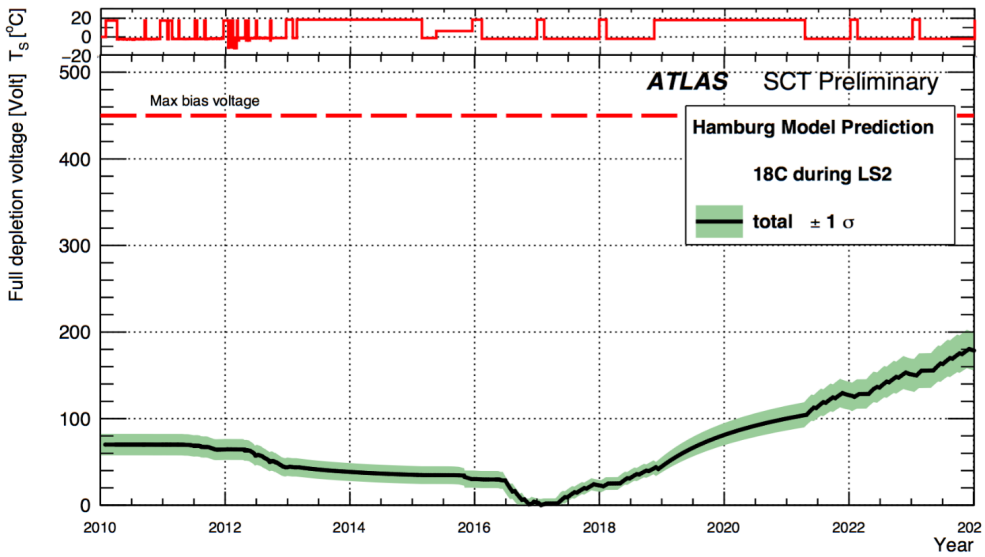
- Reverse annealing is a serious operational issue.
- If the Pixel Detector is warmed up during shutdowns the depletion voltage will increase far beyond the operational limit of 600 V.
- This is especially true for LS2 (long shutdown 2, top plot).
- But even 60 days during an end-of-year shutdown instead of 10 make a large difference (bottom plot).
- The plots show the prediction for the B-layer.

It is crucial to keep the detector cold.

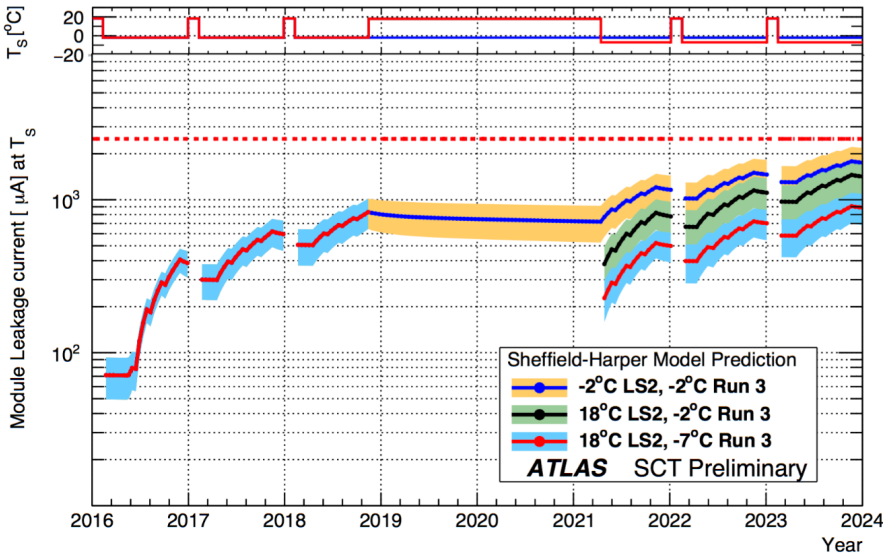




SCT Depletion Voltage



Barrel 3 Depletion Voltage



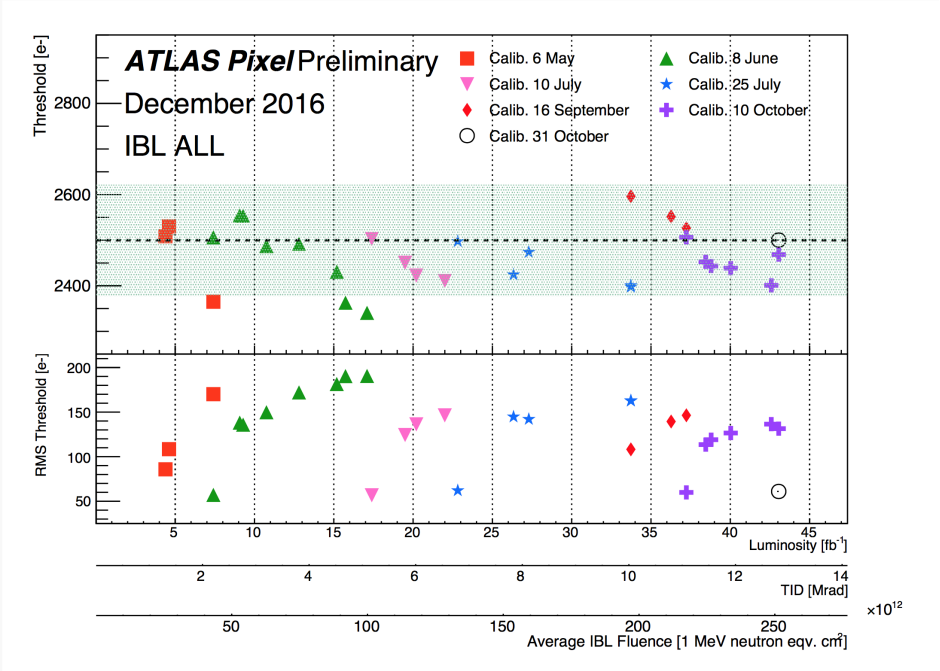
Barrel 3 leakage currents

- Since the SCT is not as close to the beam the radiation damage is not nearly as severe as in the Pixel Detector.
- The depletion voltage is expected to be around 200 V at the end of run 3.
- Far below the high voltage limit of 450 V.
- The leakage current is expected to end up at around 1.3 mA per channel.

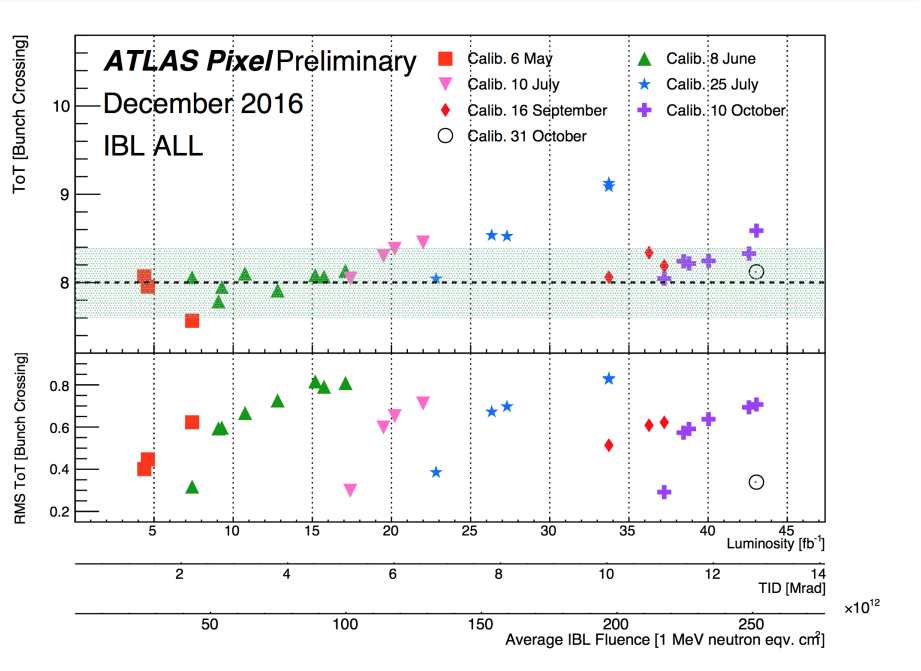
$\Longrightarrow$ Depletion of the sensors is not an issue in SCT.

IBL Calibration Drift

Threshold:

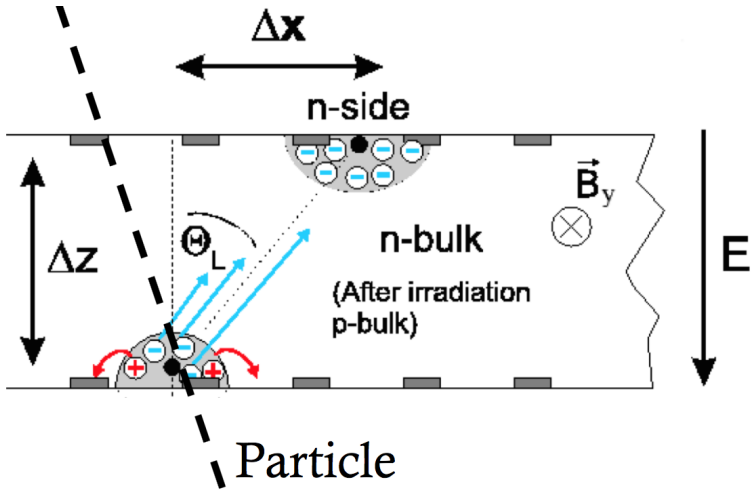


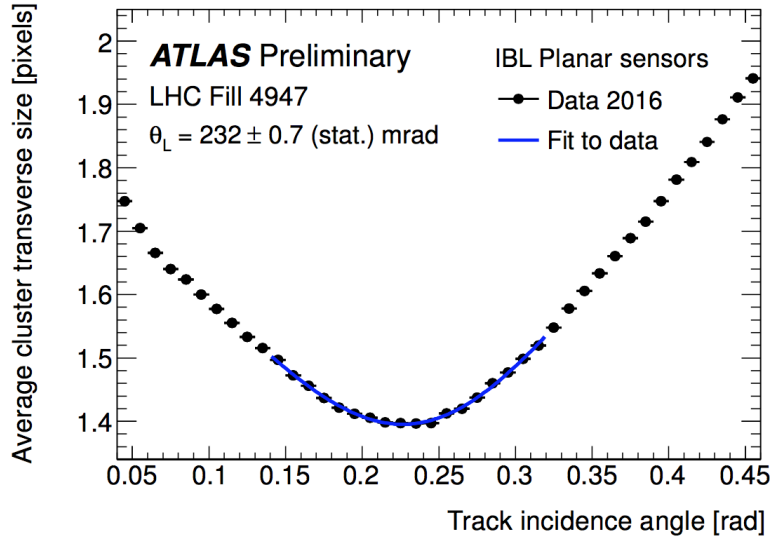
ToT:

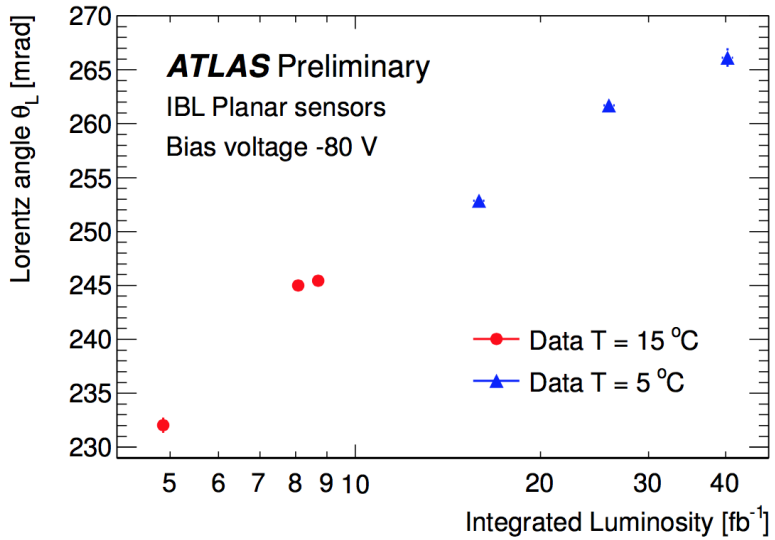


- TID causes a drift in the thresholds and the ToT tuning of the frontend.
- Most pronounced in IBL where the transistors do not have a rad-hard design.
- Frequent retuning required.
- Largest changes during the first few Mrad.
- Now well past that level so calibration is drifting less rapidly.

IBL Lorentz Angle







- Charges drift transversally in planar sensors because of the perpendicular magnetic field.
- The angle between electric field and the drift direction is called the Lorentz angle.
- This effect introduces a bias on the cluster position reconstruction.
- The electric field changes with radiation damage.
- This results in a drift of the Lorentz angle with integrated luminosity (lower plot).

Summary

- The performance of the LHC far beyond the original specification has been presenting a challenge to the operation of the detectors in terms of
  - Bandwidth.
  - Single Event Upsets.
  - Radiation damage.
- Thanks to a number of improvements and techniques SCT and Pixel continue to provide tracking with high efficiency and low deadtime to the ATLAS experiment.
- The current configuration is adequate until the end of run 2. In run 3 new measures may have to be taken to cope with any additional increase in luminosity.