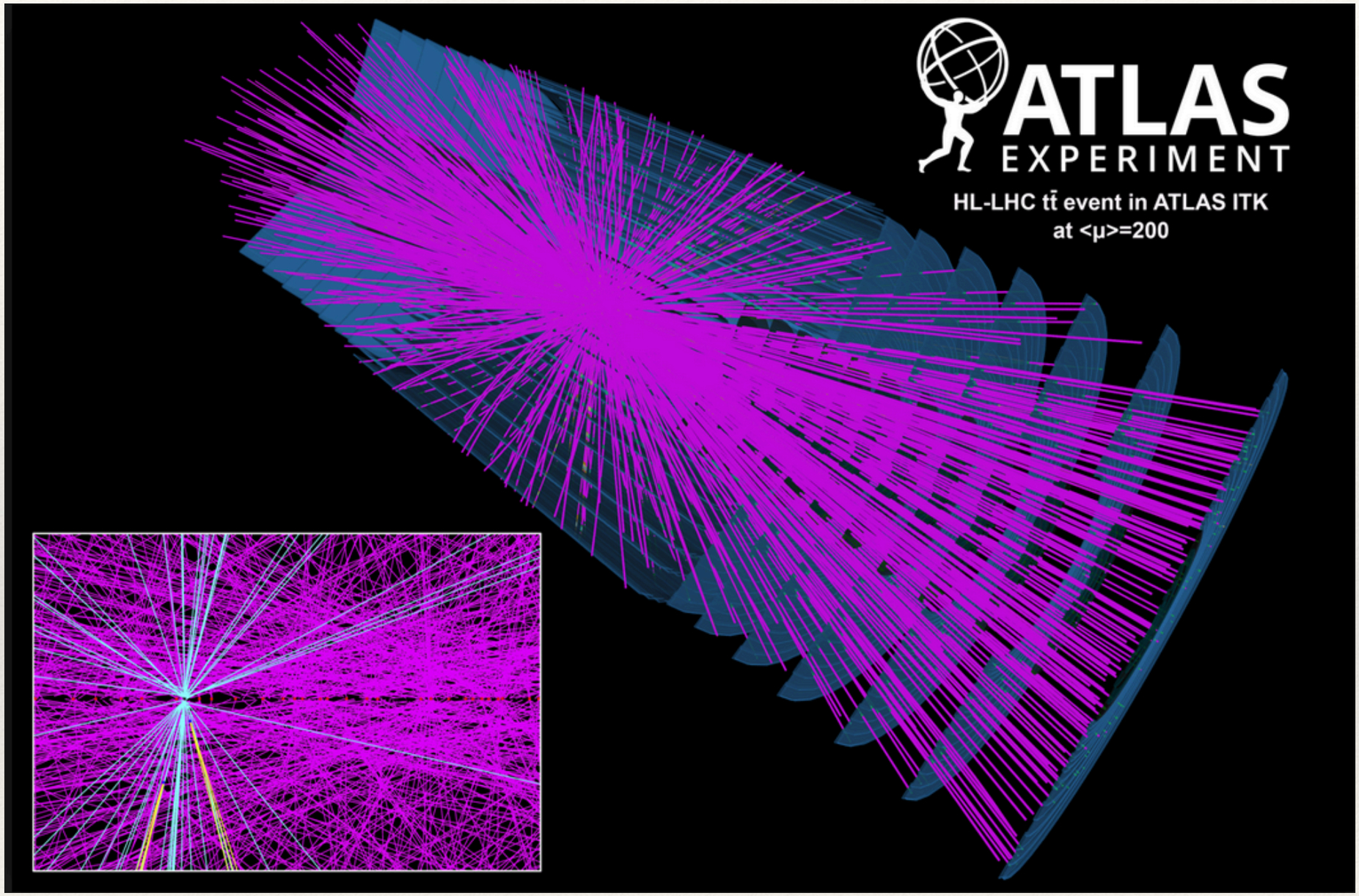
Module and electronics developments for the ATLAS ITk pixel system



Francisca Muñoz Sánchez
on behalf of the ATLAS ITk Collaboration

19th iWoRiD, 3rd July 2017. Krakow, Poland

MANCHESTER 1824
The University of Manchester

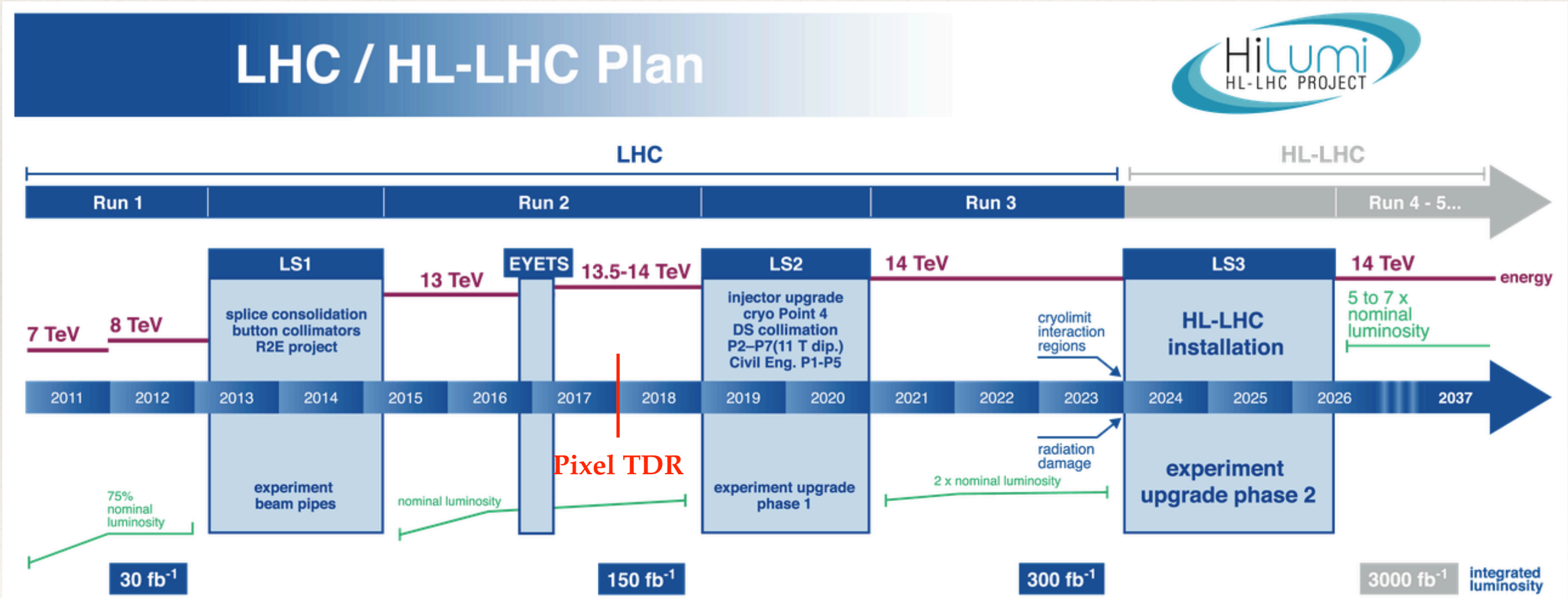
Outline

- Schedule of the HL-LHC
- The current Inner Detector and the ATLAS ITk upgrade
- The RD53 Collaboration. New Pixel Read Out Chip
- R&D on Pixel Modules:
  - Sensors: 3D and planar technologies
  - Interconnection Techniques
  - CMOS detectors
- Readout and Electronics R&D
  - High Data Rate
  - Serial Powering
- Other R&D activities
- Perspectives and Conclusions

ATLAS EXPERIMENT

Schedule of HL-LHC

- The LHC will upgrade to the High-Luminosity-LHC (HL-LHC) raising the integrated luminosity from 300 fb^{-1} (LHC) to 3000 fb^{-1} by 2035
- Exceptional technological challenges: 13 Tesla superconducting magnets, ultra-precise cavities for beam rotation, 300m long lines with low dissipation
- More accurate measurements of new particles and opening the sensitivity window to rare events that can point to new Physics



ATLAS EXPERIMENT

HL-LHC. ATLAS Inner detector upgrade

- Together with the LHC upgrade, experiments must be upgraded

- The design of the current **ATLAS inner detector** requires an upgrade to operate considering the following changes with the HL-LHC:
  - The peak luminosity: $\mathscr{L}_{\text{HL-LHC}} = \mathbf{7.5} \times \mathscr{L}_{\text{LHC}} = 7.5 \times 10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}$
  - The average pile-up: $\langle\mu\rangle_{\text{HL-LHC}} \sim \mathbf{8} \times \langle\mu\rangle_{\text{LHC}} \sim 200$
  - Integrated luminosity: $L_{\text{HL-LHC}} = \mathbf{10} \times L_{\text{LHC}} = 3000\ \text{fb}^{-1}$
  - Radiation hardness: $\phi_{\text{HL-LHC}} = \mathbf{20} \times \phi_{\text{LHC}} = 2 \times 10^{16}\ n_{eq}/\text{cm}^2$

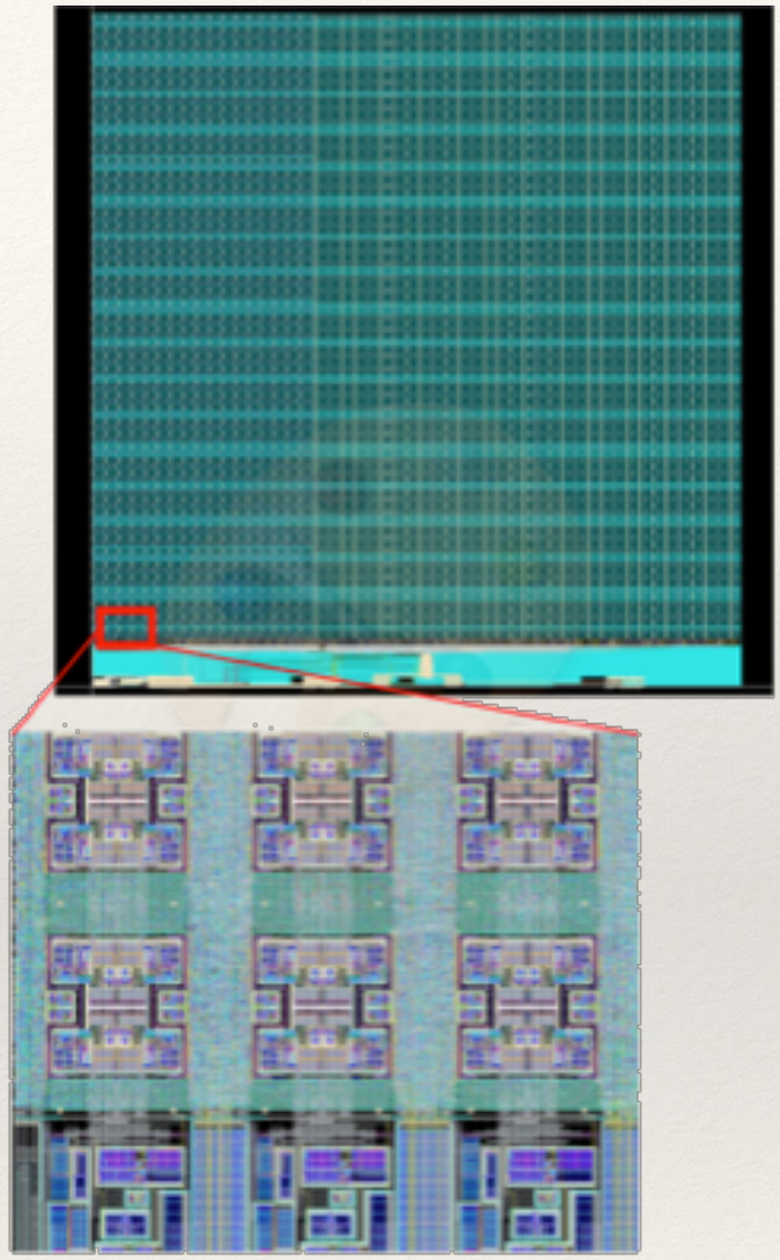
- The **new ATLAS inner tracker (ITk)** will require:
  - Increased Radiation Hardness (sensor, chip, cables…etc)
  - Higher Granularity - Smaller pixel segmentation
  - Higher data rate capabilities
  - 65 nm readout ASIC with 5Gbps maximum data rate (RD53)

ATLAS ITk talks in iWoRiD 2017:

Laurelle Veloce (Strips), Trevor Vickey (Design), Tianyang Wang and Andrea Gaudiello (CMOS), Natascha Savic (n-in-p planar sensors):

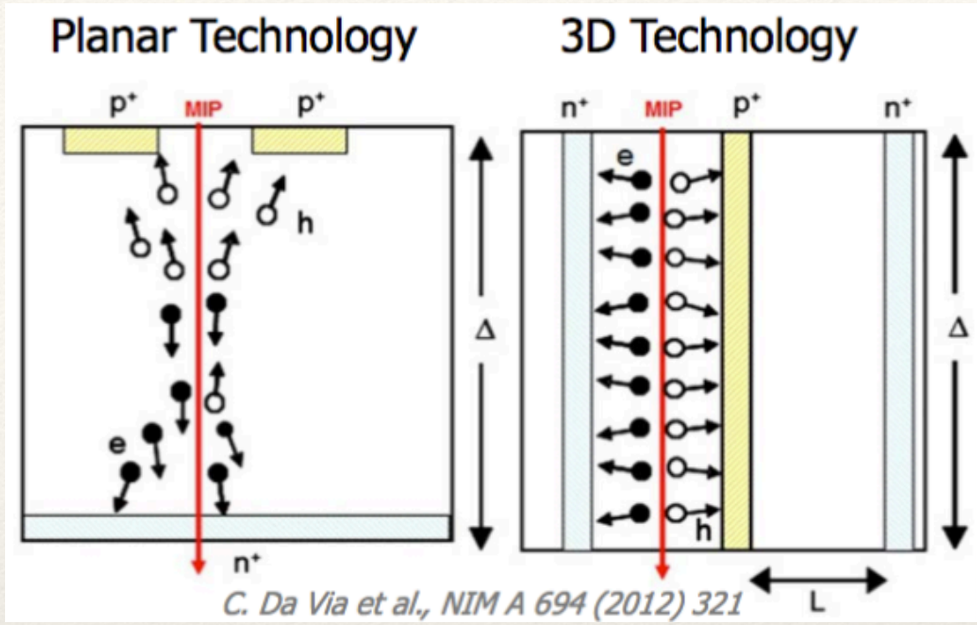
The RD53 Collaboration

- The next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC is being developed by the RD53 collaboration. Full scale (~ 20 x 12 mm^2) demonstrator by Autumn this year
  - It will use the **65nm technology** to increase radiation hardness
  - Small pixels **50 x 50 μm^2 (25 x100 μm^2)**
  - Low in-time threshold **(1000 e-)**
  - Shunt LDO implemented for compatibility with **Serial Powering**
  - Highest data rate achievable per ASIC: **5 Gbps**



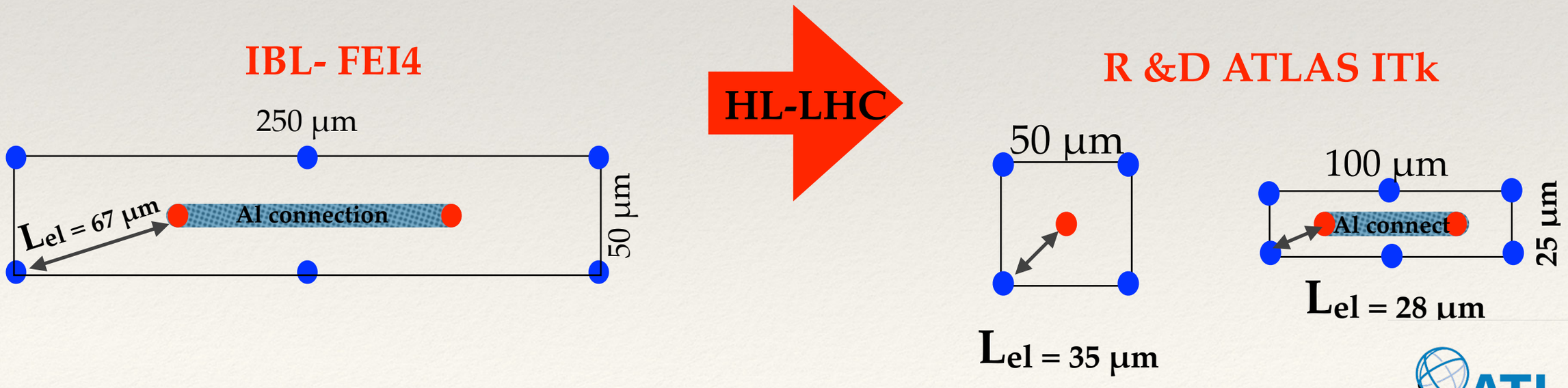
Pixel Sensors: 3D

- 3D silicon sensor technology is the prime candidate for the innermost pixel layer of the ATLAS ITk where the expected fluences will reach $2 \cdot 10$ n_{eq}/cm^2
- Shorter 3D inter-electrode (L_{el}) distance reduces the bias voltage (power dissipation, cooling), results in faster charge collection, less trapping, slim edges
- Production process time is longer and yields are lower than for planar resulting in higher final cost



25 % of the IBL pixel detectors are in 3D silicon technologies. Running successfully since June 2015. Manufactured by CNM and FBK

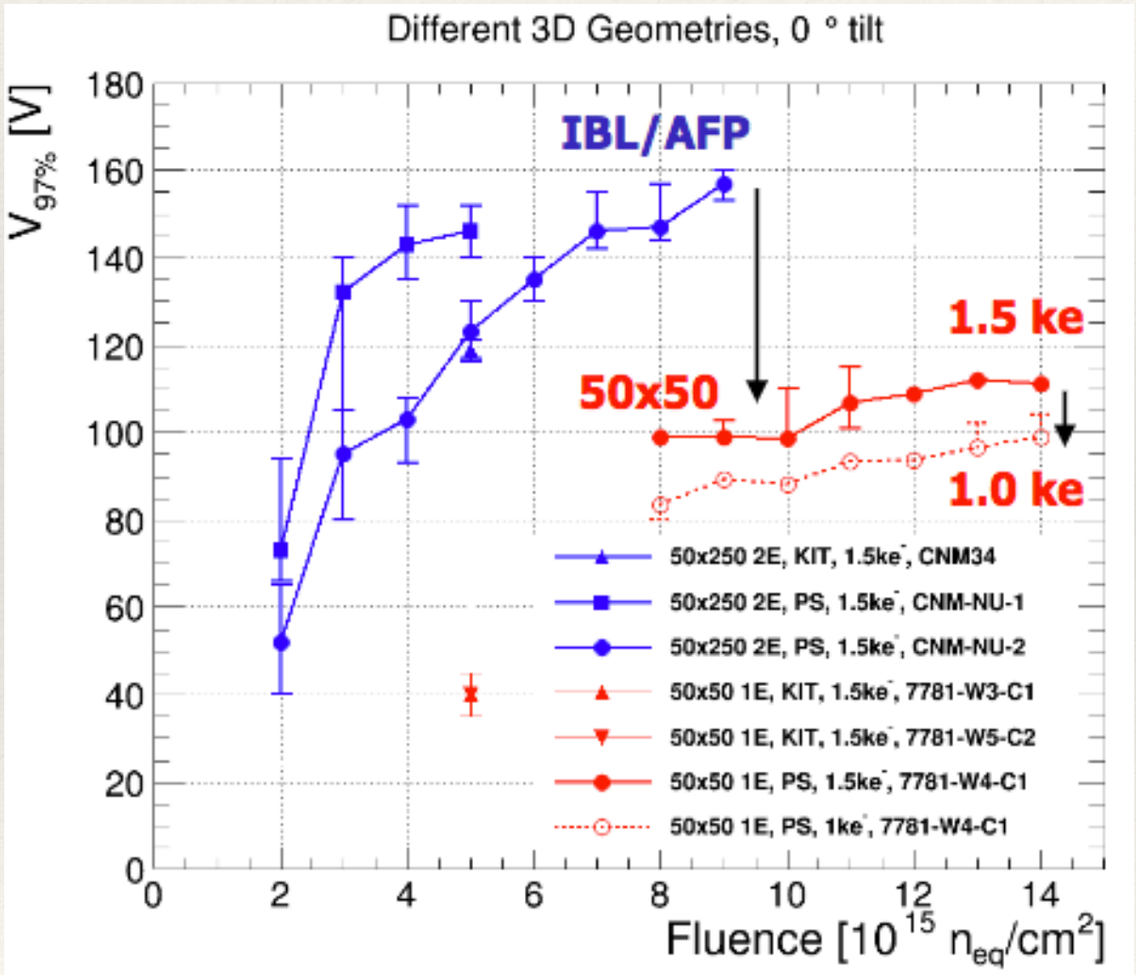
- Smaller pixel size requires technology development to decrease the electrode diameter. Final thickness for ITk still under discussion

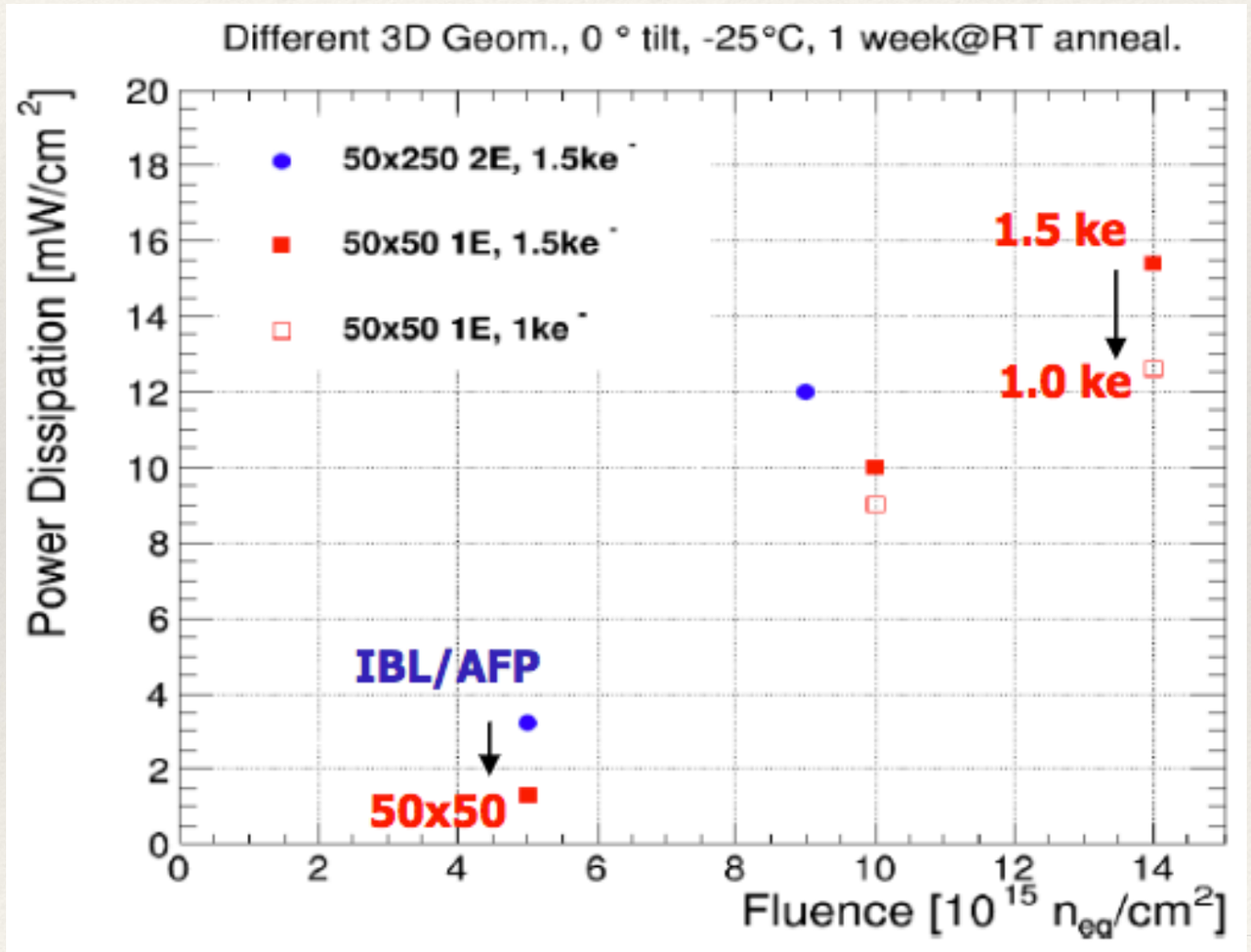


Pixel Sensors: 3D

- Small pitch 3D sensors have already been investigated before and after irradiation up to 1.4e16 neq/cm2, showing excellent detection efficiency
- The power dissipation after the expected innermost layer high irradiation fluences has been also investigated
- Both studies show very good results improving the performance over the IBL-like 3D sensors

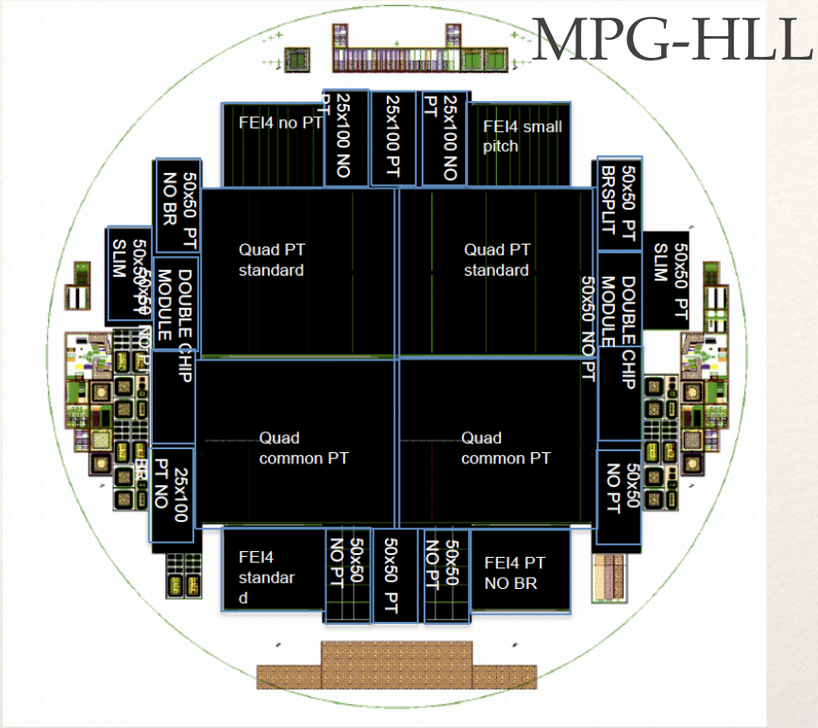
Joern Lange et al. "Radiation hardness of small-pitch 3D pixel sensors up to HL-LHC fluences". TIPP2017

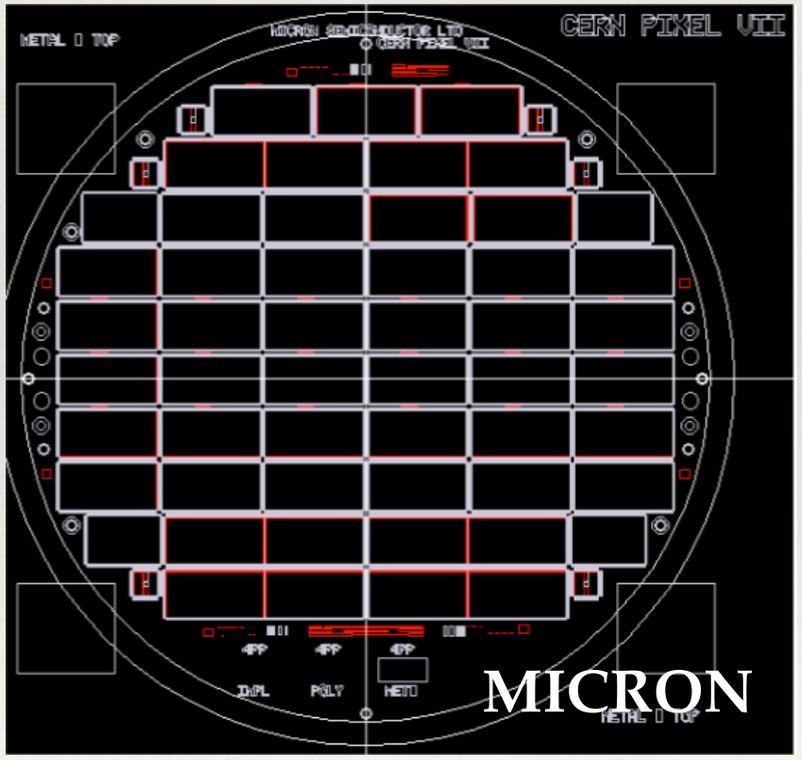




Pixel Sensors: Planar

- Planar silicon sensor technology used in IBL layer are prime candidates for the inner and outer pixel layers of the ATLAS ITk
- The cost of planar silicon technologies is lower than 3D and therefore more practical for bigger areas (outer layers)
- Thinner planar sensors are requested to deal with higher irradiation dose and power dissipation (100- 150 μm under consideration)
- New techniques for thinning with/without using support wafers are under development (see this talk from CiS by Ralf Röder et al. at TREDI2017)
- Main developments are on FE I4 quads to exercise multi-chip module assembly, active edge and RD53 compatible sensor productions
- RD53/FEI4 productions are ongoing involving several institutes and companies (only a few examples here)

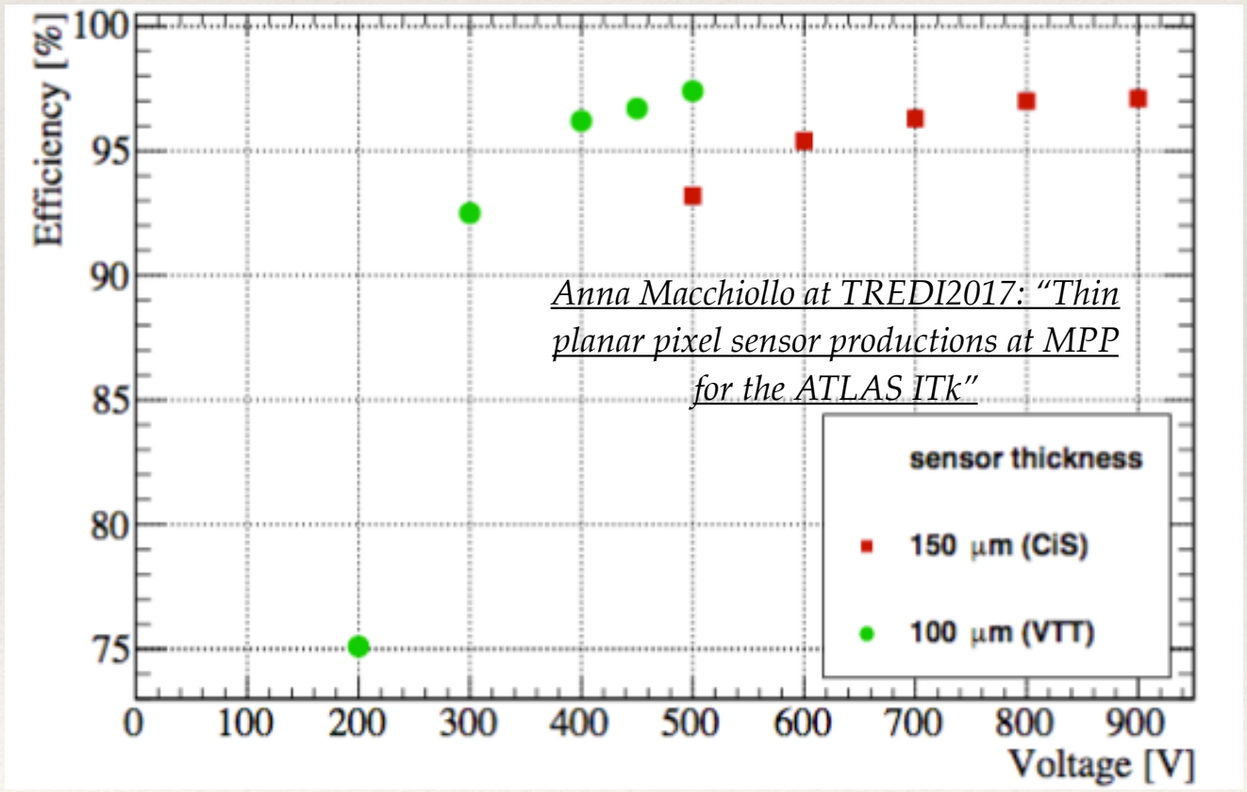




Pixel sensors. Planar

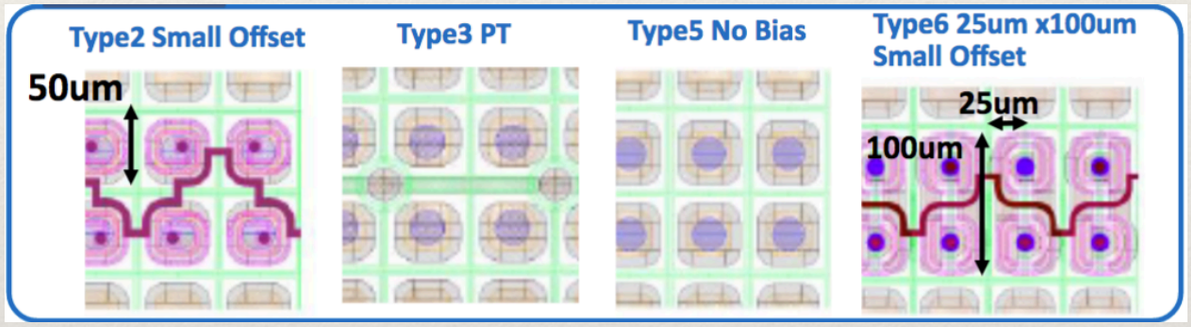
Characterisation campaigns have been carried out to study different bias structures, bias ring configurations, high incidence angle and radiation hardness (two results are included here, but intense R&D is being carried out by the ATLAS sensor community)

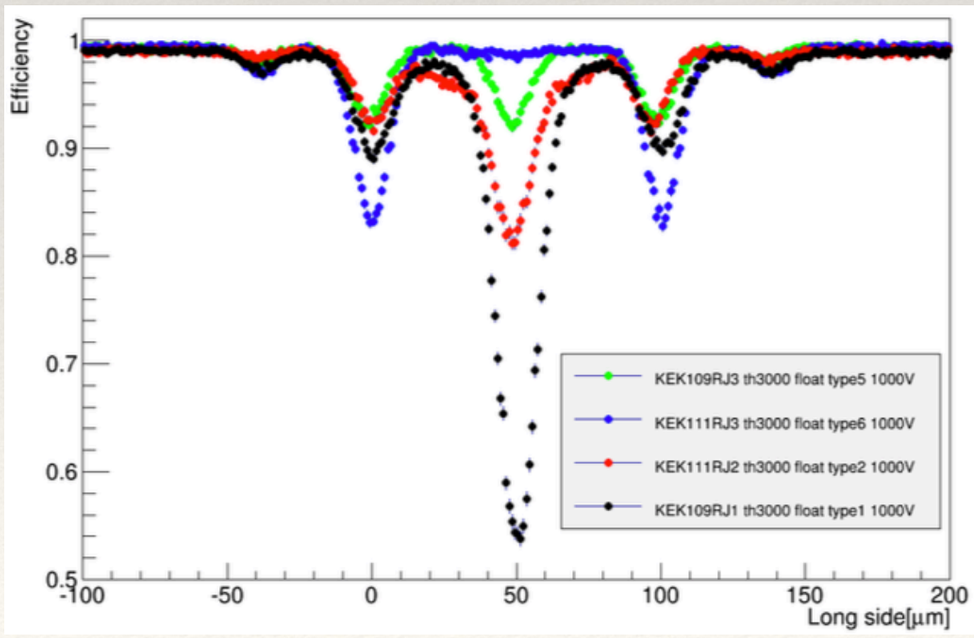
Hit Efficiency for 100 and 150 μm thick planar n-in-p sensors: FEI4 like, irradiated up to $\phi = 1 \cdot 10^{16}\ n_{eq}/cm^2$. Please see Natascha Savic's talk "Thin n-in-p planar pixel developments for the ATLAS ITK" on Thursday



Anna Macchiollo at TREDI2017: "Thin planar pixel sensor productions at MPP for the ATLAS ITk"

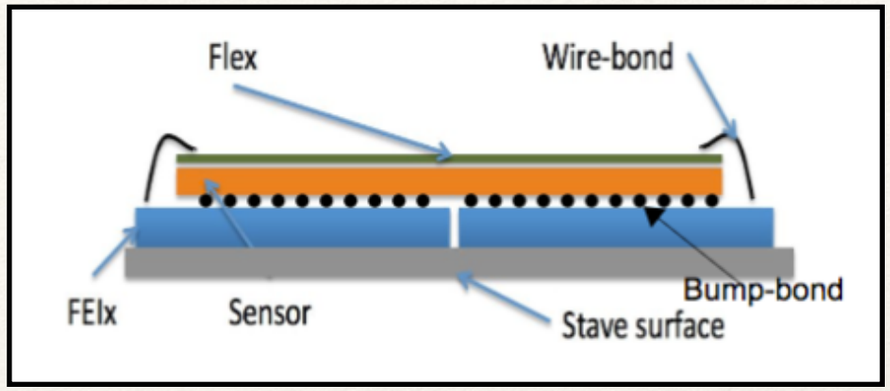
Biasing structures are needed to guarantee the sensor performance prior to assembly. But some of those structures can produce hit efficiency losses once sensors have been irradiated. As was shown by Y. Unno at TREDI2017



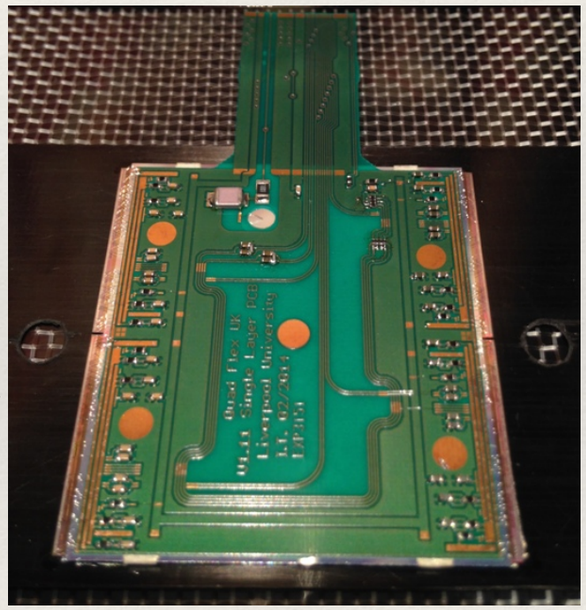


Chip-Sensor Interconnection

- Bump-bonding is the chip-sensor interconnection technique chosen for the ITk. This technique is facing new challenges
  - 50 x 50 μm^2 pixels, which is the same pitch as for IBL but 5 times higher density
  - Larger ASIC wafer size (12")
  - Higher ASIC size (~4 x 4 cm2)
  - Thinner sensors and ASIC ($\leq$ 150 μm)



Transversal section of an ITk module

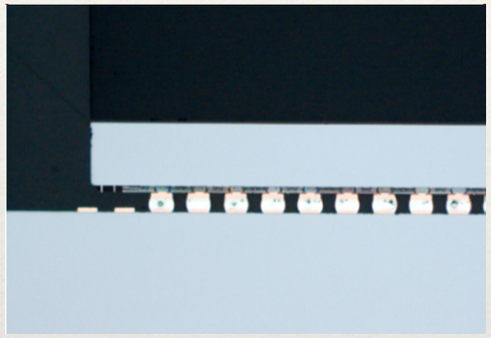


- There is an intense effort to qualify the technique for the ITk pixel detector:
  - Dummy wafers with **Daisy chain** to test the process at high density
  - Stress **compensation layers** or **handling wafers** to cope with the assembly bow
  - Evaluation of **bump deposition** vendors on 12 " wafers
  - Evaluation of **UBM deposition** by sensor vendors
  - Evaluation of in-house **flip-chip** of modules for cost-saving
  - Studies of alternative bonding methods (Indium, wafer to wafer bonding, TSV)

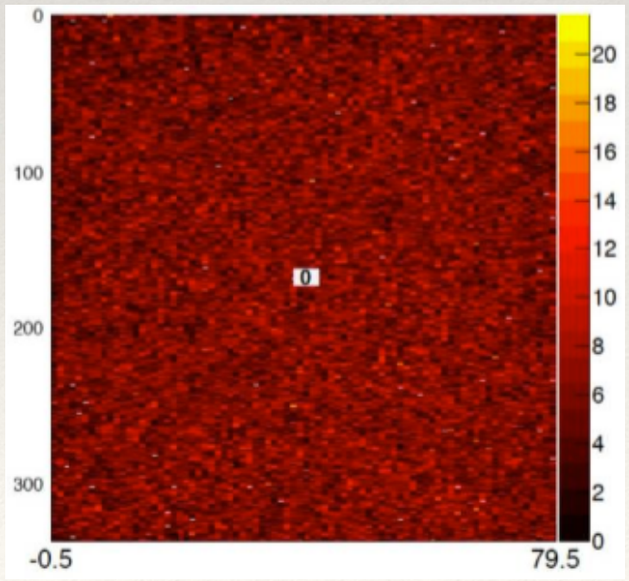
Interconnection R&D

Strong collaboration with vendors on the interconnection R&D

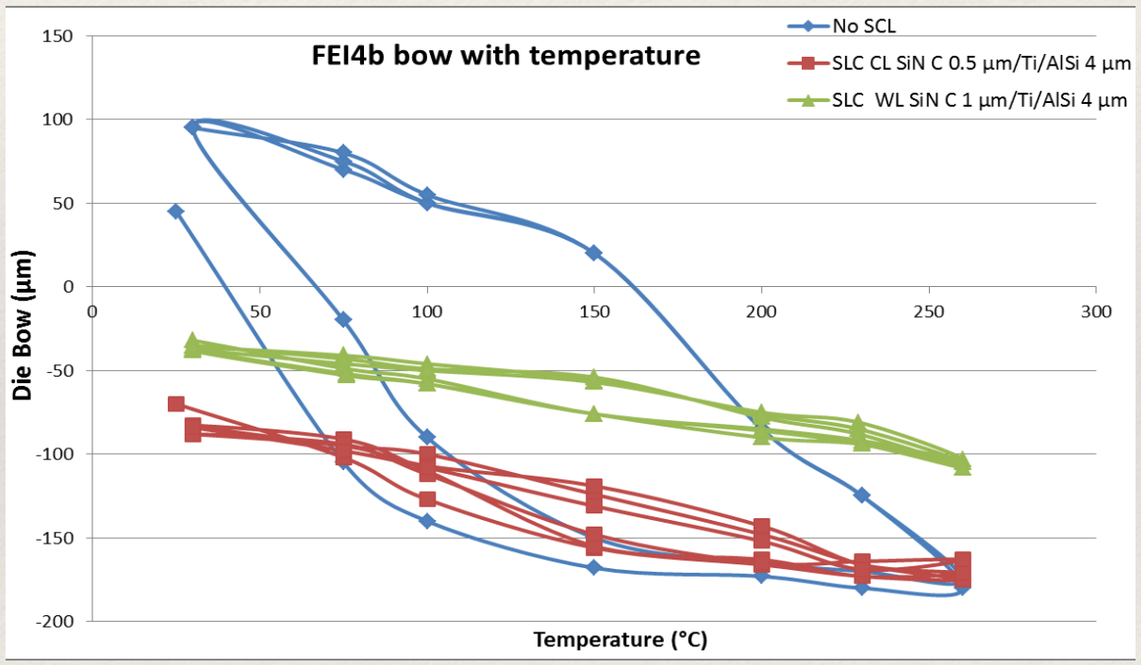
- Support wafer with IZM. Laser Removal of the support wafer



- High bump density results with CiS



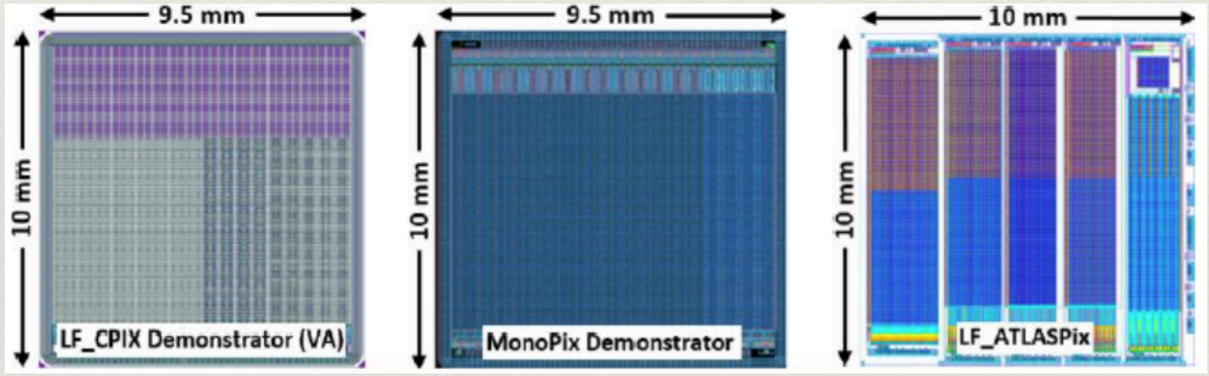
- Stress compensation layer with CEA-LETI (150 µm sensor and 100 µm ASIC) SiN compensates the offset and Al the hysteresis effect



Pixel Detectors: CMOS sensors

The ITk CMOS collaboration is actively investigating this technology, which is a candidate for the outer pixel layers of the ITk:

- Low Material budget
- Low power consumption
- Low production/assembly costs
- New read outs and pixel scheme under development
- Many prototypes being characterised
- Still in process of qualification for the ITk (hopefully for the TDR)



Please see talks: "CMOS pixel development for the ATLAS experiment at the HL-LHC" by Andrea Gaudiello

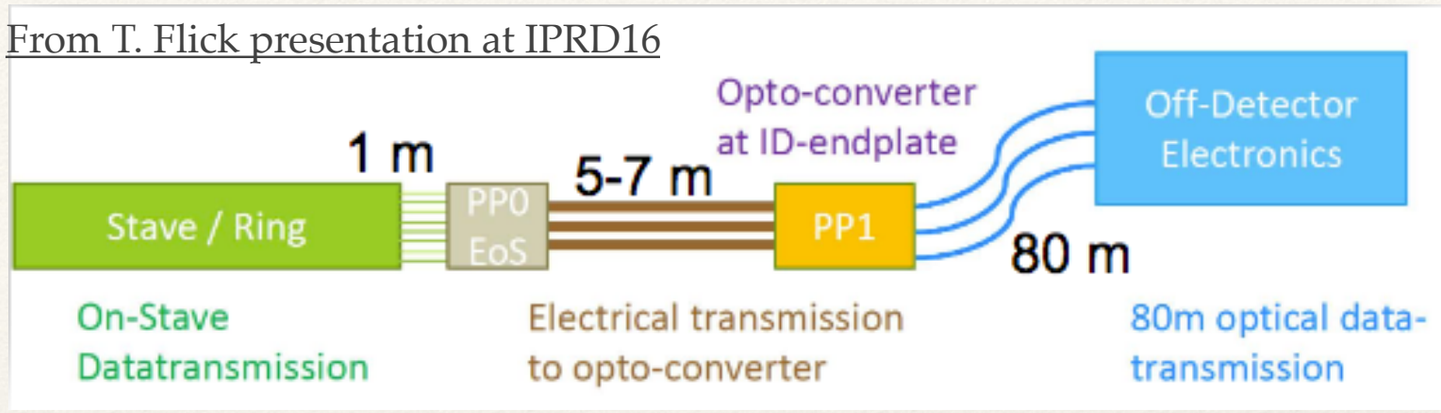
"Development of depleted monolithic CMOS sensors with fast readout architecture for the ATLAS Inner Tracker upgrade" by Tianyang Wang

Readout

Connection between on- and off-detector via electrical-optical link:

- From FE-chip to end of ITk electrically (5-7 m)
- Then optically towards the off-detector electronics (~80 m)

From T. Flick presentation at IPRD16

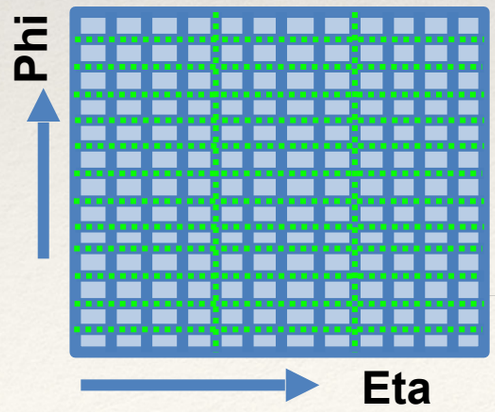


A readout system serving a data rate of several Gb/s is under development:

- A readout speed of up to 5 Gb/s per data link (FE-chip) is foreseen for the innermost layer 640 Mb/s in the outermost
- The same system will be used for data taking and detector calibration during operation
- It will integrate timing, trigger, data handling and command lines
- It is crucial to understand occupancies for a given geometry, which requires effort in coding and compression algorithms to minimise rate

Data rate = chipFreq * 1.05*(32bits*<Nhits>)/<RO>

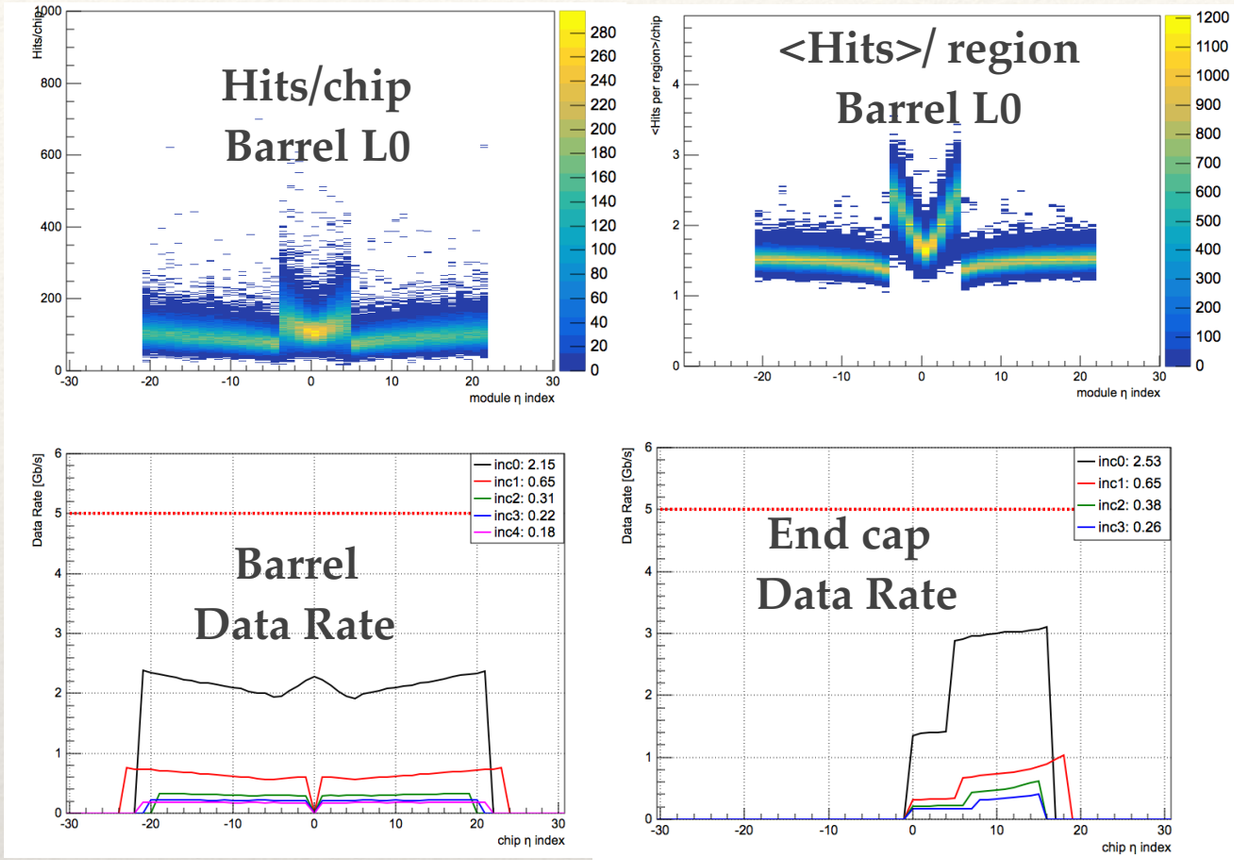
RO=regional occupancy



Occupancies & Data rates

Example: step 1.6 ITk inclined geometry for ttbar+minimum bias events

- Average hit rates and regional occupancies over phi to give eta (radial distributions)
- Regional occupancy determined over 1 x 4 in phi x eta space:
- Data Rate scales with
  - Chip Frequency
  - Chips per cable
  - Limited to 5 Gb/s per cable



Brl	<hits/chip>$_{eta}$	<<hits>/region>$_{eta}$
Lyr 0	107	1.68
Lyr 1	29	1.54
Lyr 2	15	1.55
Lyr 3	10	1.50
Lyr 4	8	1.46

Not scaled!!

<dataRate>$_{eta}$	Barrel (Gbps)	End (Gbps)
Layer 0	2.15	2.53
Layer 1	0.65	0.65
Layer 2	0.31	0.38
Layer 3	0.22	0.26
Layer 4	0.18	--

Thanks to Craig Buttar, Kenneth Wraight (University of Glasgow)

Serial Powering

Serial powering is the baseline option for the ITk pixel system:

- To save material (fewer cables)
- Being tested with shunt-regulators (Shunt-LDO) in FE-I4 modules (to operate with constant current)
- Protection chip under development to avoid losing entire chains. It will be placed on the module flexes to switch individual modules on and off

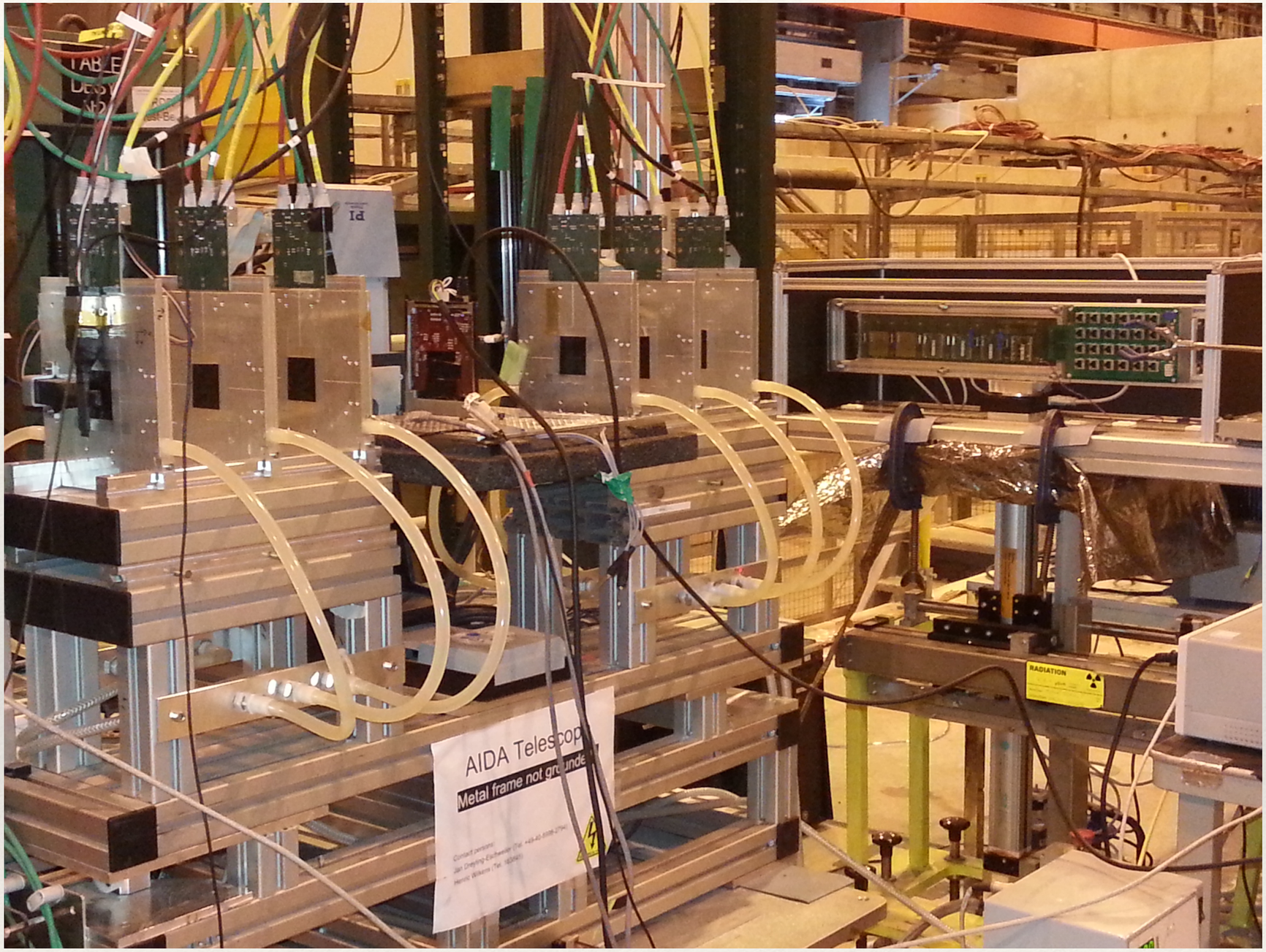
The Uk ATLAS-Pixel collaboration has its first full-size prototype of the bus tape to carry 6 serially-powered quad modules. The tape is a double-sided PCB with 25mm wide active part so it is a relatively low-mass design.
Carbon fibre, double sided stave under development

Many thanks to Ilya Tsurin (University of Liverpool)

Serial Powering. System test

A first test beam was done with a serial powered "mini-stave" a few weeks ago

- SPS H6B area (120 GeV π-)
- 4 quads modules
- Water cooling
- HSIO2-cosmic was the DAQ system
- Data taking successful with 2 modules in normal incidence
- Data taking successful with 1 module in edge incidence
- Calibration and external trigger



ATLAS-UK-PIXEL collaboration

Some other activities not covered in this talk

- Different flex prototypes being developed and tested
- Single-chip boards under development
- Data transmission and power cables under study. Material budget and shielding
- Power supplies
- Grounding and shielding studies ongoing
- Lab DAQs being upgraded to adapt to the new ASIC (RCE, USBpix)
- Jig design and development in different institutes for module mounting and assembly
- …

Summary and Perspectives

The ATLAS ITk Pixel project proposes a challenging upgrade of the current ATLAS Inner Detector. Technical Design Report due at the end of this year.

- The peak luminosity: $\mathscr{L}_{\text{HL-LHC}} = \mathbf{7.5} \times \mathscr{L}_{\text{LHC}} = 7.5 \cdot 10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}$
- The average pile-up: $\langle\mu\rangle_{\text{HL-LHC}} \sim \mathbf{8} \times \langle\mu\rangle_{\text{LHC}} \sim 200$
- Integrated luminosity: $L_{\text{HL-LHC}} = \mathbf{10} \times L_{\text{LHC}} = 3000\ \text{fb}^{-1}$
- Radiation hardness: $\phi_{\text{HL-LHC}} = \mathbf{20} \times \phi_{\text{LHC}} = 2 \cdot 10^{16}\ n_{eq}/\text{cm}^2$

In this talk, module and electronics developments for the ATLAS ITk pixel detector have been presented:

- A new Readout ASIC is under development
- Multiple sensor technologies are under qualification together with interconnection techniques
- Efforts are being made to reduce the cost: novel interconnection techniques, optimisation studies on the sensor technologies depending on the radii and assembly process

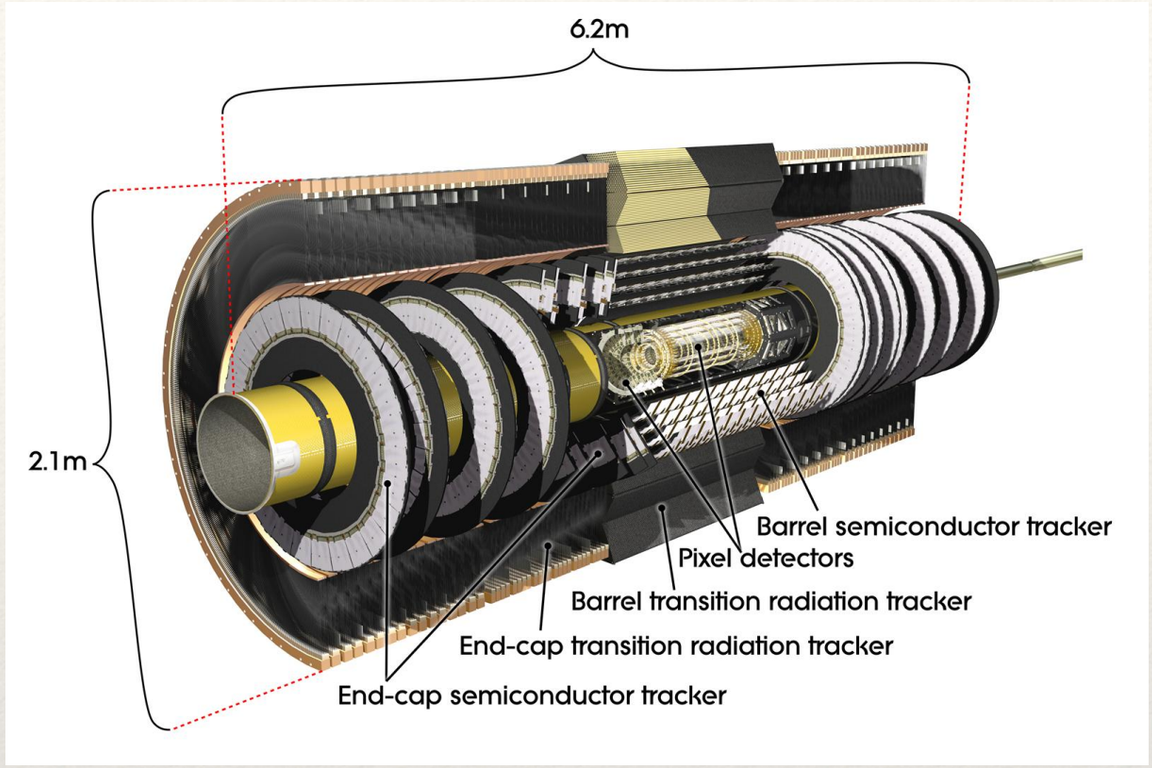
Thank you for your attention!

Dziękuję bardzo za uwagę!

HL-LHC. ATLAS Inner detector upgrade

Current ATLAS-ID

- IBL- Pixel layer (from 2015)
- Three Si-pixel layers
- Four Si-strips layers
- Straw trackers



ATLAS-ITk

- All silicon
- Five pixel layers
- Four strips layers
- Higher pixel granularity

PCB Specifications

Manufacturer: ZOT Engineering Ltd (experience, good value)
Base Material: DuPont AP8545R 100um 18/18
Bottom coverlay: DuPont LF0220 50/50
(materials available off the shelf for the 5WD service)

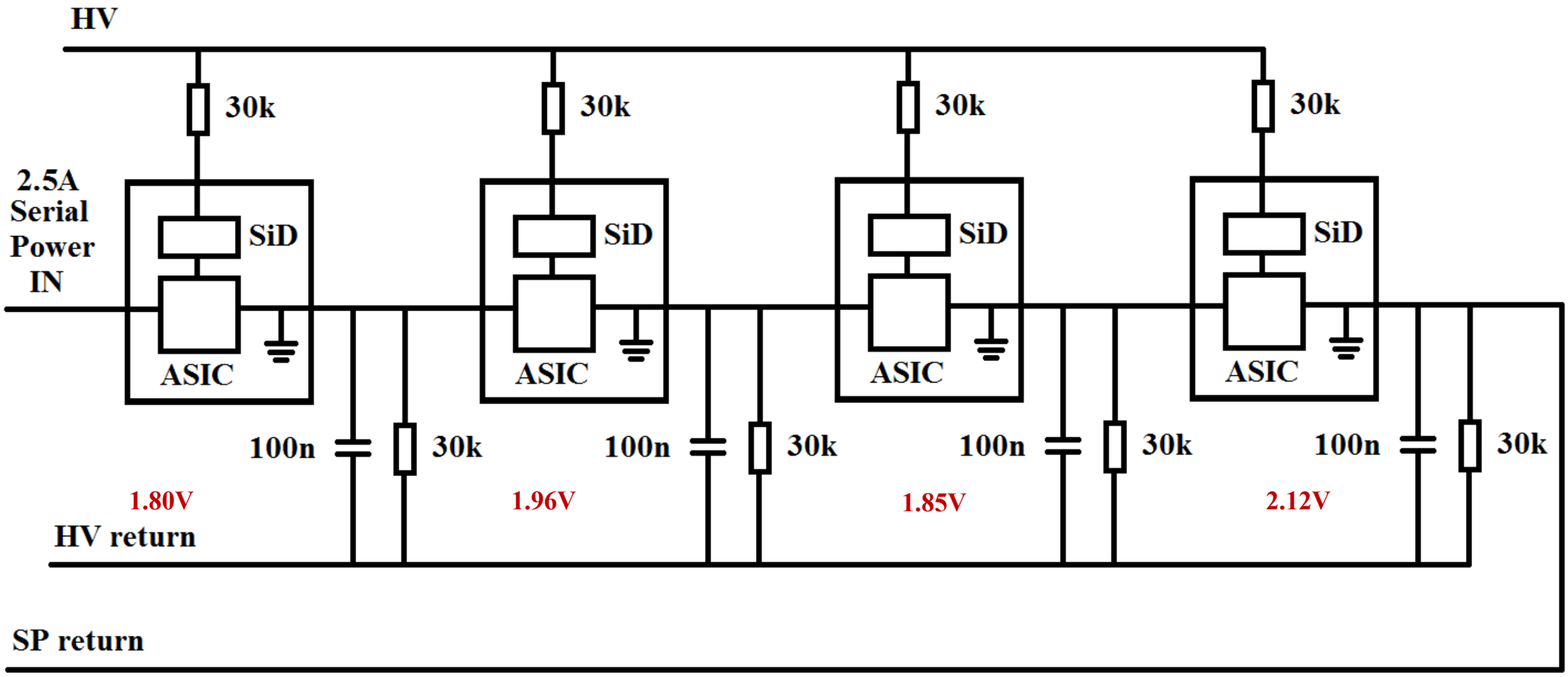
Support (for now):

Aluminium block with water cooling channel and vacuum hold down nozzles for Quad Pixel Modules

PCB glued using paper laminate method, same as for the Quad Module assembly.

HV distribution on Mini-stave

The chain has to be overpowered in order to compensate for individual voltage drop across each module



Mean Threshold and mean ToT are similar to stand-alone module calibration results