Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid-Argon Calorimeters

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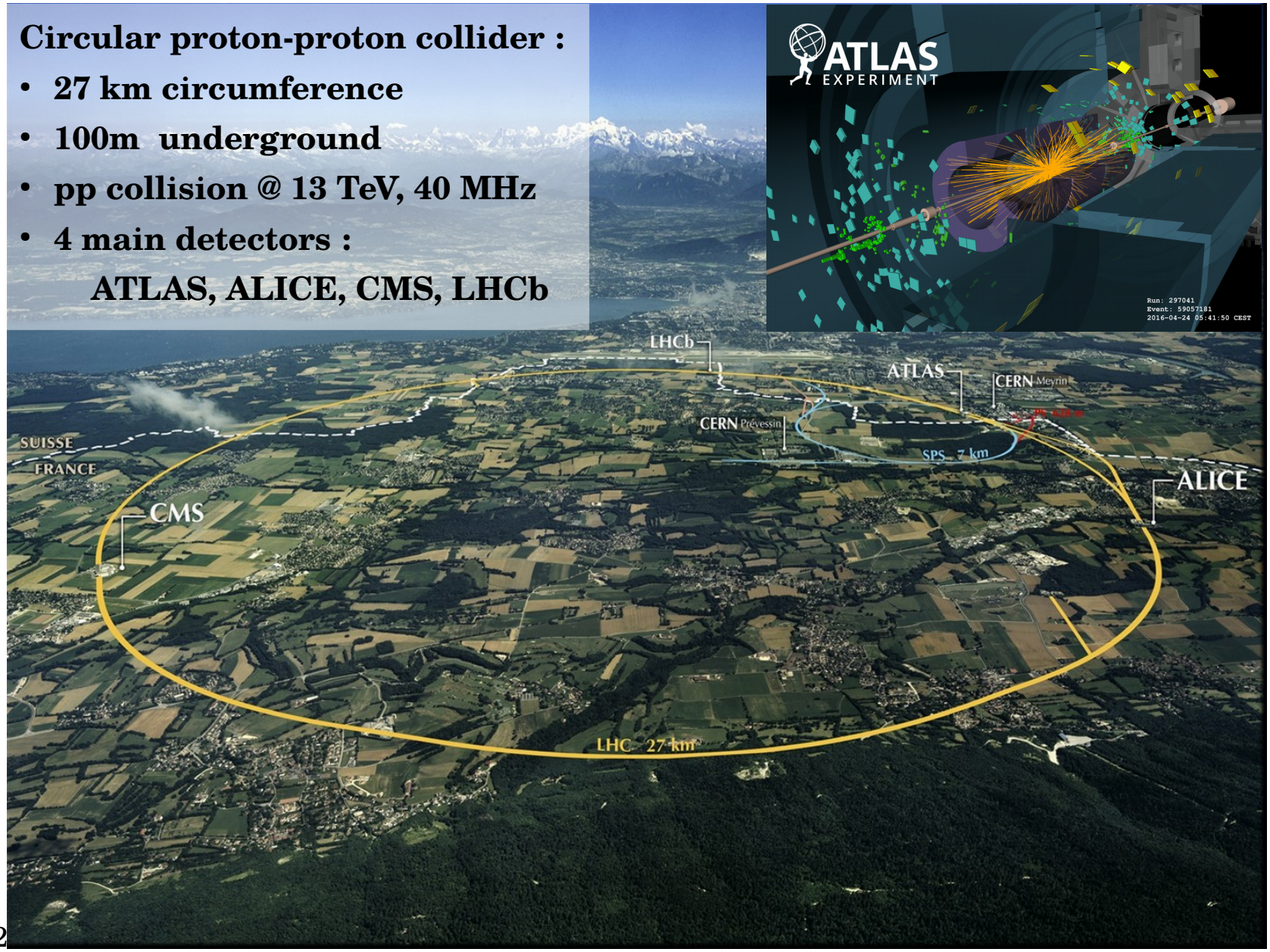
Outline

- **Introduction**
  - Large Hadron Collider
  - ATLAS detector
  - Liquid Argon Calorimeter (LAr)
  - Phase-I upgrade
- **LAr Front End electronics upgrade**
- **LAr Back End electronics upgrade**
- **Demonstrator**

Large Hadron Collider

Circular proton-proton collider :

- **27 km circumference**
- **100m underground**
- **pp collision @ 13 TeV, 40 MHz**
- **4 main detectors :**
  ATLAS, ALICE, CMS, LHCb

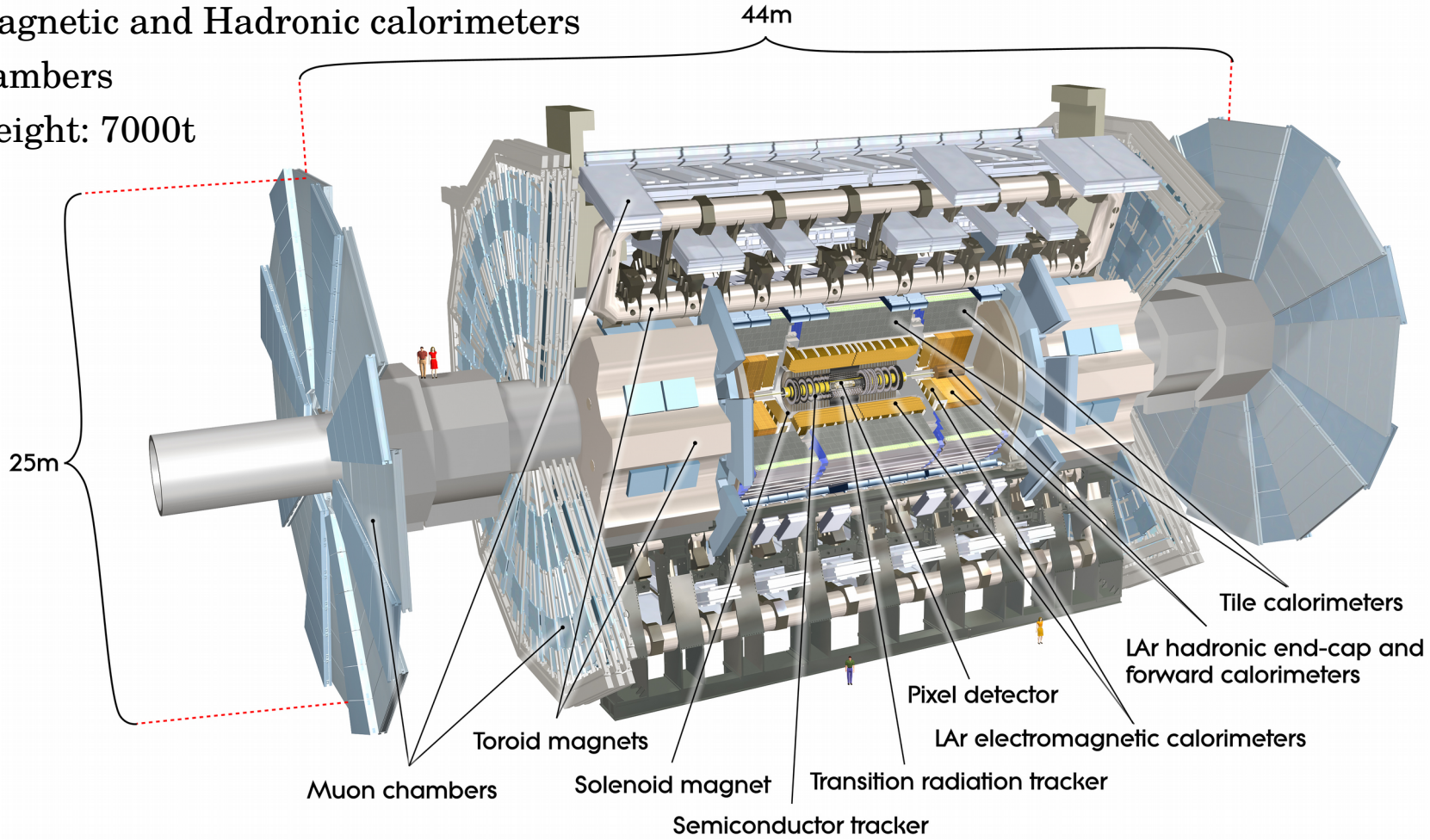


ATLAS detector

Multi-purpose detector with Forward-backward symmetric **cylindrical** geometry

- Designed to study elementary particles and their interactions
- Tracking system
- Solenoid and Toroidal Magnet
- Electromagnetic and Hadronic calorimeters
- Muon chambers

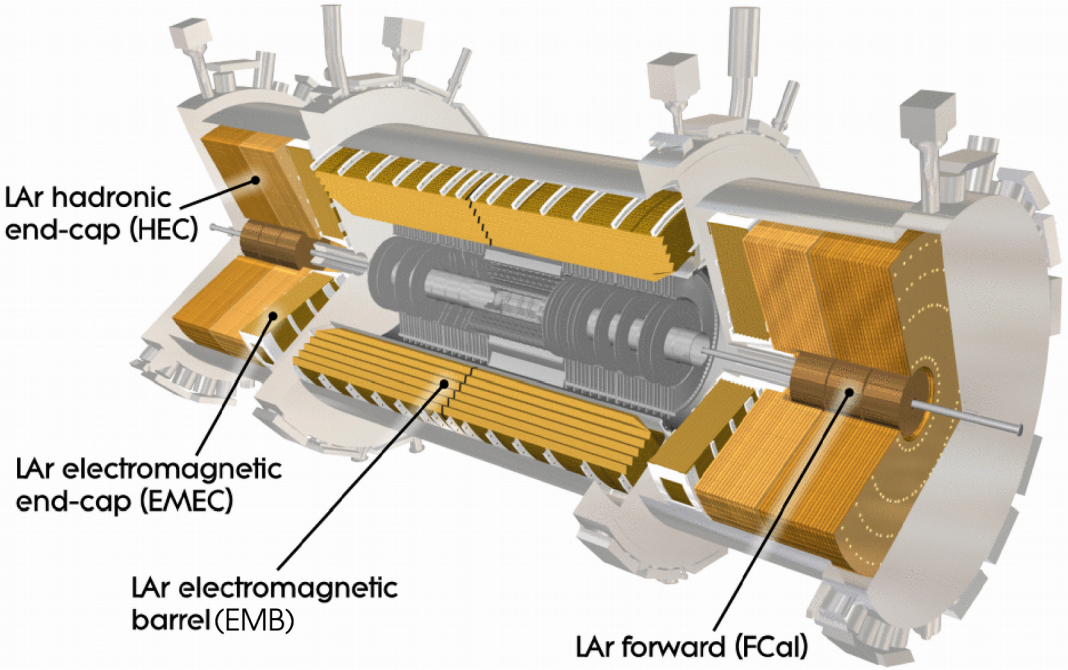
  overall weight: 7000t



ATLAS Liquid Argon calorimeter

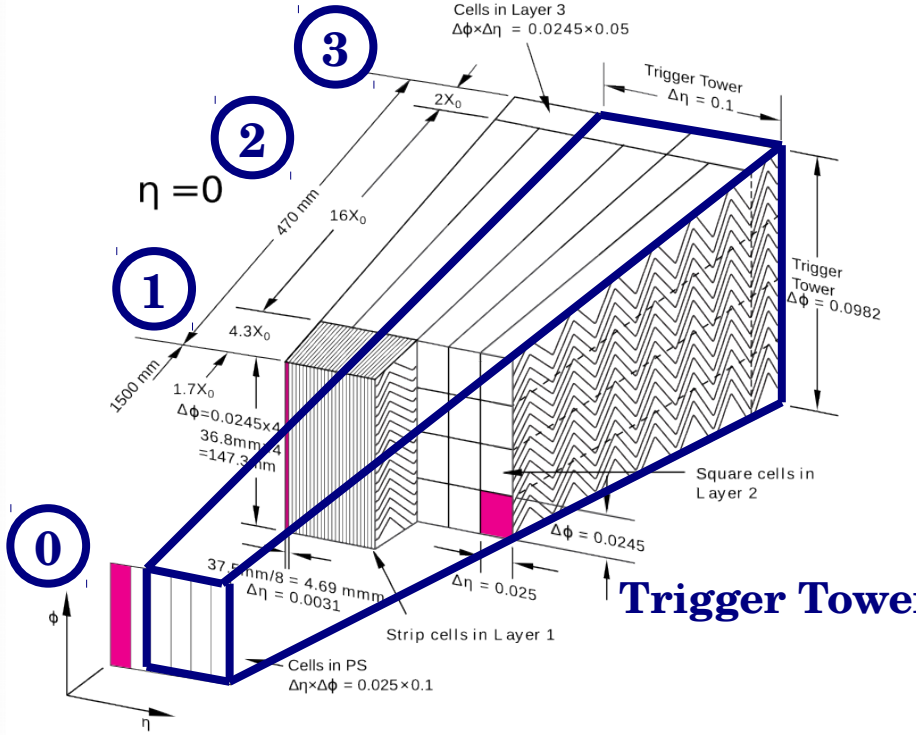
Main goal : measure **energy** and **position** of **electrons** and **photons**

- Lead / Liquid Argon sampling with accordion geometry
- Copper /Kapton electrodes
- Total of 180k calorimeter cells (4 different layers)
- 3k Trigger Towers : group of cells in (η,Φ) of size 0.1 x 0.1
- Barrel: 6x4 m, 114t ; End-Cap: radius 3m, 27t



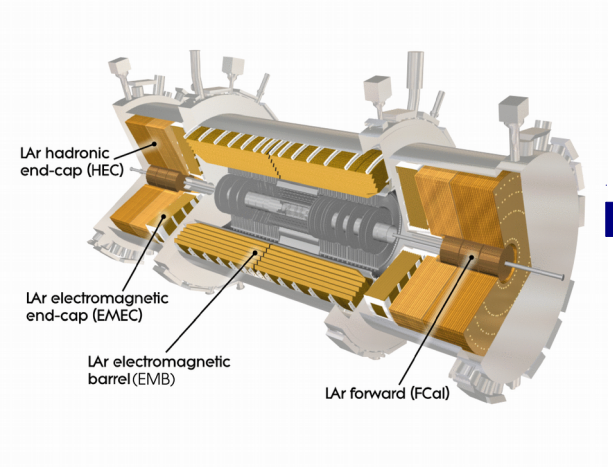
LAr = **L**iquid **Ar**gon

LAr Calorimeter Cells

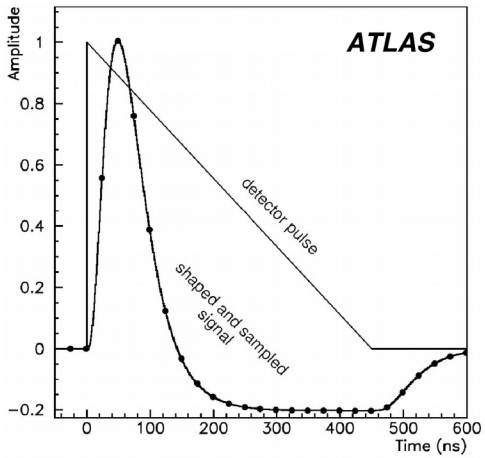


LAr measurement in a nutshell

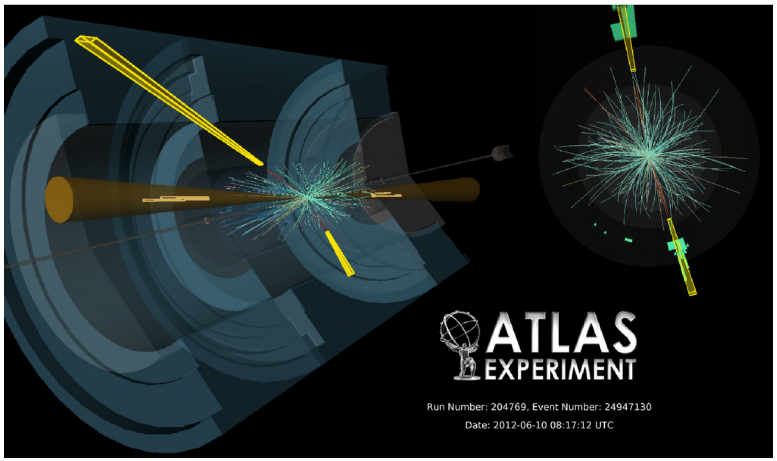
LAr calorimeter



LAr ionisation pulse



Event reconstruction



Higgs Boson Discovery

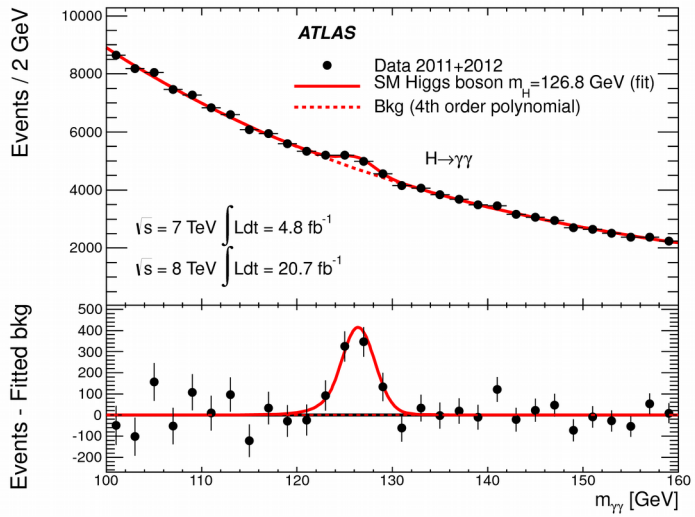
The Nobel Prize in Physics 2013

Photo: A. Mahmoud
François Englert
Prize share: 1/2

Photo: A. Mahmoud
Peter W. Higgs
Prize share: 1/2

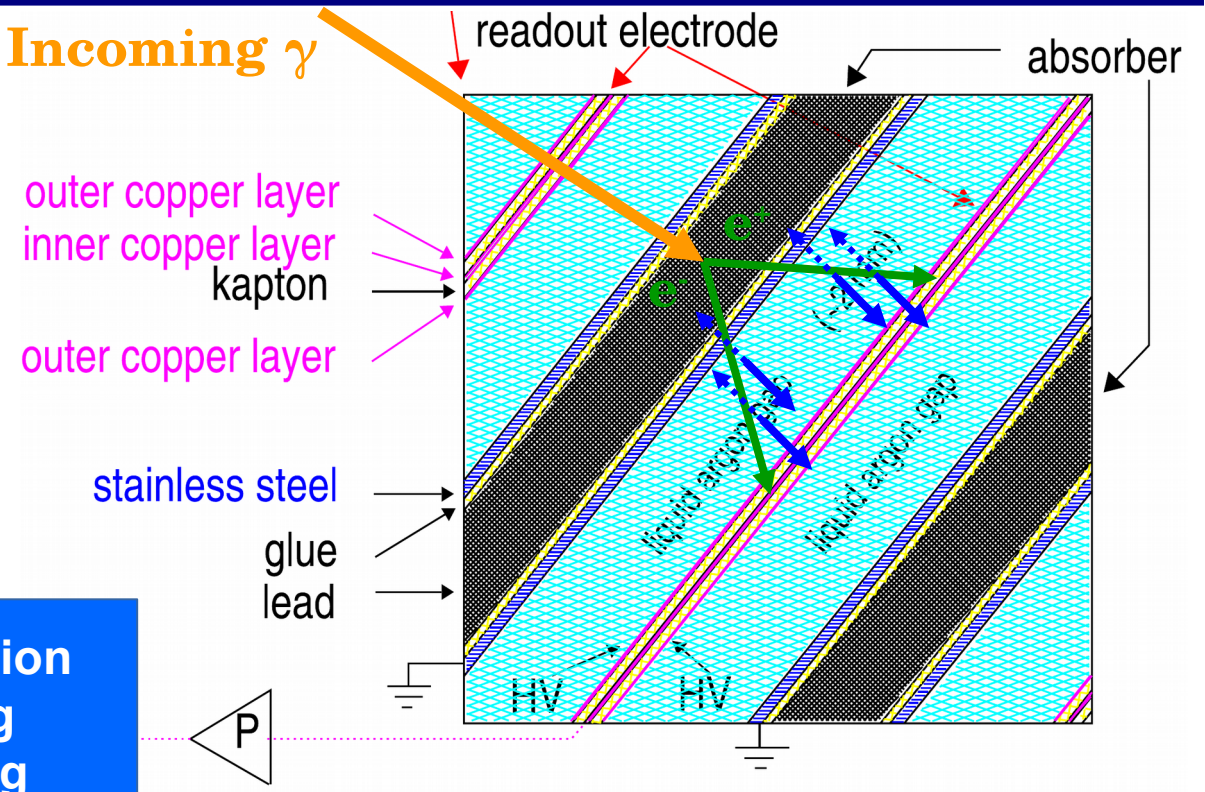
The Nobel Prize in Physics 2013 was awarded jointly to François Englert and Peter W. Higgs *"for the theoretical discovery of a mechanism that contributes to our understanding of the origin of mass of subatomic particles, and which recently was confirmed through the discovery of the predicted fundamental particle, by the ATLAS and CMS experiments at CERN's Large Hadron Collider"*

Data analysis

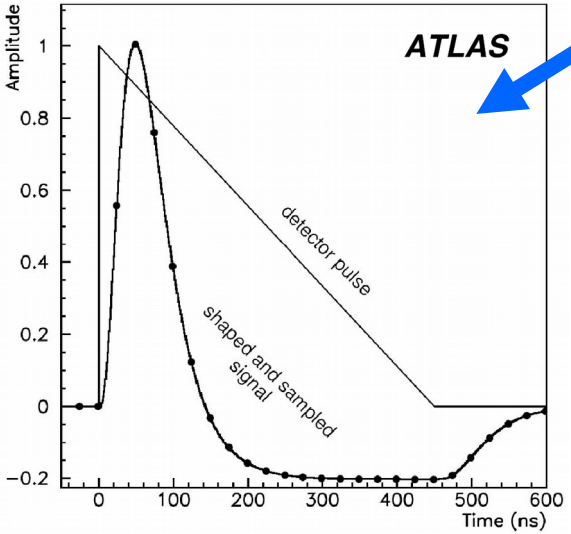


LAr ionisation pulse

- Incoming particle creates a **shower**
- Electrons in shower **ionise** liquid Argon
- Ionisation electrons create a **current**



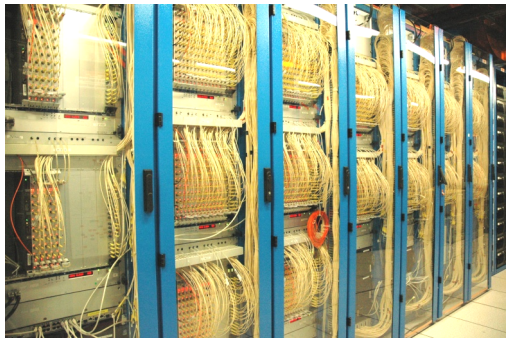
Amplification
Shaping
Sampling

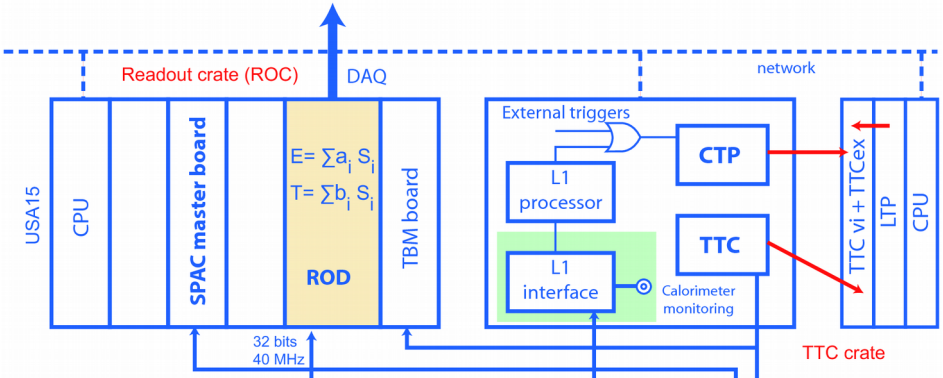


- Current is collected on electrodes and converted in Voltage
- Voltage is amplified, shaped, sampled (@40MHz) and digitized
- LAr Hardware computes the cell energy from digitized samples and send it to central DAQ

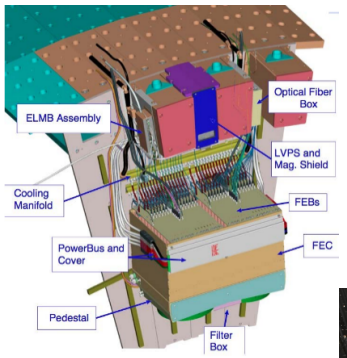
Current LAr readout electronics

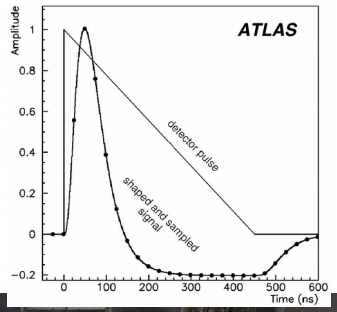
Counting Room

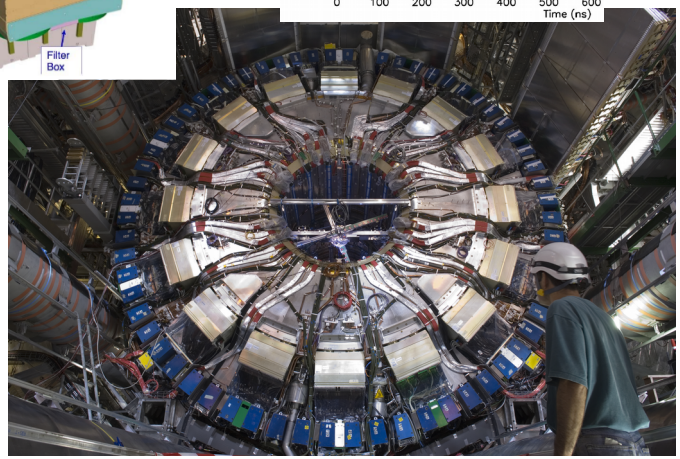


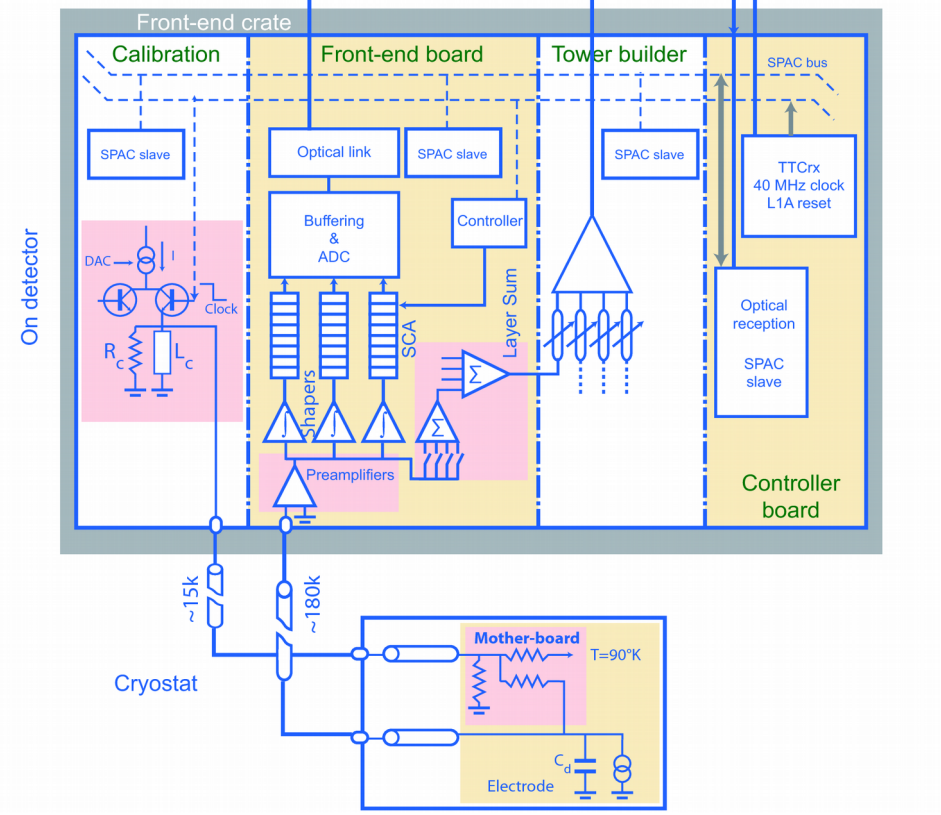


Detector Cavern (radiations)

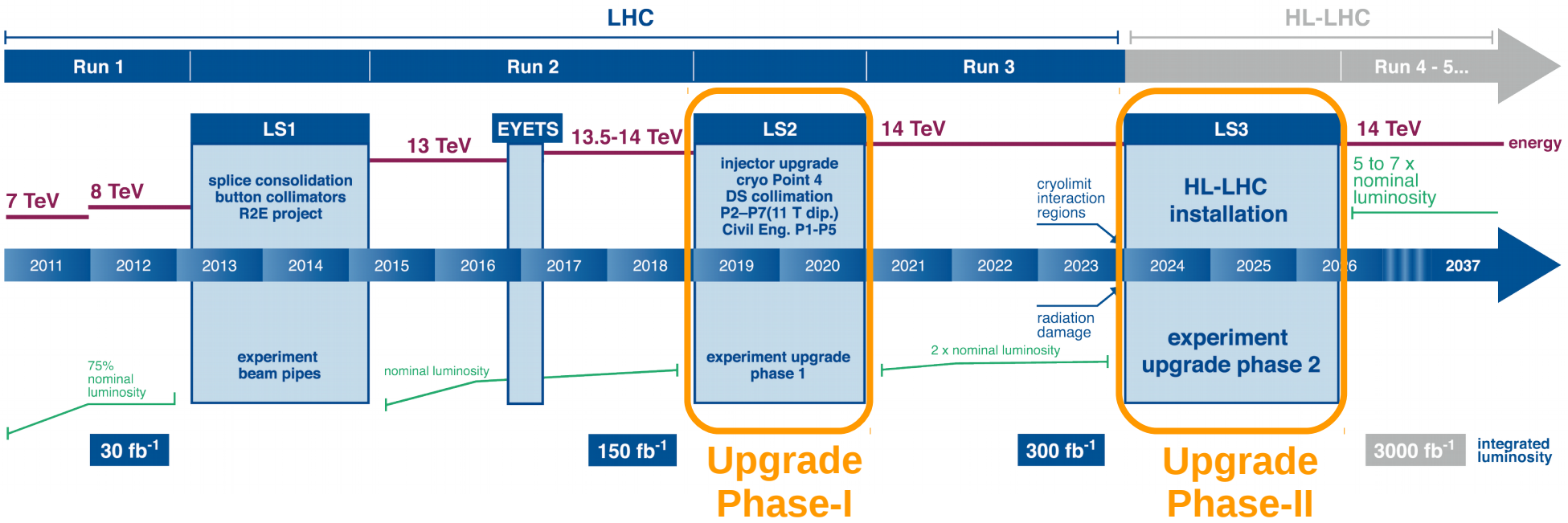








LHC / HL-LHC Plan



- **In 2016 ATLAS ran with** $\mathcal{L}_{max} = 1.3 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1},\ < \mu >= 24.2$

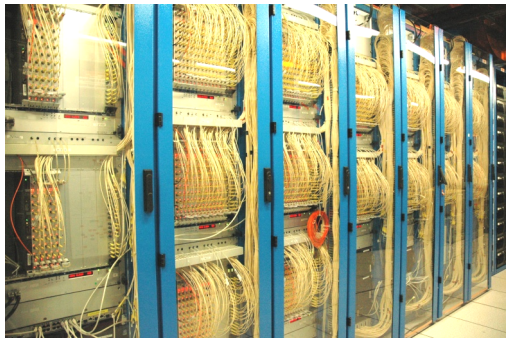
Average number of pp collision per bunch crossing

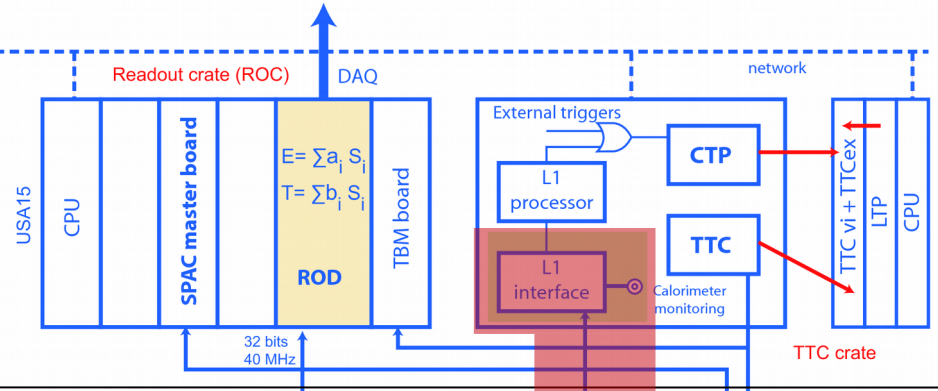
For ATLAS, upgrade planned in two phases:

- **Phase-I (2019-2020) : essentially trigger path upgrade** $\mathcal{L} \sim 3 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1},\ < \mu > \sim 80$
  - Level 1 hardware trigger maximal rate : 100 kHz
  - Single Electromagnetic trigger has to stay to 20 kHz
- **Phase-II (2024-2026) : includes main data path upgrade** $\mathcal{L} \sim 7 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1},\ < \mu > \sim 200$

Current LAr readout electronics

Counting Room





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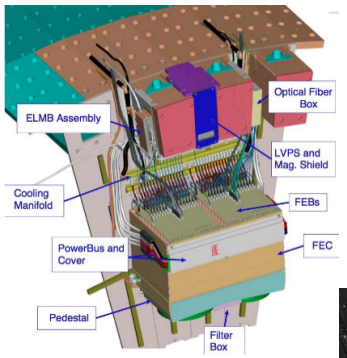
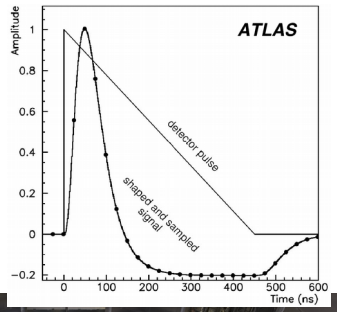
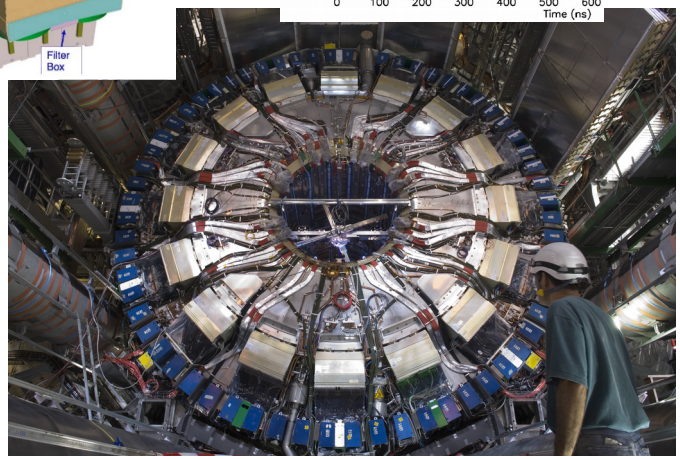
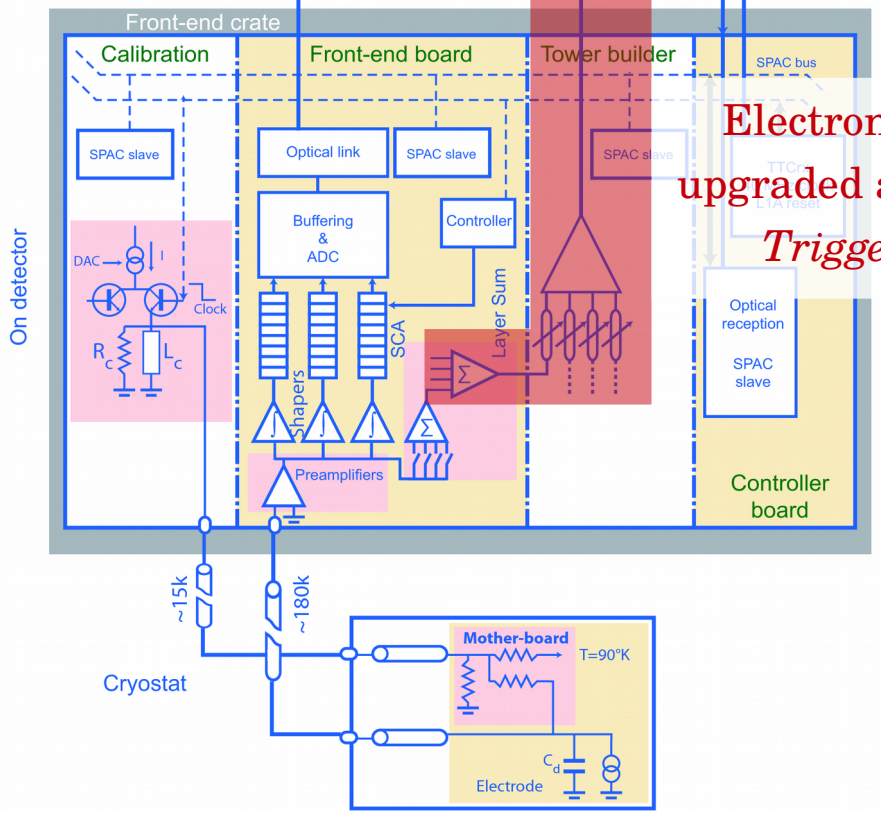




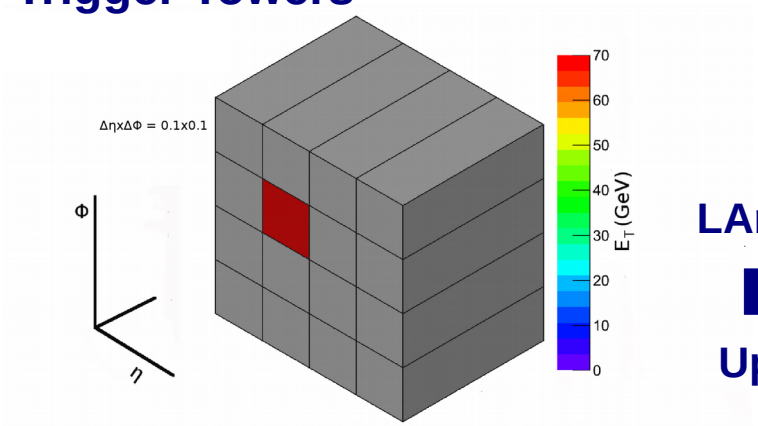




Electronics to be upgraded at Phase 1: *Trigger Path*

Higher granularity for Trigger

Trigger Towers

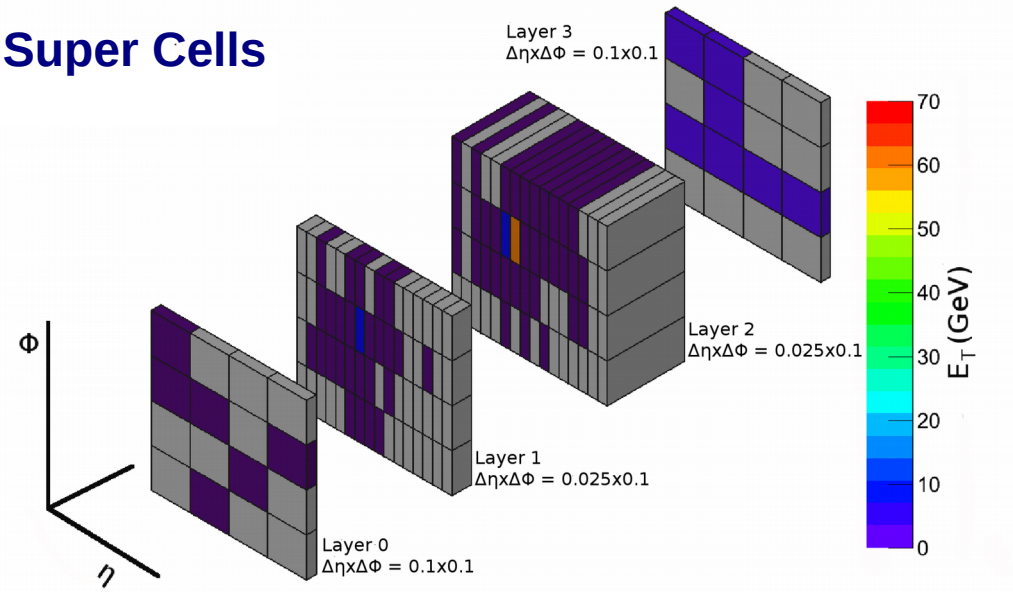


Simulation of electron with 70 GeV of transverse energy

LAr Phase 1

Upgrade

Super Cells



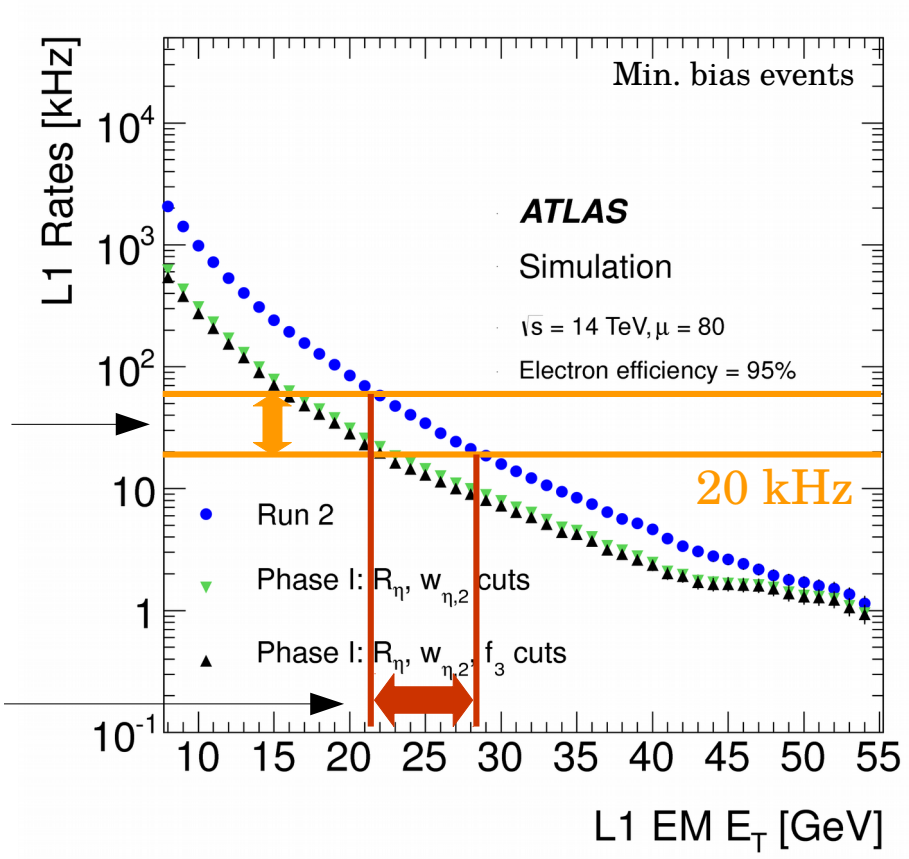
- **Current Trigger Tower too large : provide limited performance at high detector occupancy**
- **Despite luminosity increase keep low-pT thresholds and bandwidth similar to current one**
- **Improvement : Trigger Tower → Super Cells (lateral + longitudinal segmentation)**
  - 10-fold increase in granularity : Layer info + Finer segmentation in η for Layer 1 and 2
  - Higher resolution 1 GeV → 125 MeV in Layer 2, 62 MeV elsewhere
  - Shower shape info sent to L1 trigger → Apply rejection algorithms similar to offline selection

Performance Enhancement

Level 1 Trigger bandwith

$Ratio \sim 2.5$

$\Delta E_T \sim 7GeV$



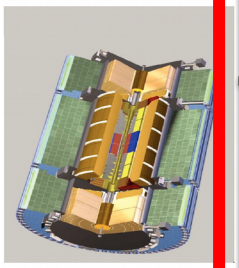
Transverse energy threshold

- Example of performance gain in trigger bandwidth for electron
- For same bandwidth as in Run2 (20 kHz) : can lower electron threshold by 7 GeV

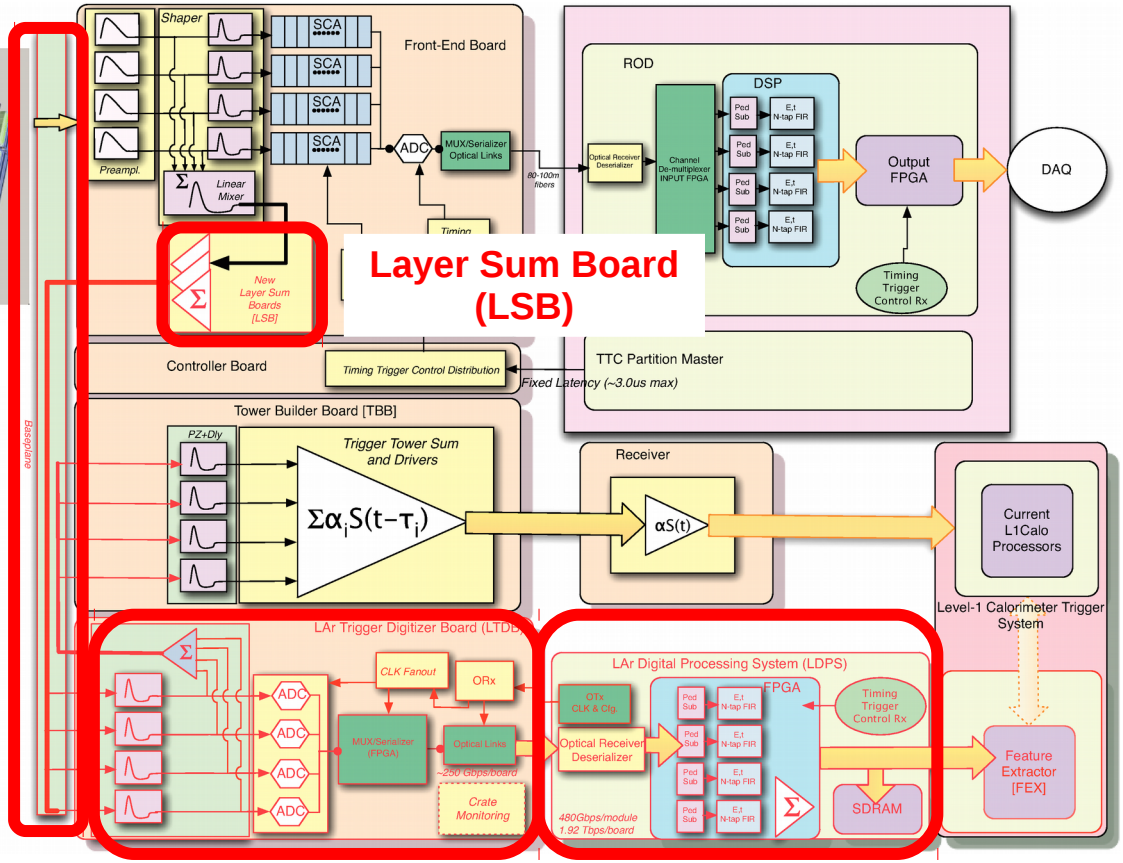
LAr Phase 1 upgrade project

New Front End (FE) electronics :

- **Layer sum board**
  - Higher granularity
- **Baseplane**
  - Increase #channels (~x10)
- **LTDB**
  - Digitize Super Cell Signals @ 40MHz
    - 12 bits precision
  - Send ADC data to Back End
  - Send old layer sum to present analog trigger system, kept as backup



Baseplane

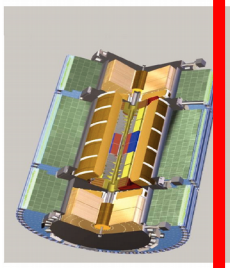


New electronic board

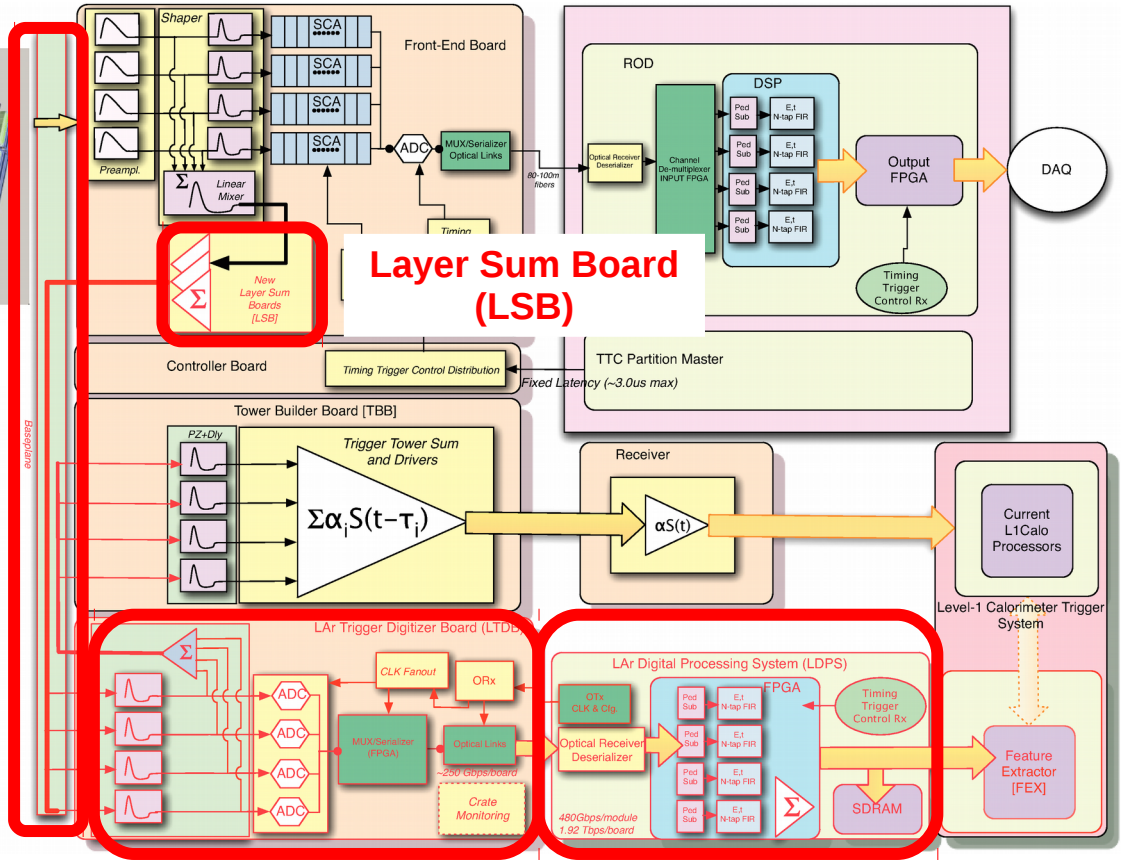
LAr Phase 1 upgrade project

New Back End (BE) electronics :

- **LDPS**
  - Read Super Cell ADC data @40MHz
  - Compute Super Cell E_T (E_T^{SC}) @40MHz
  - Send it to Phase-1 trigger system
    - Feature EXtractor (FEX)
  - Real time processing with fixed latency (1.625 µs)

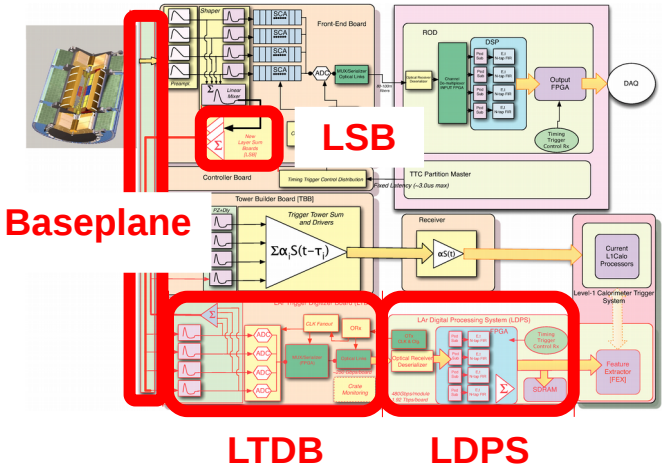


Baseplane



New electronic board

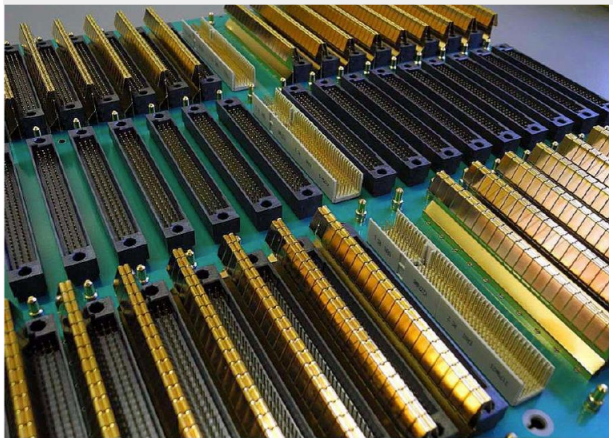
LAr Phase 1 upgrade project (2)



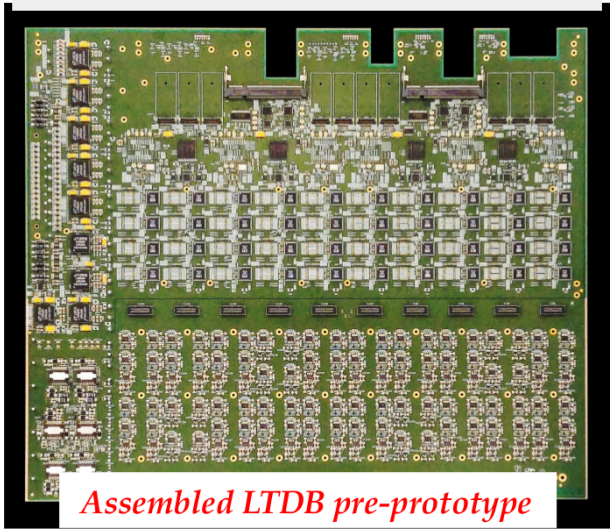
- **Goal of the chain:**
  - Convert SC signals to E_T (GeV) @ 40 MHz
  - Identify the Bunch Crossing of the signal
- **34 000 Super Cells to process**
- **~41 Tbps to Trigger system**

FEX
(new trigger system)

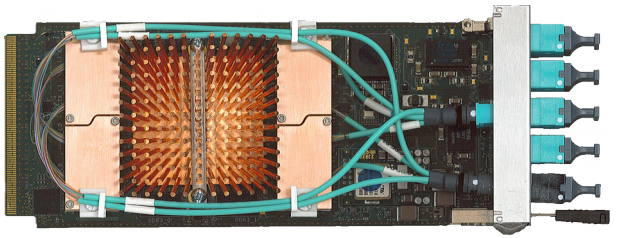
New baseplane



New Front End :
Boards with custom ASICS



New Back End :
ATCA boards



Latency Budget

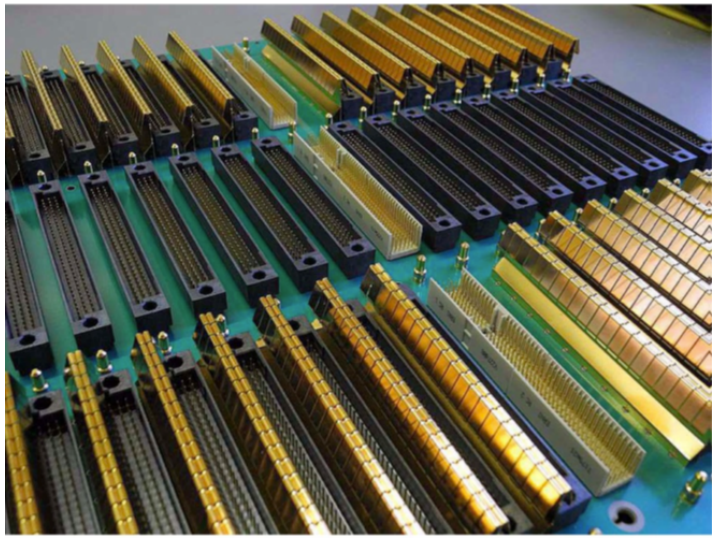
- **LAr + FEX system should have a latency below 65 Bunch Crossings (BCs) = 1.625 µs**
- **The estimated latency is 44.2 (LAr) + 14 (FEX) = 58.2 BCs**
- **LAr main latency sources : Digitization, FE → BE data transfer, E_T computation**

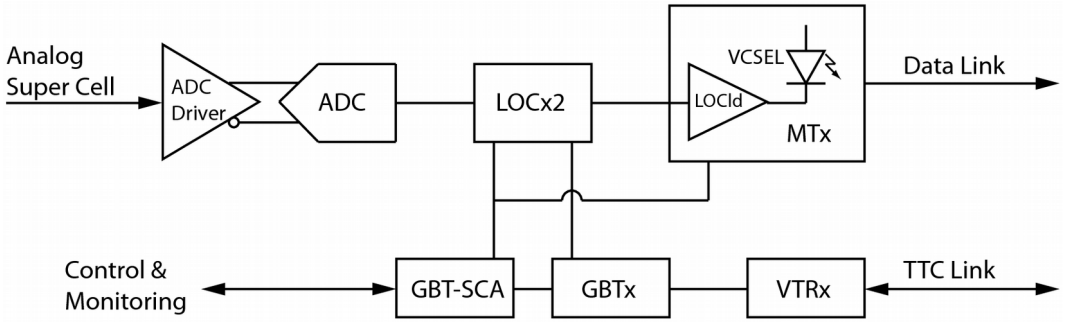
	Latency		Sub-total [BCs]	Total [BCs]
	[ns]	[BCs]		
Time-of-flight at $\eta = 2$	15	0.6		
Cable to pulse preamplifier	30	1.2		
Preamplifier and shaper	10	0.4		
			2.2	**2.2**
Digitization on LTDB	200	8.0		
Multiplexing on LTDB	25	1.0		
Serializer on LTDB	50	2.0		
Optical Cable (70 m) from LTDB to LDPS	349	14.0		
			25.0	**27.2**
Deserializer on LDPS	50	2.0		
Channel Demultiplexing on LDPS	25	1.0		
Pedestal Subtraction	25	1.0		
E_T with forward correction	125	5.0		
Digital summation	50	2.0		
Multiplexing $40-320$ MHz on LDPS	25	1.0		
Serializer on LDPS	50	2.0		
Optical cable (15 m) from LDPS to FEX	75	3.0		
			17.0	**44.2**

Front End Electronics Upgrade

New Front End Components

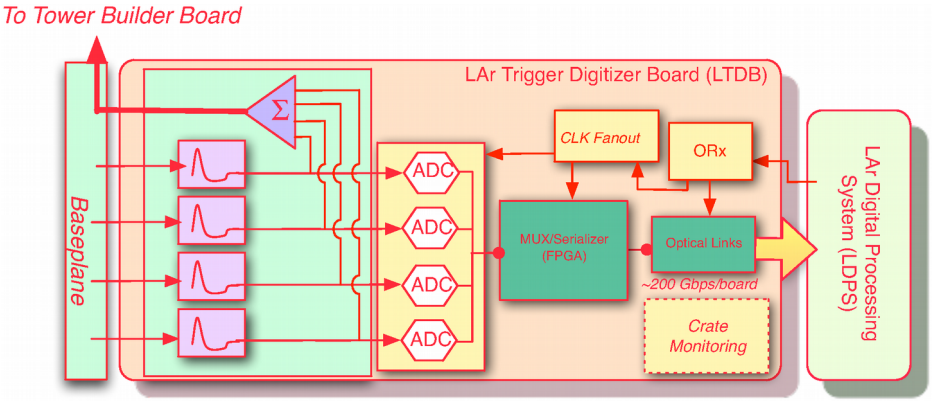
- **New Baseplane**
  - Drives new analog signals
  - Compatible with current setup
- **New Layer Sum Board**
  - Analog sum to make Super Cells
- **LTDB**
  - custom ASICs to be radiation tolerant and have low power consumption
    - ADC
    - Serializer : LOCx2
    - Transmitter : LOCld
  - Receive Trigger, Timing and Control (TTC) signals via GBT link

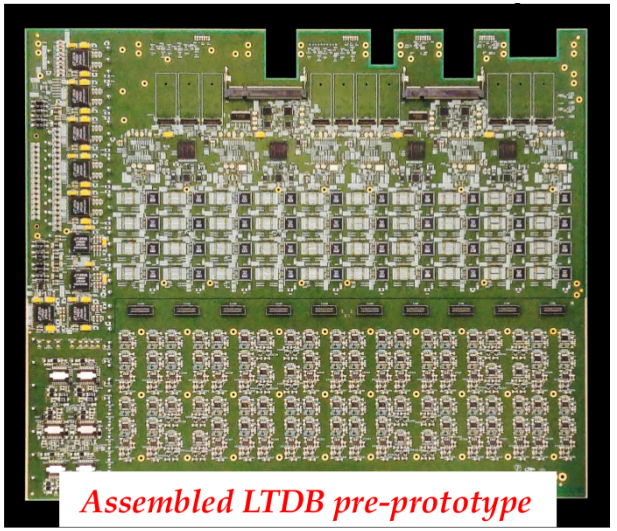


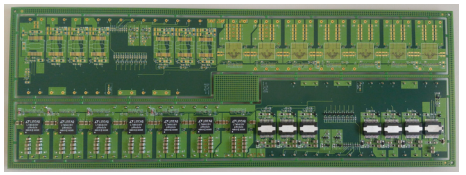


LTDB

- **124 LTDB to read 34k Super Cells (SC) analog signal**
- **Each LTDB reads up to 320 SC**
- **Digitize with 12 bits @ 40 MHz**
- **Do analog sums for present trigger (Tower Builder Board)**
- **Transmit data via optical links @ 5.12 Gbps (LOCx2+LOCld)**
- **Power provided by a Power Distribution Board** (PDB mezzanine)
  - flexibility in phase 2 upgrade
- **Pre-prototype use FPGA instead of LOCx2**
- **Prototype using almost final ASICs under tests**

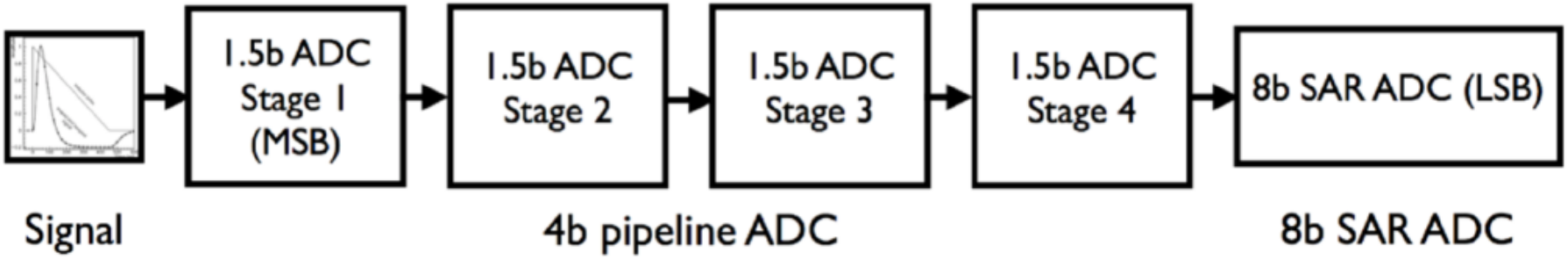




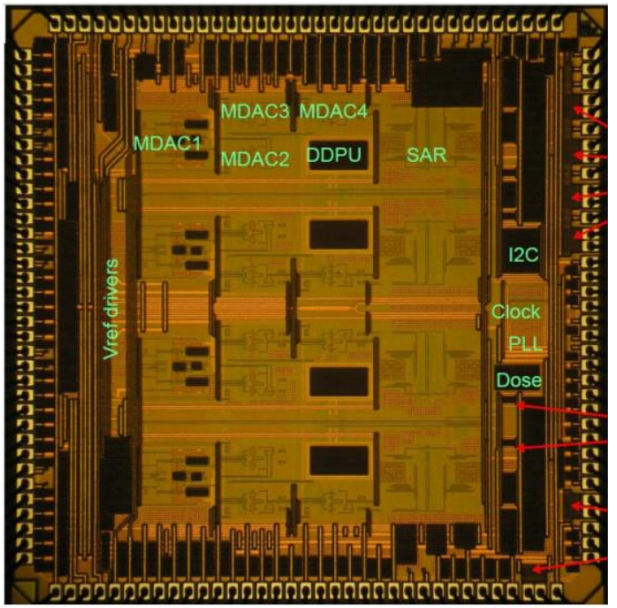


PDB

ADC custom ASIC



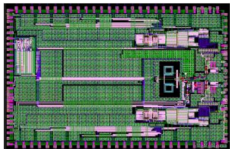
- **12 bits radiation-hard pipeline ADC**
  - TSMC 130 nm CMOS, 40 MS/s
  - ADC stages of 1.5 bits: determine the 4 most significant bits
  - 8 bits Successive Approximation Register (SAR): lower 8 bits
  - ENOB : 11
  - Die: 3.6 x 3.6 mm, 72 pins on Quad Flat No-Lead (QFN)



- **Status:**
  - 180 chips produced to validate Quality Assurance & Control procedure (QA/QC)
  - Radiation tolerance established up to 10 MRad (only 100kRad is required)

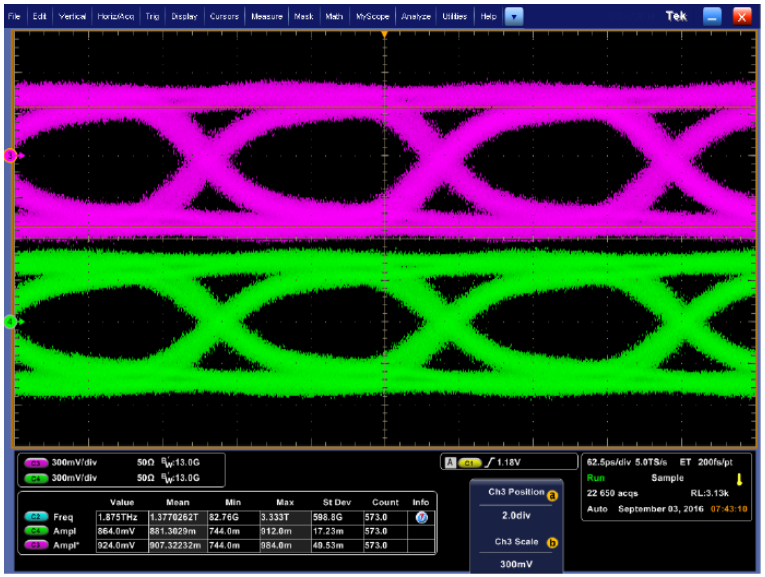
Optical Links

- **Serializer : LOCx2**

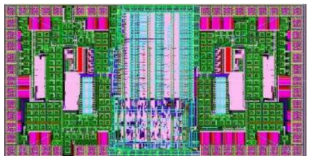


  - 250 nm Silicon-On-Sapphire
  - Dual channel 14 bits serializer
  - Output @ 5.12 Gbps
  - Power consuption : 1 W
  - Die : 6.036x3.68 mm, 100 pins QFN

LOCx2 eye-diagram after 182 kRad



- **Optical emitter : LOCld**
  - Dual channel VCSEL driver
  - Same technology as LOCx2
  - Die : 2.114x1.090mm, 40 pins QFN

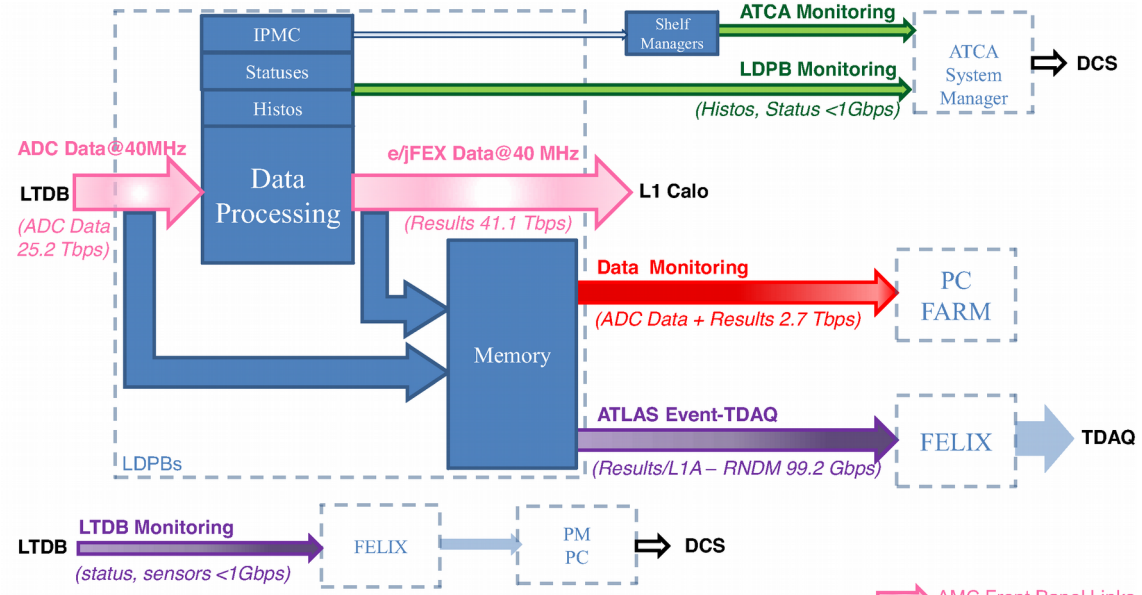


- **Chips QA should start in July**
- **ASICs are radiation tolerant**
  - No change of output eye-diagram after 200kRad of irradiation (LOCx2 & LOCld)

Back End Electronics Upgrade

Phase 1 Back End System

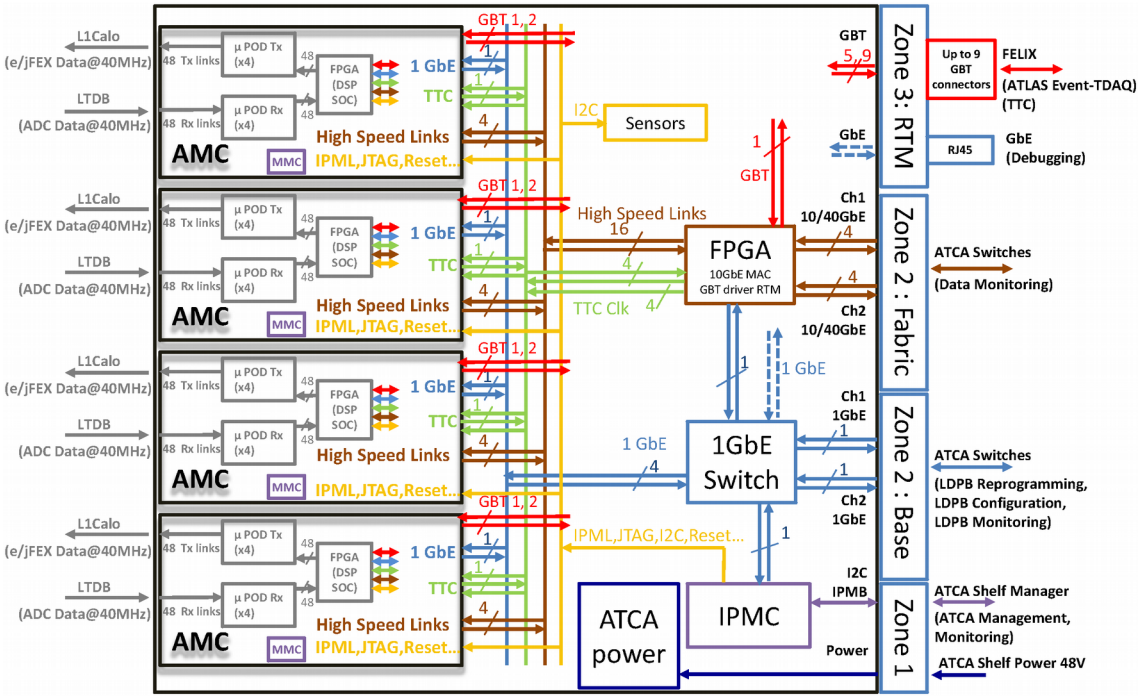
- **Input :**
  - ADC from FE (25.2 Tbps)
  - Trigger Timing and Control signals (TTC)
- **Output :**
  - Super Cells energy to Trigger (41.1 Tbps)
  - Data monitoring through 10 GbE
  - Data readout via regular ATLAS DAQ (FELIX)
- **Main Boards : LAr Digital Processing Blade (LDPB)**
  - 31 blades to read 124 LTDB



LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

LDPB

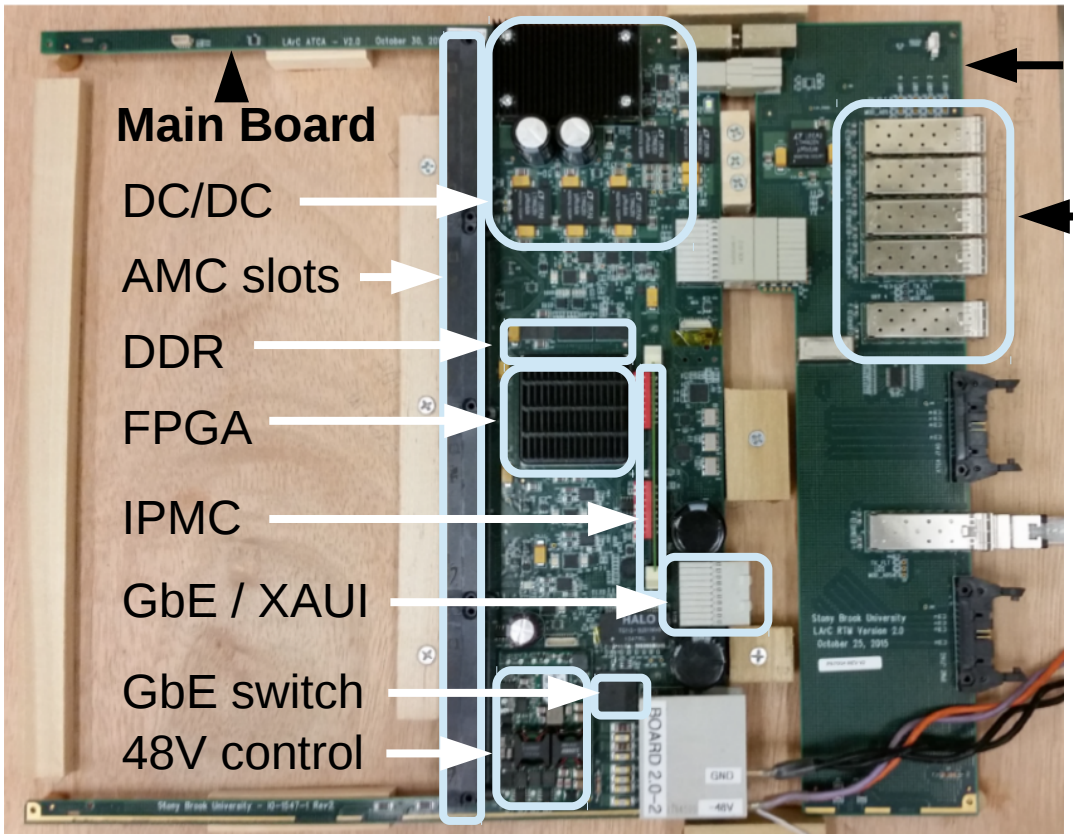


LDPB ATCA boards :

- 1 carrier: LArC
  - Drives 1/10 GbE, GBT and TTC communications
  - Power management by IPMC card
  - FPGA : Virtex7 (Xilinx)
- 4 Advanced Mezzanine Card: LATOME
  - 192 input fibres @ 5.12 Gbps
  - 192 output fibres @ 11.2 Gbps
  - Main data flow : compute E_T^{SC}
  - FPGA : Arria10 (Intel)

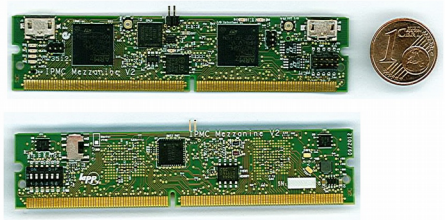
Carrier – LArC

LArC (carrier)



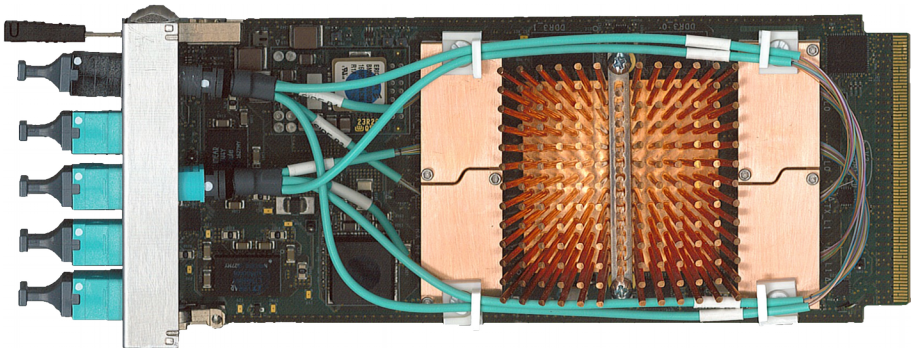
- **22 layers PCB**
- **Max power load : 400W**
- **Features validated:**
  - Power management
  - 1 and 10 GbE interfaces
  - GBT SFP input link
  - Communications w/ AMC FPGA

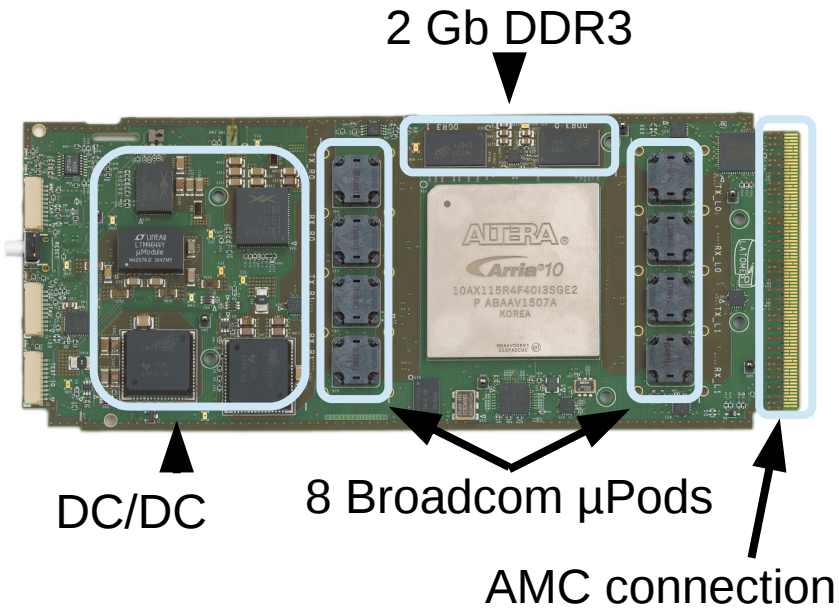
IPMC (power management)



Mezzanine – LATOME

LATOME (advanced mezzanine)

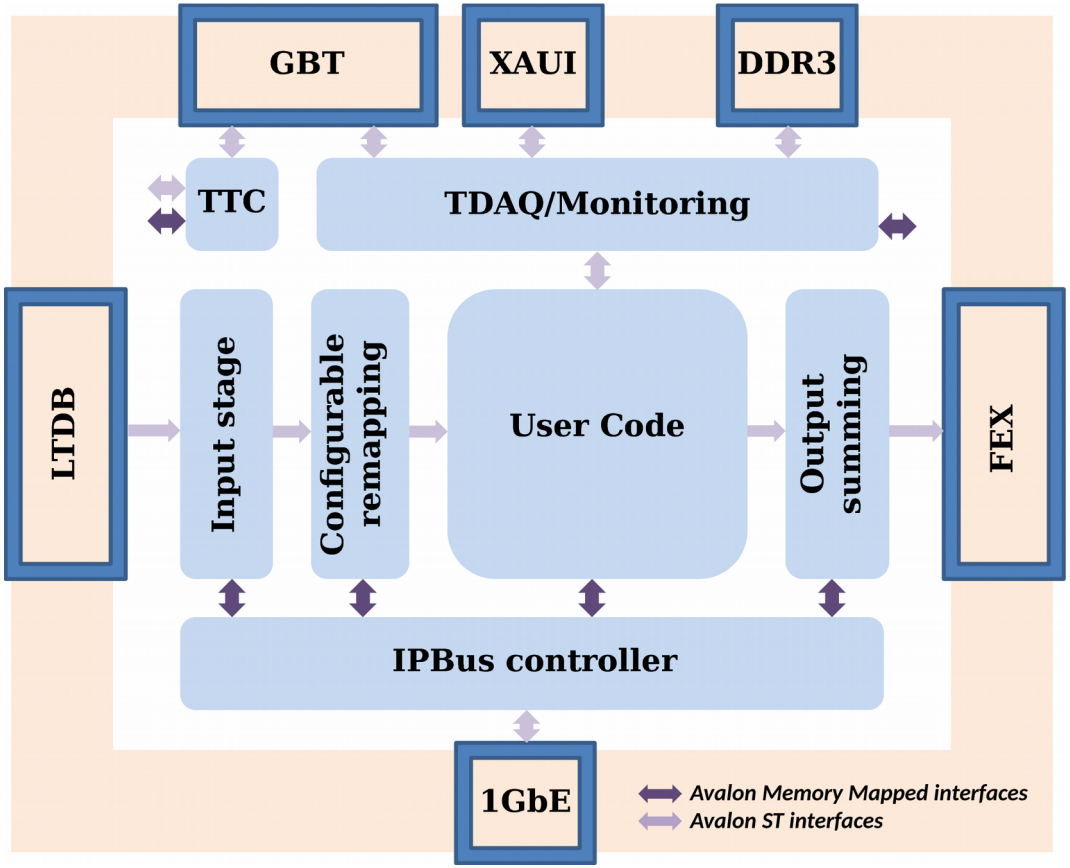




- **LATOME – LAr Trigger prOcessing Mezzanine :**
  - 16 layers PCB
  - 8 Broadcom µPods : 8 x 12 links
  - Receive LTDB data @ 5.12 Gbps (up to 48 links)
  - Compute E_T^{SC}, remap data to ease FEX algorithm, send results @ 11.2 Gbps (48 links)
  - TTC signals from carrier
- **Features validated :**
  - Optical links up to 11.2 Gbps
  - 1 GbE interface
  - GBT interface

LATOME Firmware

- **LATOME firmware divided in several functional blocks**
  - different clocks: 240, 280 and 320 MHz
- **Input stage**
  - Synchronisation of input LTDB data
- **Configurable remapping**
  - Group Super Cells as expected by FEX
- **User code :**
  - Compute E_T^{SC}
  - Bunch crossing assignment
- **TTC :** Decode TTC info
- **TDAQ/Monitoring**
  - Synchronise data with TTC info
  - Sent it via GBT/10GbE



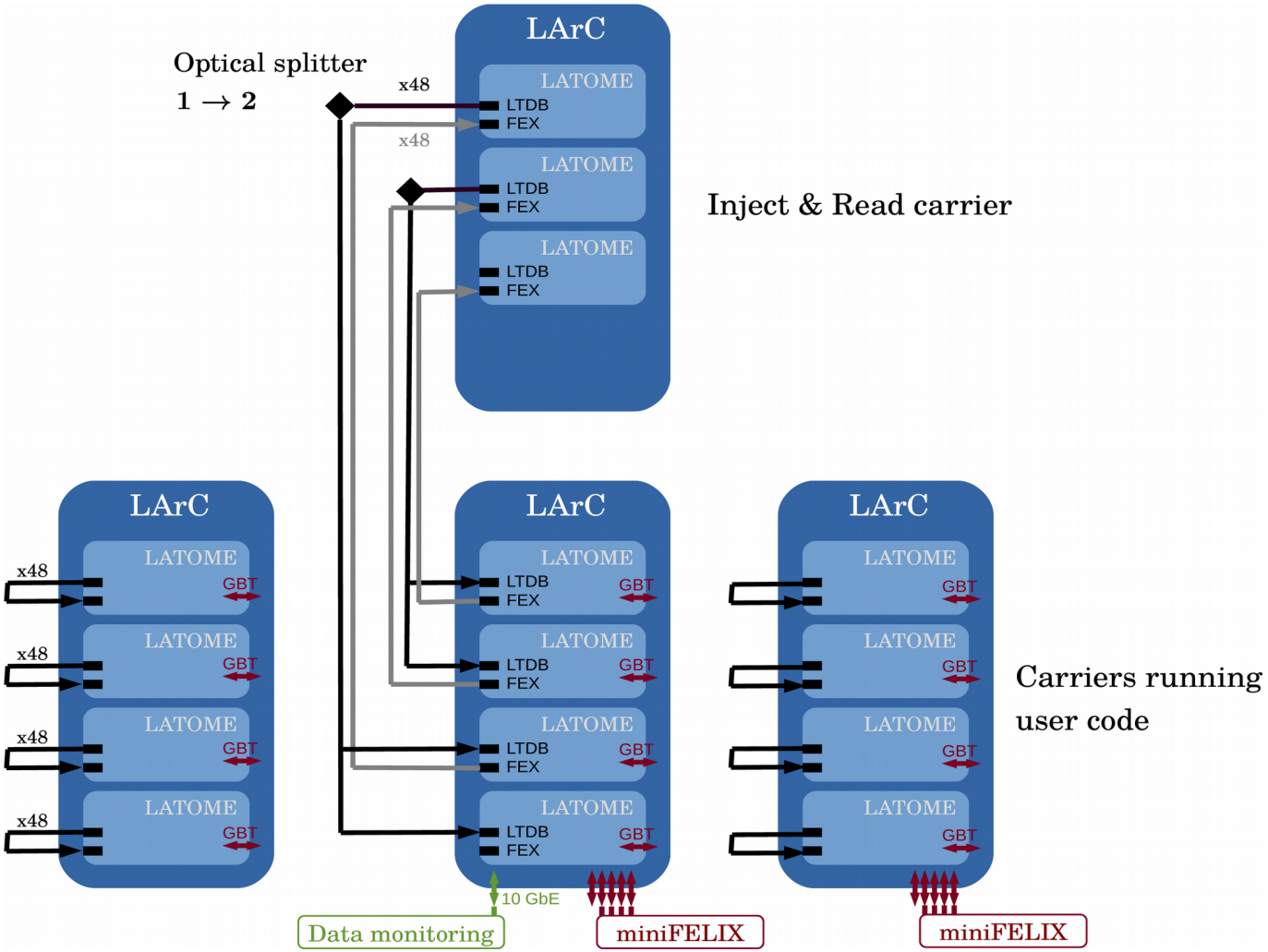
- **Output summing :** Compute sums for FEX
- **IPbus controller :** Slow control via 1GbE

Back End Integration Test

Goal : validate that system works without power & thermal issues before large scale production of the boards

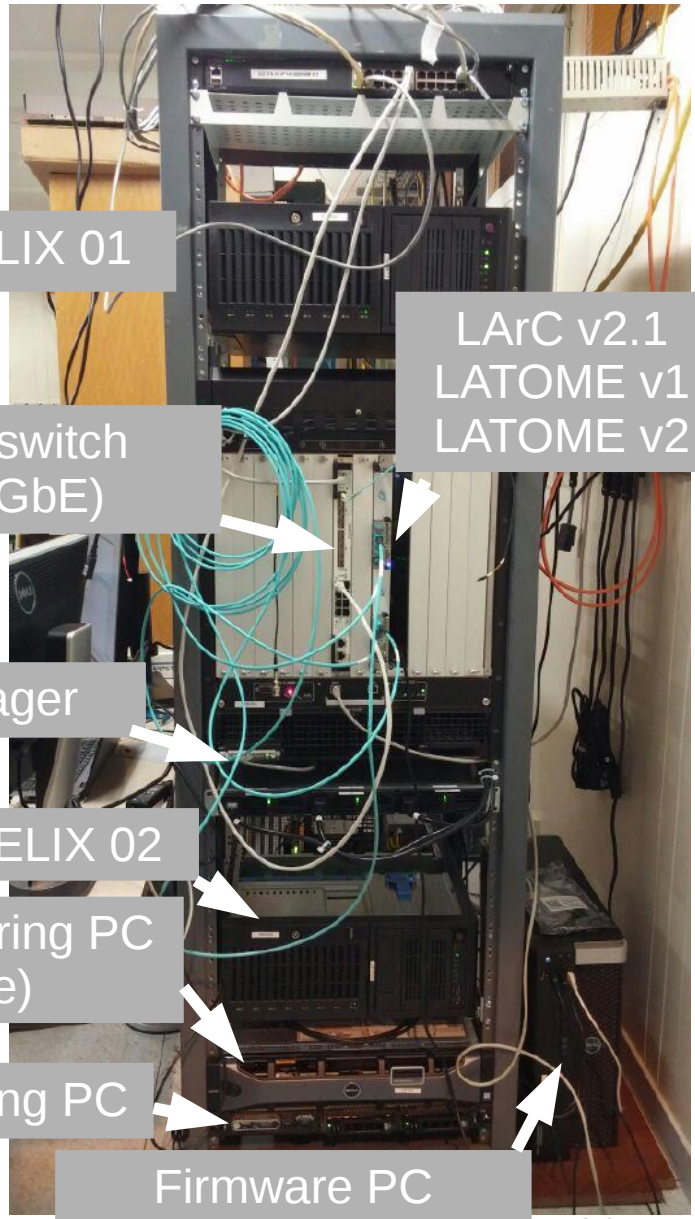
- **Planned Integration Test**
  - Connect boards to real setup @ CERN
- **1 Inject & Read carrier :**
  - Inject « LTDB » data , Read « FEX » data

    → data verification
- **3 carriers w/ user code :**
  - compute E_T for L1 (FEX)
  - Send monitoring data via GBT & 10 GbE
  - Decodes TTC signals



Integration Test Status

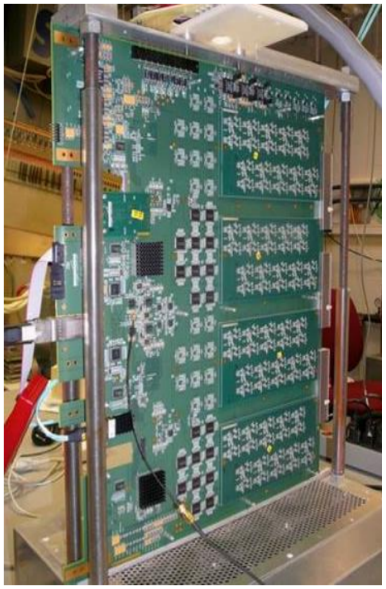
- **ATCA crate to host LDPB**
- **FELIX pc for TTC and DAQ**
- **PC with 10 GbE for data monitoring**
- **Ongoing: Main data path validation**
- **Tests will take place up to fall 2017**



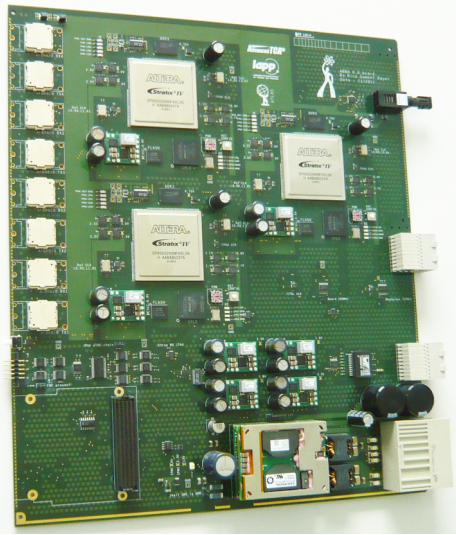
Demonstrator

Demonstrator System

- **LAr Phase 1 Upgrade proof of principle**
  - Demonstrator installed on 1/32 of barrel region (summer 2014)
  - FE : two LTDBs demonstrators
  - BE : **A**TCA test **B**oard for **B**aseline **A**cquisition (ABBA)
  - Reads super cells data to enable offline analysis

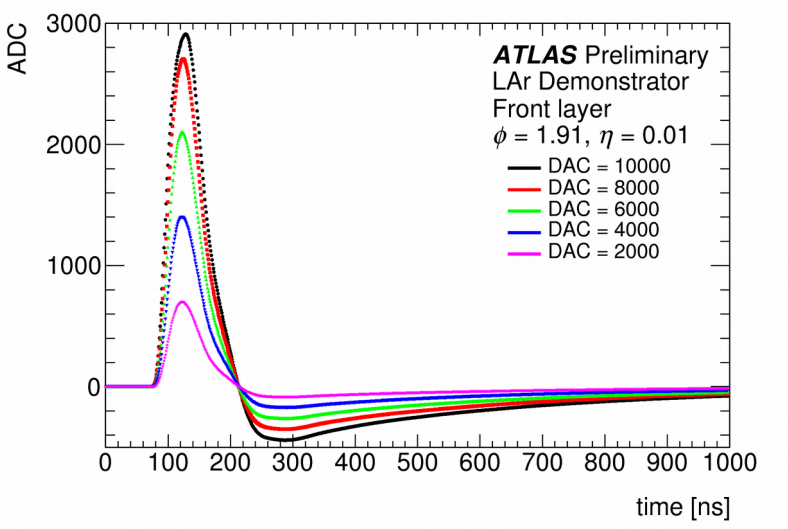


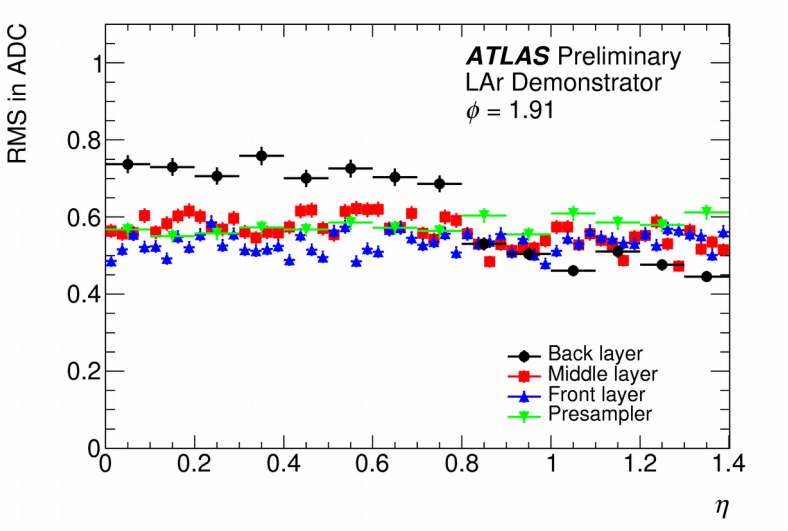
- **LTDB demontrator :**
  - Commercial 12 bits ADC (not radiation-hard)
  - Multiplexing of data output via FPGA
- **ABBA :**
  - ATCA boards with 3 FPGA
  - Data readout via IPbus protocol on 10 GbE network



Demonstrator Data

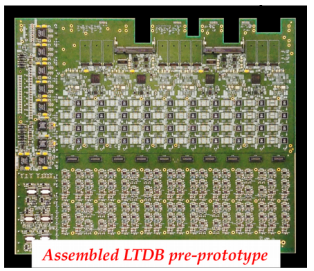
- **Calibration**
  - Inject calibration pulses with different amplitudes (DAC)
  - Size and shape of pulses are as expected
  - Good linearity
- **Collisions (pp and Heavy Ions)**
  - Collect demonstrator data when ATLAS triggers in demonstrator acceptance
  - Compare Demonstrator readout and ATLAS one
  - Noise level well below 1 ADC count : consistent with test bench measurements
- **Early 2018 : replace boards by LTDB and LDPB final prototypes**



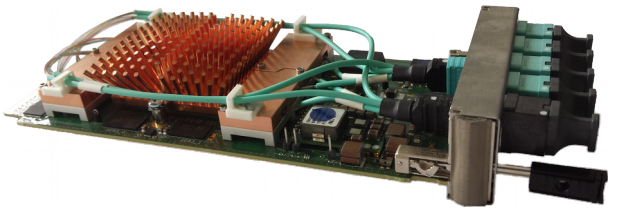


Conclusion

- **The ATLAS Liquid Argon calorimeter electronics will be upgraded during LHC Long-Shutdown 2 (2019-2020)**
- **Only the trigger path will change**
  - Increase of granularity to improve trigger performances
  - Digitization and Readout @ 40 MHz



- **The LTDB (Front End) and LPDS (Back End) systems are being developed and tested**
  - Data output total rate to trigger system : 41.1 Tbps
  - Radiation tolerant custom ASICs are produced
  - LTDB prototype is being tested
  - LDPS integration tests have started
  - **Production will start in 2018**



- **A demonstrator of the new trigger scheme is already installed and took some data with LTDB and ATCA pre-prototype →** useful experience gain

BACKUP

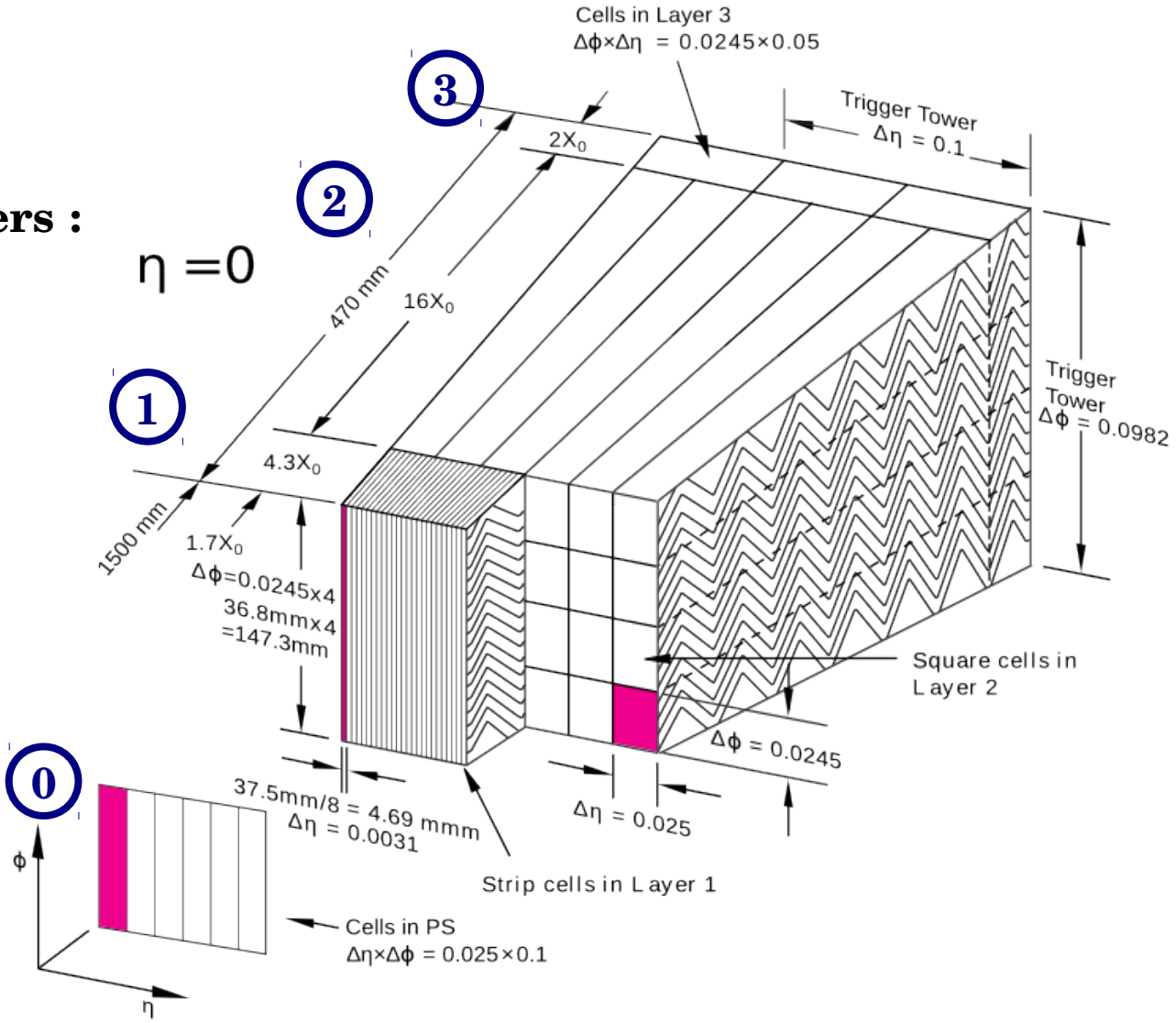
LAr calorimeter cells

LAr calorimeter made of 4 layers :

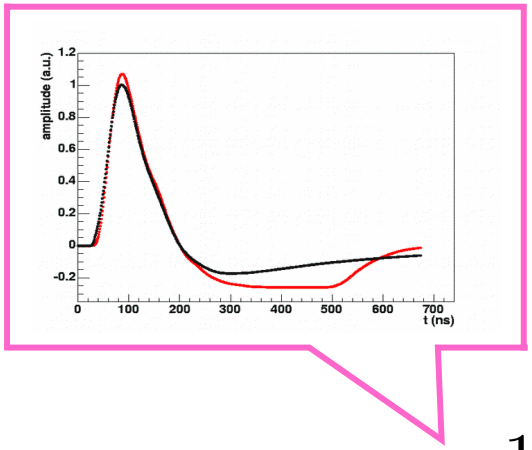
0. Energy loss correction
1. γ/π^0 separation
2. Main energy deposit
3. High energy showers

High granularity:

- Good energy resolution
- Good background rejection
- Good vertex association



Pulse → Energy



$$E_{cell} = F_{\mu A \to MeV} \times F_{DAC \to \mu A} \times \frac{1}{\frac{M_{phys}}{M_{cali}}} \times R \left[\sum_{j=1}^{N_{samples}} a_j (s_j - p) \right]$$

Cell energy

Sampling fraction

Calibration board

ADC to DAC (Ramps)

Pulse Samples

Optimal Filtering Coefficients

Pedestals

LAr Readout System

CTP

BUSY

TTC Signals

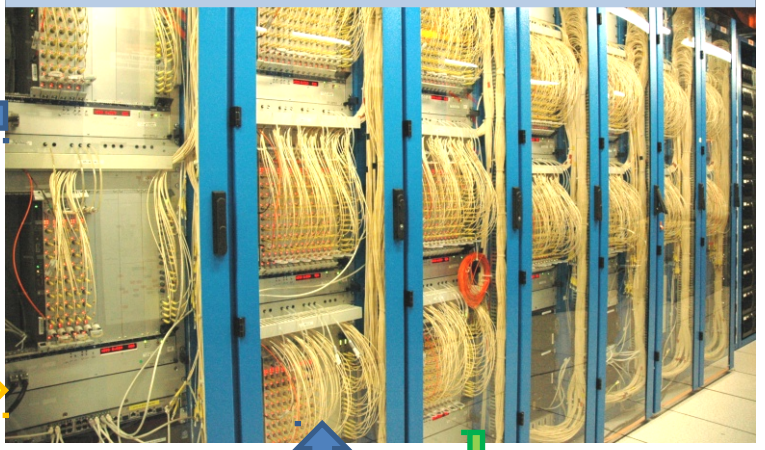
HLT

34 ROS PCs

DATA
762 Slinks

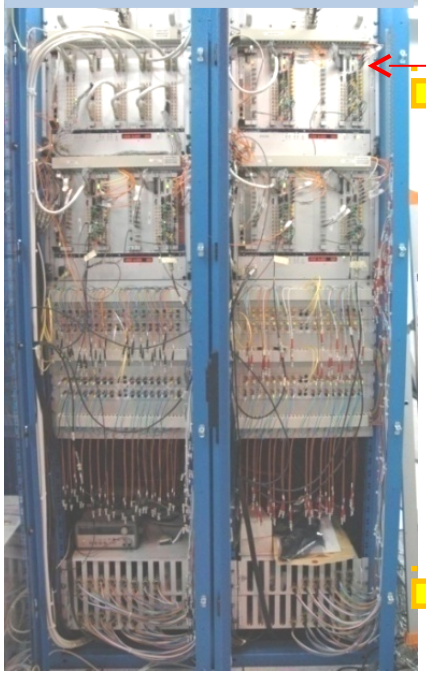
XOFF (762)

LAr BE Crates ReadOut Electronics



192 RODs in
16 ROD Crates

LAr TTC System



4 TTC Crates
6 TTC partitions

TTC Signals 16 fibres, BE Boards Configuration (TTC)

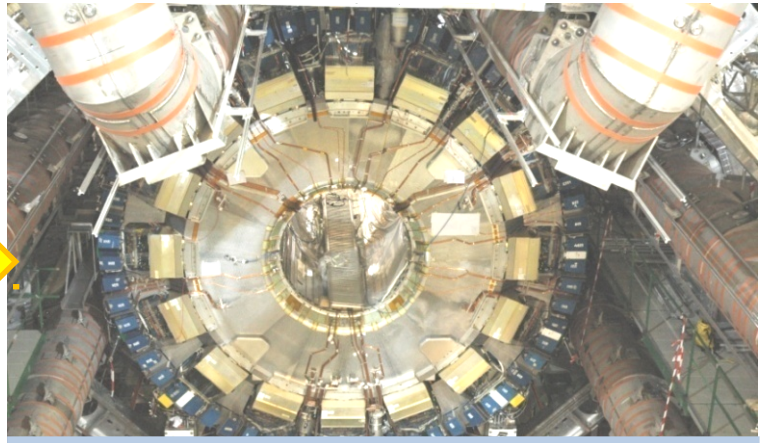
BUSY (16)

DATA
1524 Glinks

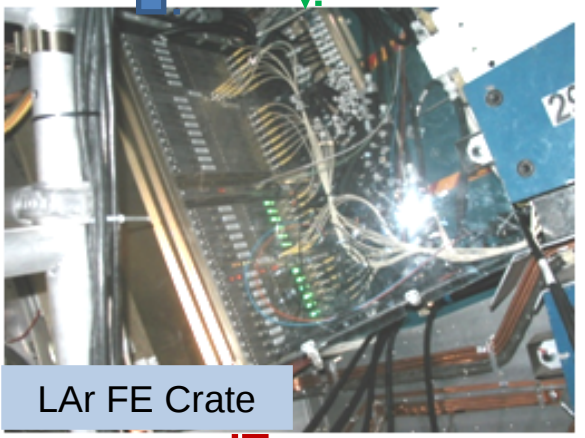
FE Boards
Configuration
(SPAC)

TTC Signals
122 fibres (*2)

FE Boards
Configuration
(TTC)



Barrel side view with FE Crates

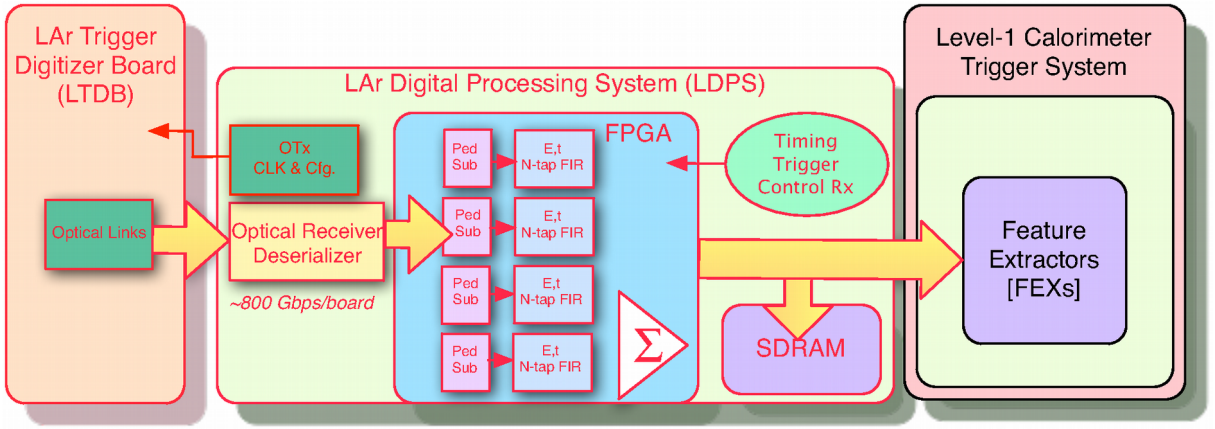


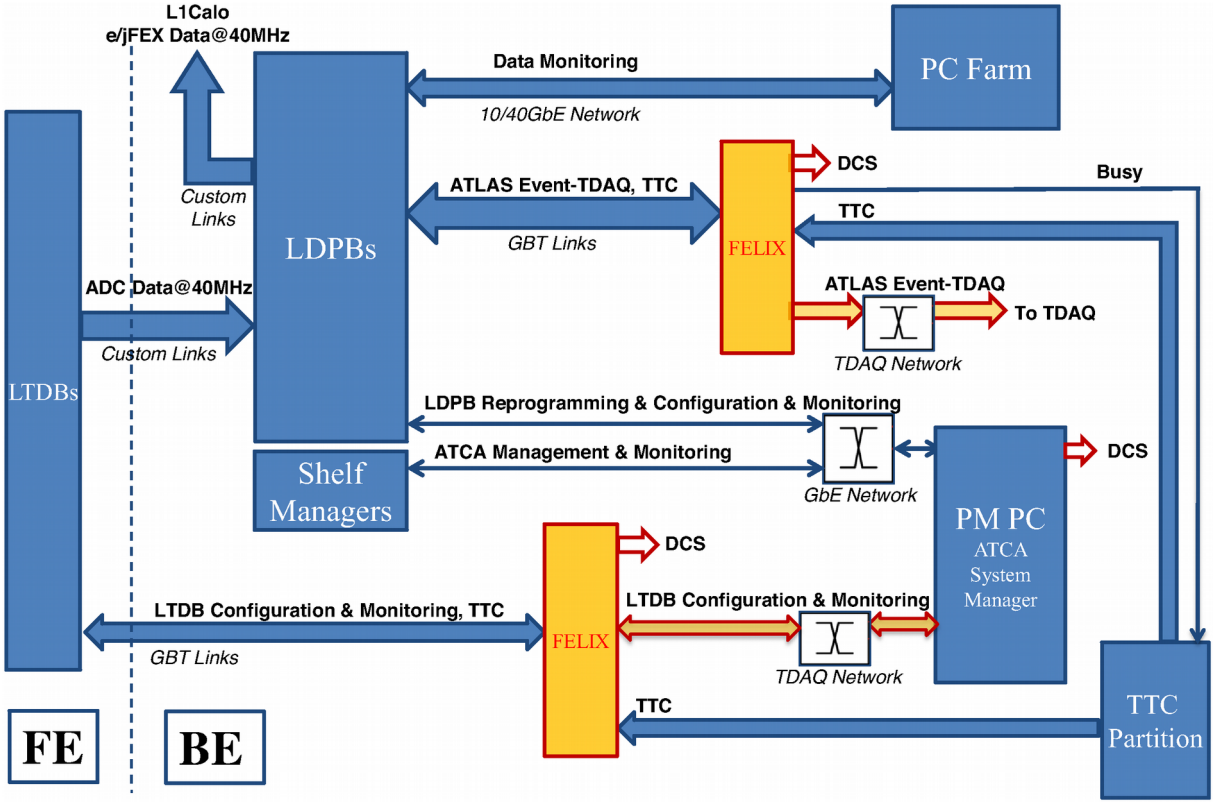
LAr FE Crate

Trigger DATA
L1 Receivers
(Analog)

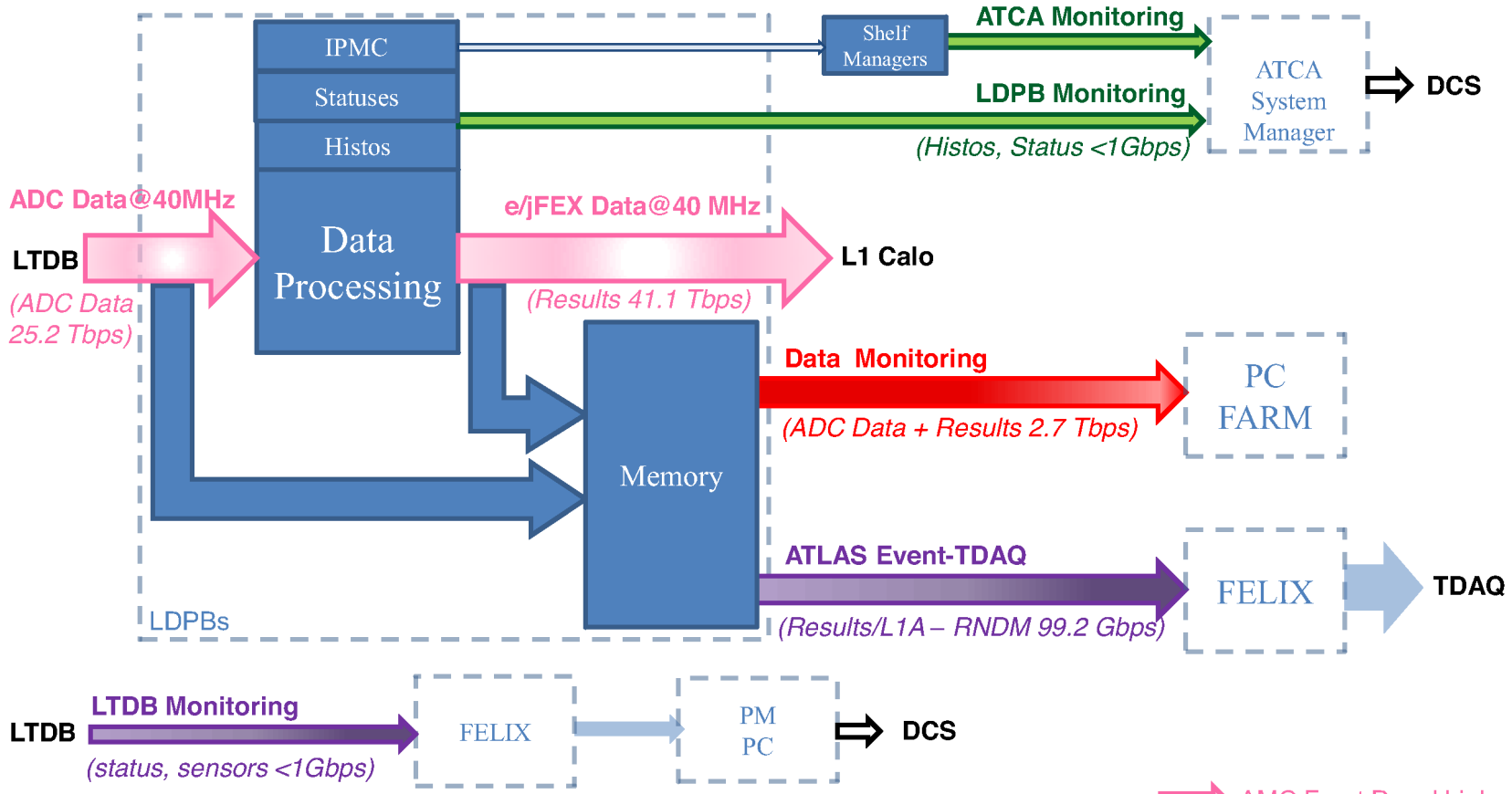
1524 FEBs in
58 FE Crates
(122 HFECs)

Phase 1 Back End System





Phase 1 Back End System (2)



LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

AMC Front Panel Links
GbE Network
10/40 GbE Network
GBT links
DCS
TDAQ Network