

Integrated CMOS sensor technologies for the CLIC tracker

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Abstract

Integrated technologies are attractive candidates for an all silicon tracker at the proposed future multi-TeV linear e^+e^- collider CLIC. In this context CMOS circuitry on a high resistivity epitaxial layer has been studied using the ALICE Investigator test-chip. Test-beam campaigns have been performed to study the Investigator performance and a Technology Computer Aided Design based simulation chain has been developed to further explore the sensor technology.

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INTEGRATED CMOS SENSOR TECHNOLOGIES FOR THE CLIC TRACKER

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1 Introduction

The Compact Linear Collider (CLIC) is an option for a future linear e^+e^- collider at CERN in the post LHC era, reaching a centre of mass energy up to 3 TeV [1, 2, 3, 4]. To perform highly precise physics measurements, a single point resolution of $7 \,\mu$ m and a material budget of $1 - 2\% X_0$ per layer need to be reached in the large area tracker detector. To suppress beam induced background particles, a time stamping accuracy of ~ 10 ns is required for the main tracker [2, 5]. A large surface (~ 100 m²) all-silicon tracker is planned to address these requirements. Integrated technologies are promising candidates in view of large-scale production and low material budget. Test beam campaigns to study the Investigator High Resistivity (HR) CMOS test chip have been performed at the CERN SPS with a 120 GeV pion beam. As a reference system, the CLICdp Timepix3 telescope has been used, providing an excellent tracking and timing resolution on the Device Under Test (DUT) plane of ~ 2 μ m and 1 ns, respectively [6].

2 The Investigator chip

Within the ALICE ITS upgrade project, a fully monolithic chip, the ALPIDE [7], has been developed in a 180 nm High Resistivity (HR) CMOS process (see Figure 1). Using the same process, the Investigator test-chip has been developed [8, 9]. Various pixel layouts are implemented in different mini-matrices with 8×8 pixels, to study the impact of the pixel layout on the performance. The standard process has been modified, inserting an additional n-layer (see Figure 2) to create a deep planar pn-junction and achieve full lateral depletion of the sensor. The output of the source follower of each individual pixel is connected to a dedicated output buffer with a rise time of ~ 10 ns.





Fig. 1. Investigator standard process schematic cross section.

Fig. 2. Investigator modified process schematic cross section.

The output buffers are read out by external ADCs, sampling the individual pixel response with a frequency of 65 MHz [9]. The presented studies have been performed for a mini-matrix with a pixel pitch of $28 \,\mu\text{m}$ and a bias voltage of 6 V, using chips with an epitaxial layer thickness of $18 \,\mu\text{m}$ for the standard, and $25 \,\mu\text{m}$ for the modified process.

3 Test beam data taking and reconstruction

If at least one pixel crosses a seed threshold, the full analogue waveform of all 8×8 pixels is read out. In Figure 3, a typical waveform of a pixel with a particle hit, as well as the fit function to reconstruct the waveform, are presented.



Fig. 3. Single pixel waveform reconstructed by a fit of the function f(t).

During the analysis, a threshold is applied on single pixel level. Since this threshold is lower than the seed threshold during data taking, it is referred to as the neighbour threshold. Adjacent pixels with a signal larger than the neighbour threshold are combined to a cluster; and the position is reconstructed by linear charge interpolation and η -correction. The distance between the predicted track position on the Investigator and the reconstructed hit position is required to be within 100 μ m. Moreover, tracks passing through the outer half of the edge pixels are discarded to avoid e.g. effects from the finite track prediction resolution.

4 Test-beam results

To explore the charge collection of the modified process in detail, results are projected onto the predicted track position within individual pixel cells (in-pixel presentation). A uniform efficiency distribution can be observed within the pixel cell (see Figure 4). Figure 5 shows the mean cluster size, defined as the number of pixels in a cluster above threshold. As expected from geometrical considerations, the lowest cluster size is observed in the pixel centre. The charge is shared most likely to one neighbour at the pixel edges, and to more than one neighbour at the pixel corners. As shown in Figure 6, the impact of charge sharing is also reflected in the distribution of the highest pixel signal (seed signal) in a cluster: the more charge is shared between the pixels, the lower the seed signal.



Fig. 4. Efficiency withinFig. 5. Mean cluster sizeFig. 6. Mean seed signalthe pixel cell.within the pixel cell.within the pixel cell.

A global efficiency higher than 99% and a spatial and timing resolution with respect to the reference tracks of ~ 6 μ m and ~ 5 ns, respectively, have been measured. Even though the measured timing resolution is limited by the ADC sampling frequency and the rise time of the output buffer, the results are well within the requirements for the CLIC tracker. In a next phase of R&D the results on the Investigator test chip will be used to optimise the pixel layout for a fully integrated chip for the CLIC tracker.

5 Simulation

A simulation chain using GEANT4 [11] to model the energy deposit in the sensor, a 2-dimensional Technology Computer Aided Design (TCAD) [12] simulation to model the device and perform a transient simulation of the charge collection, and a parametric model to simulate energy fluctuations and to perform the position reconstruction has been developed [13]. The electrostatic potential from the TCAD simulation is shown in Figure 7 and 8, respectively for the standard and modified process. As indicated by the white lines, the depletion for the standard process does extend over the full lateral size of the pixel, whereas the expected full lateral depletion can be observed for the modified process. Results are compared between simulation and data in Figure 9 - 11.



Fig. 7. Electrostatic potential Fig. 8. Electrostatic potential from from TCAD for the standard process. TCAD for the modified process.

A comparison of the mean cluster size in the X-direction within the pixel cell is presented for the standard process in Figure 9, showing a trend of larger cluster sizes at the borders of the pixel at 0 and 1 in data, which is well described by the simulation. For the modified process, an excellent agreement can be observed between simulation and data in the residual distribution in Figure 10, as well as in the resolution, defined as the Root Mean Square (RMS) of the residual distribution, for different neighbour thresholds in Figure 11.



modified process.

Fig. 9. X cluster size withinpixel cell standard process.

Fig. 10. Spatial residual Fig. 11. Spatial residual modified process.

Summary 6

The ALICE HR CMOS Investigator test chip has been explored in detail by in-pixel test beam studies and a simulation based on GEANT4 and TCAD. The simulation results reproduce the test beam measurements, showing a good understanding of the technology. An efficiency of > 99% and a spatial and timing resolution of $6\,\mu\text{m}$ and $5\,\text{ns}$, respectively, have been measured, using a mini-matrix with a pitch of $28\,\mu\text{m}$ and a bias voltage of 6 V. The measured performance indicates the suitability of the technology for the CLIC tracker and the presented studies are used in a next R&D phase as input for the design of a fully integrated chip for the CLIC tracker.

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