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PACIFIC

a readout ASIC for the LHCb Scintillating Fibre Tracker

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On behalf of the LHCb SciFi Collaboration

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LHCb Upgrade

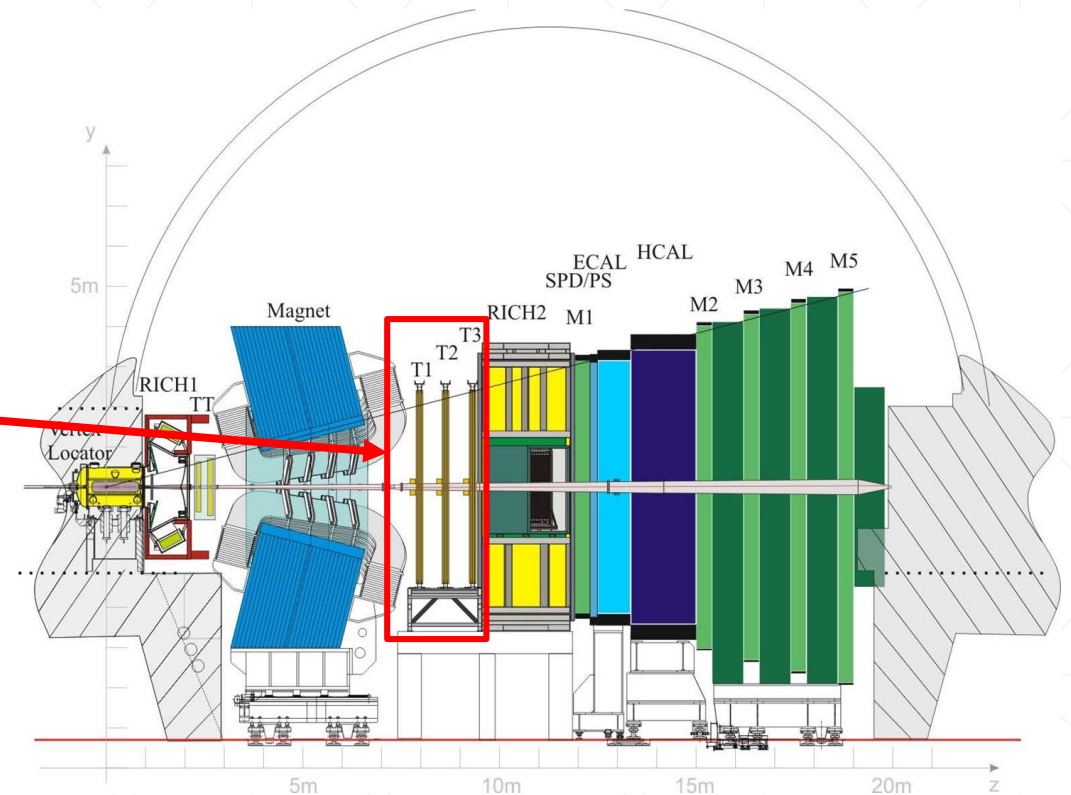
increase the luminosity to $2 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$ to boost significantly the physics reach

- more severe radiation environment
- 40MHz readout triggerless
- $5 \times$ current occupancy

the current Tracking Stations
(Gas Straw Tube Tracker + Silicon Tracker)
replaced by

Scintillating Fibre Tracker

total area 340m^2 , resolution $< 100\mu\text{m}$



Schematic view of the current LHCb detector

Scintillating Fibre Tracker (SciFi)

- 250 μ m diameter scintillating fibre wound into a 6-layer 2.5m-long fibre mat
- ✓ one end equipped with a mirror
- ✓ read out by SiPM arrays (single channel: 250 μ m \times 1.625mm, 104pixels)

- 3 \times Tracking Stations \Rightarrow 524,000 SiPM channels

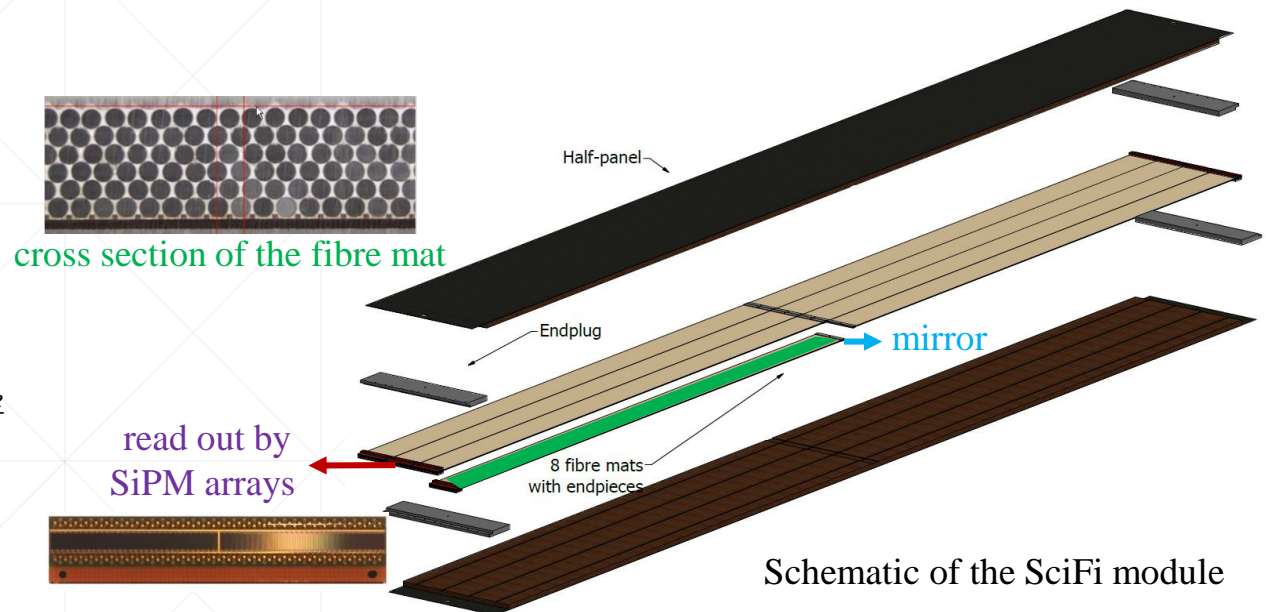
More related talks:

SciFi-A large Scintillating Fibre Tracker for LHCb by Ulrich Uwer

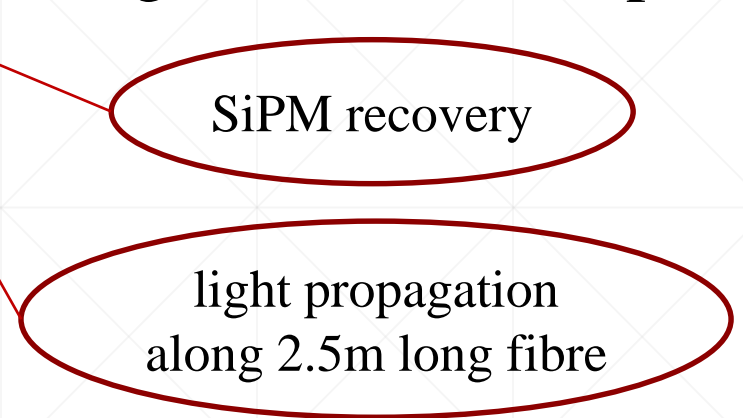
23/5/2017 TIPP parallel section

Characterisation of the Hamamatsu silicon photomultiplier arrays for the LHCb Scintillating Fibre Tracker Upgrade by Axel Kuonen

23/5/2017 TIPP parallel section



Design Challenges for the Readout ASIC

- handle the long-tail SiPM signals with high detector occupancy ?
 - ✓ minimize the spillover effect
 - ✓ reduce dead time
 - ✓ sufficient response plateau
 - in total 524,000 SiPM channels to be read out at 40MHz ?
 - ✓ most efficient way to digitize and process the data
 - ✓ low power consumption
- 

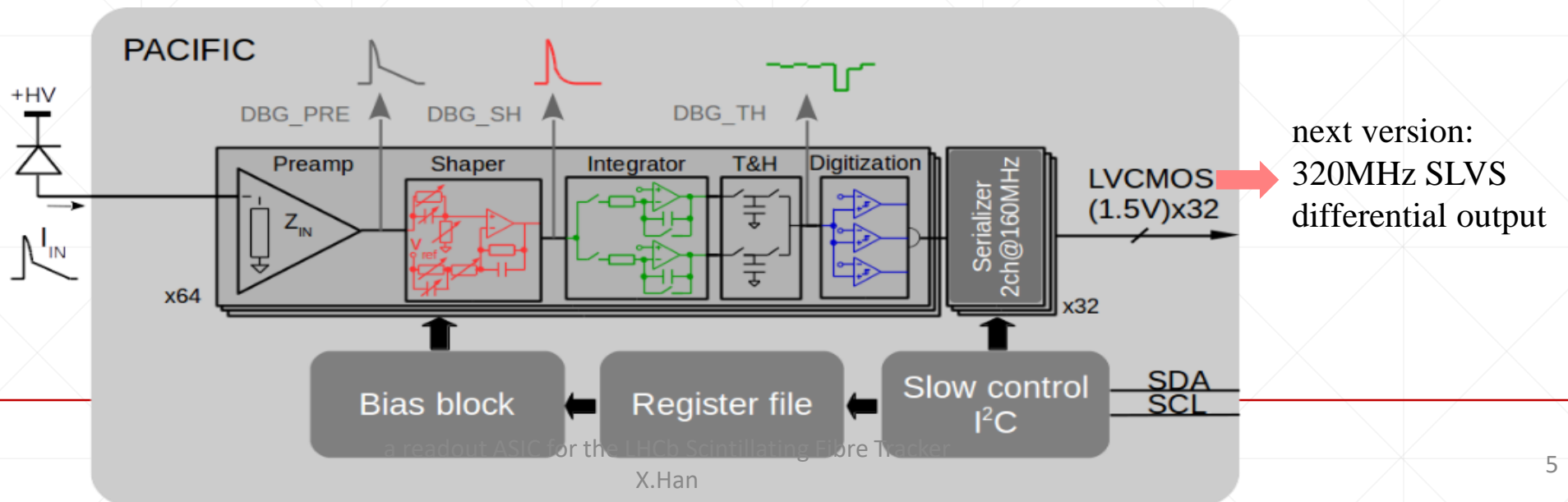
PACIFIC

a low Power Asic for the sCIntillating FIbre traCker

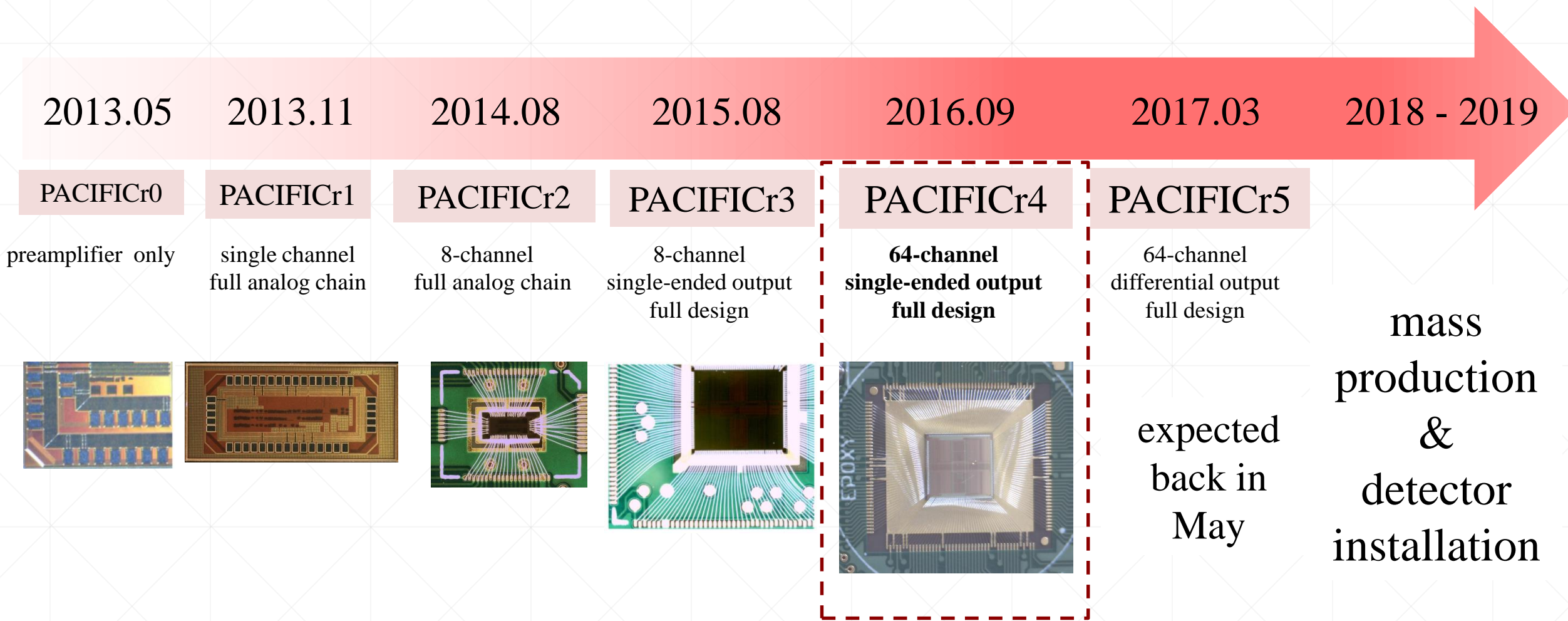
- 64-channel current mode input
- **configurable fast shaper : minimize spillover**
- **interleaved gated-integrators per channel: minimize dead time**
- **2-bit non-linear digitisation per channel : minimum data for sufficient tracking information**
- adjustable input anode DC voltage (4-bit DAC, 50mV/LSB)

power consumption <10mW/channel

CMOS 130nm Technology

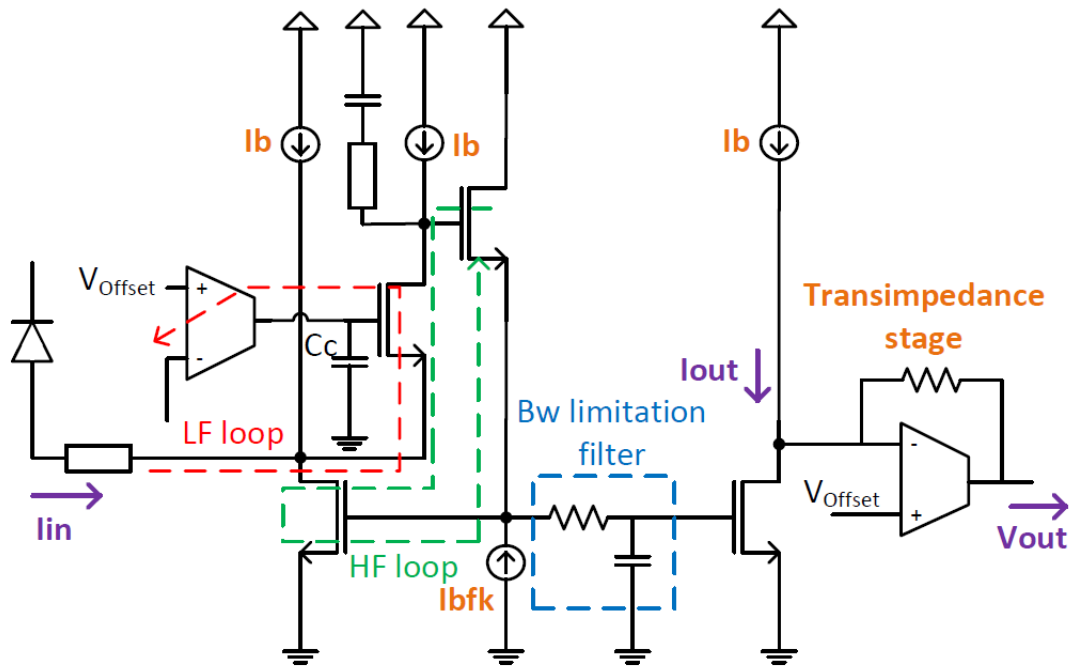


Prototype

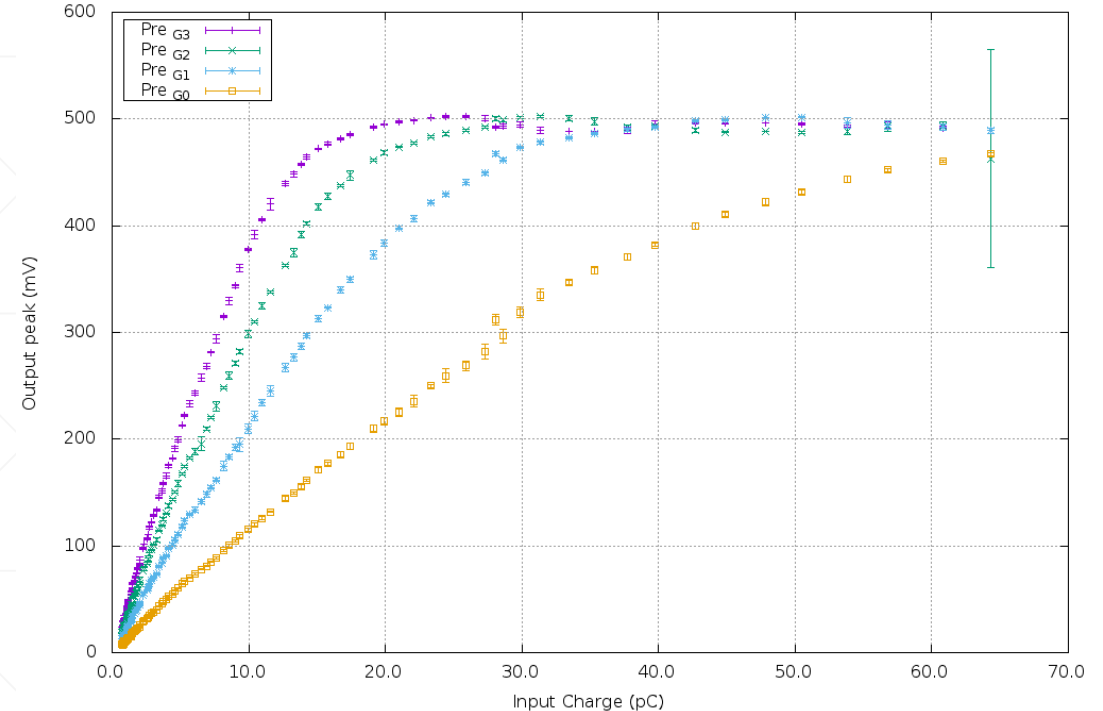


Preamplifier

- double feedback **current conveyor** (50 Ω input impedance, 250MHz bandwidth)
- **4 \times selectable gains** at the output mirror
- closed loop **transimpedance amplifier** to convert current into voltage



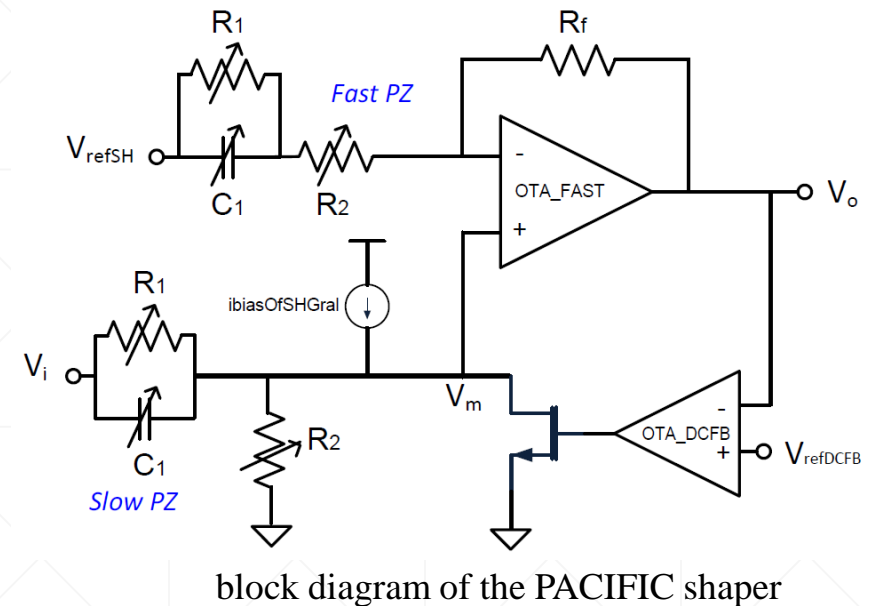
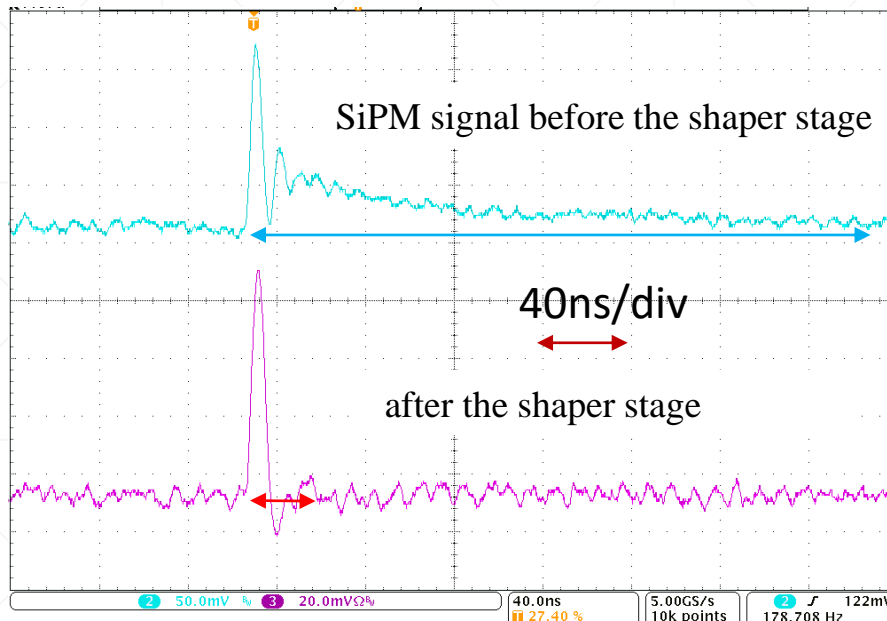
block diagram of the PACIFIC preamplifier



PACIFICr4 preamplifier linearity measured with charge injection

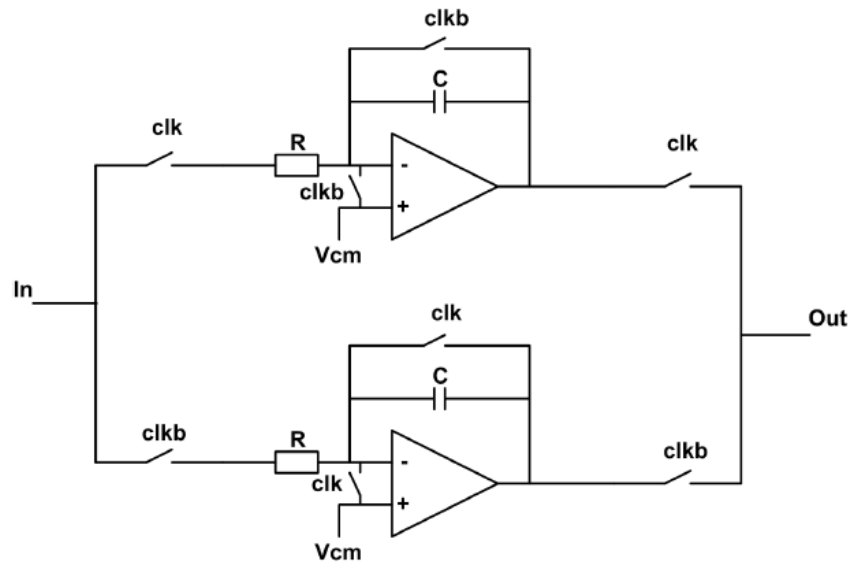
Fast Shaper

- **double pole-zero cancellation for the SiPM signals**
- ✓ first pole-zero cancels the slow component from SiPM capacitance and quenching resistor
- ✓ second pole-zero cancels the fast component from trace parasitics and input impedance
- **parameters tunable via slow control registers to adapt to different types of SiPMs**

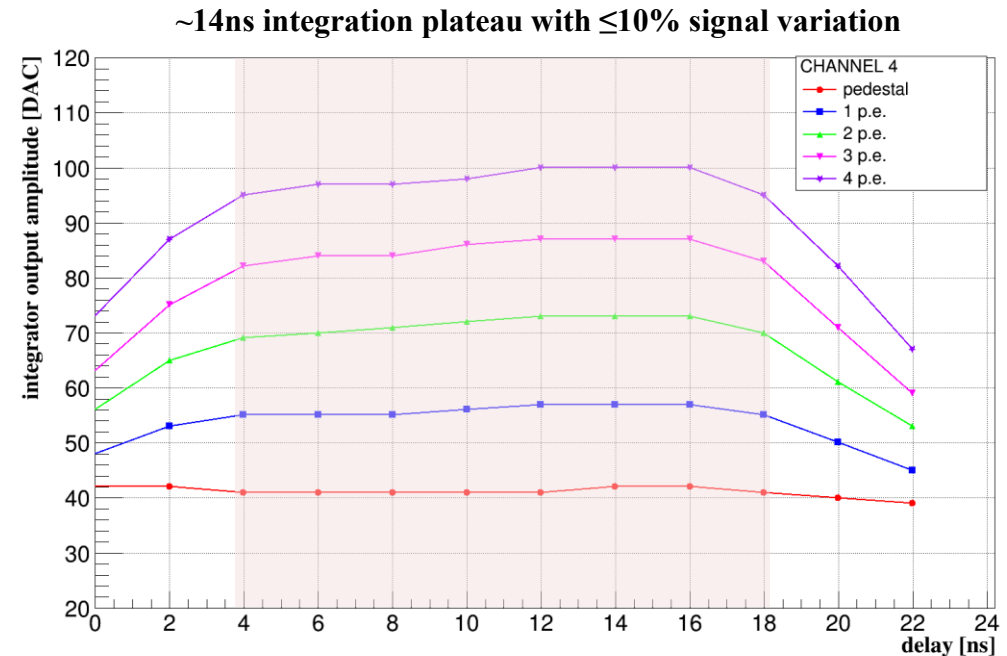


Interleaved Gated Integrators

- one integrator is working, while the other is reset : minimum dead time
- integration synchronized with the system clock



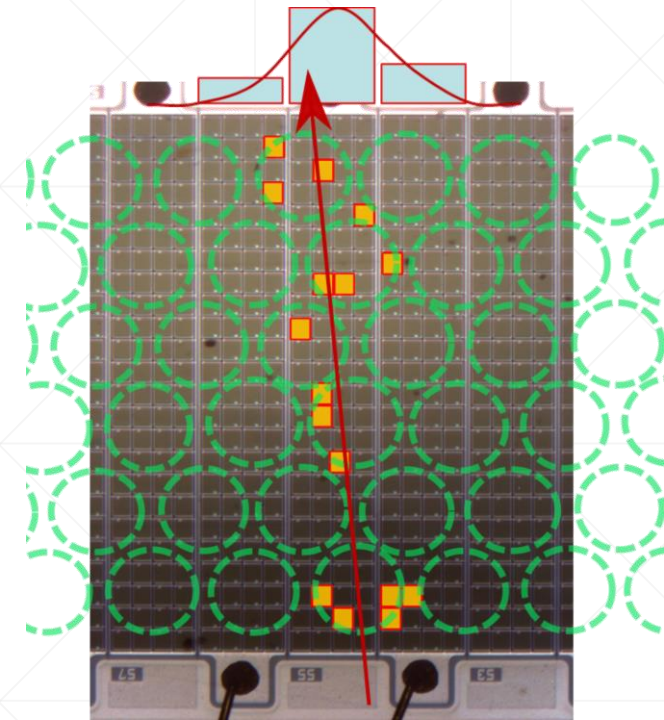
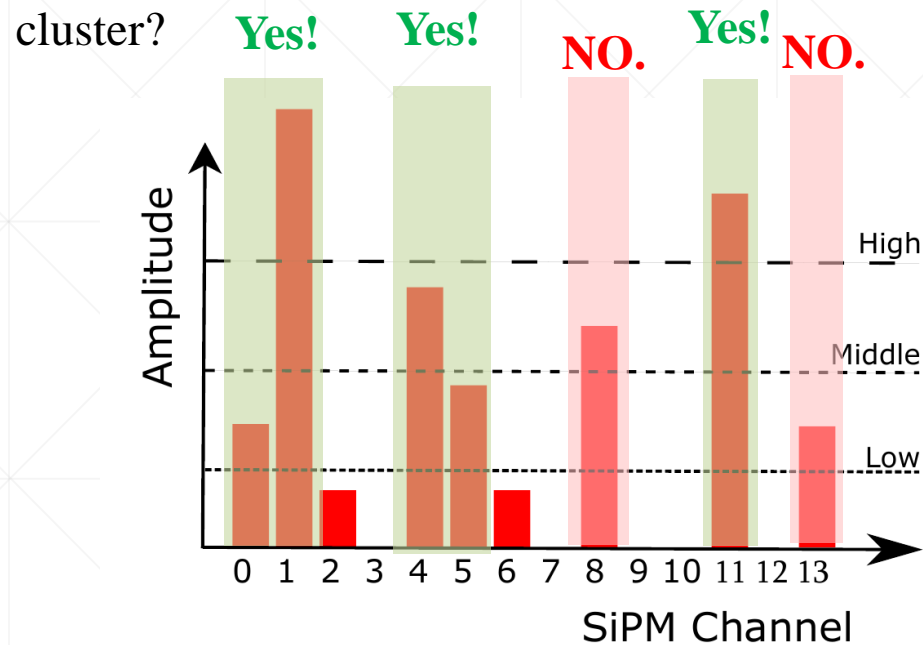
block diagram of the PACIFIC interleaved gated integrators



PACIFICr4 integrator response measured with light injection

Digitisation

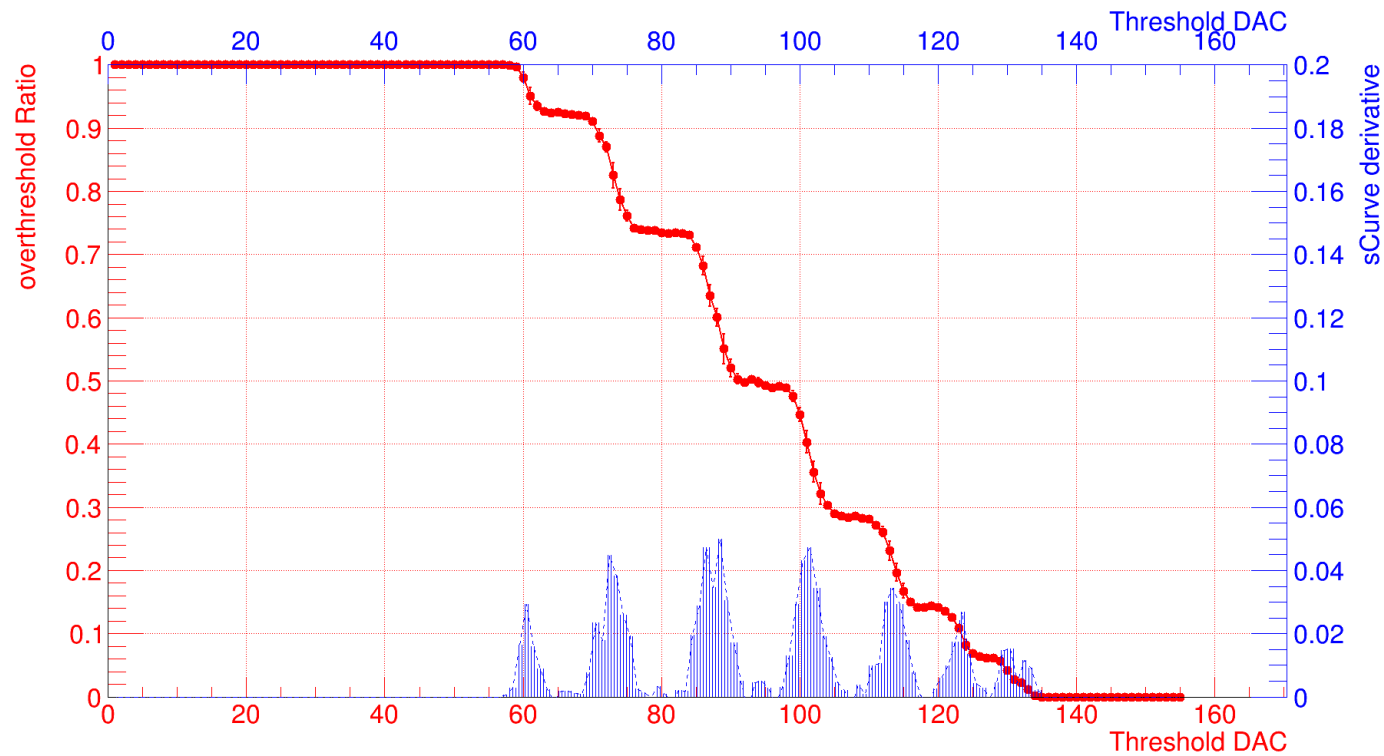
- analog signal digitized by three threshold-tunable comparators per channel
- three thresholds based on the cluster algorithm
 - ✓ **low** threshold: noise suppression
 - ✓ **middle** threshold: cluster candidate
 - ✓ **high** threshold: single channel clusters



sketch of a typical cluster produced when particles passing through the SciFi detector

Light Injection Result

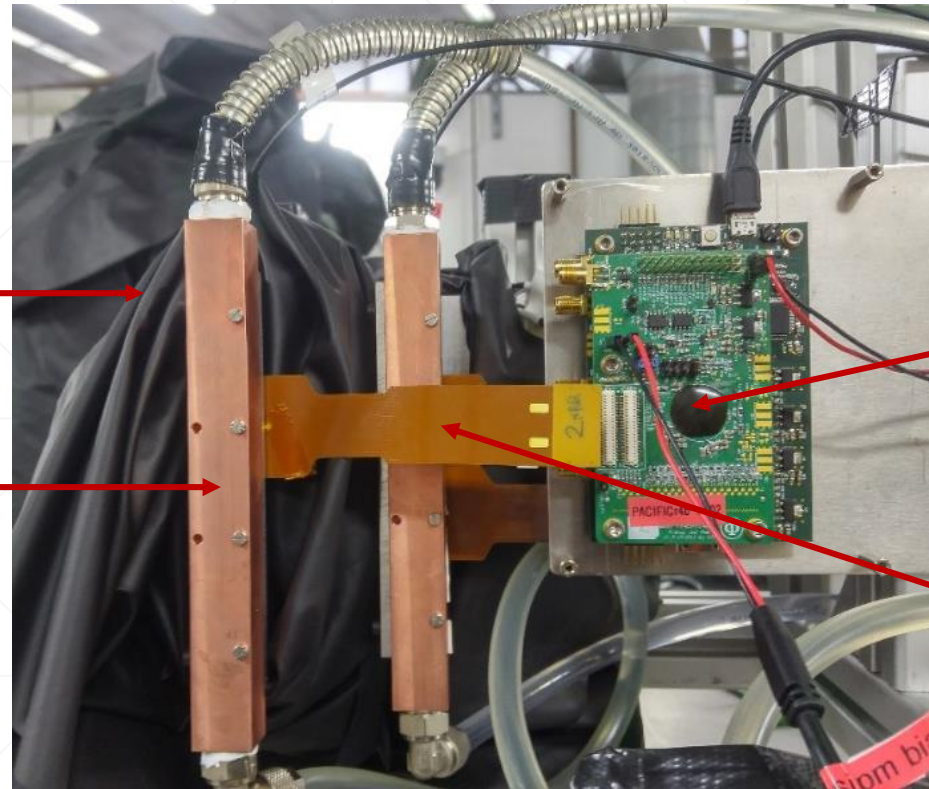
- 5ns-width light pulse generated by vertical-cavity surface-emitting lasers (VCSEL)
- using SciFi custom SiPM arrays



PACIFIC threshold scan result : clear photo-peak steps

Test Beam at DESY 2017

- DESY beamline T22, Feb 2017
- 1~6 GeV electrons (maximum rate @ 2 GeV) continuous beam



SciFi prototype module
covered in black blanket for light tightness

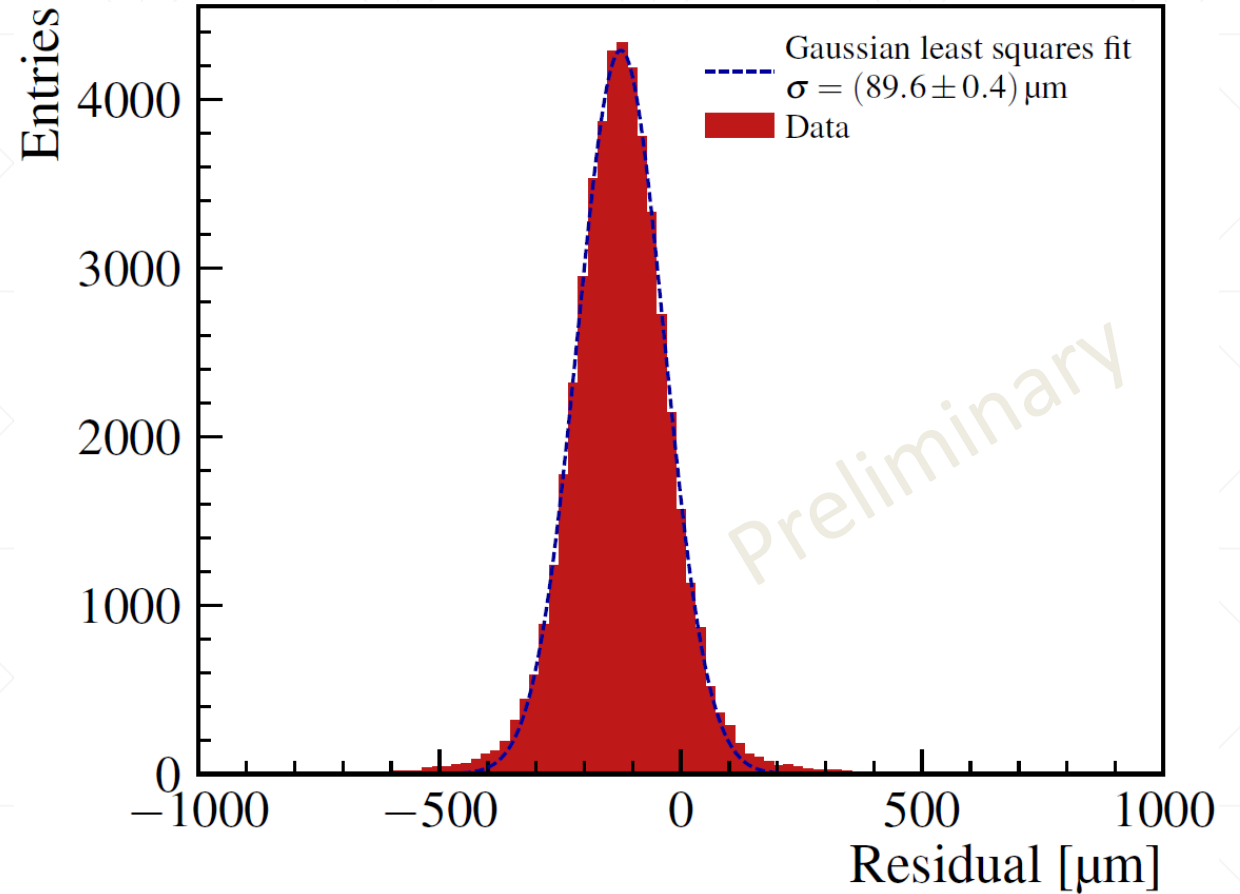
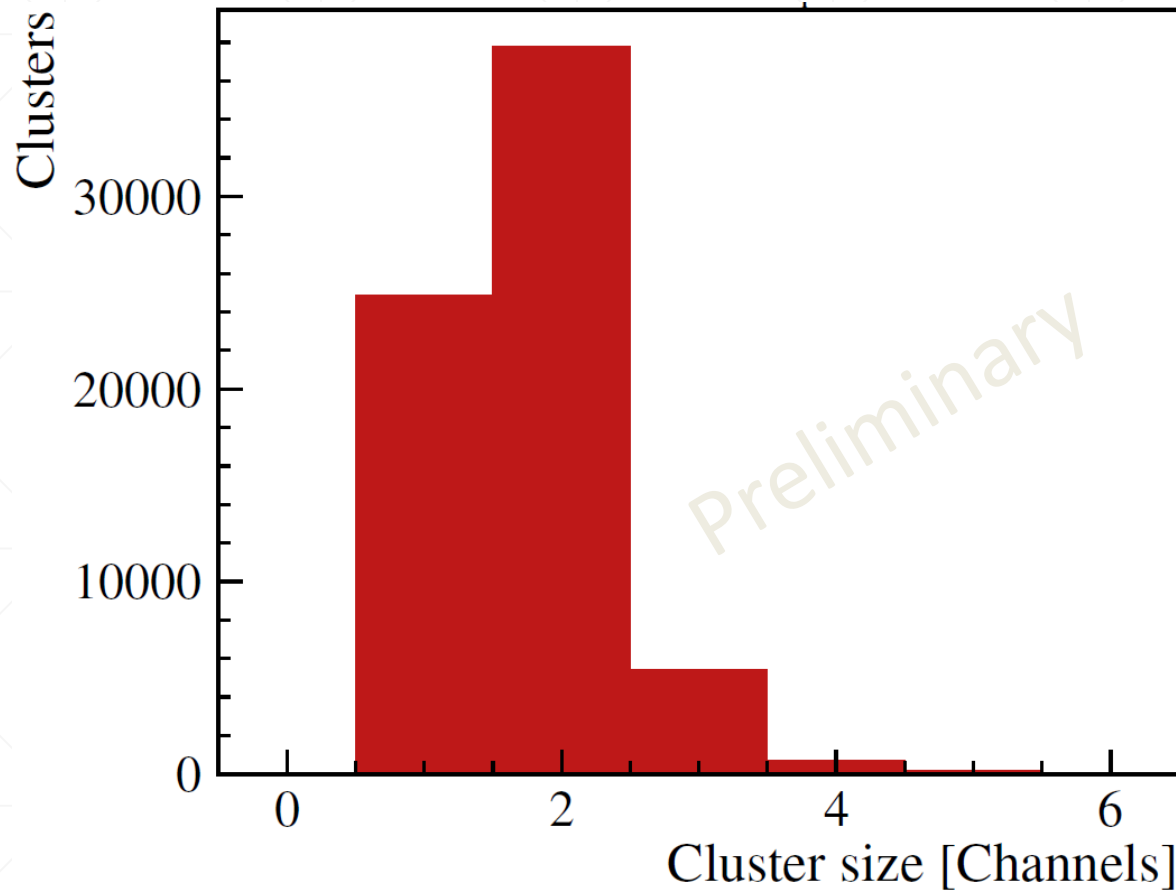
cooling bar
to keep the SiPM temperature stable

wire-bonded PACIFICr4
with glob top

SciFi SiPM array
with flex cable

SciFi module read out by custom SiPM arrays and PACIFICr4

Cluster Size & Spatial Resolution



Conclusions and Future Plans

- a low power ASIC designed for the LHCb Scintillating Fibre Tracker
 - ✓ configurable fast shaper
 - ✓ minimum integration dead time
 - ✓ 40MHz readout
 - ✓ 2-bit data per channel to encode signal amplitude
- the full design prototype has been evaluated in the test beam at DESY in Feb 2017
- a new version with SLVS differential output submitted and will be back soon
- plan to launch engineering run at the end of 2017

Thank you!

Questions?

