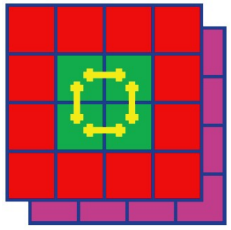
The Phase-I Upgrade of the ATLAS First Level Calorimeter Trigger (L1Calo)

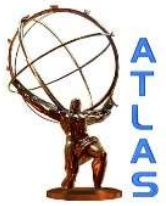
International Conference on Technology and Instrumentation in Particle Physics

- 22-26 May 2017, Beijing -

Victor Andrei (KIP Heidelberg)

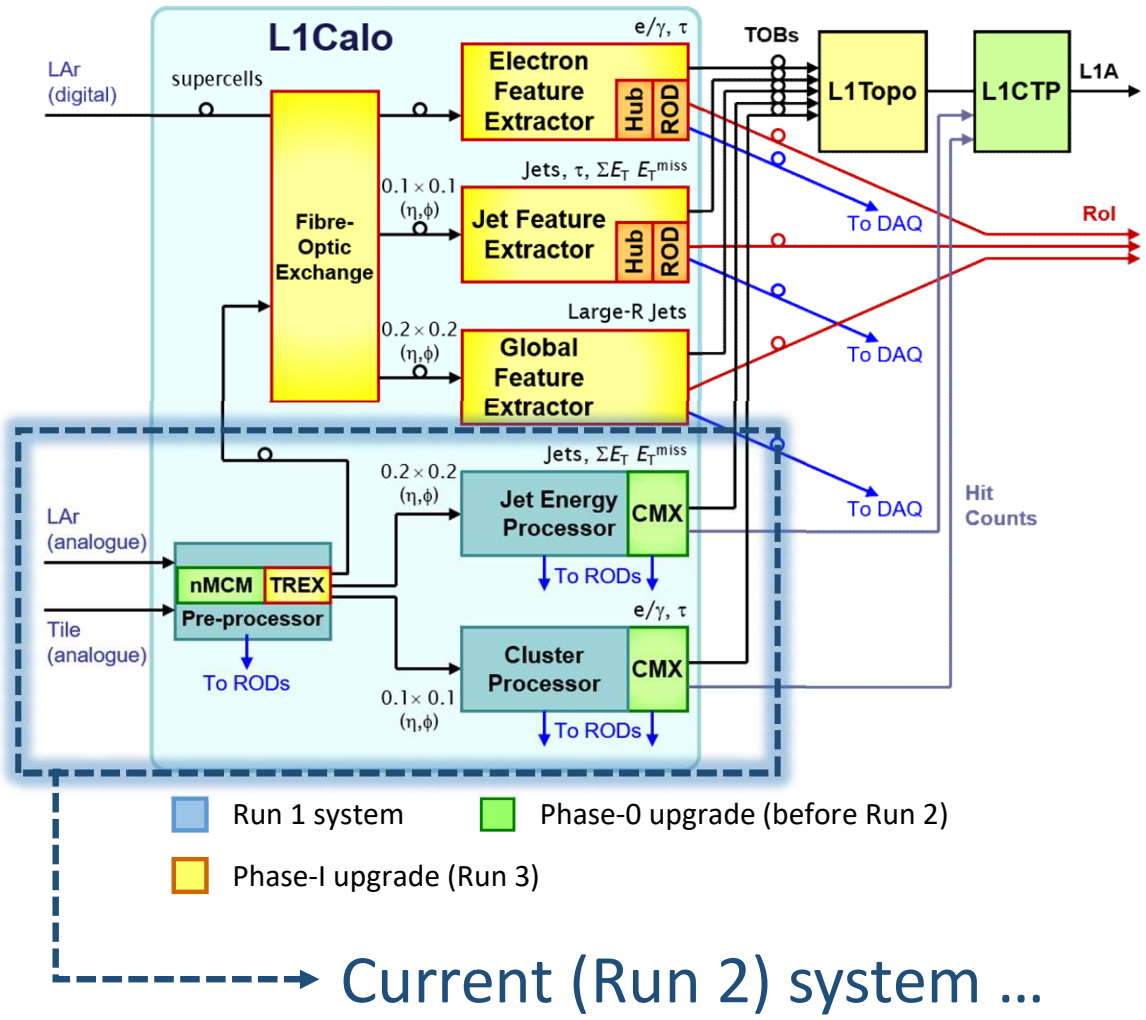
on behalf of the ATLAS Collaboration





Outline

- ATLAS L1Calo trigger system
  - Current architecture (Run 2)
  - Phase-I upgrade (Run 3)
- New L1Calo digital trigger
  - Algorithms
  - Prototype modules
- Test results with the prototypes
- Outlook



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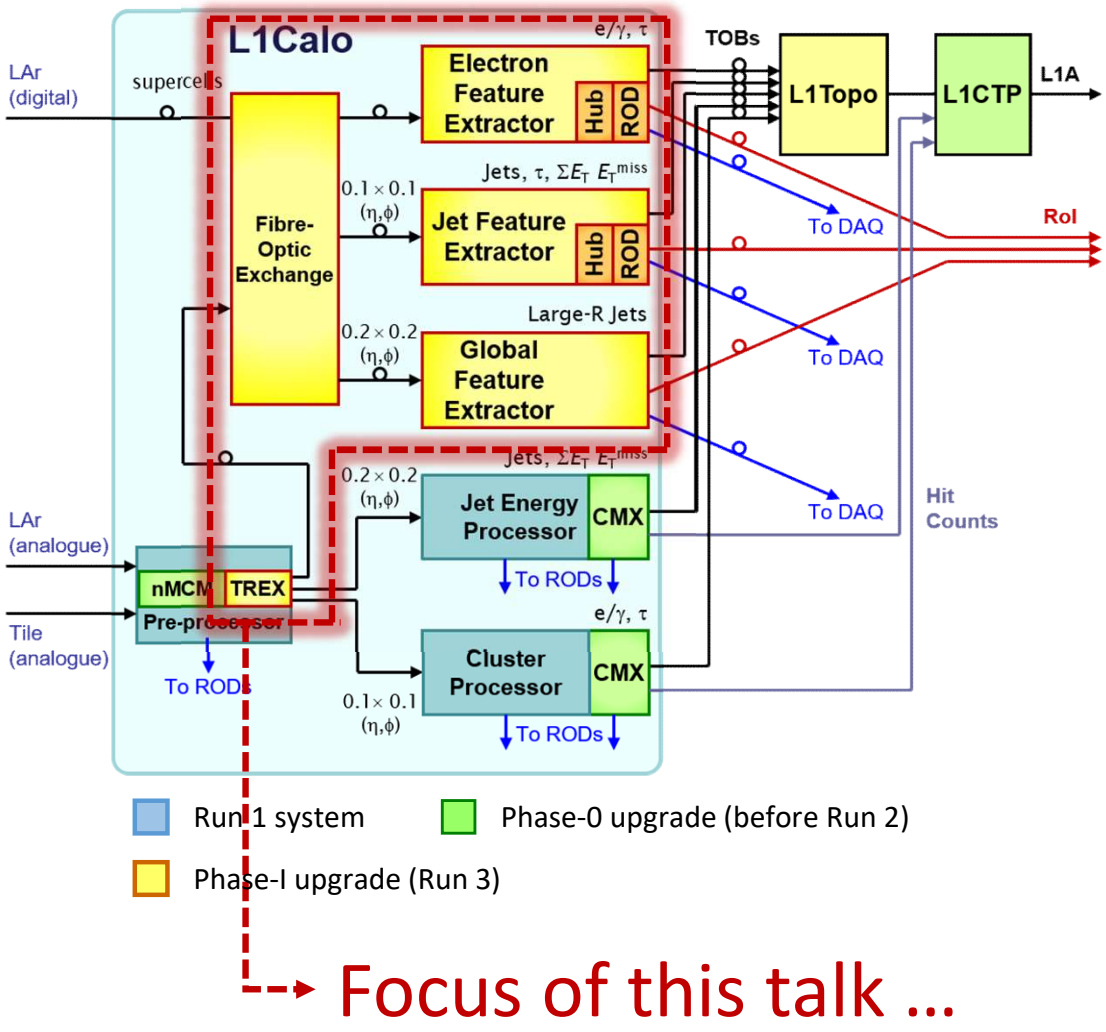

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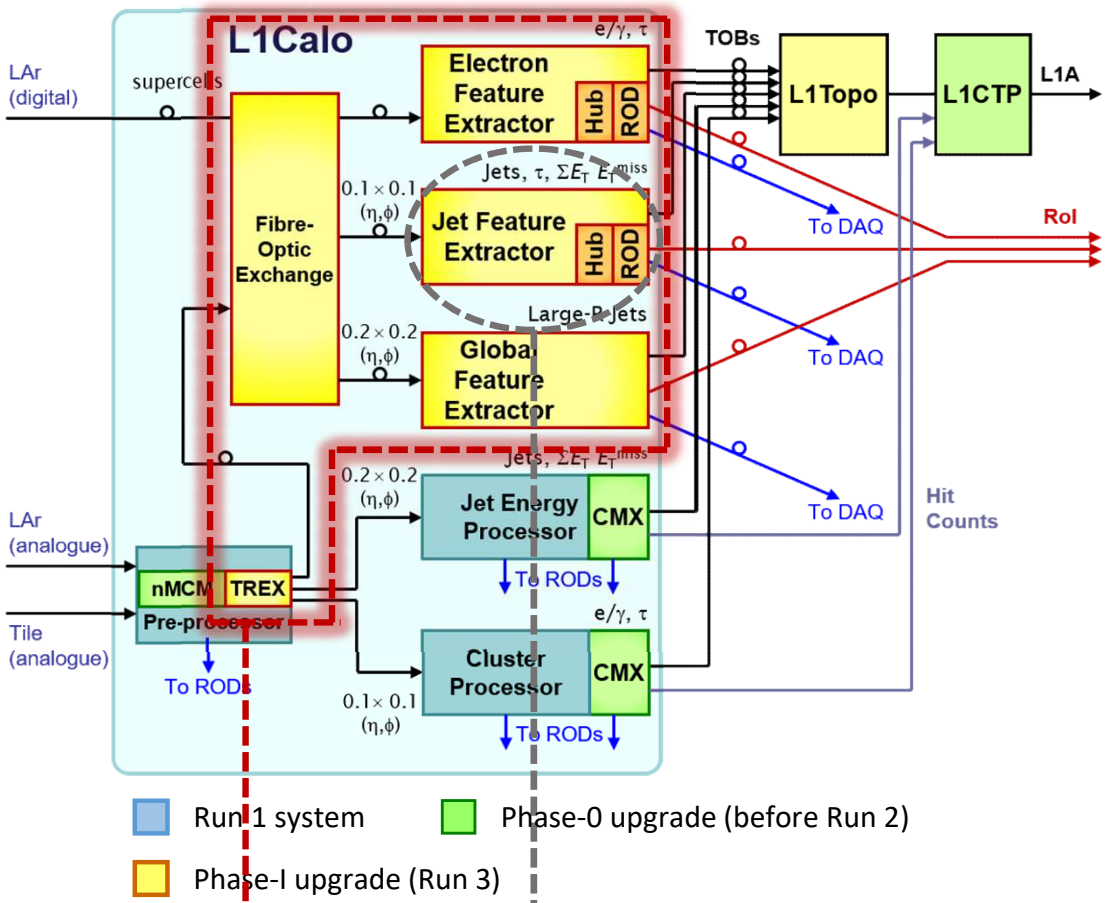
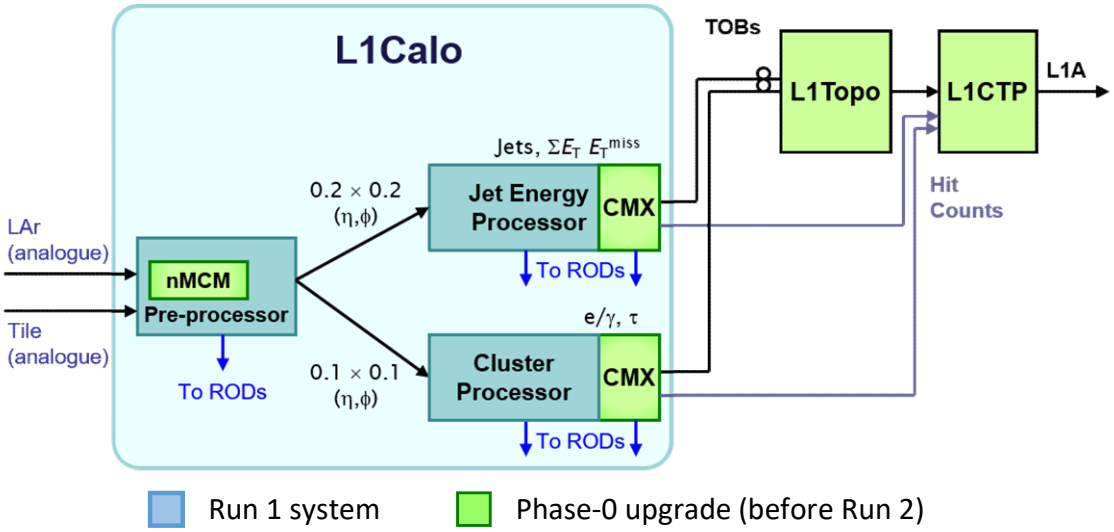


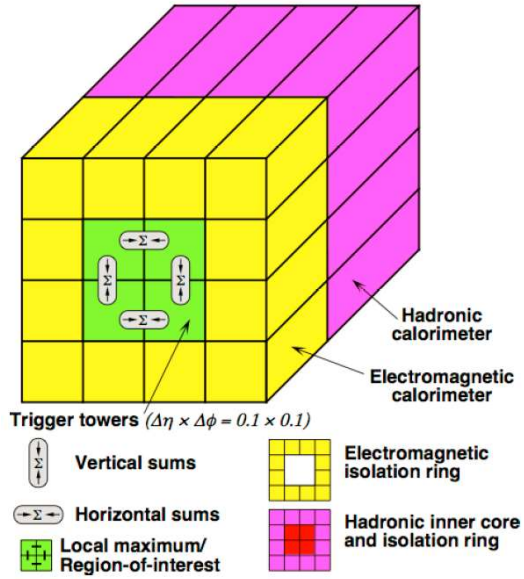
→ Focus of this talk …

Presented later today by Christian Kahra …

ATLAS L1Calo in Run 2

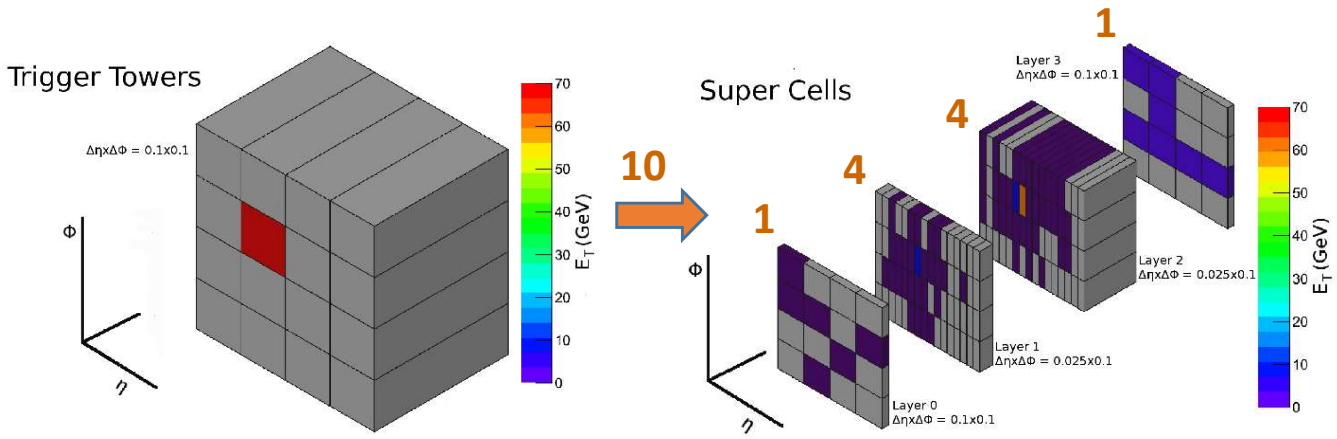
- Hardware-based, pipelined system
- Input
  - Coarse analogue *trigger-towers* (from LAr & Tile Calorimeters)
- Processing
  - Digitisation, pile-up subtraction, bunch-crossing ID, E_T calibration (PreProcessor)
  - Sliding-window based object identification (Cluster & Jet-Energy Processors)
- Output
  - Real-time digital results to L1Topo and CTP (~2 μs after the collision)
  - Event data to DAQ (≤100 kHz)
  - Regions-of-Interest (RoI) to HLT

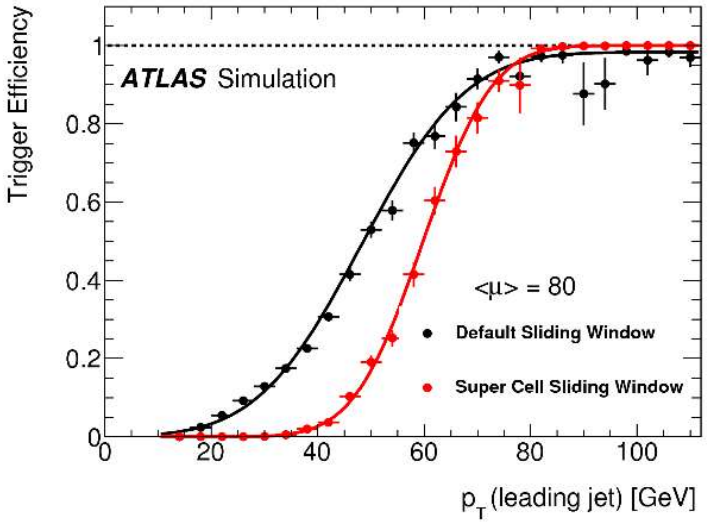


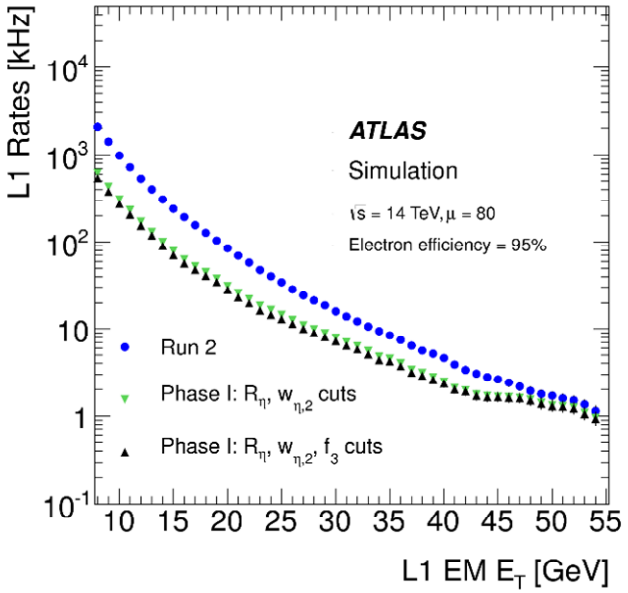


Phase-I Upgrade (2019-2020)

- Increased LHC luminosity
  - More interactions per bunch-crossing (μ)
  - Higher event rates
- Finer-granularity input from LAr Calorimeter
  - 10 super cells per trigger-tower
  - Better resolution and background rejection

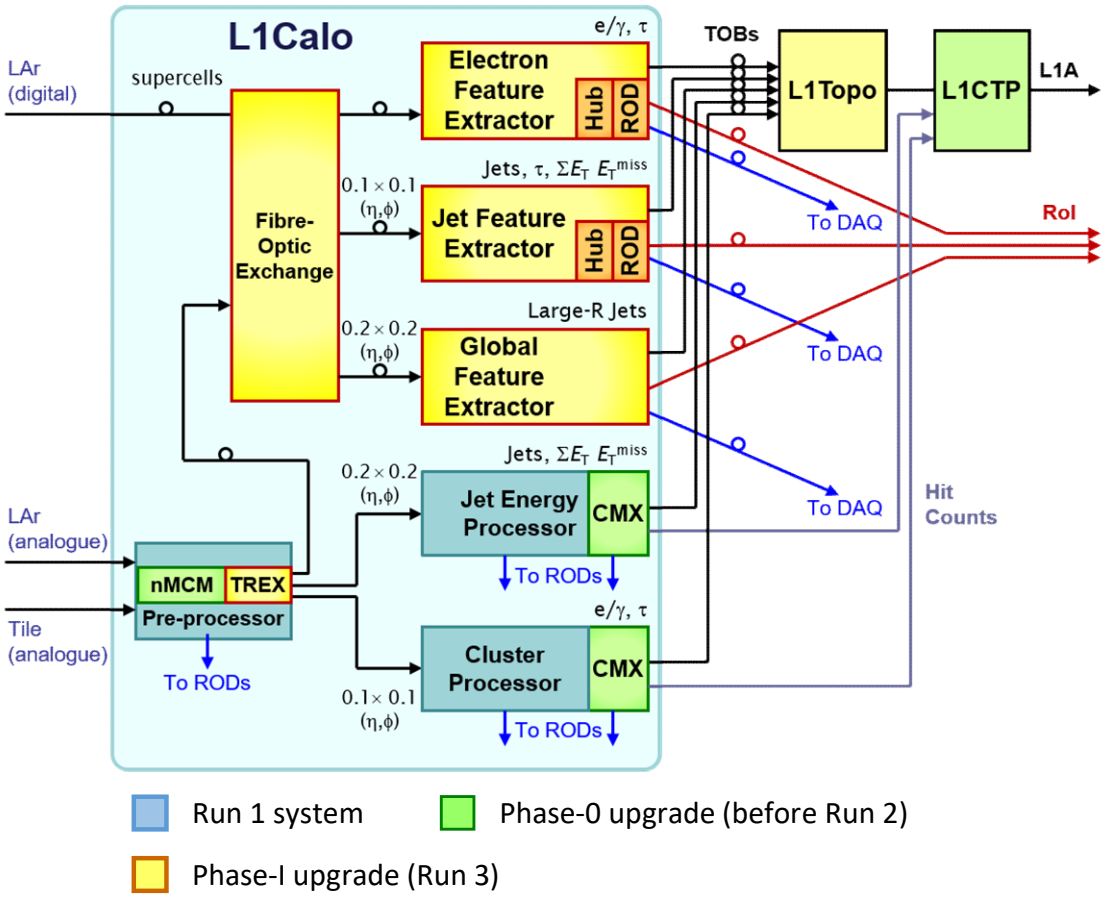






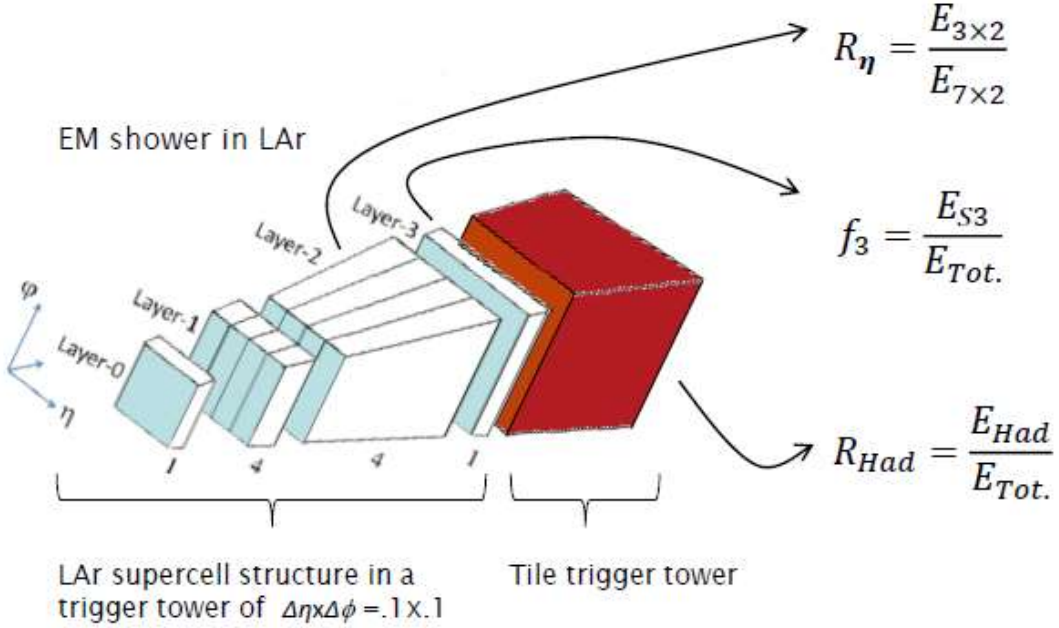
L1Calo in Phase-I Upgrade

- New Feature Extractor (FEX) processors
  - Improved object-finding algorithms
- Digital super-cells from LAr
  - ≤ 12.8 Gbps optical links
- Analogue trigger-towers from Tile
  - Tile Rear Extension (TREX) modules in the PreProcessor
    - provide Tile digitised results to FEXes
    - maintain legacy trigger data path
  - Replaced by digital Tile PreProcessor in Phase-II
- Fibre Optic Exchange (FOX)
  - Re-maps LAr & Tile input to FEXes
- Trigger rate and latency as in Run 2



Electromagnetic Feature Extractor (eFEX)

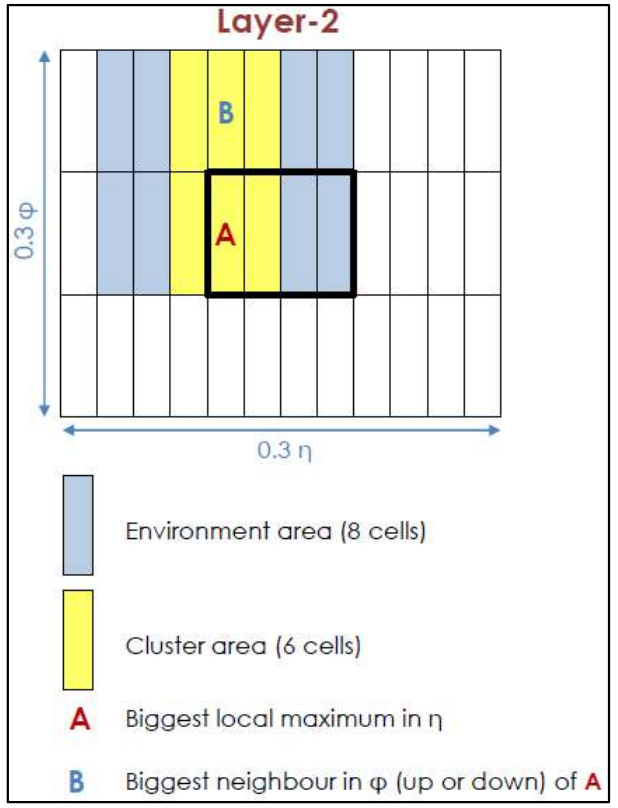
- Identifies **e/γ** and **τ** candidates
- Computes energy (hadronic vetos)



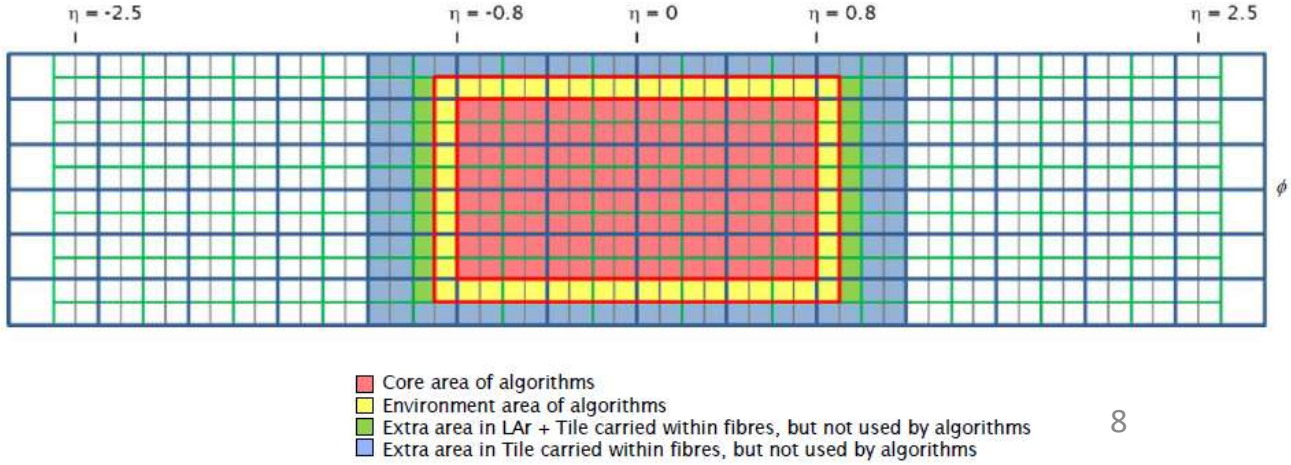
$$R_{\eta} = \frac{E_{3\times2}}{E_{7\times2}}$$

$$f_3 = \frac{E_{S3}}{E_{Tot.}}$$

$$R_{Had} = \frac{E_{Had}}{E_{Tot.}}$$

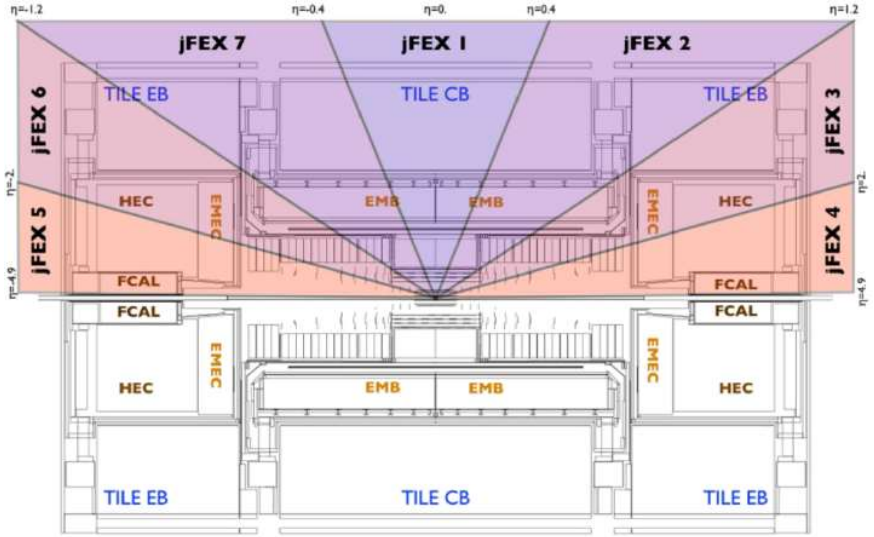


- 24 ATCA modules covering $|\eta| \leq 2.5$
  - Typical module coverage: 1.7 x 0.8 (Δη x Δφ)



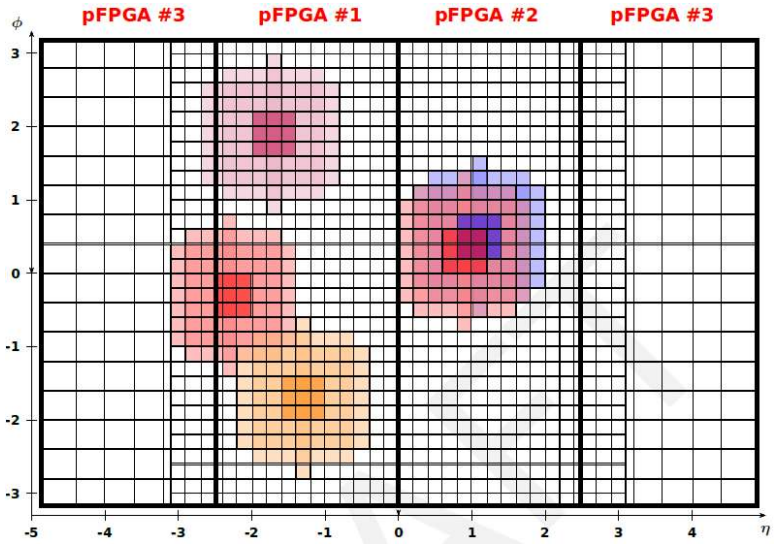
Jet Feature Extractor (jFEX)

- Identifies jets (large τ), ΣE_T, E_T^{miss}
  - Gaussian weighting jets (1.7 x 1.7 and 0.9 x 0.9)
- 7 ATCA modules covering $|\eta| \leq 4.9$
  - Each jFEX processes a whole φ ring
  - 0.1 x 0.1 input trigger-tower data
- *Covered by Christian Kahra's talk*



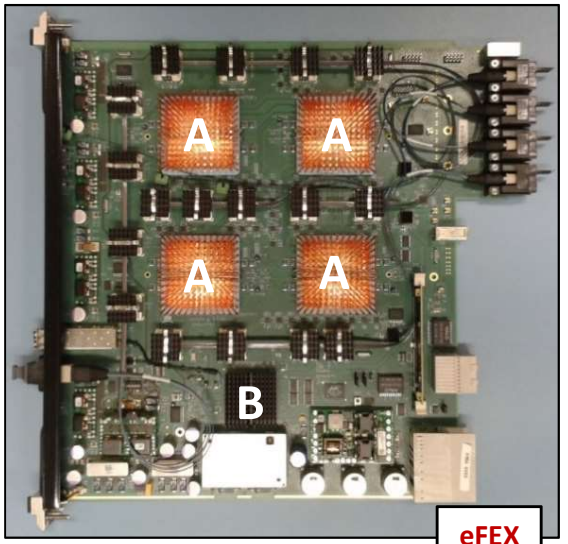
Global Feature Extractor (gFEX)

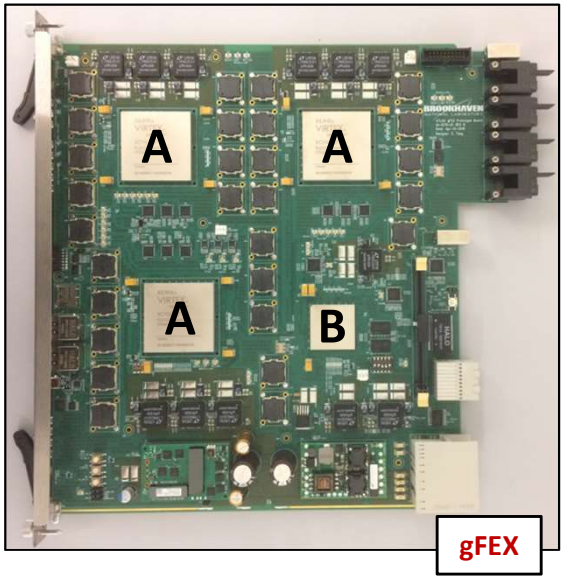
- Identifies large-radius jets
  - Jet-level pile-up subtraction
- Computes global event observables
  - E_t^{miss}, jets-without-jets, centrality, etc.
- Single ATCA module to process the entire calorimeter data
  - 0.2 x 0.2 input tower-sum data



eFEX & gFEX Prototype Modules

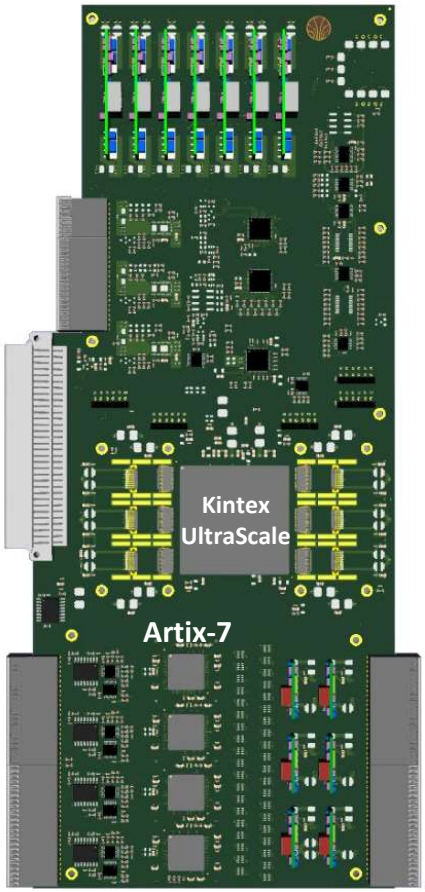
- PCBs: 22-layer (eFEX), 26-layer (gFEX)
- FPGAs (Xilinx)
  - Algorithms (**A**): Virtex-7 (eFEX), Virtex UltraScale (gFEX)
  - Control, readout, monitoring (**B**): Virtex-7 (eFEX), Zynq (gFEX)
- High speed optical links (≤ 12.8 Gbps)
  - eFEX: 144 inputs, 36 outputs, 17 MiniPODs
  - gFEX: 280 inputs, 60 outputs, 28 MiniPODs
- High speed data sharing (≤ 12.8 Gbps)
  - Up to 424 on-board differential pairs
- Status
  - Full prototypes manufactured and under test
  - Firmware algorithms in development





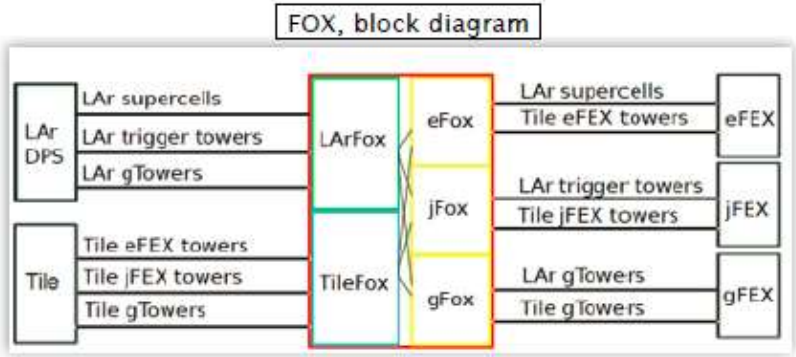
Tile Rear Extension (TREX)

- Sends Tile digitised results to FEXes and to legacy processors
  - 32 VME-RTM modules covering $|\eta| < 1.6$
- PCB: 18-layer (prototype)
- FPGAs (Xilinx)
  - 4 Artix-7 (LVDS fan-out)
  - 1 Kintex UltraScale (processing, control, readout & monitoring)
- High-speed links (≤ 12.8 Gbps)
  - Optical: 13 input, 49 output
  - 6 Samtec FireFly (O-Tx/Rx)
  - LVDS (≤ 1 Gbps): 170 on-board, 73 output
- Status
  - Prototype being manufactured
  - Firmware under development

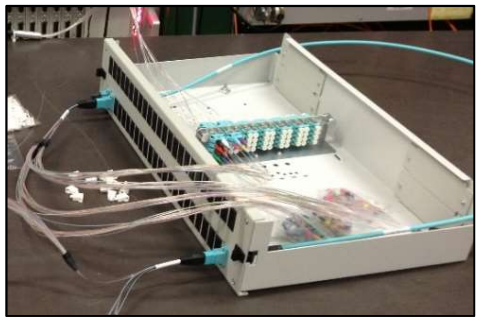


Fibre Optical Exchange (FOX)

- Re-maps signals from LAr and TREX/Tile to FEXes
  - ~7100 input links
- Passive optical devices for re-mapping and splitting

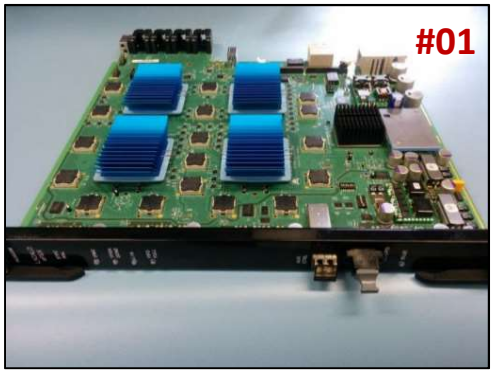


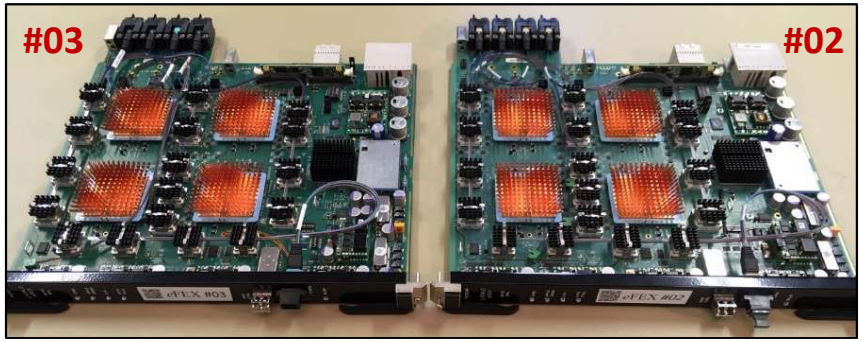
- Status
  - Demonstrator manufactured & tested
  - Mapping mostly defined

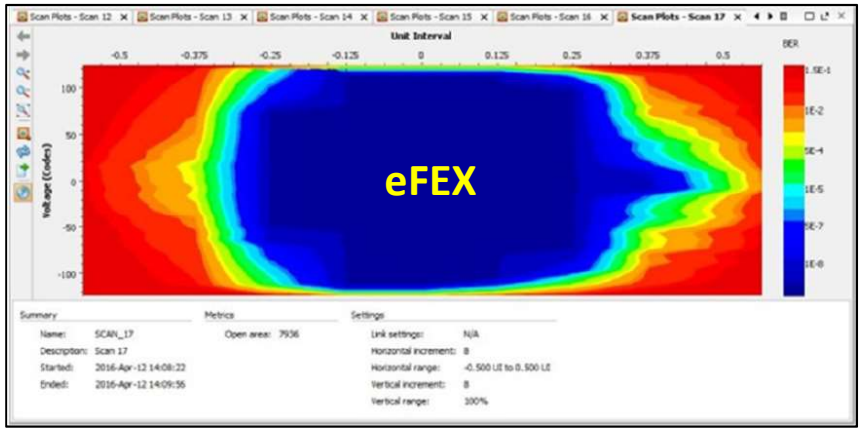


eFEX Test Results (1)

- 3 prototypes manufactured and tested
- Link tests @11.2 Gbps
  - @CERN: with LATOME (LAr)
    - 1st eFEX prototype and partial link tests only
    - FOX demonstrator
  - @RAL: with 2 FEX Test Modules (FTMs)
    - all 3 eFEX prototypes and all optical I/O links
    - 32 inter-FPGA links
    - 14 backplane links (@10.24 Gbps)
  - IBERT PRBS-31, 8b/10b encoding
  - No errors down to BER < 10^{-14} for 99% of links
  - Faulty links due to
    - a few bad high-speed buffers
    - poor PCB routing on one link
    - power sag because of insufficient copper in power plane
    - optical connectors sensitive to cleanliness



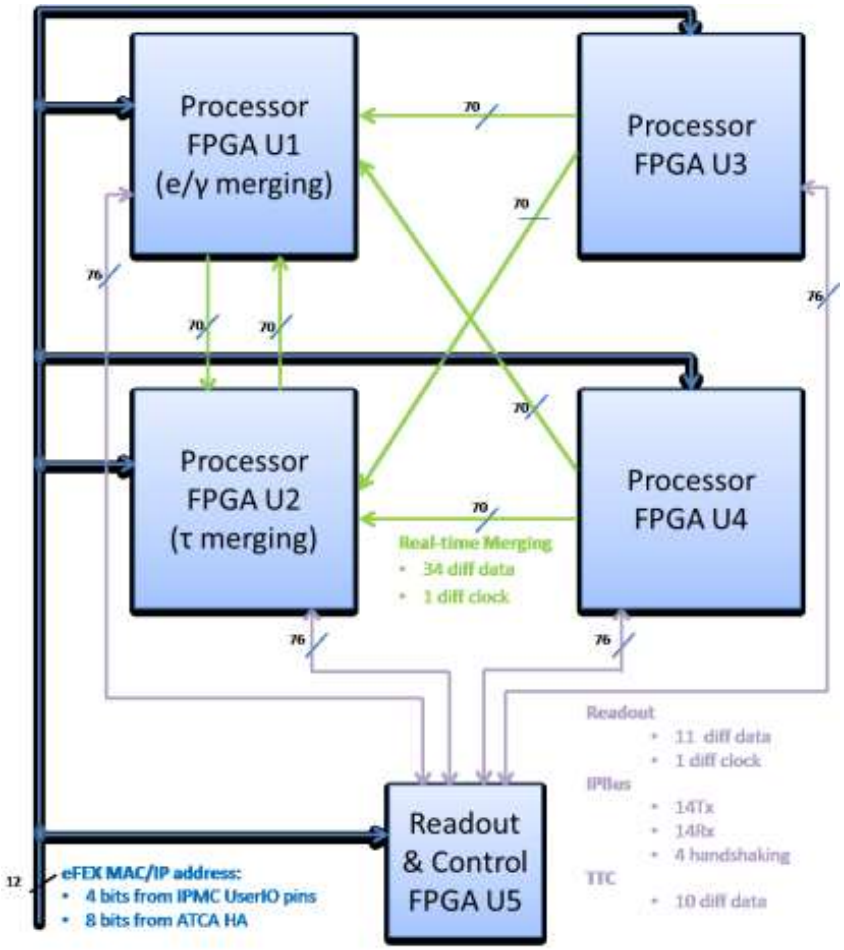




Typical channel 2-D eye scans @11.2 Gbps

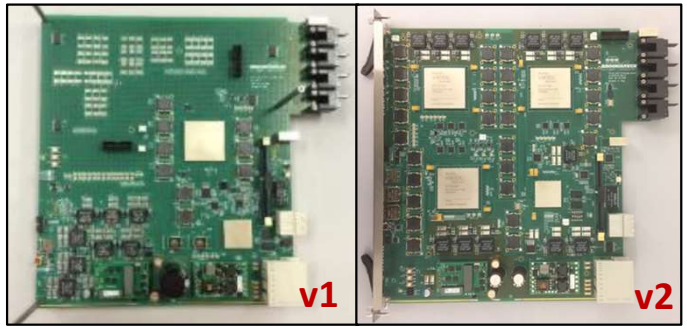
eFEX Test Results (2)

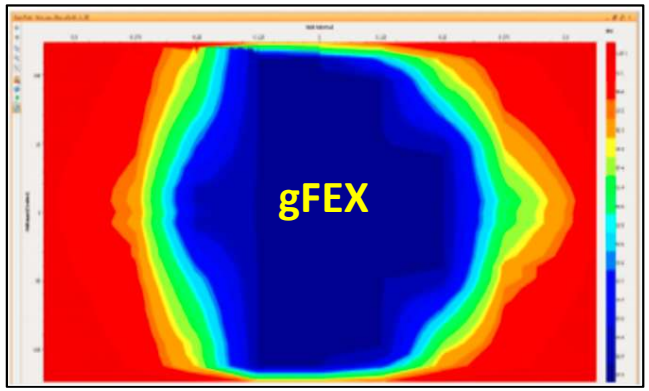
- GPIO tests
  - Dual-star communication
  - Readout & TTC distribution
  - 362 LVDS pairs, >25% error-free margin
- IPBus & IPMC tests
  - All interfaces work properly including basic IPMC functionality
- Power consumption
  - ATCA blade limit: 400 W
  - Measured: ~280 W (all MGTs on)
- Temperature
  - Max 67°C (3 adjacent, fully powered eFEXes)
- Very good results, handful of modifications required for pre-production



gFEX Test Results (1)

- 2 prototype versions manufactured and tested
- Link tests
  - @CERN: with LATOME (LAr)
    - gFEX v1 prototype and partial link (48) tests only
    - FOX demonstrator
    - IBERT PRBS-31, ≤11.2 Gbps, 8b/10b encoding
    - BER < 10^{-14}
    - Faulty links due to bad transmitters
  - @BNL: loopback mode
    - gFEX v1 & v2 prototypes
    - all optical I/O links up to 12.8 Gbps
    - on-board electrical links up to 25.6 Gbps
    - GPIO up to 1.2 Gbps
    - All links stable





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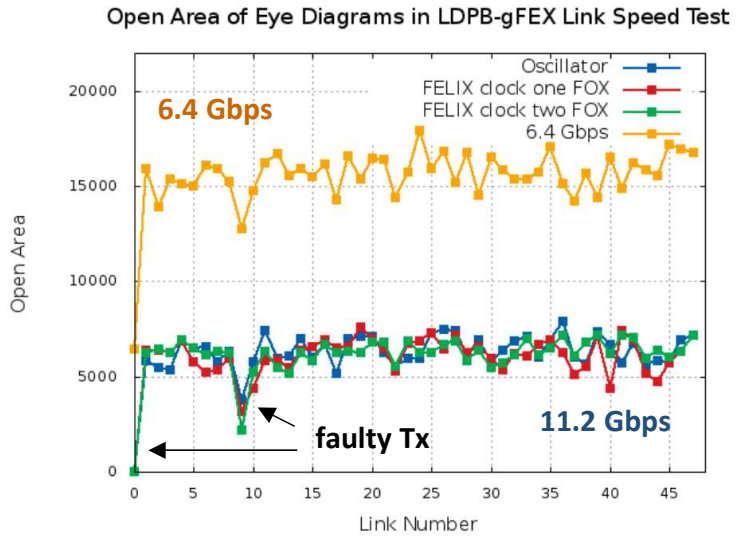
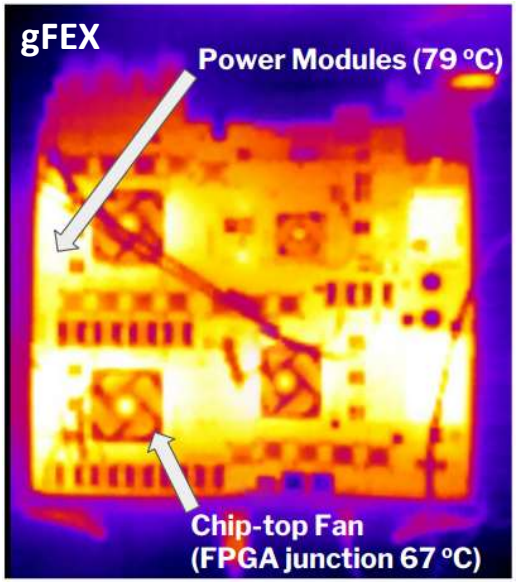
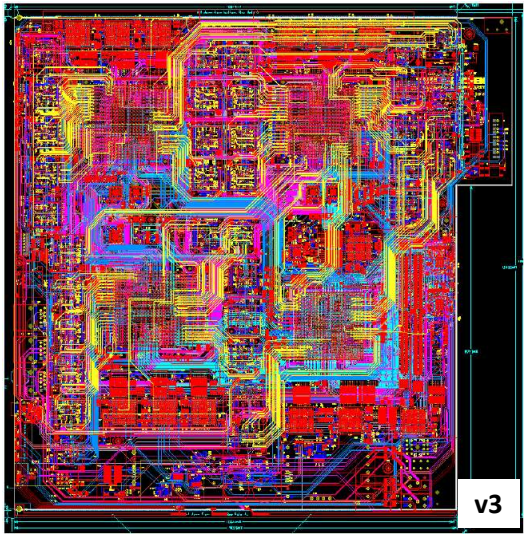


gFEX Test Results (2)

- Integration tests with FELIX (DAQ)
  - Input link : 4.8 Gbps (timing & control)
  - Output links : 9.6 Gbps (event data)
  - All links stable
- IPMC tests
  - Environment set up, tests in progress
- Power consumption & temperature
  - 300 W/module (v2 gFEX, all MGTs enabled)
  - ≤ 80°C (without cooling)
- gFEX pre-production module (v3)
  - 26 → 30 layer PCB
  - 28 → 35 MiniPODs
  - UltraScale → UltraScale+ (Virtex & Zynq)
  - Routing completed, manufacturing to start soon



Measured outside ATCA w/o cooling



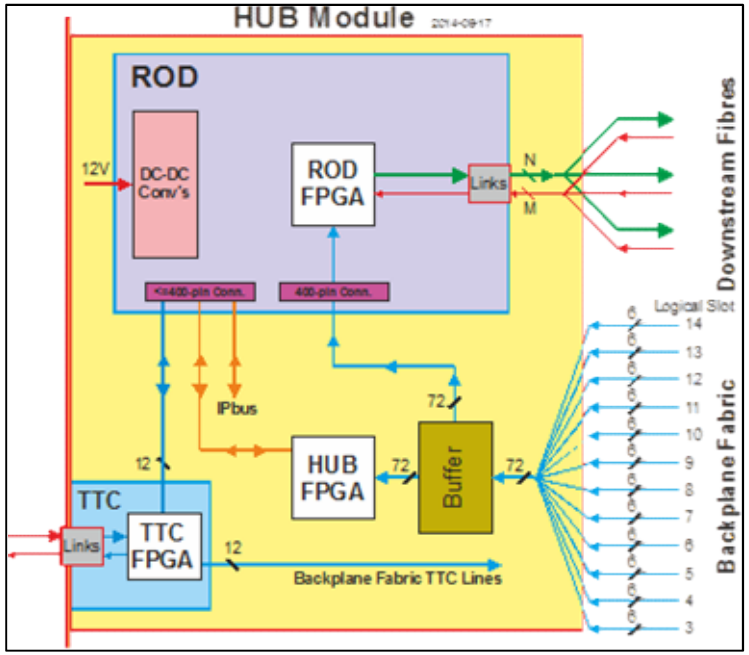
Outlook

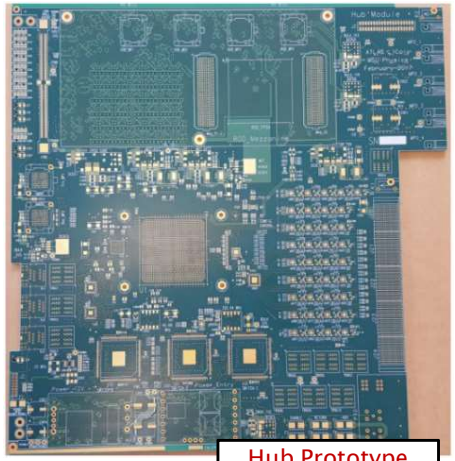
- Prototyping and testing to continue during 2017
  - Next hardware iterations in preparation
  - Main testing at home institutes, joint tests @CERN (with LAr and DAQ)
- Surface test facility @CERN
  - To include all Phase-I L1Calo modules & external source/receiving modules
  - Verify hardware and algorithms
  - Prepare for system integration & commissioning
  - In long-term: testing & debugging platform for Run 3
- Final production to start in 2018
- Underground installation scheduled for 2019
  - After the official end of Run 2
- Integration & commissioning during the entire LHC long shutdown (2019-2021)

BACK-UP

L1Calo Hub

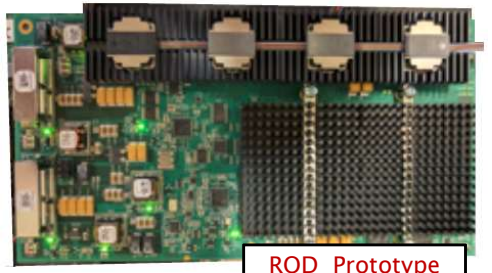
- Control and clock hub in eFEX & jFEX shelves
  - 2 modules per shelf
- FPGA
  - Xilinx Virtex UltraScale
- High-speed links
  - Electrical @6.4 Gbps: 72 inputs, 12 outputs, 2 bidirectional (Hub-to-Hub)
  - Optical @4.8 Gbps: 1 input
- Status
  - Prototypes out for manufacture
  - Firmware in development




Hub Prototype

L1Calo ROD

- Hosted on Hub
- Sends FEX data (RoI & event data) to HLT & DAQ
- FPGA
  - Xilinx Virtex-7
- High-speed links
  - 24 optical links @9.6 Gbps (2 MiniPODs)
- Status
  - Prototypes manufactured and under test (all links ok)
  - Firmware in development


ROD Prototype