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Readout of the upgraded ALICE-ITS

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ABSTRACT

The ALICE experiment will undergo a major upgrade during the second long shutdown of the CERN LHC. As part of this program, the present Inner Tracking System (ITS), which employs different layers of hybrid pixels, silicon drift and strip detectors, will be replaced by a completely new tracker composed of seven layers of monolithic active pixel sensors. The upgraded ITS will have more than twelve billion pixels in total, producing 300 Gbit/s of data when tracking 50 kHz Pb–Pb events. Two families of pixel chips realized with the TowerJazz CMOS imaging process have been developed as candidate sensors: the ALPIDE, which uses a proprietary readout and sparsification mechanism and the MISTRAL-O, based on a proven rolling shutter architecture. Both chips can operate in continuous mode, with the ALPIDE also supporting triggered operations. As the communication IP blocks are shared among the two chip families, it has been possible to develop a common Readout Electronics. All the sensor components (analog stages, state machines, buffers, FIFOs, etc.) have been modelled in a system level simulation, which has been extensively used to optimize both the sensor and the whole readout chain design in an iterative process. This contribution covers the progress of the R&D efforts and the overall expected performance of the ALICE-ITS readout system.

1. Introduction

ALICE is a heavy ion experiment installed at the CERN LHC designed to study strongly interacting matter, in particular the properties of the Quark-Gluon Plasma (QGP). ALICE Collaboration is preparing a major upgrade of the detector that will be installed during the Long Shutdown 2 of the LHC in the years 2019–2020, with the baseline goal of handling 50 kHz Pb–Pb event rate (luminosity $\mathcal{L} = 6 \times 10^{27}$ cm^{-2} s^{-1}) [1].

As part of this program the innermost detector of ALICE, the Inner Tracking System (ITS) [2], will be completely replaced by a new lightweight, high resolution apparatus consisting of seven cylindrical layers of Monolithic Active Pixel Sensors (MAPS). This will improve the impact parameter resolution by a factor of 3 in the transverse plane and by a factor of 5 longitudinally, the overall tracking efficiency and the p_T resolution at low p_T. A new readout system matching the performance of the upgraded ITS is as well under development.

2. System overview

The seven cylindrical layers composing the ITS will be instrumented with identical MAPS. To meet the design pseudorapidity coverage of $|\eta| \leq 1.22$ for 90% of the most luminous region, the layers are organized in three groups with different lengths at different radii (cf. Fig. 1). The three innermost layers are about 30 cm long and positioned at 23 mm, 31 mm and 39 mm radii. The two middle layers (about 80 cm long) are placed at 194 mm and 247 mm radii. The two outermost layers are about 150 cm long and positioned at 353 mm and 405 mm radii. While all layers share the same sensors, the mechanical support and connections layout is different for the innermost three (Inner Barrel) and the outermost four (Outer Barrel).

The total active area of the ITS will be close to 10 m^2, divided into approximately 25 thousand chips of 4.5 cm^2 area each, for a total of 12.5×10^9 binary pixels. The ITS will be able to deliver a maximum data throughput close to 2 Tbit/s, even if for baseline operations this rate drops to about 300 Gbit/s. To minimize the material budget, a combination (buses and cables) of passive electrical links is used to stream the data from the sensors to the Readout Electronics, which is located about 4 m from the end of

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the outermost layers. To simplify maintenance and installation, all connections will be bound to a single side of the detector. The Readout Electronics will distribute control and clock signals to the ITS and manage the data streaming and communication with the Common Readout Units (CRU) in the Counting Room [3] (cf. Fig. 2) using the CERN GBT [4] optical links.

3. Pixel sensor readout

A dedicated R&D program led to the development of monolithic pixel sensors specifically tailored to the ITS requirements of extremely low material budget and power consumption (cf. Table 1). As a result two families of sensors, ALPIDE and MISTRAL-O have been realised using the TowerJazz 0.18 μm CMOS Imaging Sensor process [5]. These chips have the same dimensions (15 mm × 30 mm), as well as identical electrical interfaces and communication protocol. Despite differences in requirements between the Inner and Outer Barrel (cf. Table 1), the goal is to use the same pixel sensor family for both. The ALPIDE family embeds innovative architectural and front end solutions to minimize power consumption and increase speed, while the MISTRAL-O is based on a more conventional rolling shutter architecture specifically modified for the ITS needs. At present the ALPIDE family is the baseline solution, and therefore will be used to illustrate the readout chain.

The ALPIDE chip has a fully digital output and embeds a sparsifying readout architecture (priority encoder) that can work in both triggered and continuous modes. Pixels have a pitch of 28 μm × 28 μm and are arranged in a matrix of 512 rows by 1024 columns. The matrix is logically divided into 32 identical submatrices (regions) of 16 double-columns each. Each single double-column uses an asynchronous priority encoder (cf. Fig. 3) to stream the data from the pixels to the periphery [6]. Data retrieved from the double-columns is first buffered in the peripheral memories, then passed to a serializer and streamed out. There is no free-running clock distributed to the whole matrix, thus greatly reducing power dissipation.

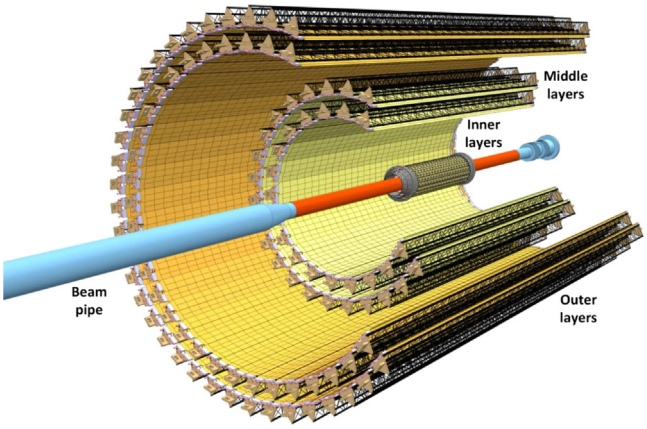

Fig. 1. Layout of the upgraded ALICE-ITS [2].

Within the pixel cell front end the signal from the amplifier is fed into a comparator with programmable threshold (cf. Fig. 4). The relatively long amplifier shaping time (about 5 μs) acts as an analogue memory. The chip readout is performed on a snapshot of the states of all the comparators within the matrix, different from the standard rolling shutter designs. The pixel cell contains three memory elements that can buffer consecutive events to minimize dead time. Data taking is governed by the use of the trigger signal. When it is asserted, the outputs of fired comparators are latched in one of the in-pixel buffers.

In triggered mode of operation the trigger signal is directly connected to the ALICE Central Trigger Processor [3]. On each

Table 1
General requirements for the pixel chip [2].

Parameter	Inner Barrel	Outer Barrel
Silicon thickness	50 μm	50 μm
Spatial resolution	5 μm	10 μm
Chip dimensions	15 mm × 30 mm	15 mm × 30 mm
Max. power density	300 mW/cm^2	100 mW/cm^2
Event time resolution	< 30 μs	< 30 μs
Detection efficiency	> 99%	> 99%
Fake hit rate[a]	$< 10^{-5}$	$< 10^{-5}$
TID radiation hardness[b,c]	2700 krad	100 krad
NIEL radiation hardness[b,d]	1.7×10^{13}	10^{12}

[a] Per pixel per readout frame.
[b] This includes the safety factor of 10, revised values w.r.t. TDR.
[c] Total ionizing dose.
[d] Non-ionizing energy loss (1 MeV n_{eq}/cm^2).

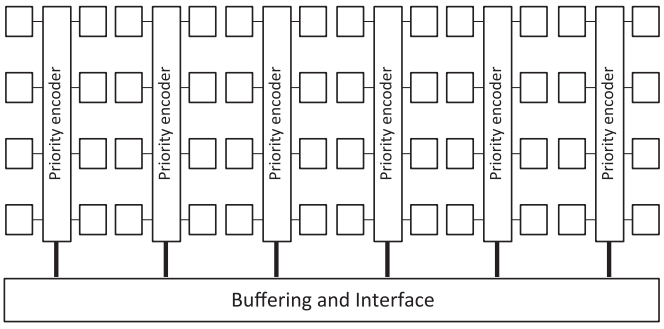

Fig. 3. Sketch of the ALPIDE architecture.

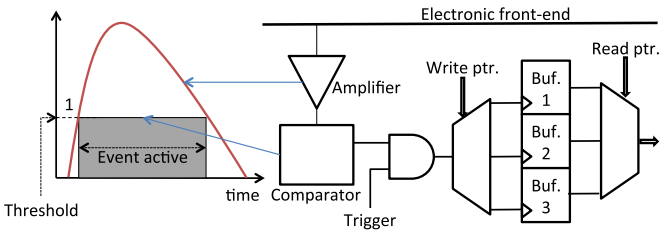

Fig. 4. ALPIDE pixel cell.

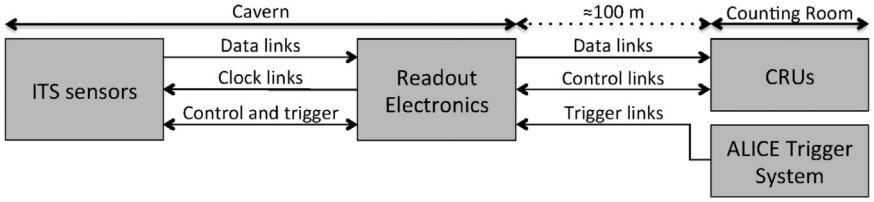

Fig. 2. Architecture of the upgraded ITS readout system.

trigger an acquisition window is opened for a short period of time (about 250 ns), during which the outputs of fired comparators are latched into the pixel buffers. Outside of the acquisition windows, the buffers are insensitive to incoming signals. Physics events closer in time than the amplifier shaping constant may be recorded multiple times (cf. Fig. 5).

In continuous mode of operation the assertion of the trigger is asynchronous from the physics events and managed internally by the sensor with a programmable time base. The acquisition window stays open all the time between two trigger pulses, allowing to record any comparator firing within this time slice (cf. Fig. 6). Similar to the triggered mode, if physics events happen on the boundaries of two acquisition windows, they will be recorded in both corresponding snapshots.

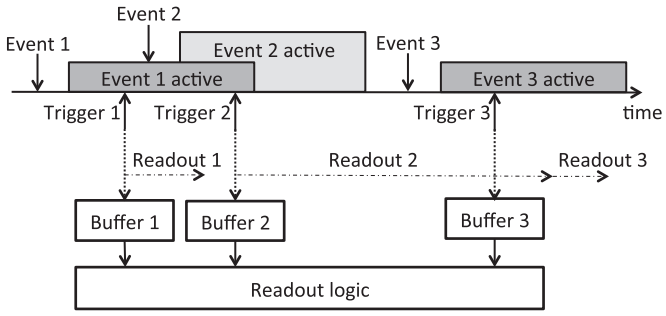

Fig. 5. Principle of the triggered mode of operation.

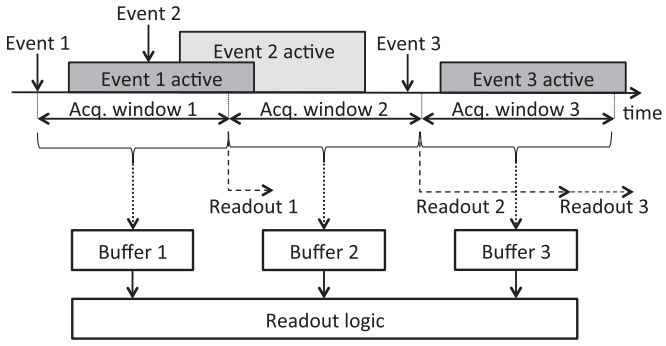

Fig. 6. Principle of the continuous mode of operation.

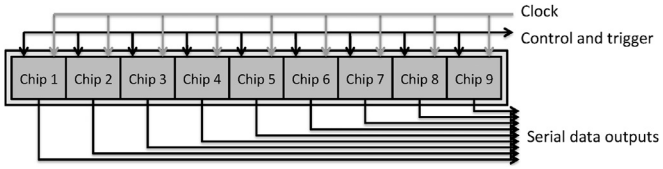

Fig. 7. The Inner Barrel stave readout architecture.

4. Stave readout

As already mentioned, the ITS uses different layout configurations for the Inner and Outer Barrel. In the Inner Barrel sensors are arranged in staves, each one containing nine chips (cf. Fig. 7). Every chip drives a dedicated high-speed serial data line with a bandwidth of 1.2 Gbit/s (including 8b/10b encoding). All the sensors in the stave share clock and control lines in a multidrop topology. The three layers of the Inner Barrel are composed of 12, 16 and 20 such staves respectively.

In the Outer Barrel sensors are grouped in modules, each containing 14 chips arranged in two parallel rows of seven (cf. Fig. 8). For every row (half-module), a master chip handles the communication with the Readout Electronics, receiving the clock and control signals, and streaming the data at 400 Mbit/s with 8b/10b encoding. The remaining six slave sensors are connected to the master using a local shared bus. Like in the Inner Barrel, the master chips of different modules receive control and clock signals in a multidrop topology. It has to be remarked that the master and slave chips, as well as the Inner Barrel chips, are physically identical, simply configured differently. Modules are arranged in half-staves containing four (layers 3 and 4) or seven (layers 5 and 6) of them (cf. Fig. 8). Two half-staves finally form a mechanical self-supporting unit called a stave. In the Outer Barrel layers 3 and 4 are composed respectively of 24 and 30 staves carrying 8 modules each while layers 5 and 6 instead use respectively 42 and 48 longer staves carrying 14 modules each.

5. Readout Electronics

The Readout Electronics will consist of modular units called Readout Units, identical for all the layers. It will operate at the radial distance of 1 m from the beamline and about 4 m away from the outermost ITS layer in a mild radiation environment (Total Ionizing Dose of 10 krad, Non-ionizing Energy Loss of 10^{11}1 MeV n_{eq}/cm^2). Every Readout Unit will read out a single stave in both the Inner and Outer Barrel, for a total of 192 units. Each of them hosts FPGAs to operate the connected sensors and manage the data stream. The data to and from the ITS will be transferred electrically using 5 m Samtec Twinax copper assemblies with twelve differential pairs. In the Inner Barrel a single cable connects each stave to its Readout Unit, while in the Outer Barrel four cables are needed. To communicate with the CRUs in the ALICE Counting Room, the Readout Unit will be equipped with three GBT links (cf. Fig. 9), which will provide a payload of 9.6 Gbit/s for data transmission, 3.2 Gbit/s for receiving

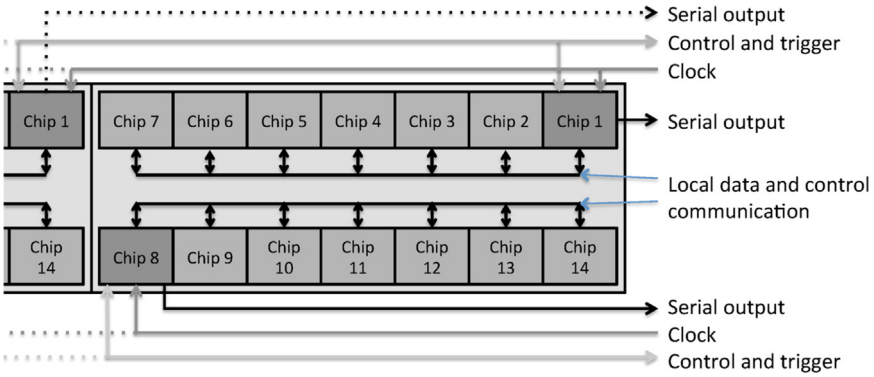

Fig. 8. The Outer Barrel half-stave readout architecture.

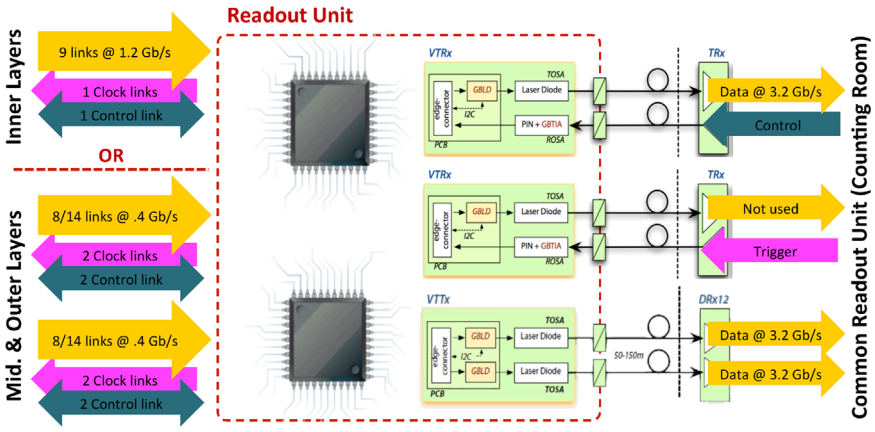

Fig. 9. The architecture of the Readout Unit.

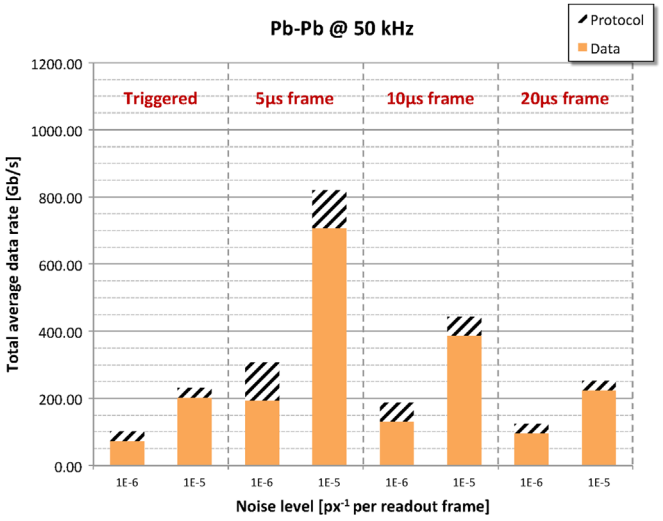

Fig. 10. Expected data rates for Pb–Pb runs at 50 kHz.

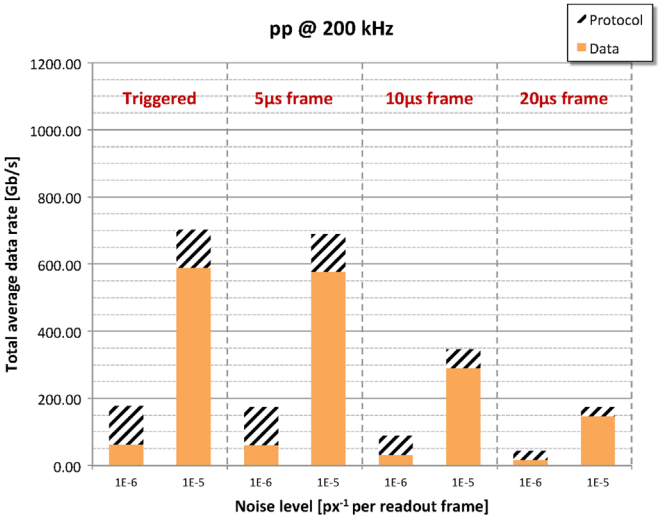

Fig. 11. Expected data rates for pp runs at 200 kHz.

the trigger information and 3.2 Gbit/s for downlink from the Counting Room (configuration and control).

6. Performance simulations

A dynamic SystemC [7] model, simulating all the sensor IP blocks and the transmission lines characteristics up to the Readout Electronics has been implemented to both help to design the sensor and to optimize the whole system topology. Furthermore, it has been extensively used to simulate the ITS performance in various running conditions. The model uses Monte Carlo Pb–Pb and pp physics simulation events as input and delivers clock cycle accuracy in simulating the entire readout process. Together with the physics data, a full parameterization of the sensor (analogue front end, priority encoder timing, buffer size, available bandwidth, noise level, protocol implementation, etc.) allows us to effectively explore and benchmark different design solutions in short time.

The plots in Figs. 10 and 11 illustrate the performance of the optimized final design for two baseline modes of operation, 50 kHz Pb–Pb and 200 kHz pp respectively. The results for two noise values are shown (one of the most stringent parameters for successful system implementation): the worst case situation of 10^{-5} per pixel per readout frame and the more realistic value of 10^{-6} per pixel per readout frame. Each figure reports the results for the triggered mode and three different settings of the continuous mode, with acquisition windows of 5 µs, 10 µs and 20 µs, with the breakdown of data and protocol contributions. A practical limit for the ITS maximum performance comes from the bandwidth allocated to the ITS by the ALICE Online–Offline System [8], which stands at 320 Gbit/s. Data in figures illustrates how the ITS can meet the baseline operation well within this constraint. However, the ITS has been designed to operate at much higher rates than the baseline, the maximum values are listed in Table 2. This opens the opportunity for future luminosity upgrades of ALICE without the need for any major update of the ITS.

Table 2
The maximum interaction rates possible for the upgraded ITS.

Event type	Triggered	5 µs[a]	10 µs[a]	20 µs[a]
Pb–Pb	200 kHz	150 kHz	200 kHz	200 kHz
pp	300 kHz	1 MHz	1 MHz	1 MHz

[a] Acquisition window length in continuous mode.

7. Conclusions and outlook

The ALICE-ITS upgrade is ongoing and final installation is foreseen for the Long Shutdown 2 of the LHC. The R&D effort results show how all the ITS components can match the design

goals, supporting the aggressive decision of going for a fully monolithic tracker. The SystemC simulations proved essential in guiding the full design process, being also able to estimate the ITS performance for conditions far beyond the baseline. The ITS upgrade effort will continue until the end of 2018.

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