AIDA-2020-MS58

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Advanced European Infrastructures for Detectors at Accelerators

Milestone Report

Definition of optical and electrical coupling of readout, interface functionality and DIF design

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13 April 2017

The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

This work is part of AIDA-2020 Work Package **14: Infrastructure for advanced calorimeters**.

The electronic version of this AIDA-2020 Publication is available via the AIDA-2020 web site <http://aida2020.web.cern.ch> or on the CERN Document Server at the following URL: <http://cds.cern.ch/search?p=AIDA-2020-MS58>

Grant Agreement No: 654168

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Horizon 2020 Research Infrastructures project AIDA-2020

MILESTONE REPORT

DEFINITION OF OPTICAL AND ELECTRICAL COUPLING OF READOUT, INTERFACE FUNCTIONALITY AND DIF DESIGN

MILESTONE: MS58

Document identifier:	AIDA-2020-MS58
Due date of deliverable:	End of Month 24 (April 2017)
Report release date:	13/04/2017
Work package:	WP14: Infrastructure for advanced calorimeters
Lead beneficiary:	CNRS
Document status:	Final

Abstract:

Calorimeters for Linear Collider detectors can have up to 100M readout cells. The number of digital readout devices has to be small so that individual components such as Detector InterFace cards, DIF, have to serve up to 10,000 calorimeter cells. DIF cards, optimised in size and power consumption, are developed. The first step documented in this report is the definition of the interfaces and the DIF design. The milestone has been reached by the design and production of prototype boards of the DIF for the Analog Hadron Calorimeter, AHCAL, and the Semi-Digital Hadron Calorimeter, SDHCAL. The status of DIF development for a Silicon-Tungsten Electromagnetic Calorimeter, SiW ECAL, for which the high level integration is particularly challenging, is given.

The Advanced European Infrastructures for Detectors at Accelerators (AIDA-2020) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168. AIDA-2020 began in May 2015 and will run for 4 years.

Delivery Slip

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Authored by	Ch. Combaret M. Reinecke K. Krüger	CNRS-IPNL DESY DESY	30/03/17
Edited by	K. Krüger	DESY	02/04/17
Reviewed by	R. Pöschl [WP coordinator] F. Simon [WP coordinator] F. Sefkow [Scientific coordinator]	CNRS-LAL MPG-MPP DESY	07/04/17
Approved by	Scientific Coordinator		13/04/17

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Executive summary

Highly granular calorimeters designed for Linear Collider detectors require readout electronics integrated into the detector. The large channel count of the detectors means that the individual readout devices like the Detector Interface cards, DIF, need to handle a large number of detector channels and many readout ASICs. On the other hand they have to respect the space and power constraints given by fact that they are located within the detector volume. DIF cards for two hadron calorimeter prototypes for Linear Collider detectors, the SDHCAL and the AHCAL, are developed and a definition on space constraints for the SiW ECAL has been settled.
The design of both DIFs for the hadron calorimeters is well progressed, and prototype boards have been produced. The next steps are tests of the DIFs with the existing calorimeter prototypes in the lab and in beam tests, to demonstrate the viability of the concept. The experience with the prototypes will provide important input for the extrapolation to the full size collider detector (Deliverable 14.6).

1. INTRODUCTION

Calorimeters for Linear Collider detectors are designed for Particle Flow reconstruction algorithms, leading to very high granularity and large channel counts. Two concepts for highly granular hadronic calorimeters, developed within the CALICE collaboration [1], are the SDHCAL, based on Resistive Plate Chambers (RPCs), and the AHCAL, based on scintillator tiles read out by Silicon Photomultipliers (SiPMs). The SIW ECAL, with silicon as active element and tungsten as absorber, is much more compact than the hadron calorimeter. In addition, in a final detector it will be situated inside the hadron calorimeters leading to tight space constraints. All these calorimeters require readout electronics integrated into the active layers of the detector. One central component of the frontend electronics is the DIF card that provides the interface between the very frontend readout electronics of a layer and the outside. Since the DIFs are located inside the detector volume, compactness and low power consumption are important features.

All calorimeters develop new DIFs. Those of the AHCAL and the SDHCAL groups are in a more advanced state. Since the DIFs fulfill similar tasks, and both calorimeters use readout ASICs from the ROC family [2] developed by the OMEGA microelectronics, the requirements for the two DIFs are similar. Nevertheless, they differ in some aspects: the granularity of the calorimeters is different; the readout ASICs need a different communication protocol; the foreseen location of the DIFs inside the main collider detector differ leading to different space constraints; and the AHCAL has an LED calibration system that the SDHCAL does not have because of the different active technology. For the SiW ECAL a DIF has been used in beam tests, however its dimensions are not compatible for use in a compact detector.
The new DIFs are designed to be able to handle the layer sizes and data volumes foreseen in a collider detector like the International Large Detector (ILD). They will be used in tests of prototype detectors in the lab and in beam tests, which will provide important feedback for the design of the collider detector electronics.

2. AHCAL DIF

The AHCAL DIF is one of three interface boards, that connect an active layer of the AHCAL to the DAQ and external power the supply: the DIF providing the DAQ interface, the POWER board providing the interface to the power supply, and the CALIB board providing the functionalities for the LED calibration system. A set of mostly passive interface boards (Central Interface Board CIB and Side Interface Board SIB) hosts the DIF, POWER and CALIB boards and provides the connection to the readout boards, the HBUs (Hcal Base Unit).

The AHCAL DIF can handle up to 18 HBUs, arranged in 3 slabs of 6 HBUs connected in series. The DIF controls up to 72 SPIROC2[2] readout ASICs with up to 2592 readout channels. The communication is split into 6 parallel open collector lines (2 per slab), handling a maximum of 12 ASICs each.

The AHCAL DIF connects to the DAQ system via an intermediate board, the Link Data Aggregator (LDA). The communication between the LDA and the connected DIFs is handled on HDMI cables with a custom communication protocol. The DIF receives the ASIC configuration data and local DAQ commands from the LDA, and sends the data collected from the ASICs to the LDA. For debugging purposes a USB2 interface is provided. The HDMI and USB connectors are housed on the CIB.

The AHCAL DIF receives a common 40 MHz clock from the LDA by a dedicated line pair on the HDMI connection, and derives the 5 MHz slow clock that is needed for the SPIROC2 ASICs. For debugging purposes, it can also generate these clocks.

The AHCAL DIF houses a Xilinx Zynq XC7Z020-1CLG484I that includes an FPGA and an ARM9 microcontroller.

To meet the compactness requirements of the ILD detector, the AHCAL DIF is limited in size to 9.4 x 8.1cm². The total height of CIB, DIF and external cooling plate is limited to the layer spacing pitch of 2.55 cm.

The AHCAL DIF has been designed (for a more detailed description see [3]), and a prototype production run has been completed (see Figure 1). The produced DIFs have been tested successfully. A larger production run is planned, and the produced DIFs will be used in different AHCAL beam test prototypes to evaluate their performance.

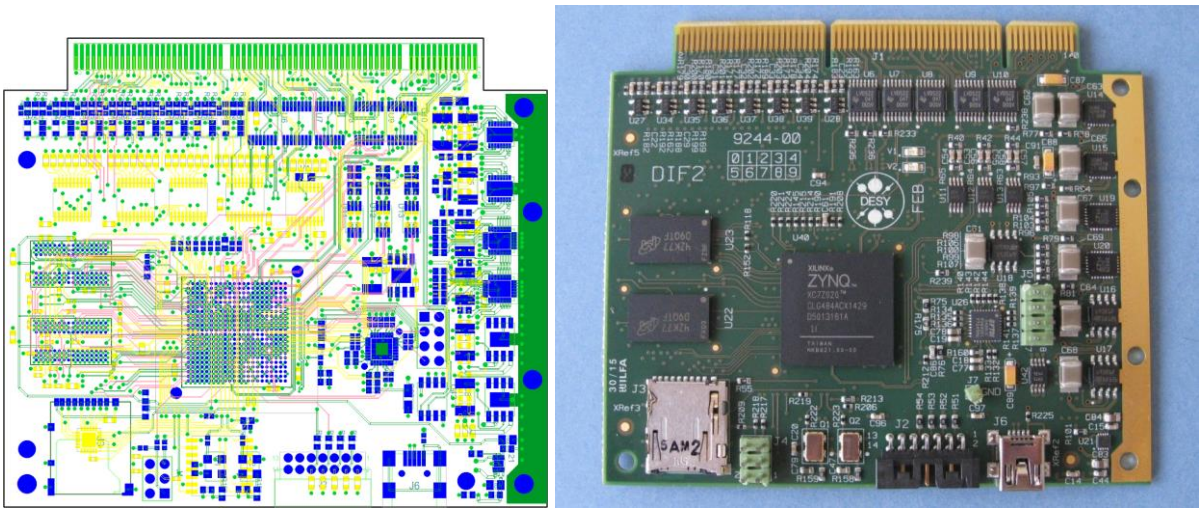

Figure 1: Layout (left) and photo (right) of the AHCAL DIF

3. SDHCAL DIF

The SDHCAL DIF is designed to be the interface board between the ASU board (Active Sensors Unit) that embeds the HARDROC3[2] readout ASICs and the back-end board (connected to the DAQ software). The DIF can also assure the direct interface to the DAQ software.

The SDHCAL DIF controls the ASICs configuration through redundant I2C, triggers the ASICs readout and sends data to the DAQ boards and /or DAQ software according to the global detector finite state machine.

The SDHCAL DIF can handle up to 432 HARDROC3 ASICs (for a 1x3 m^2 detector) with up to 27648 readout channels. For speed and reliability reasons, the communication with the ASICs has been split over 12 parallel lines of maximum 36 ASICs each. For each line, the ASIC configuration and the ASIC readout are on separated dedicated lines (both doubled for redundancy, two I2C busses for configuration and two open collector serial links for data readout).

A block diagram representing all functionalities of the SDHCAL DIF is given in Figure 2.

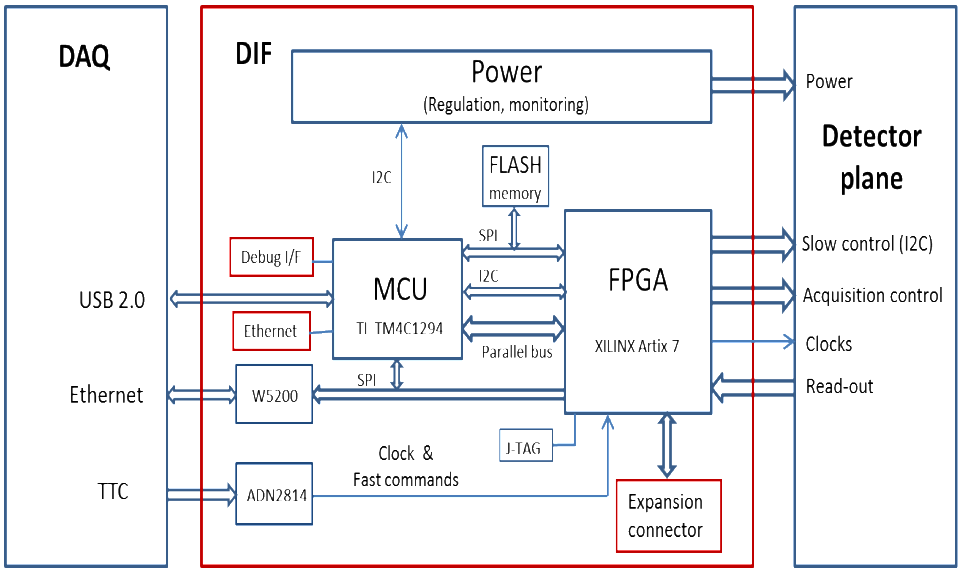

Figure 2: block diagram of the SDHCAL DIF functionalities

The SDHCAL DIF is developed with both a FPGA and a MCU to ensure communication with both ASICs and back-end boards (using GBT link) or DAQ software (using Ethernet link).

The SDHCAL DIF receives clock and synchronous commands from the central detector system or via a TTC (CERN standard Time, Trigger and control) optical link or via a GBT link (LHC upgrade standard optical link). This ensures all ASICs are in phase and take data at the same time.

The SDHCAL DIF receives all ASICs configuration data and local DAQ commands either from a local TCP-IP interface or from the GBT link (in this case, the DAQ software communicates with the back-end board instead of communicating directly with the SDHCAL DIF). In the same way, data coming from the ASICs are sent or to the DAQ software through the TCP-IP interface or to the back-end board through the GBT link. A USB2 interface is integrated for debugging purposes.

The SDHCAL DIF has to take into account several constraints:
- To meet the compactness requirements of the ILD detector, the SDHCAL DIF has to be minimal (or little) space consuming and to be as close as possible to each ASIC line. Therefore, it has been designed to measure 70x6 cm^2.
- As all connectors to the ASICs have to be on the same side of the detector, the DIF has to provide low voltage to all ASICs with which it communicates. The peak power consumption of all ASICs has been estimated to be 93 W. As the ASICs can be power pulsed (to limit power consumption, ASICs hibernate between beam spills), the DIF embeds super-capacitors supplying the peak power when needed within a limited global power budget.

First SDHCAL DIFs were recently produced. The DIF firmware to control the different functionalities of the DIF is being developed.

4. SIW ECAL DIF

The concept of the SiW ECAL calls for up to 13 ASU to be configured, supplied with low voltage and read out via the DIF. Each of the ASUs has 1024 channels.
As a first step towards deliverable D14.6 the geometrical constraints for the DIF have been settled: in e.g. the ILD Detector the DIF is to be installed between the ECAL and the HCAL which are separated by only 67 mm including 25 mm mechanical tolerance. In the other dimension, the DIF has to be less than 70 mm in size, as the cooling of the detector electronics takes up the remaining space. The constraints are coupled to the work package WP14.5 and are coordinated.
The DIFs used so far successfully in beam tests, are connected by an adapter card of around 180x500 mm^2 in size to the actual detector. Also this adapter card will have to be reduced to a size of 180x10 mm^2 and will most likely be integrated into the DIF.
The development of new hardware will start out now from the existing DIF and will take advantage where possible of the work done for the hadron calorimeters. The coordination will be assured by meetings of the work package WP14 and within the CALICE collaboration.
The schedule aims for the demonstration of the concept with layers of the SIW ECAL prototype during 2018, being thus in phase with the timeline for the deliverable D14.6.

5. CONCLUSION

Highly granular calorimeter, such as the SDHCAL and the AHCAL concepts developed for Linear Collider detectors, need integrated readout electronics to cope with the huge number of readout channels. Within WP14, Detector Interface cards, DIFs, are developed that can handle several thousand channels, while respecting stringent space and power requirements. DIFs for both calorimeter concepts have been designed, and prototypes have been produced. The next steps include the test of both DIFs with the respective calorimeter prototypes in the lab and in beam tests. These tests under realistic conditions will provide necessary input for the extrapolation to the full size collider detector (Deliverable 14.6).

REFERENCES

[1] CALICE Collaboration, https://twiki.cern.ch/twiki/bin/view/CALICE/WebHome.
[2] S. Callier *et al., ROC chips for imaging calorimetry at the International Linear Collider*, JINST 9 (2014) C02022
[3] M. Reinecke, AIDA-2020 note in preparation

ANNEX: GLOSSARY

Acronym	Definition
ASU	Active Sensor Unit: basic detector unit in the SDHCAL
DIF	Detector InterFace Board between the active detector layers and the DAQ
HBU	HCAL Base Unit: basic detector unit in the AHCAL
MCU	MicroController Unit