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CMOS LOW NOISE MONOLITHIC FRONTENDS FOR Si STRIP DETECTOR READOUT

P. Aspell[1], R. Boulter[2], A. Czermak[3], P. Jalocha[3], P. Jarron[1], A. Kjensmo[4], W. Lange[1], E. Nygård[1], A. Rudge[1], O. Toker[1,2], M. Turala[3], H. Von Der Lippe[4], U. Walz[5], P. Weilhammer[1] and K. Yoshioka[1]

ABSTRACT

A brief summary of first tests of several monolithic frontend chips is presented. They are designed for readout of silicon strip detectors and have in common that they are all based on the same charge-sensitive preamplifier / shaper configuration, for which the main design goal was the lowest possible noise at low power consumption. Measurements show that low-noise levels of ENC = 165 e^- + 12 e^- / pF have been reached.

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1) CERN, Geneva, Switzerland
2) SEFT, Helsinki, Finland
3) Institute of Nuclear Physics, Cracow, Poland
4) Senter for Industriforskning, Oslo, Norway
5) Fachhochschule, Heilbronn, Germany

1. INTRODUCTION

The quality of tracking systems with Si strip detectors, which aim for very good spatial resolution, depends to a large extent on the noise performance of the frontend monolithic amplifier. Based on the design of a continuously sensitive charge-sensitive preamplifier and shaper system, using a cascode configuration with capacitive and resistive feedback, a number of circuits have been developed for very low noise Si strip detector readout. Besides some prototype circuits, two full-size 128 channel readout chips have been designed, built and tested. One chip is a general purpose readout chip for Si vertex detectors, the other chip is meant for applications which need self-triggering capability, in particular for γ-ray and X-ray detection.

In this article, an overview on first results on the performance of these circuits is presented, with emphasis on noise performance.

2. THE PROTOTYPE CIRCUIT

The basic structure of the CMOS charge-sensitive preamplifier / shaper, which is used as the main building block for different VLSI chips discussed throughout this article, is based on the AMPLEX-principle [1], as shown in Fig. 1.

Measurements have shown that with this design it was possible to closely approach the theoretical low-noise limit, determined by the inherent channel white noise only and given by the expression [2,3]

$$ENC = \frac{C_t e}{q}\sqrt{\frac{\Gamma(\eta+1)kT}{3g_m T_p}} \qquad (1)$$

where :

C_t	is the total input capacitance
e	is the base of the natural logarithm
q	is the electron charge
Γ	is the excess noise factor
η	is the ratio between the bulk to channel and gate to channel transconductance of the input transistor
g_m	is the transconductance of the input transistor
kT	is Bolzmann's constant times temperature
T_p	is the shaper peaking time.

A detailed description of the performance of a first prototype chip containing this design is given in [3]. See Section 7 for some results.

3. PERFORMANCE OF THE PROTOTYPE CIRCUIT WITH A Si DETECTOR

The prototype chip with a charge-sensitive amplifier, shaper and hold system has been connected to a Si strip detector and also to Si diodes with 2×2 mm^2 area. An external trigger circuit was added in order to record signals from γ and X-rays in these detectors. The noise performance of this system was calibrated with γ-rays from ^{241}Am and 6 different X-ray sources (Cu, Rb, Mo, Ag, Ba, Tb). X-ray lines from 8 keV (Cu) to 44 keV (Tb) could be observed. Figure 2 shows as an example the energy spectrum of Tb X-rays measured with a Si diode, using the 1 μs channel of the prototype chip. The Kα line (44.2 keV) and the Kβ line (50.7 keV) are clearly distinguished. The width of the lines is in agreement with the expected noise of the system. Figure 3 shows the measured energy for the 7 different sources. The fitted width of the signal peaks is somewhat bigger than the width of the pedestal, partly due to background X-ray signals from Np X-rays from the mother source (Rb, Mo, Ag) and partly due to external noise pickup (Ba, Tb). With reference to the width of the pedestal distrubution, the observed noise is ENC = 280 e^- RMS, in agreement with the expected total load capacitance of 18 pF.

4. A CHIP FOR DETECTION OF X-RAYS AND GAMMAS (Xchip)

This chip is specially designed for reading out silicon strips detecting X-rays and gammas fully absorbed by the detector and therefore in the absence of an external trigger.

A principle outline of a single channel is shown in Fig. 4. It is designed for reading out a double-sided Si strip detector with p- and n-strips parallel to each other.

The first part is an amplifier / shaper stage of the type described, but including two amplifiers in order to read out and add signals both from the p- and the n-side of the detector to enhance the signal over noise ratio.

The last part contains in the upper branch a stretcher circuit and a Sample and Hold to store the peak of the signal, whereas in the lower branch it has a discriminator to generate the trigger.

Figure 5 shows an oscilloscope single shot picture of how a 10 keV signal is found and measured by the system. The upper trace shows the time continuous analogue output. Before the real signal arrives, the output of the stretcher has picked up the highest signal before that, but obviously was below threshold. Then the signal arrives and this peak value is kept. After the signal has reached the peak, the trigger output comes as shown by the second trace. The third trace is an external reset signal.

The channel described was assembled as a 64 channel chip which includes readout facilities, such as trigger output, hit channel address and analogue signal value. See Section 7 for some results.

5. A MULTICHANNEL GENERAL PURPOSE CHIP (Viking)

This chip is designed to achieve optimal performance in resolution. The speed and input capacitance is chosen such that it is well suited for LEP type Si vertex detectors. It consists of 128 channels of the type shown in Fig. 1. Signals in all channels are held simultaneously and all analogue values are read out in a multiplexed serial form.

Special attention was given to the noise performance of the chip. See Section 7 for some results.

Figure 6 shows chip photographs of both the Viking and Xchip.

6. AMPLIFIER / SHAPER FOR USE AT LHC

This prototype chip contains 4 channels with amplifier and shaper also of the same type as in Fig. 1.

The peaking time of this system is 45 ns which is sufficiently fast enough for LHC environments, if it is used together with a special analogue deconvoluting unit [4] which can provide a timing resolution of 15 ns (BCO-time for LHC).

7. RESULTS

Figure 7 shows the measured Equivalent Noise Charge (ENC) for the different chips. The difference is due to difference in peaking times, input transistor width and drain currents. Applying (1) on the measured results indicates that the excess noise factor for this process is : $\Gamma \simeq 1.5$.

Table 1 shows the main parameters and first results on noise performance for the different chips.

REFERENCES

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[3] E. Nygård et al., Nucl. Instrum. Methods A301 (1991) p. 506-516.

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Table 1

Specifications

Process	1.5 μm bulk CMOS (n-well)	
Layout Pitch	47.5 μm	× 2 for Xchip
Peaking Time	1 μs - 1.5 μs 45 ns	Prototype, Viking, Xchip LHC-amplifier
Power Consumption	~ 1.2 mW/chn ~ 3 mW/chn ~ 1.6 mW/chn	Prototype, Viking Xchip LHC-amplifier
Noise Slopes	12 e/pF 17 e/pF 17 e/pF 70 e/pF	Prototype (1.5 μs peaking time) Viking (1.0 μs peaking time) Xchip (1.5 μs peaking time) LHC-amplifier (45 ns peaking time)

Figure Captions

Fig. 1 : Schematic of charge sensitive preamplifier with shaper, sample and hold and buffer.

Fig. 2 : Energy spectrum of Tb X-rays measured with a 2×2 mm^2 Si diode and the prototype amplifier using 1 μs shaping time.

Fig. 3 : Measured energy for 6 different X-ray sources plus Am..

Fig. 4 : Principle of one individual channel of Xchip.

Fig. 5 : Oscilloscope picture of a captured signal in a Xchip channel.

Fig. 6 : Chip photographs of Xchip (right) and Viking (left).

Fig. 7 : Measured equivalent noise charge (ENC) vs. input capacitance for the different chips.

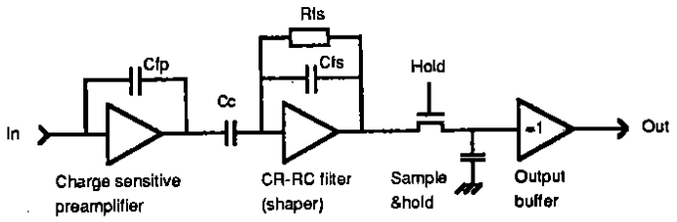

Rfs
Cfp
Cfs
Hold
Cc
In
-1
Out
Charge sensitive
preamplifier
CR-RC filter
(shaper)
Sample
&hold
Output
buffer

Fig. 1

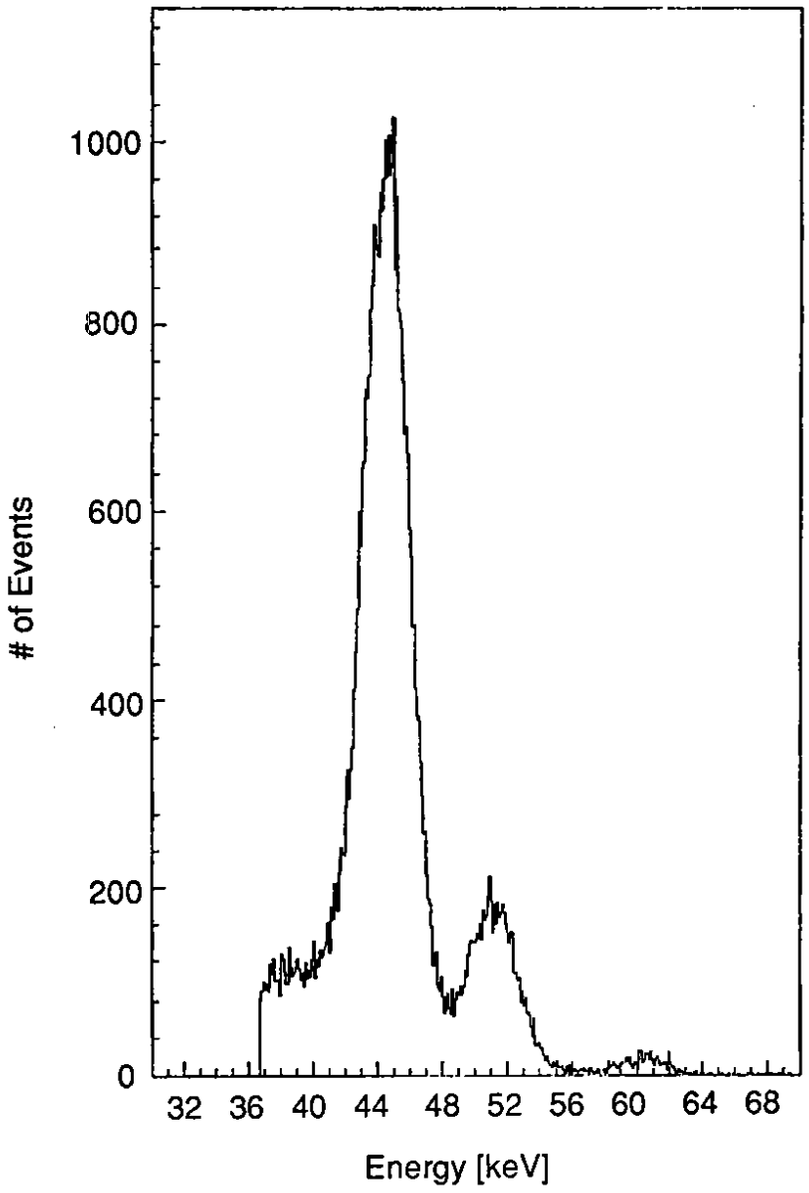

1000
800
600
400
200
0
# of Events
32 36 40 44 48 52 56 60 64 68
Energy [keV]

Fig. 2

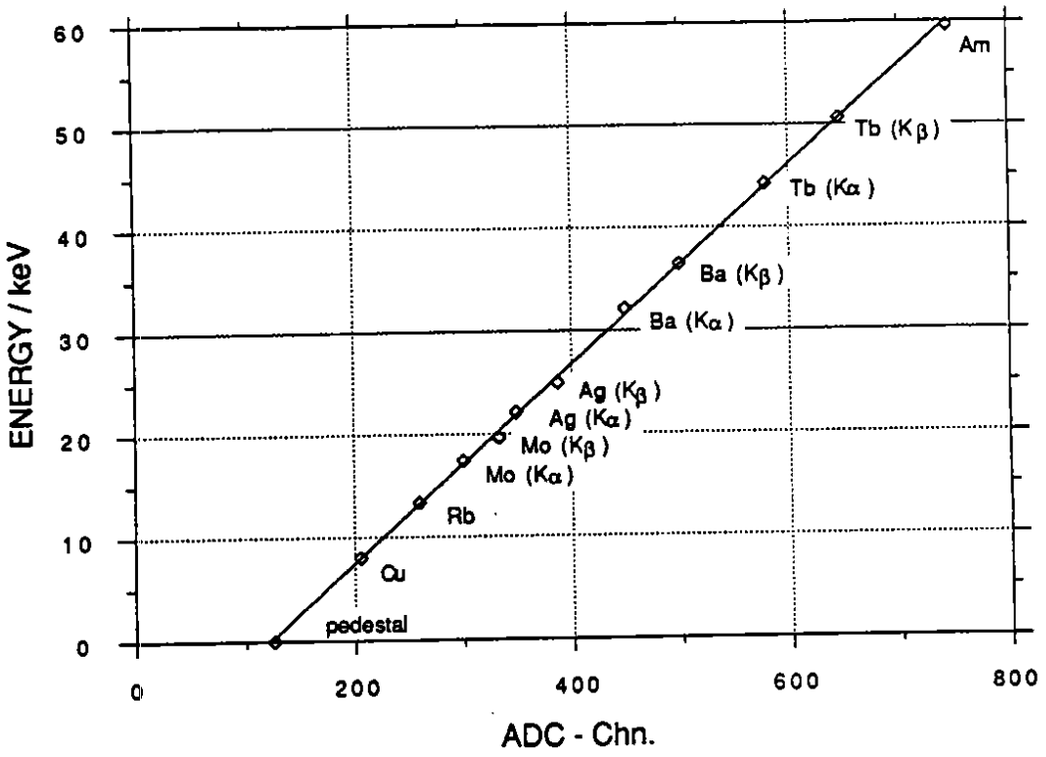

ENERGY / keV
ADC - Chn.
0
10
20
30
40
50
60
0
200
400
600
800
pedestal
Cu
Rb
Mo (Kα)
Mo (Kβ)
Ag (Kα)
Ag (Kβ)
Ba (Kα)
Ba (Kβ)
Tb (Kα)
Tb (Kβ)
Am

Fig. 3

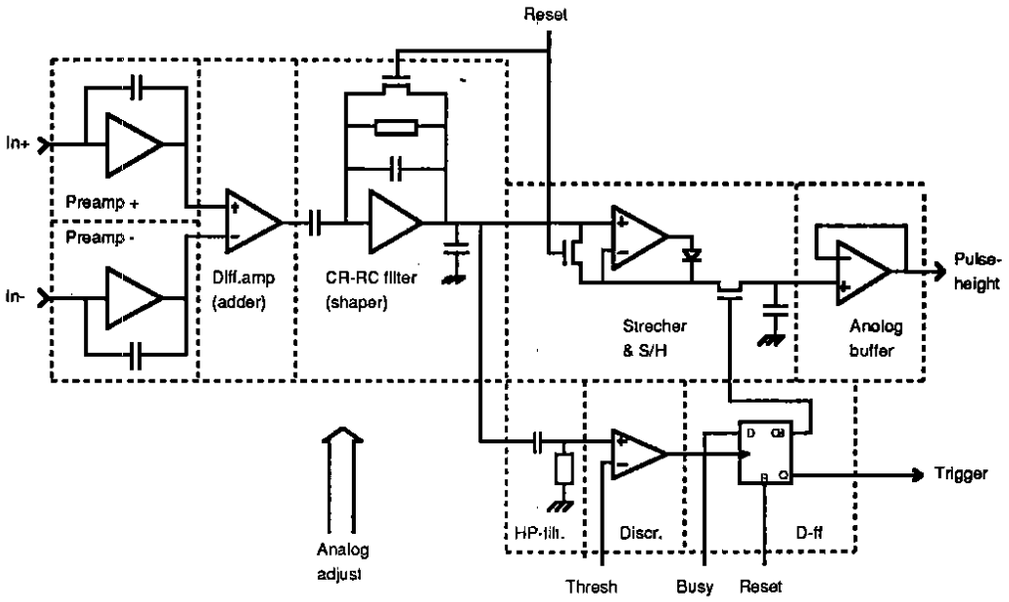
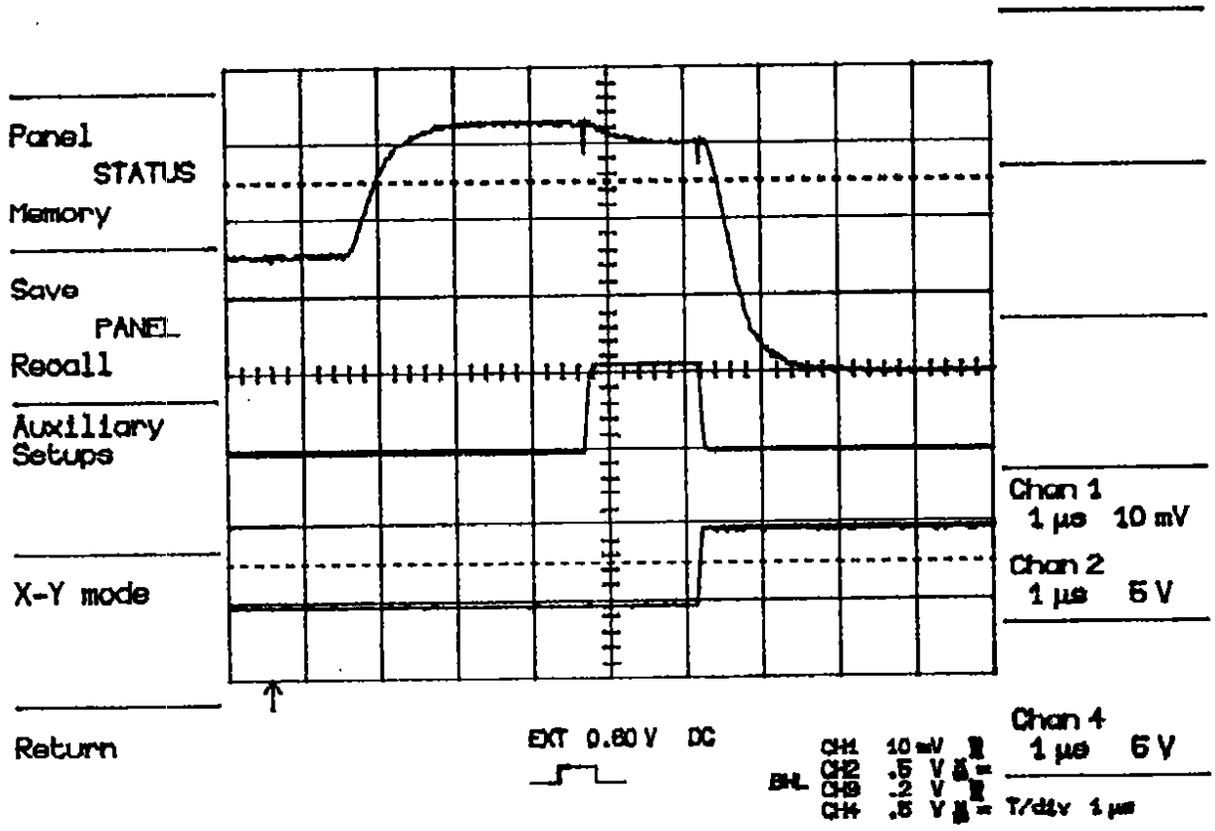

Reset
In+
Preamp +
Preamp -
In-
Diff.amp
(adder)
CR-RC filter
(shaper)
Strecher
& S/H
Analog
buffer
Pulse-
height
Trigger
Analog
adjust
HP-filt.
Discr.
D-ff
Thresh
Busy
Reset

Fig. 4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STATUS
Memory
Save
PANEL
Recall
Auxiliary
Setups
X-Y mode
Return
Chan 1
1 µs 10 mV
Chan 2
1 µs 5 V
Chan 4
1 µs 5 V
EXT 0.80 V DC
CH1 10 mV
CH2 .5 V
CH3 .2 V
CH4 .5 V
T/div 1 µs

Fig. 5

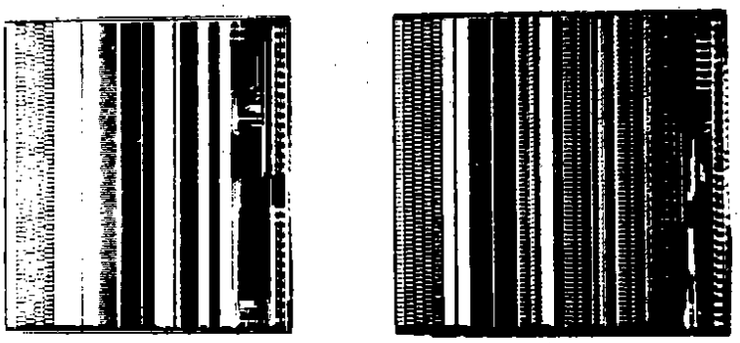

Fig. 6

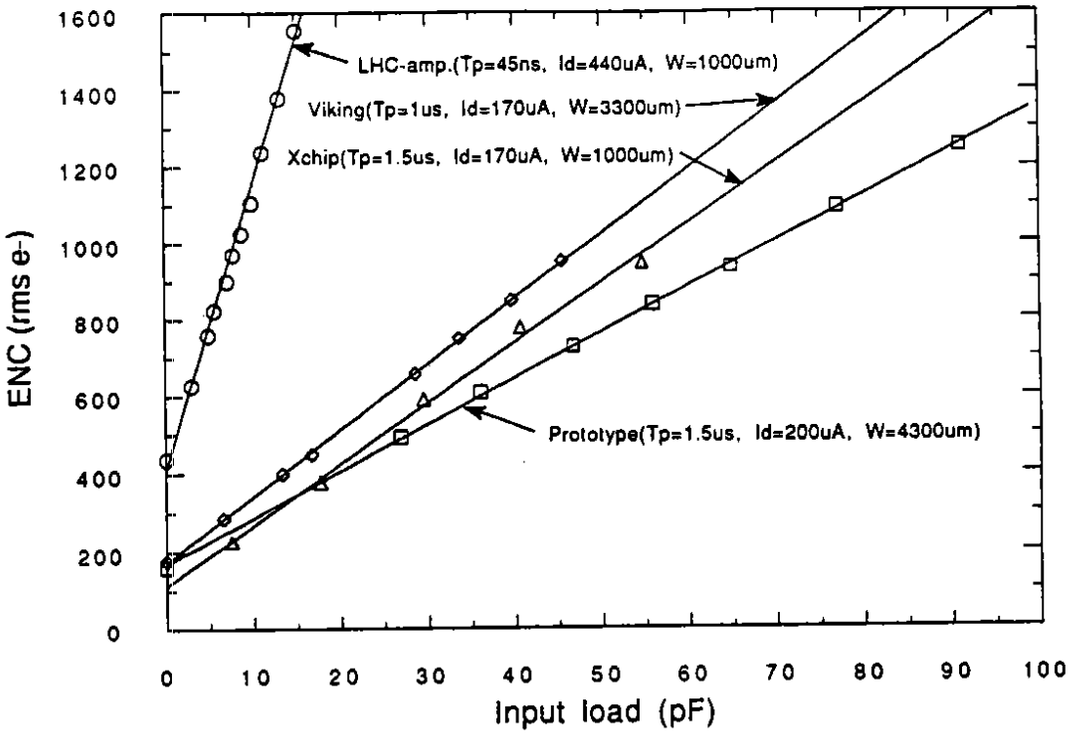

Fig. 7

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