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Front end optimization for the monolithic active pixel sensor of the ALICE Inner Tracking System upgrade

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Abstract: ALICE plans to replace its Inner Tracking System during the second long shut down of the LHC in 2019 with a new 10 m^2 tracker constructed entirely with monolithic active pixel sensors. The TowerJazz 180 nm CMOS imaging Sensor process has been selected to produce the sensor as it offers a deep pwell allowing full CMOS in-pixel circuitry and different starting materials. First full-scale prototypes have been fabricated and tested. Radiation tolerance has also been verified. In this paper the development of the charge sensitive front end and in particular its optimization for uniformity of charge threshold and time response will be presented.

Keywords: Analogue electronic circuits; Pixelated detectors and associated VLSI electronics; Radiation-hard electronics; Electronic detector readout concepts (solid-state)

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1 Introduction

The ALICE Inner Tracking System (ITS) at CERN will be replaced with an entirely new detector during the second long shutdown of the LHC in 2019 [1]. The objectives of the upgrade are to improve the impact parameter resolution by a factor 3, improve the standalone tracking efficiency and p_T resolution, and increase the readout rate capability to exploit Pb-Pb interactions at 50 kHz and proton-proton interactions at 1 MHz. The new layout has 7 detection layers with the innermost layer radius of 22 mm. The total sensitive surface of $\sim 10\,\mathrm{m}^2$ is covered by 12.5 Gpixels to achieve a spatial resolution of $\sim 5\,\mu$m. The reduction of material budget X/X_0 from 1.14 to 0.3% reduces the multiple scattering that would otherwise deteriorate tracking resolution, especially in the low momentum region.

The pixel chip requirements are shown in the table 1. The ALICE PIxel DEtector (ALPIDE) development targets to reduce power density well below 100 mW/cm^2 and integration time much shorter than 30 μs. The requirements of a thin sensor ($< 50\,\mu$m), high granularity ($30 \times 30\,\mu\mathrm{m}^2$), large area (15 mm×30 mm) and moderate radiation tolerance with respect to other LHC experiments make this application an ideal case to fully benefit from the advantages of the monolithic active pixel sensor technology. The TowerJazz 180 nm CMOS imaging sensor process has been selected for the pixel chip implementation.

Figure 1 shows the process cross-section where the sensor and readout electronics are integrated in the same silicon die. The charge collection is performed by the nwell and p-epi junction diode. The spacing between nwell and surrounding pwell reduces the sidewall junction capacitance. A special feature of this technology is the deep pwell to shield the PMOS nwell from the epitaxial layer, thus preventing it from collecting signal charge in place of the nwell collection electrode.

Table 1. Pixel chip requirements

Parameter	Value
Chip Size	15 mm × 30 mm
Silicon thickness	50 μm
Pixel Size	O(30 × 30) μm^2
Readout Time	< 30 μs
Power density	< 100 mW/cm^2
Detection efficiency	> 99%
Fake hit rate	< 10^{-5} per readout frame and pixel
TID radiation hardness	2.7 Mrad
NIEL radiation hardness	1.7×10^{13} 1MeV n_{eq}/cm^{-2}

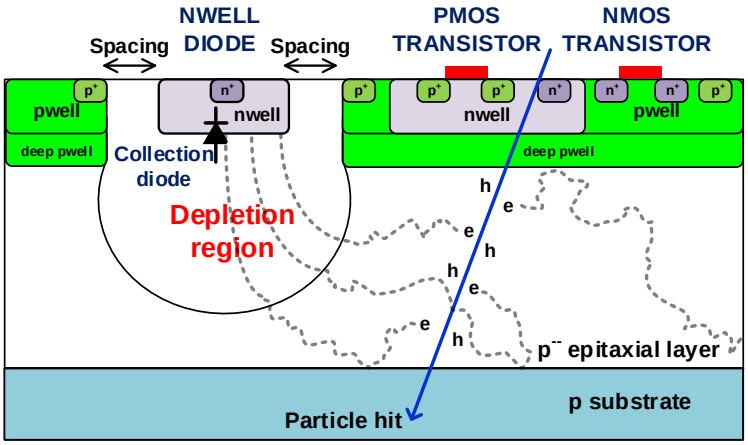

Figure 1. Cross section of the TowerJazz 180 nm CMOS imaging process.

This allows for PMOS transistor implementation at the pixel level, widening the architecture choice for the in-pixel circuit. It is possible to apply a reverse substrate bias votlage via the substrate to increase the depletion region volume and reduce the collection diode junction capacitance. The foundry provides the possibility to select the wafer starting material epitaxial layer thickness in the 18 μm to 40 μm range and a resistivity value between 1 kΩ and 8 kΩ. The gate oxide thickness of 3 nm provides a good Total Ionizing Dose (TID) tolerance [2, 3].

The R&D on monolithic pixel sensors started in 2011 with the design and characterization of small-scale prototypes for sensor optimization and radiation tolerance verification. Subsequently full-scale prototypes (pALPIDE) with a size of 3.0 × 1.5 cm^2, containing 1024 × 512 pixels were submitted [4–6]. The first two versions, pALPIDE-1 and pALPIDE-2, have been successfully tested and they satisfy the ALICE ITS requirements. The third version, pALPIDE-3, with all final functionalities for the detector integration, just came from foundry in October 2015. This paper addresses the development of the charge sensitive front end and in particular its optimization for charge threshold and time response uniformity.

2 ALPIDE principle of operation

2.1 In-pixel hit discrimination

The ALPIDE architecture is based on in-pixel hit discrimination and zero suppression readout by priority encoding [7]. The simplified block diagram and signal flow of the in-pixel circuit are shown in figure 2. The charge signal is integrated at the input node PIX_IN with a typical collection time of $\sim$ 10 ns. The PIX_IN voltage signal amplitude is equal to the ratio of the collected charge Q_{IN} to the total input capacitance C_{IN}. The reset circuit restores the input baseline voltage level within a time of around 1 ms. It also provides compensation for the sensor leakage current which is expected to be below 2 pA. The signal is amplified by the front-end that acts as a delay line with a peaking time of around 2 μs. The discriminated output OUT_D is put in coincidence with the STROBE signal, allowing the latching of the hit information in the multi event buffer memory. The data is readout by a hit-driven architecture that has activity only when there are stored hits.

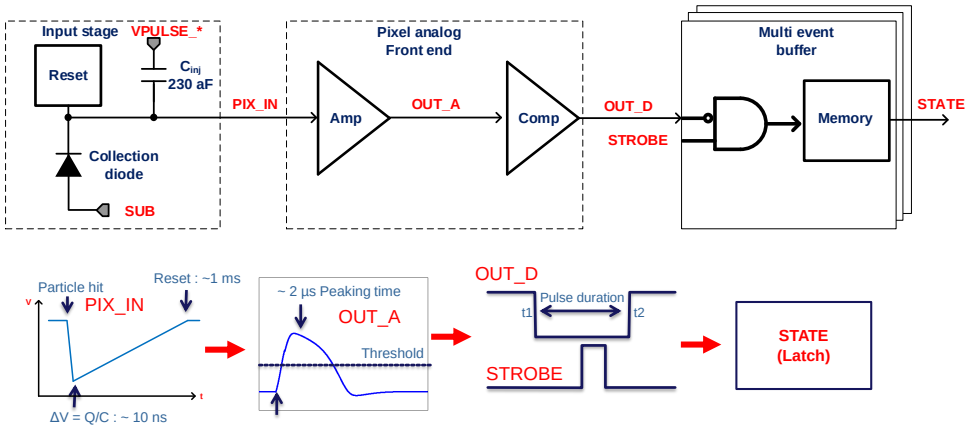

Figure 2. In-pixel hit discrimination block diagram and signal flow.

2.2 Sensor configuration and reset

The sensor input node circuit layout, cross-section and schematic are shown in figure 3. The collection nwell electrode has an octagonal shape with 2 μm diameter and an nwell to pwell spacing between 2 μm and 4 μm. The sensor reset could be provided either by a diode or a PMOS. The reset diode with a p^+ implant in the collection nwell is very compact, but the drawback is that the reset current depends on the sensor leakage current and signal amplitude. The reset PMOS requires a larger area and has a larger contribution to the input capacitance. The advantage is that the PMOS conductance is controlled by the bias current IRESET, larger than sensor leakage current. The variations on collection electrode geometry and sensor reset are implemented in different sectors of the pixel chip prototype.

2.3 Pixel analog front end

The working principle of the in-pixel analog front-end (figure 4a) is based on charge transfer from a large capacitance to a small capacitor to generate voltage gain. The charge signal creates a negative

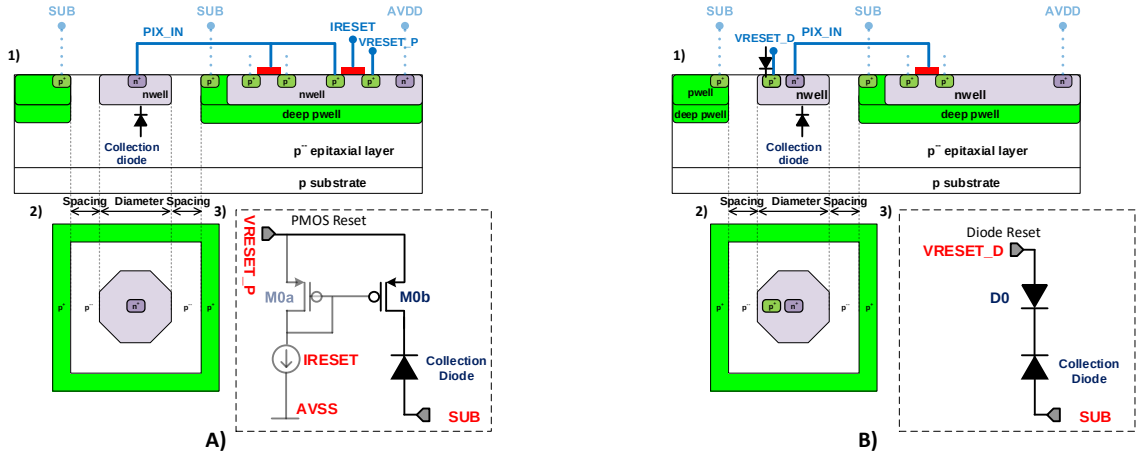

Figure 3. Input stage 1) cross-section, 2) top view and 3) schematic: reset A) PMOS B) Diode.

voltage step $\Delta V_{\mathrm{PIX\_IN}} = Q_{\mathrm{IN}}/C_{\mathrm{IN}}$ at the input node PIX_IN. The transistor M1 with current source IBIAS from VDDA acts as a source follower, forcing the source voltage to follow the M1 gate voltage. This causes transfer of charge $Q_{\mathrm{source}} = C_{\mathrm{source}} \cdot \Delta V_{\mathrm{PIX\_IN}}$ from C_{source} to $C_{\mathrm{OUT\_A}}$ in case the current sink to GNDA is IBIAS. So ideally $\Delta V_{\mathrm{OUT\_A}}$ is:

$$\Delta V_{\mathrm{OUT\_A}} \approx \frac{Q_{\mathrm{source}}}{C_{\mathrm{OUT\_A}}} = \frac{C_{\mathrm{source}} \Delta V_{\mathrm{PIX\_IN}}}{C_{\mathrm{OUT\_A}}} = \frac{C_{\mathrm{source}}}{C_{\mathrm{OUT\_A}}} \Delta V_{\mathrm{PIX\_IN}} = \frac{C_{\mathrm{source}}}{C_{\mathrm{OUT\_A}}} \frac{Q_{\mathrm{IN}}}{C_{\mathrm{IN}}} \tag{2.1}$$

Therefore, a large voltage gain is obtained if $C_{\mathrm{SOURCE}} \gg C_{OUTA}$.

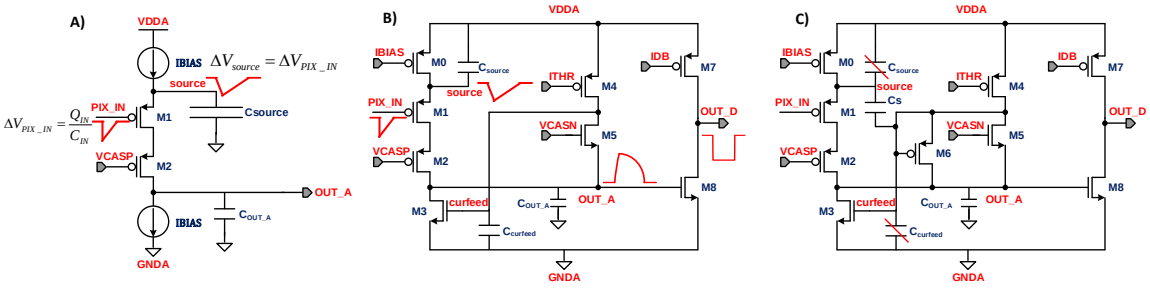

Figure 4. Pixel front end schematic A) principle B) practical implementation C) presented circuit.

The circuit practical implementation is shown in figure 4b. A second branch (M4, M5) is used to generate a low frequency feedback: the curfeed net, loaded with C_{curfeed} capacitance and connected to the gate of M3 is adjusted for M3 to absorb IBIAS+ITHR current. The voltage bias VCASN and current bias ITHR define the baseline value of OUT_A and the return to baseline after a particle hit. OUT_A controls the gate of the second stage input transistor M8, and the baseline is defined such that $I_{\mathrm{M8}} < IDB$. The distance of the OUT_A baseline voltage to the point where $I_{\mathrm{M8}} = IDB$ defines the charge threshold. If OUT_A voltage level is higher than the threshold point $I_{\mathrm{M8}} > IDB$, the discriminated active low output on OUT_D is generated. Transient plots for OUT_A and OUT_D are shown in figure 5.

All transistors in the front-end work in weak inversion, where the nominal values for the current bias parameters are IBIAS = 20 nA and ITHR = 0.5 nA. This allows to achieve a power consumption

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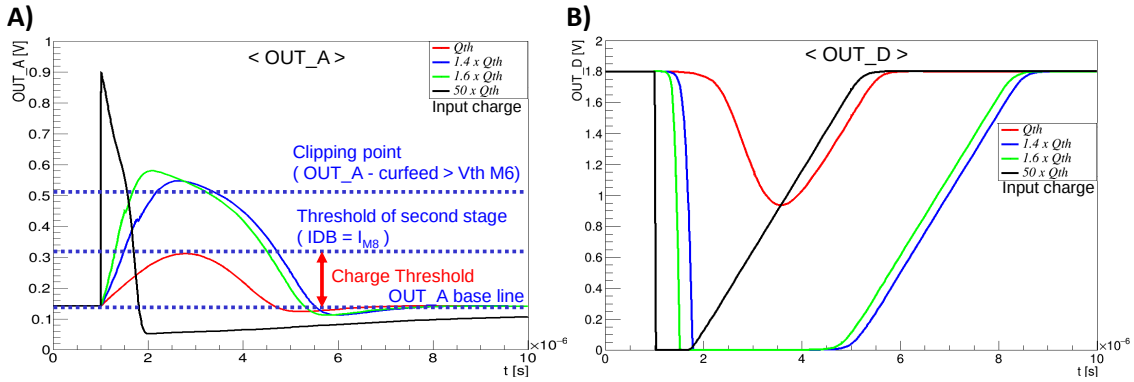

Figure 5. Pixel front end transient plots A) OUT_A B) OUT_D.

as low as ~ 40 nW with 1.8 V power supply. To compact the front-end layout, C_{source} and $C_{curfeed}$ are combined in one capacitance C_S as shown in figure 4c. A clipping mechanism is implemented to limit the pulse duration for very large input signals. This is achieved with transistor M6 in diode connection: source and gate are connected to the curfeed node and the drain is connected to the OUT_A node. Normally M6 is reverse biased, but when the OUT_A signal is high enough to forward bias it, M6 provides additional discharge current to compress the pulse duration. The clipping effect is noticeable for input charges larger than 1.4 times the charge threshold both for OUT_A and OUT_D.

3 pALPIDE-2 measurement results

The pALPIDE-2 front-end has a charge threshold of ~ 150 e^- with rms noise of ~ 10 e^- for nominal bias setting and −6 V substrate voltage bias. The pALPIDE-2 chip has been successfully characterized in a beam test before and after the exposure to non-ionizing radiation of 1.0×10^{13} 1MeV n_{eq}/cm^2. Figure 6 shows detection efficiency, fake-hit rate, spatial resolution and cluster size as a function of the ITHR bias, that is proportional to the charge threshold. The results are presented for an epitaxial layer thickness of 25 μm, nwell-pwell spacing of 2 μm and a substrate voltage of −6 V. At nominal threshold setting (ITHR = 500 pA), the detection efficiency is close to 100% with a fake hit rate below 10^{-8} hits/pixel/event. The spatial resolution of 5 μm is achieved with an average cluster size of ~ 2 pixels. These results show that the pALPIDE-2 satisfies the ALICE ITS requirements.

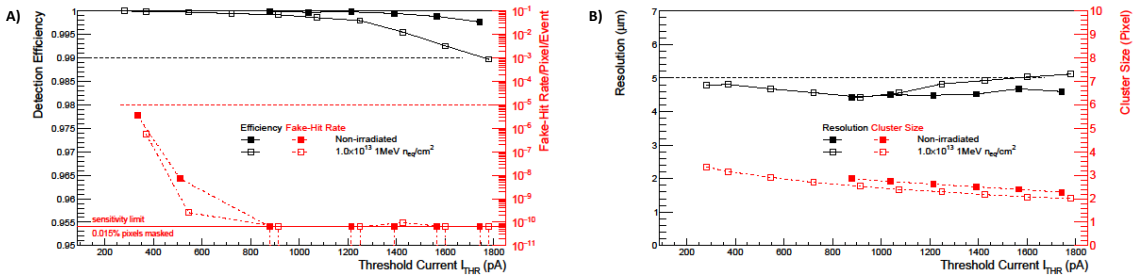

Figure 6. pALPIDE-2 beam test results by using a 6 GeV π-source A) detection efficiency and fake-hit rate B) spatial resolution and cluster size.

The pixels in Sector 0 and Sector 1 have been implemented with a different width for the front-end input transistor, 0.22 μm and 0.92 μm, respectively. Figure 7 compares the fake-hit rate as function of the threshold current. In the low threshold region where the signal-to-noise ratio is low, the Gaussian noise dominates and the fake-hit rate is similar for the two sectors. Increasing the threshold, for high signal-to-noise ratio, the fake-hit rate is (much) higher for the sector with the smaller transistor. Random telegraph noise [8] has been observed in this technology and it is well-known to affect smaller transistors much more than large ones. We believe this is the explanation for the much larger fake hit rate observed for the sector with the minimum size for the input.

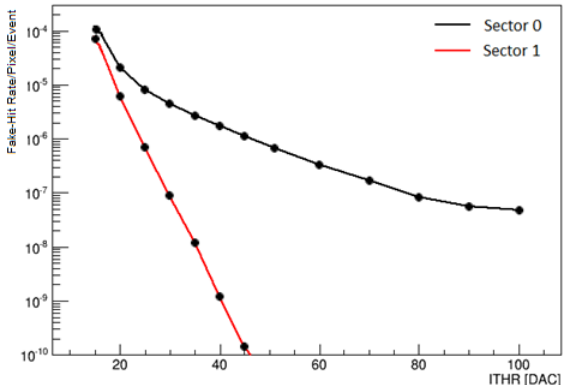

Figure 7. pALPIDE-2 fake-hit rate for Sector 0 (M1 $W = 0.22$ μm) and Sector 1 (M1 $W = 0.92$ μm).

4 Front end optimization in pALPIDE-3

4.1 Charge threshold uniformity

The circuit schematic and layout are shown in figure 8. The influence of mismatch of each transistor on the charge threshold has been evaluated with Monte-Carlo simulations. Transistor sizes have then been scaled to optimize the charge threshold spread with the constraint to fit the front-end in 220 μm^2.

Table 2 shows the size and relative contribution to the charge threshold mismatch for each transistor. The rms_0 parameter is the normalized root mean square of the mismatch value for 1 μm^2 transistor area, which depends on the functionality of the transistor in the circuit. The effective transistor contribution is:

$$\text{rms} = \frac{\text{rms}_0}{\sqrt{\text{AREA}}} \tag{4.1}$$

Table 2. Transistor size and contribution to charge threshold mismatch.

	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	Cs
rms [e]	2.70	0.06	0.03	0.22	4.63	0.92	0.17	0.34	0.58	0.04	0.91
W/L [μm/μm]	1.8/8.5	0.92/0.18	0.22/0.18	0.5/5	2/8.4	0.5/10	0.5/3	0.42/7	0.22/4	0.42/0.2	Cap. : 344 fF
Area [μm^2]	15.3	0.16	0.04	2.5	16.8	5	1.5	2.94	0.88	0.08	43.09
rms [e]	0.69	0.14	0.14	0.14	1.13	0.41	0.14	0.20	0.62	0.14	0.14

The total charge threshold mismatch $\mathrm{rms}_{\mathrm{tot}}$ is given by the weighted sum of squares:

$$\mathrm{rms}_{\mathrm{tot}} = \sqrt{\sum_{i=0}^{9} \frac{(\mathrm{rms}_{0_i})^2}{A_i}}, \quad \left(A_{\mathrm{tot}} = \sum_{i=0}^{9} A_i \right) \tag{4.2}$$

In order to minimize $\mathrm{rms}_{\mathrm{tot}}$, a large transistor area A_i should be allocated for transistors with large rms_0^2. This is the case for the current bias transistors (M0, M4, M5, and M7) and their size is limited by layout area. The area of the input transistor M8 of the second stage is a compromise between large area for low mismatch and small area to reduce the capacitance load on OUT_A and increase the gain. Schematic level simulations after this optimization yield a minimum charge threshold of 78 e^- with 1.7 e^- rms, post layout simulations a minimum threshold of 92 e^- with 2.0 e^- rms due to the gain reduction caused by the parasitic capacitances. These values correspond to a reduction of mismatch by factor ~ 3 with respect to the pALPIDE-2 circuit.

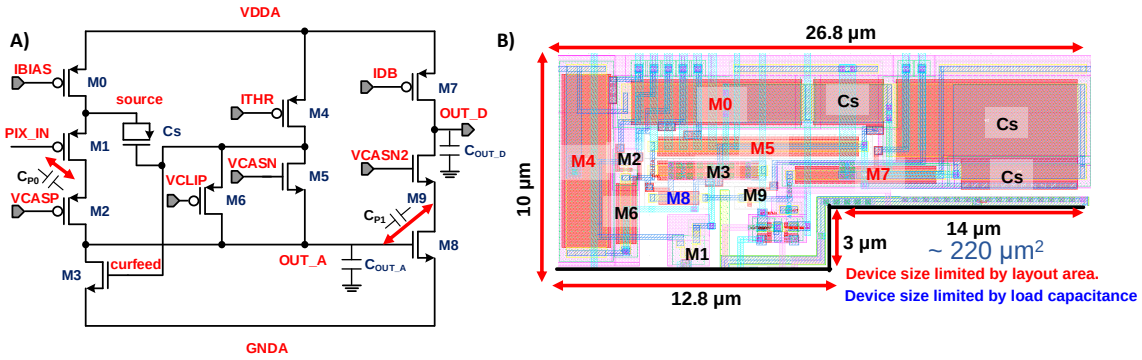

Figure 8. Optimized front end in pALPIDE-3 A) schematic with parasitic capacitance B) layout.

Monte Carlo simulations take into account transistor parameter variations but no variations of parasitic capacitances. Therefore a detailed study on the impact of the parasitic capacitances has been performed. In particular the Miller effect amplifies the effect of parasitic capacitance and its variation impacts the value and variation of the charge threshold. Therefore cascode transistors are used to avoid parasitic capacitances between high gain nodes. In the ALPIDE frontend circuit transistor M2 avoids the parasitic capacitance between PIX_IN and OUT_A. This was already implemented in pALPIDE-1&2 to avoid an increase of the effective input capacitance. The second stage of the front-end provides a high gain between OUT_A and OUT_D when operating close to the discrimination threshold. Figure 8 shows C_{P1}, the parasitic capacitance between the gate and drain of transistor M8. In the pALPIDE-3 transistor M9 is implemented to decouple C_{P1} from OUT_D, thus reducing the sensitivity of the charge threshold to C_{P1}. The circuit layout extraction yields $C_{\mathrm{P1}} = 0.38$ fF. The charge threshold sensitivity to 25% variation of C_{P1}, corresponding to 0.1 fF, has been calculated. Without the cascode transistor M9, the sensitivity is 2.2 e^-/0.1 fF, whereas with M9 the sensitivity is reduced to 0.6 e^-/0.1 fF. Therefore, M9 is fundamental to reduce the charge threshold sensitivity to variation of C_{P1} to a value negligible compared to the rms of 2 e^- induced by transistor mismatch.

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4.2 Time response uniformity

ALPIDE can operate in triggered mode, where the front end works as analog memory as the pulse formed upon the incidence of a particle hit keeps the hit information for a certain duration. A STROBE signal arriving during the time this pulse is above threshold allows the discriminated output to be latched. Figure 9 shows OUT_D leading (t1) and trailing edge (t2) as a function of the input charge signal. The leading edge follows a typical time walk curve that decreases for increasing input charge. The trailing edge of OUT_D increases for increasing charge up to the clipping point, whereafter the pulse duration is compressed down to a saturation value for very large input charges.

The parameters improving the pulse duration uniformity have been analyzed both for OUT_A and OUT_D. The analog output OUT_A discharging time depends on the discharging current and the capacitive load $CT_{\mathrm{OUT\_A}}$. The discharging current is defined by ITHR or clipping transistor current I_{M6} when the signal is below or above the clipping point, respectively. Therefore, the OUT_A pulse duration uniformity is improved by a wider M4 to reduce ITHR variation, a longer M6 to reduce the clipping point variation and by introducing the cascode transistor M9 to reduce $C_{\mathrm{OUT\_A}}$ variation. The clipping transistor M6, instead of being diode connected, can have the gate controlled by a selectable voltage level VCLIP, thus adding the possibility to tune the clipping point. The discriminated output OUT_D return to steady state time is subject to slew rate limitation:

$$\frac{dv_{\mathrm{OUT\_D}}}{dt} = \frac{IDB}{C_{\mathrm{OUT\_D}}} \tag{4.3}$$

OUT_D pulse duration uniformity is reduced with a longer M7 reduces IDB variation.

Figure 9 reports leading edge and trailing edge timing and variation for an input charge at threshold, before the clipping point, at the clipping point and at a very large value. After the circuit and transistor size optimization, from pALPIDE-2 to pALPIDE-3 the pulse duration uniformity is improved by a factor 2.

The STROBE window can be defined to latch all charges above threshold: the maximum delay is defined by the minimum trailing edge value for large input charges, and the duration is defined by the latest leading edge value occurs for charges at or near threshold. The STROBE delay has to

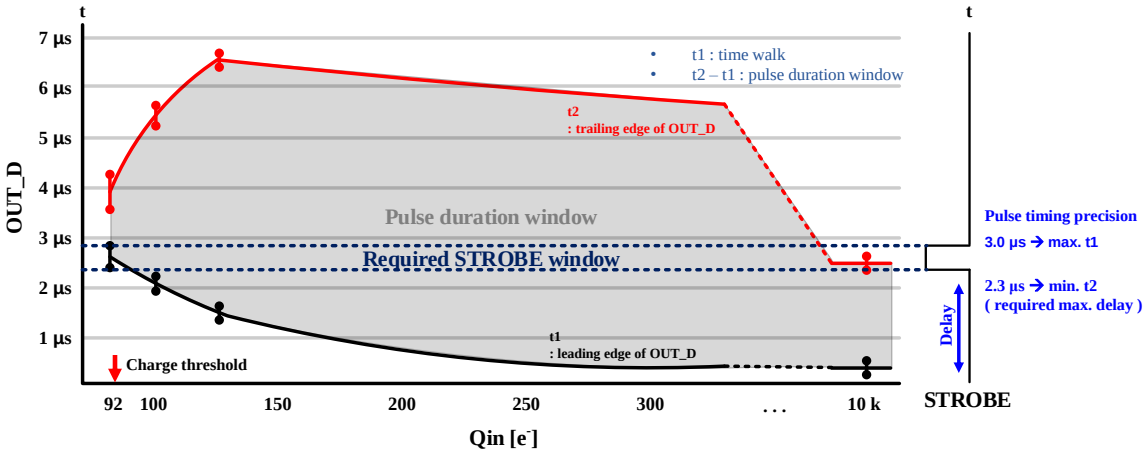

Figure 9. Pulse duration window with variation and STROBE window.

Table 3. Pulse duration variation result from simulation.

pALPIDE-2			pALPIDE-3			condition
Qin	t1 [μs]	t2 [μs]	Qin	t1 [μs]	t2 [μs]	
118 e	2.03 ± 0.35	52 ± 114	92 e	2.9 ± 0.20	3.4 ± 0.57	Threshold
128 e	1.7 ± 0.30	5.8 ± 0.98	10 e	2.0 ± 0.12	5.2 ± 0.15	Before clip.
18 e	0.8 ± 0.07	77 ± 0.48	13 e	1.3 ± 0.03	64 ± 0.09	Clip. point
10 ke	0.01 ± 0.01	19 ± 0.30	10 ke	0.22 ± 0.002	2.35 ± 0.08	Large Q_{in}

be larger than the trigger latency of 1.6 μs. Taking into account 5σ variation a STROBE window between 2.3 μs and 3.0 μs is required. A different strobe window can be applied to latch a fraction of the signals above threshold.

5 Conclusion

The ALPIDE chip is the Monolithic Active Pixel Sensor that will equip the ALICE ITS. It is implemented in the Tower Jazz 180 nm CMOS technology. The sensor performance of pALPIDE-2 prototype has been validated with beam tests and it fully satisfies the requirements. ALPIDE features a novel front-end that performs in-pixel discrimination with 40 nW power consumption, and fits in one-quarter of $\sim 30\ \mu\text{m} \times 30\ \mu\text{m}$ pixel area. A further optimized version of this front-end has been implemented in pALPIDE-3 to improve the pulse duration uniformity and the pixel-to-pixel charge threshold mismatch. Detailed Monte-Carlo simulations have been performed to implement the front-end in the available area and minimize the charge threshold variation. A cascode transistor in the second stage mitigates the impact of variation of parasitic capacitance on front-end uniformity. The possibility to have a voltage-controlled clipping point has been added as well. From simulation the charge threshold mismatch is 3 times lower and the pulse duration uniformity is improved by a factor 2.

pALPIDE-3 is divided in 8 sectors, each one with a different sensor reset and front-end circuit combination. The implemented front-end evolves incrementally: the starting point is pALPIDE-2 scheme, and one feature at the time is added to reach the final optimized circuit. pALPIDE-3 has been submitted in June 2015 and received from foundry in October 2015. The final chip for the ALICE ITS detector will be submitted in February 2016.

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