

Charge collection properties of a depleted monolithic active pixel sensor using a HV-SOI process

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2016 JINST 11 C01063

(<http://iopscience.iop.org/1748-0221/11/01/C01063>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 131.169.4.70

This content was downloaded on 30/01/2016 at 20:45

Please note that [terms and conditions apply](#).

17TH INTERNATIONAL WORKSHOP ON RADIATION IMAGING DETECTORS
28 JUNE – 2 JULY 2015,
DESY, HAMBURG, GERMANY

Charge collection properties of a depleted monolithic active pixel sensor using a HV-SOI process

S. Fernandez-Perez,^{a,b,1} M. Backhaus,^a M. Fernandez-Garcia,^c C. Gallrapp,^a T. Hemperek,^d
T. Kishishita,^d H. Krueger,^d M. Moll,^a C. Padilla^b and H. Pernegger^a

^aCERN,

Route de Meyrin 385, Geneva, Switzerland

^bIFAE,

Campus UAB 08193, Barcelona, Spain

^cIFCA – Universidad de Cantabria,

Av. de los Castros, Santander, Spain

^dUniversity of Bonn,

Nussallee 12, Bonn, Germany

E-mail: sonia.fernandez@cern.ch

ABSTRACT: New pixel detector concepts, based on commercial high voltage and/or high resistivity CMOS processes, are being investigated as a possible candidate to the inner and outer layers of the ATLAS Inner Tracker in the HL-LHC upgrade. A depleted monolithic active pixel sensor on thick film SOI technology is being extensively investigated for that purpose. This particular technology provides a double well structure, which shields the thin gate oxide transistors from the Buried Oxide (BOX). In addition, the distance between transistors and BOX is one order of magnitude bigger than conventional SOI technologies, making the technology promising against its main limitations, as radiation hardness or back gate effects. Its radiation hardness to Total Ionizing Dose (TID) and the absence of back gate effect up to 700 Mrad has been measured and published [1]. The process allows the use of high voltages (up to 300 V) which are used to partially deplete the substrate. The process allows fabrication in higher resistivity, therefore a fully depleted substrate could be achieved after thinning. This article shows the results on charge collection properties of the silicon bulk below the BOX by different techniques, in a laboratory with radioactive sources and by edge Transient Current Technique, for unirradiated and irradiated samples.

KEYWORDS: Radiation-hard detectors; Particle tracking detectors (Solid-state detectors); Particle detectors; Hybrid detectors

¹Corresponding author.

Contents

1 Introduction	1
2 Thick film HV-SOI monolithic detector prototype: XTB01 & XTB02 Prototypes	2
3 Charge collecting properties of the silicon bulk	3
4 Edge TCT measurements	7
5 Summary	9

1 Introduction

The Large Hadron Collider (LHC) plans to operate with an integrated luminosity ten times higher than its design value up to $L = 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ during the High Luminosity LHC (HL-LHC) [2]. As a consequence detectors have to accommodate the expected high hit occupancies, increased data rates and be able to cope with the strong radiation environment, especially in its inner layers. Accordingly, the ATLAS strategy is to fully replace its Inner Detector. The performance requirements of the pixel detector layers [3] of the new Inner Tracker (ITk) are summarized in table 1, where inner and outer layers are distinguished. The ATLAS CMOS collaboration is seeking new detector concepts as an option for the ITk pixel layers [4]. The partially Depleted Monolithic Active Pixel Sensor (DMAPS) [5, 6] in thick film Silicon-On-Insulator (SOI) technology presented in this paper is one of these detector concepts. The accomplishment of the mentioned requirements by a monolithic detector would lead to a new era of the HEP detectors, with a significant cost advantage and simpler detector-FE-electronics assembly. Currently, the main limitation of SOI devices is radiation hardness, which is more complex for SOI devices, and signal response time to comply with LHC bunch spacing of 25 ns.

Table 1. ATLAS Inner Tracker requirements for the HL-LHC.

	Inner Layers (<6 cm)	Outer Layers (>6 cm)
Particle rate	10 MHz/mm ²	1 MHz/mm ²
Total Ionizing Dose (TID)	1 Grad	50 Mrad
Non Ionizing Energy Loss (NIEL)	$2 \times 10^{16} n_{\text{eq}}\text{cm}^{-2}$	$1 \times 10^{15} n_{\text{eq}}\text{cm}^{-2}$
Silicon Area	0.8 m ²	10.8–20.8 m ²

2 Thick film HV-SOI monolithic detector prototype: XTB01 & XTB02 Prototypes

A new monolithic active pixel sensor built in 180 nm thick film SOI CMOS technology designed by the University of Bonn was fabricated using the XFAB process [7]. The Buried OXide (BOX) isolates the full CMOS electronics technology from the substrate which is reverse biased and used as a sensor diode as illustrated in figure 1. In contrast to other SOI technologies, the XFAB thick film SOI provides a double well structure to shield the thin gate transistors from the BOX. The transistors bulk silicon is partially depleted (PD). This makes the technology promising against the radiation effects on the transistors. TID and absence of back gate effects were proven up to 700 Mrad [1]. The process makes it possible to apply high bias voltages (up to 300V) which are used to partially deplete the substrate and to fabricate devices in higher resistivity ($1 \text{ k}\Omega \cdot \text{cm}$) is possible. Therefore a fully depleted substrate could be achieved after thinning. Currently there is no backside processing, thus the HV is applied from the top using a p^+ implant ring.

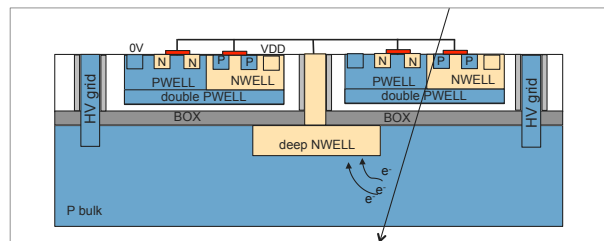


Figure 1. A pixel cross section of the XTB01 prototype. Not to scale.

The first prototype fabricated, called XTB01, is $300 \mu\text{m}$ thick, with a size of $5 \text{ mm} \times 2 \text{ mm}$. The substrate is p-type silicon with $100 \Omega \text{ cm}$ resistivity. The charge is collected in a small deep n-well of $10.5 \mu\text{m} \times 14 \mu\text{m}$ size. This reduces the capacitance with respect to high voltage CMOS approaches, which have a large deep n-well nearly filling the pixel area ($33 \mu\text{m} \times 125 \mu\text{m}$) as charge collecting electrode [8]. The deep n-well is connected to the readout circuitry as illustrates in the pixel cross section shown in figure 1. A standard 3T pixel cell [5] is implemented in each pixel. Either the output signal of a single pixel can be permanently monitored, or the full matrix can be read out using a rolling shutter with correlated double sampling. Such a readout is too slow for an ATLAS application but is sufficient for the characterization of first prototypes. In case this prototype becomes an option for the ATLAS ITk layers, a new readout architecture would be implemented. The chip includes four independent matrices with different pixel sizes ($25 \mu\text{m} \times 25 \mu\text{m}$, $50 \mu\text{m} \times 50 \mu\text{m}$ ($\times 2$), $100 \mu\text{m} \times 100 \mu\text{m}$) and n-well sizes. The HV is applied from an outer guard ring, and in addition the chip includes three additional grids surrounding each pixel of all matrices. The HV can be applied through these grids, too. All measurements presented in this paper were performed on the $50 \mu\text{m} \times 50 \mu\text{m}$ pixel matrices. A detailed description of the chip design is given in [9].

A new version, called XTB02, was designed by University of Bonn to investigate purely the charge collection properties of the silicon bulk bellow the BOX. Thus, in XTB02 the deep n-well is not connected any more to the readout circuitry but is kept as an output going to an external amplifier, so this prototype behaves as a simple passive diode. The chip size, geometry and distances to the BOX are comparable to the XTB01 prototype. However the process has slightly changed: some process modifications were implemented to reduce the high leakage current observed in the

XTB01 prototype, and to increase the diode breakdown voltage [1]. XTB02 was also designed with several matrices with different pixel sizes. Figure 2 illustrates the cross section of the two pixel diode types, both 100 μm pitch, investigated in this paper. The pixel shown in figure 2a includes a p-stop structure surrounding every pixel, while the one shown in figure 2b includes an structure which can be biased and does not penetrate the BOX, called p-field. The aim of both structures is to modify the electrical field bellow the BOX and to break the conductive channel formed in the bulk due to BOX space charge formed after irradiation [1].

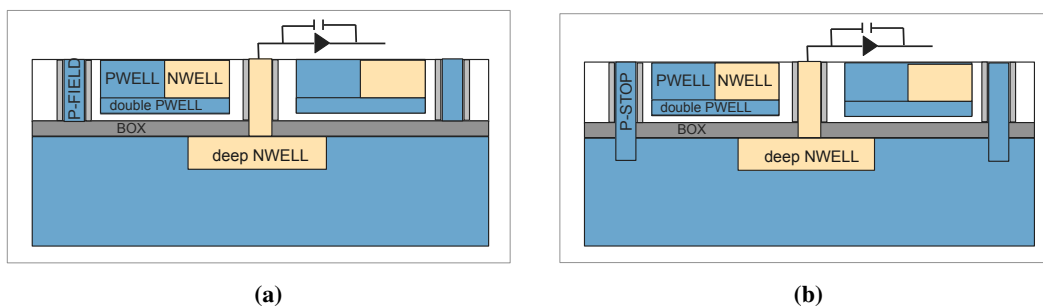


Figure 2. Prototype XTB02 (a) pixel cross section corresponding to matrix 1A, which possess a p-stop to reduce the leakage current (b) pixel cross section corresponding to matrix 2A, which possess a structure called p-field to reduce the leakage current.

Figure 3 shows a comparison between the Current-Voltage curves in logarithmic scale of prototype XTB01 and XTB02 with all those structures kept floating. The leakage current decreases by a factor of ten and the breakdown voltage increases from 150 V to above 300 V in prototype XTB02 for unirradiated samples.

3 Charge collecting properties of the silicon bulk

The test system, which was used to configure the single pixel, is composed of a Multi I/O board to make the digital interface with the computer, a General Purpose Adapter Card (GPAC) to provide all the analogue functionalities to the chip, and a Device Under Test (DUT) board. To measure the charge collection properties of the silicon bulk bellow the BOX a measurement method and analysis was developed. Previous source measurements were performed using a correlated double sampling method using the fast ADC on the GPAC, but the measurement noise, and the lack of charge collection time information were identified as measurement limiting factors [1, 9].

To characterize the charge collection properties, two radioactive sources were used: ^{55}Fe and ^{90}Sr . The ^{55}Fe x-rays deposit all its energy in few micrometers from the surface while a Minimum Ionizing Particle (MIP) of ^{90}Sr deposits energy all along its path. Therefore, the prototype functionality as a pixel sensor was tested using a ^{55}Fe source for calibration and ^{90}Sr for charge collection measurements. The measurement method consists of probing the analogue output signal of the pixel with an oscilloscope, storing the pixel analogue signal and analyse the properties of the signals off-line. This was possible by triggering on the signal, above a threshold slightly higher than the signal baseline, and vetoing the reset periods, in order to record every waveform containing a hit and still some waveforms with no hit. An off-line analysis was developed in order to select the waveforms containing a hit and to extract the collected charge, and charge collection time.

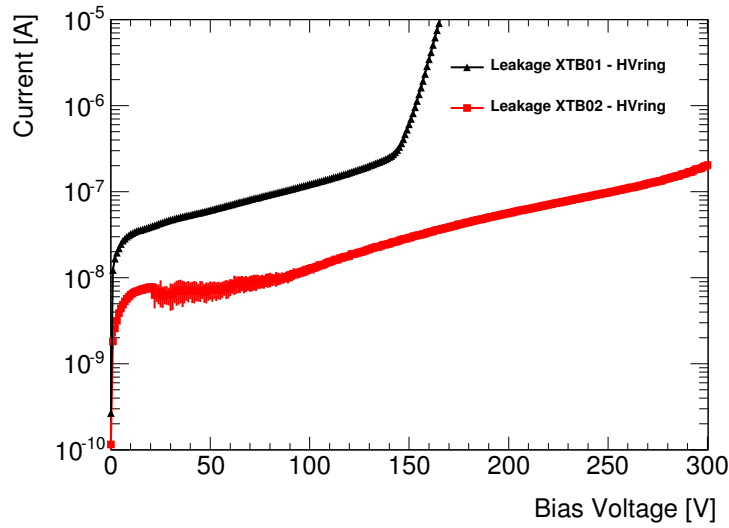


Figure 3. Current-Voltage curves comparison between prototype XTB01 and prototype XTB02, which includes different structures to reduce the leakage current. The voltage is applied on the most external guard ring, so called HVring.

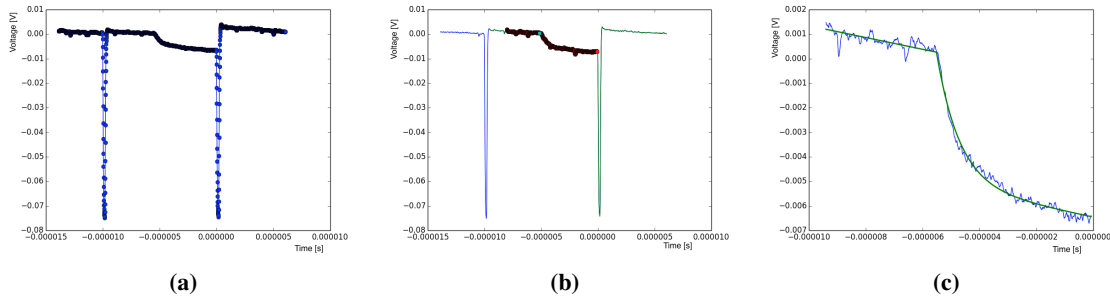


Figure 4. Offline analysis on a $50\ \mu\text{m} \times 50\ \mu\text{m}$ pixel at a biased voltage of 30 V and $0\ ^\circ\text{C}$. (a) raw data smoothing (b) reset identification and removal (c) hit fitted to the function described in equation 3.1 to extract the collected charge and charge collection time.

First the algorithm smooths the raw data without reducing the number of points as shown in figure 4a. Then, it checks for resets within the output signal as shown in figure 4b (in such a case the reset is deleted). At that point, if the signal size is higher than an adjustable threshold, the analyser proceeds, and a cut on the slew rate needs to be passed in order to be processed further. In case a hit is detected, the following function is fitted and collected charge and charge collection time are obtained from the fit parameters:

$$\begin{aligned}
 t \leq t_0 & \quad f = a + m \cdot (t - t_0) \\
 t > t_0 & \quad f = a + m \cdot (t - t_0) + b \cdot \left(e^{\frac{t-t_0}{c}} - 1 \right)
 \end{aligned} \tag{3.1}$$

where b is the collected charge, c the charge collection time and t_0 the hit detection time. If the mentioned cut is not passed, the waveform just contains the charge accumulated due to the leakage

current, and no hit. Those cases are used to calculate the electronic noise, which is given by the RMS of the Gaussian distribution of the leakage current centered at zero.

Three samples were measured: one unirradiated, and two neutron irradiated to $1 \times 10^{13} n_{eq} cm^{-2}$, and to $5 \times 10^{13} n_{eq} cm^{-2}$. The irradiated samples were stored at $-20^\circ C$ temperature to avoid annealing. All samples were calibrated with ^{55}Fe at a bias voltage of 100 V and then characterized with ^{90}Sr at several bias voltages. The temperature was $0^\circ C$ for all measurements in the unirradiated sample, while it was $-30^\circ C$ for all measurements in the irradiated samples, to reduce the leakage current and therefore the noise.

Figure 5a shows the ^{55}Fe spectra of a $50 \mu m \times 50 \mu m$ pixel, biased to $-100 V$ unirradiated. The spectrum is measured as signal size in Volt and it is used for calibration of the signal size to collected charge. The mean value of the Gaussian fit corresponds to 5.9 keV, permitting to calculate the conversion factor, $K = (11.59 \pm 0.79_{(sys)} \pm 0.01_{(stat)}) \times 10^{-6} V/e$. This value is used to determine the collected charge by the ^{90}Sr in e^- . Figure 5b shows the ^{90}Sr spectra of the same pixel at $-120 V$, for all hits detected within a charge collection time of 150 ns in the unirradiated sample. The most probable value of the Landau distribution divided by $80 e^-/\mu m$, gives a depletion depth of $33.9 \pm 2.7 \mu m$. This value perfectly agrees with the theoretical depletion calculated to be $34.8 \mu m$ for $100 \Omega \cdot cm$ material.

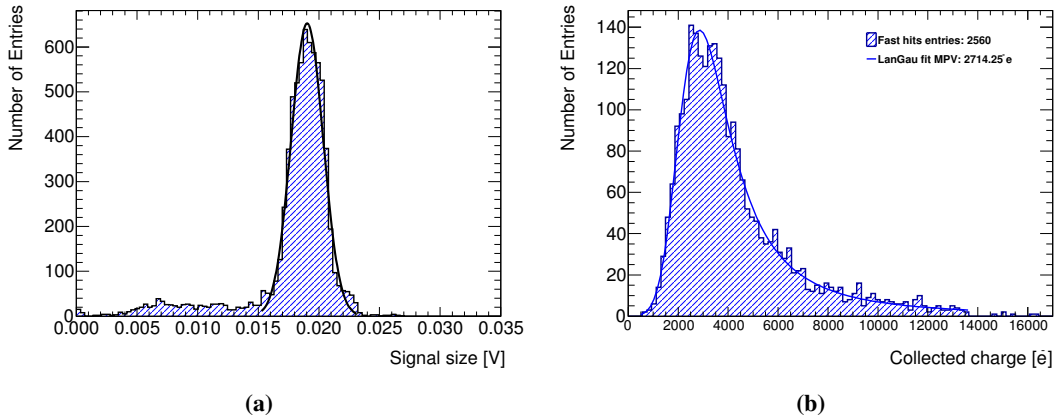


Figure 5. Prototype XTB01 sample unirradiated (a) ^{55}Fe spectra of $50 \mu m \times 50 \mu m$ pixel at 100 V and $0^\circ C$. (b) ^{90}Sr spectra of the same pixel at 120 V and $0^\circ C$.

When all the detected hits are considered, two different contributions to the collected charge are observed. Figure 6 shows the charge collection time versus the collected charge for the unirradiated sample at 30 V and 120 V, and for the neutron irradiated to $1 \times 10^{13} n_{eq} cm^{-2}$ at 120 V. As observed, some hits are collected within 150 ns while others are collected much slower, which we interpret as charge collection by diffusion as posed to charge collection by drift (faster signals). By increasing the HV on the unirradiated sample, the charge is collected faster. This can be explained by the fact that depletion depth increases and therefore the drift contribution to the collected charge increases as well. As expected, the slow charge contribution completely disappears after irradiation which is explained by the trapping of the charge carriers in the silicon bulk.

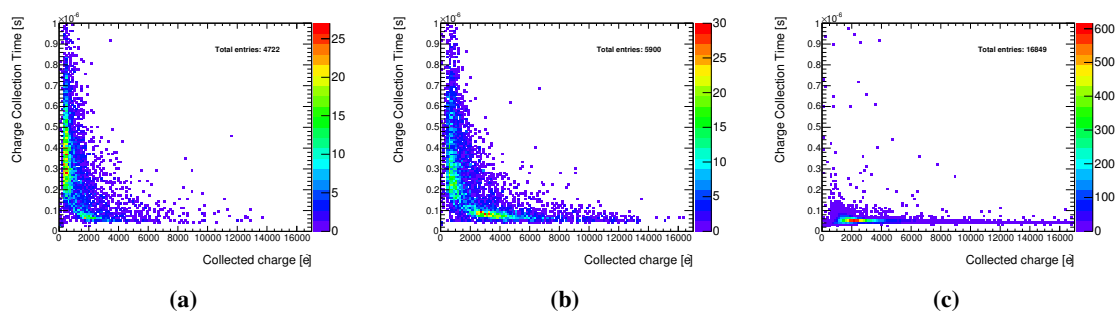


Figure 6. Prototype XTB01, charge collection time versus collected charge of a $50\ \mu\text{m} \times 50\ \mu\text{m}$ (a) unirradiated 30 V (b) unirradiated 120 V (c) neutron irradiated to $1 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ at 120 V.

Figure 7a shows the bias voltage versus the most probable value of the collected charge for all samples, where it becomes visible that the sample irradiated to $5 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ collects more charge than the sample irradiated to $1 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ at the same conditions. A similar behaviour has been observed for low resistivity substrates ($10\text{--}20\ \Omega \cdot \text{cm}$) by G.Kramberger, I. Mandic et al. [10]. Radiation induced removal of acceptors causes a decrease in effective doping concentration N_{eff} with fluences up to $1 \times 10^{15}\ n_{\text{eq}}\text{cm}^{-2}$. This increases the depletion width and consequently increases the collected charge of irradiated samples up to that dose. For higher fluences the collected charge would start to decrease as a consequence to charge trapping on radiation induced defects. The discovery of the acceptor removal effect in our prototype would make this technology very attractive. High resistivity would not be needed to increase the collected charge, at least for applications up to $1 \times 10^{15}\ n_{\text{eq}}\text{cm}^{-2}$. The depletion depth was calculated using the most probable value of the Landau distribution divided by $80\ e^-/\mu\text{m}$ for the unirradiated sample as shown in 7b. The depletion is proportional to the square root of the bias voltage, as expected.

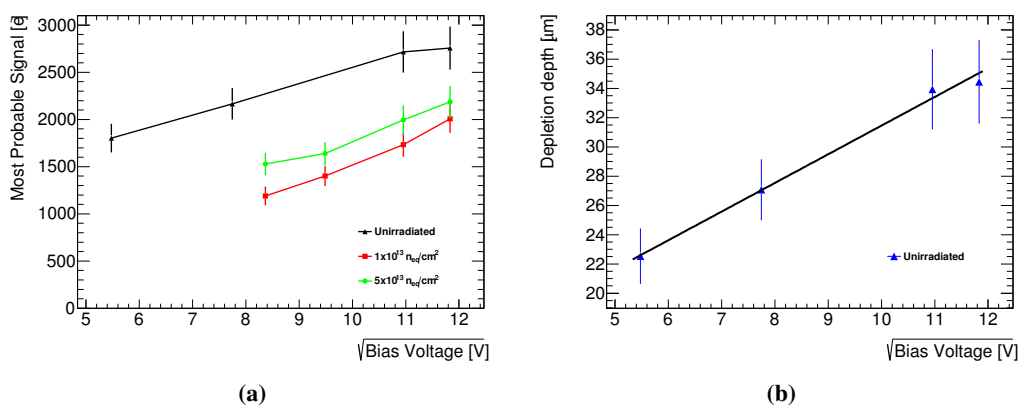


Figure 7. Prototype XTB01. (a) shows the most probable value of the collected charge versus voltage for all the samples at different voltages. The sample irradiated to $5 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ collects more charge than sample $1 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ at same conditions. (b) shows the depletion depth versus voltage for the unirradiated sample.

4 Edge TCT measurements

Edge Transient Current Technique (TCT) measurements study the development of the depletion region and its corresponding electric field within a silicon detector [11]. During the measurement infra-red laser pulses (1064 nm) of 150 pico seconds are penetrating the device through the sensor edge generating a path of electron hole pairs. The movement of these charge carriers in the presence of an electric field induces a current signal on the readout electrode of the DUT. Moving the sample perpendicular to the focused laser beam allows to determine the shape and properties of the depleted region. Edge TCT measurements were performed on the prototype XTBO2, in its two diode versions shown in figure 2, using the setup of the CERN SSD group. The drawing in figure 8a illustrates the readout and biasing scheme used for edge TCT measurements on a single pixel.

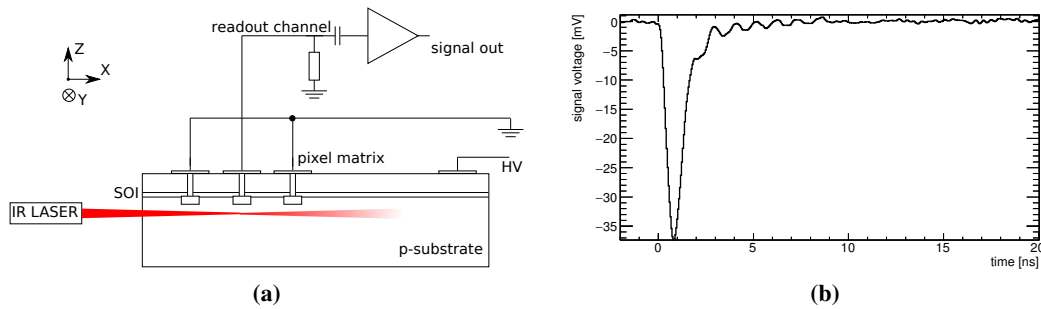


Figure 8. (a) Schematic drawing of the edge TCT measurement setup showing the readout scheme for a single pixel. (b) Current signal induced during a edge TCT measurement in the center of the depletion region of matrix 2A at 300 V.

The induced current signal in the passive diode shown in figure 8b is amplified by a fast current amplifier (40 dB) and recorded by a high bandwidth oscilloscope. The integration time used to calculate the collected charge is 5 ns. The minimum spatial resolution of the measurement depends on the Gaussian width ($\sigma = 10 \mu\text{m}$) of the focused laser spot. As the measurement represents a convolution of the depletion region and the width of the laser, structures below $40 \mu\text{m}$ are dominated by the contribution of the laser and are overestimating the real structure width. All scans were performed at room temperature.

The depletion depth growth of a single pixel contained in matrix 2A is shown in figure 9. Two ZY scans at 100 V and 300 V where the p-field structure was kept floating are shown in figures 9a and 9b, respectively. The grey line represents the BOX and the black square the pixel pitch. The region in which higher charge is collected corresponds to the region below the n-well where the electric field is highest. The depletion depth in the bulk direction agrees with the calculation in section 3 and the results of the source measurement in the laboratory. The depletion depth in the y direction seems to increase with HV in a different way. In a $100 \mu\text{m} \times 100 \mu\text{m}$ pixel with $40 \mu\text{m} \times 50 \mu\text{m}$ n-well we expect that the remaining $30 \mu\text{m}$ at the sides of the n-well were fully depleted at 100 V. However, neither at 300 V the pixel seems to be fully depleted in the y direction. Figure 9c shows the collected charge along the depth of the pixel for bias voltages at the external bias ring ranging from 0–300 V while the p-field was kept floating. The Full Width at Half

Maximum (FWHM) in the z direction extracted from the previous plot (which can be considered as the depletion depth) versus voltage is shown in figure 9d. The depletion depth does not grow linearly to the square root of the bias voltage due to the fact that the measurement is dominated by the laser width as mentioned before.

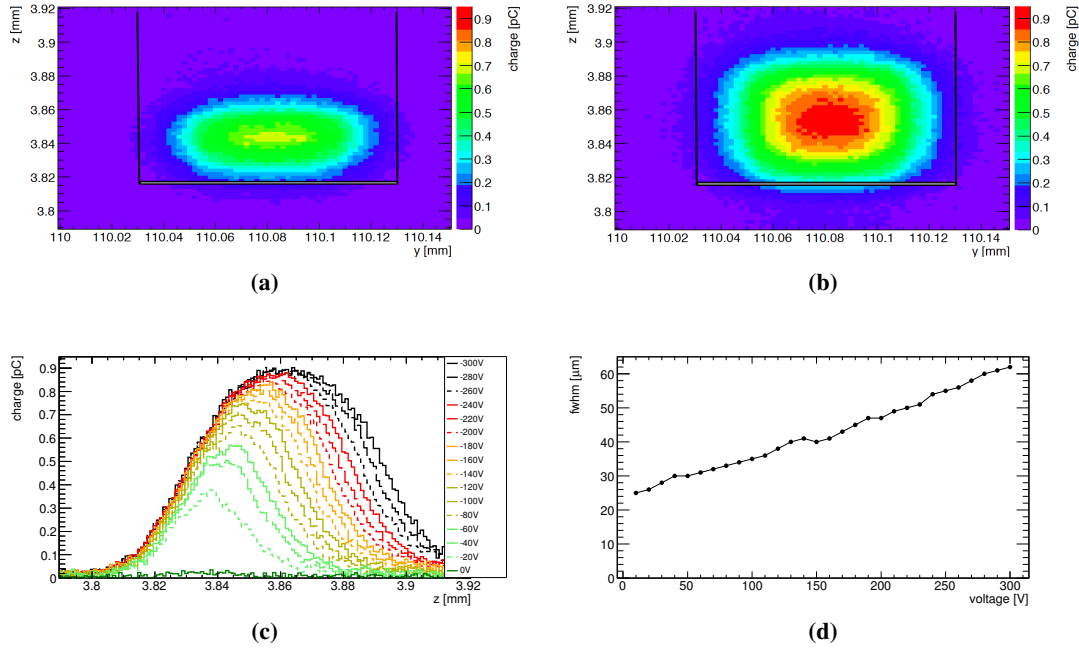


Figure 9. Depletion depth growth on a single pixel of $100\ \mu\text{m}$ pitch in matrix 2A where the p-field structure was kept floating. A ZY scan is shown for different bias voltage (a) 100 V and (b) 300 V, whereas (c) shows the collected charge for a bias voltage range from 0 V to 300 V versus depth and (d) the FWHM as measure of the depleted zone in the z direction versus the voltage.

To investigate the effect of the p-field structure on the depletion zone, the p-field structure was biased to different voltages for a fixed bias voltage of the external ring of 100 V. The ZV scan on figure 10a shows the pixel response at a ring bias voltage of 100 V when the p-field was biased to 100 V. These results can be compared with figure 9a where the p-field was kept floating. The change of the shape shows that the potential of the p-field influences the depletion in the y direction. To quantify this change, the FWHM was extracted from the collected charge at different voltages at the p-field in y direction as shown in figure 10b. The depletion depth z direction seemed to be independent of the applied p-field voltage and stayed at about $34.5\ \mu\text{m}$. From this can be concluded that the depletion depth can be increased up to $60\ \mu\text{m}$ for a bias voltage of 300 V. Surprisingly the same voltage does not show much impact on the lateral depletion width for a floating p-field structure. But a voltage of 100 V on the p-field structure and the external ring extends the lateral depletion width by $5\ \mu\text{m}$ compared to the floating configuration and no growth in the bulk direction. Similar results are obtained for matrix 1A which contains the p-stop structure. The decrease of signals charge in pixel boundary regions has also been observed in similar structure with low resistivity substrates [12].

An extensive study using TCAD simulations has been started to investigate the field distribution in the substrate.

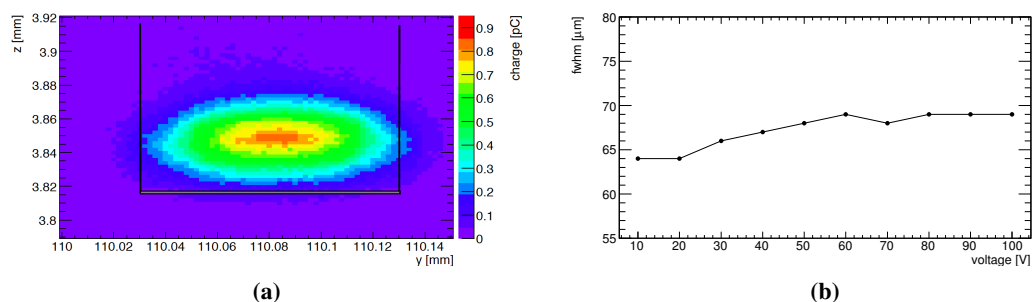


Figure 10. Depletion depth growth on a single pixel of $100\ \mu\text{m}$ pitch in matrix 2A where the external bias ring is kept constant at 100 V and the p-field structure is biased at different voltages. (a) shows a ZY scan for 100 V applied on both, the external ring and the p-field. (b) shows the depletion depth in the y direction in function of the p-field voltage for 100 V at the external bias ring.

5 Summary

The XFAB thick film SOI technology is extensively investigated on monolithic prototype for the HL-LHC. Electronics radiation hardness and no back-gate effect has been proven up to 700 Mrad. The unexpected high leakage current before irradiation observed in the first version of the chip (XTB01) was corrected in the second prototype (XTB02) by slight changes in the process. As a consequence, XTB02 presents a factor of 10 less leakage current and an increase of the breakdown voltage to above 300 V is observed. In addition, the p-field / p-stop structures implemented in XTB02 to reduce the leakage current specially after irradiation, seems to positively influence the charge collection in the y direction when it is biased.

The depletion depth grows as expected in depth, proven on XTB01 with sources in the laboratory and on XTB02 with edge TCT measurements, whereas it grows differently in the y direction leading to a decreased signal between pixels. Clear ^{55}Fe and ^{90}Sr spectra in irradiated devices up to $5 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ have been obtained and characterized. The sources measurements show that the irradiated sample to $5 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$ collects more charge than the irradiated sample to $1 \times 10^{13}\ n_{\text{eq}}\text{cm}^{-2}$, giving a possible hint to Acceptor Removal Effect, which has been observed in other low resistivity devices.

As a conclusion, the XFAB SOI technology shows promising results for depleted monolithic pixel layers in HL-LHC.

Acknowledgments

The authors are greatly indebted to A. Rozanov for providing the XTB02 samples, I. Mandic for very useful discussions and support and the CERN DSF workshop for wire bonding of the chips.

This research project has been supported by a Marie Curie Initial Training Network fellowship of the European Community's Seventh Framework Programme under contract number PITNGA-2011-289161 (TALENT).

References

- [1] S. Fernandez-Perez et al., *Radiation hardness of a 180 nm SOI monolithic active pixel sensor*, *Nucl. Instrum. Meth. A* **796** (2015) 13.
- [2] P. La Rocca and F. Riggi, *The upgrade programme of the major experiments at the Large Hadron Collider*, *J. Phys. Conf. Ser.* **515** (2014) 012012.
- [3] N. Wermes, *Pixel Detectors for Charged Particles*, *Nucl. Instrum. Meth. A* **604** (2009) 370 [[arXiv:0811.4577](https://arxiv.org/abs/0811.4577)].
- [4] H. Pernegger, *Development of radiation hard CMOS Active Pixel Sensors for HL-LHC*, in proceedings of *The 13th Pisa Meeting on Advanced Detectors*, La Biodola, Isola d'Elba, Livorno, Italy, 24–30 May 2015.
- [5] R. Turchetta et al., *A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology*, *Nucl. Instrum. Meth. A* **458** (2001) 667.
- [6] I. Peric and C. Takacs, *Large monolithic particle pixel-detector in high-voltage CMOS technology*, *Nucl. Instrum. Meth. A* **624** (2010) 504.
- [7] A. Holke et al., *A 200V partial SOI 0.18 μ m CMOS technology*, in proceedings of *The 22th International Symposium on Power Semiconductor Devices & ICS (ISPSD)*, Japan, (2010), pg. 257–260.
- [8] HVCMOS collaboration, I. Peric, *Active pixel sensors in high-voltage CMOS technologies for ATLAS*, [2012 JINST 7 C08002](https://arxiv.org/abs/1207.4002).
- [9] T. Hemperek, T. Kishishita, H. Krüger and N. Wermes, *A Monolithic Active Pixel Sensor for ionizing radiation using a 180 nm HV-SOI process*, *Nucl. Instrum. Meth. A* **796** (2015) 8 [[arXiv:1412.3973](https://arxiv.org/abs/1412.3973)].
- [10] G. Kramberger et al., *Initial acceptor removal in p-type silicon*, in proceedings of *10th Anniversary “Trento” Workshop on Advanced Silicon Radiation Detectors*, FBK, Trento, Italy, 17–19 February 2015.
- [11] C. Gallrapp et al., *TCT, eTCT and I-DLTS measurement setups at the CERN SSD Lab*, in proceedings of *24th RD50 Workshop*, Bucharest, Romania, 11–13 June 2014
- [12] ATLAS CMOS PIXEL collaboration, B. Ristic, *Measurements on HV-CMOS Active Sensors After Irradiation to HL-LHC fluences*, [2015 JINST 10 C04007](https://arxiv.org/abs/1412.1589) [[arXiv:1412.1589](https://arxiv.org/abs/1412.1589)].