# GBLD10+: a compact low-power 10 Gb/s VCSEL driver



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# GBLD10+: a compact low-power 10 Gb/s VCSEL driver

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Abstract: We report the design and implementation of the GBLD10+, a low-power 10 Gb/s VCSEL driver for High Energy Physics (HEP) applications. With new circuit techniques, the driver consumes only 31 mW and occupies a small area of 400 $\mu$m $\times$ 1750 $\mu$m including the IO PADs and sealrings. These characteristics allow for multiple GBLD10+ ICs to be assembled side by side in a compact module, with each one directly wire bonded to one VCSEL diode. This makes the GBLD10+ a suitable candidate for the Versatile Link PLUS (VL$^+$) project, offering flexibility in configuring multiple transmitters and receivers.

Keywords: VLSI circuits; Analogue electronic circuits; Optical detector readout concepts

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## 1 Introduction

The Versatile Link (VL) project was a joint ATLAS-CMS effort aiming at developing a radiation hard bi-directional optical link for use in the phase-I LHC upgrade program [1]. As the main building block on the transmission side, the GigaBit Laser Driver (GBLD) was developed to operate at a data rate of 5 Gb/s with a power consumption around 300 mW [2]. The Versatile Link PLUS project ($VL^+$) targets the phase II upgrades of the ATLAS and CMS experiments [3]. With the high-luminosity operation of LHC in phase II, data transmission requires very high data rates and low power dissipation. $VL^+$ has to support data rates up to 10 Gb/s in the upstream direction. As an initial step towards this target, we have designed and demonstrated the first 10 Gb/s radiation-hard laser driver (GBLD10) in 130-nm CMOS with a power consumption of 85 mW [4]. Similar to the GBLD, the GBLD10 is packaged in a 4 mm × 4 mm QFN24 package and is used to drive a Transmit Optical Sub-Assembly (TOSA) in an Enhanced Small Form-factor Pluggable (SFP+) module.

Targeting at the phase II upgrade, the GBLD10+ is an enhanced Vertical Cavity Surface Emitting Laser (VCSEL) driver running at 10 Gb/s. Compared to the GBLD and GBLD10 [2, 4], the GBLD10+ features an ultra-low power consumption around of 31 mW. It also has a compact size of 1750 $\mu$m × 400 $\mu$m. The common-cathode output driver topology with on chip VCSEL bias implemented in the GBLD10+ saves assembly costs and simplifies the PCB design by eliminating external components on the PCB. Besides the compact size, the GBLD10+ also has a symmetrical PAD structure for digital and power IOs, which provides the users with the flexibility to choose the channel count in a customized form-factor die-to-die bonding module layout. As an example, figure 1 shows a transceiver module, which can run at 30 Gb/s upstream and 2.5 Gb/s downstream. It can be easily implemented by three GBLD10+ and one GigaBit Trans-Impedance Amplifier (GBTIA+) running at 2.5 Gb/s. The GBLD10+ has 40 PADs in total, 3 of which are high-speed

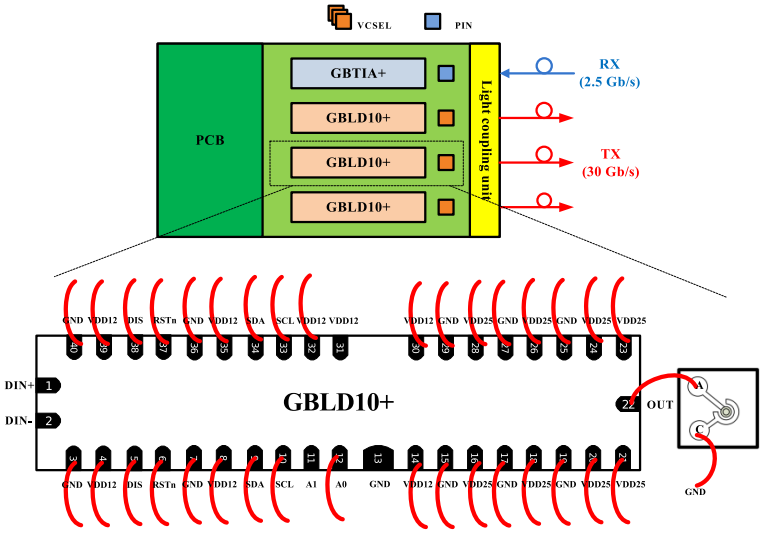


**Figure 1.** Transceiver module with three GBLD10+ and one GBTIA+.

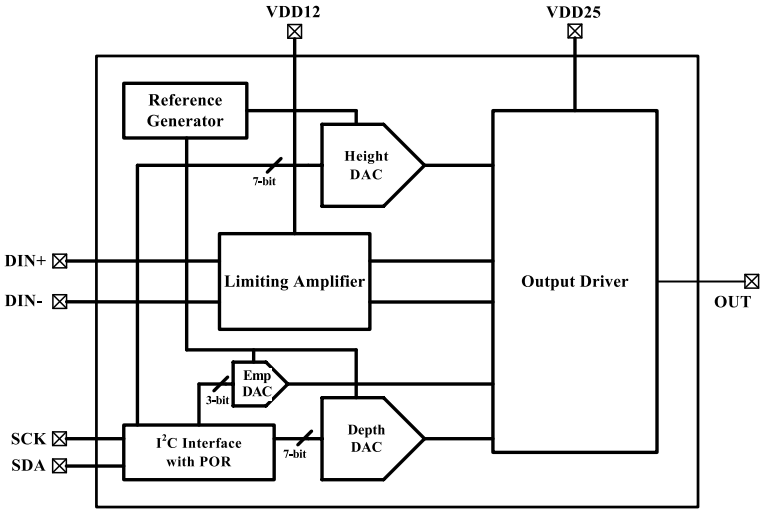


**Figure 2.** GBLD10+ block diagram.

PADs (DIN+, DIN- and OUT) with a size of 70 $\mu$m $\times$ 57 $\mu$m while the rest are standard PADs with a size of 120 $\mu$m $\times$ 75 $\mu$m. The size of the PADs greatly limits the available active area for the core circuit, which leads to the challenges to reach a speed of 10 Gb/s, as explained later in the paper.

## 2 Design of GBLD10+

### 2.1 GBLD10+ architecture

The block diagram of the GBLD10+ is shown in figure 2. The core circuits include the limiting amplifier and the output driver. Two 7-bit Digital-to-Analog Converters (DACs) are designed to program both the biasing and modulation amplitude, with a resolution of 0.16 mA. The GBLD10+ also features a configurable pre-emphasis function with the emphasis amplitude controlled by a



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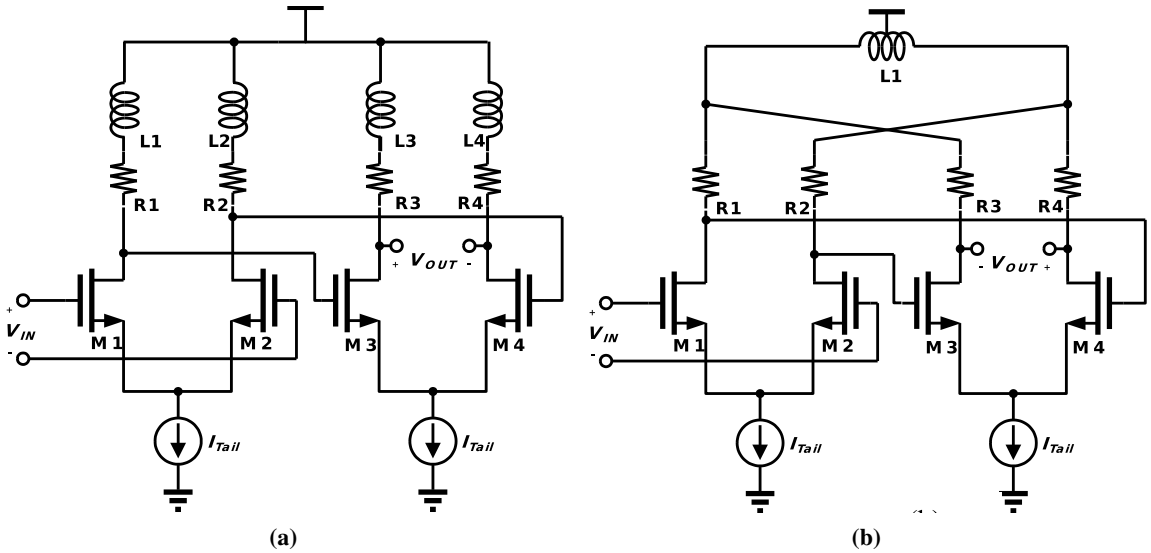



**Figure 3.** Limiting amplifier topologies: (a) traditional inductor peaking topology; (b) shared-inductor peaking topology.

3-bit DAC. A reference generator generates the process and temperature independent current for the DACs. All the DACs are controlled through the $I^2C$ interface. A Power On Reset (POR) circuit and the $I^2C$ circuit are used to set the default DAC values after the chip power up. The $I^2C$ and POR circuits are triplicated to make the chip immune to Single Event Upsets (SEUs). Different from the GBLD and GBLD10 that are powered from single 2.5 V supplies, the GBLD10+ uses dual supply voltages — 1.2 V and 2.5 V, for power-saving considerations. The output driver has to be powered by 2.5 V because of the large threshold voltage of the VCSEL. All the other blocks, including the limiting amplifier and DAC, are powered by the 1.2 V supply.

### 2.2 Limiting amplifier

A limiting amplifier is designed to provide sufficient input swing (> 800 mV) for the output driver. There are two reasons to introduce the limiting amplifier before the output driver: first one is to increase the power efficiency of the output driver by completely switching in and out its tail current as the VCSEL modulation current; the second reason is to guarantee that the modulation current is independent of the input voltage swing which comes from the serializer and has a range of 200 mV–1.2 V. Therefore, users can program the modulation depth linearly through the DAC without the need to consider the effects of the input swing. To accommodate the minimum swing of 200 mV, a limiting amplifier with a minimum gain of 12 dB is needed to make sure the input swing of the output driver is always above 800 mV. High bandwidth is also desired to avoid limiting the bandwidth of the driver. To meet the gain and bandwidth requirements, as well as the stringent area requirement, a two-stage inductor peaking topology is proposed. The traditional inductor peaking approach shown in figure 3 (a) [5] needs two inductors in each stage, occupying a large die area. To minimize the area, we proposed to use a topology that shares the inductors between the first and second stages, as shown in figure 3 (b) [6]. To further shrink the area, a three-terminal inductor,

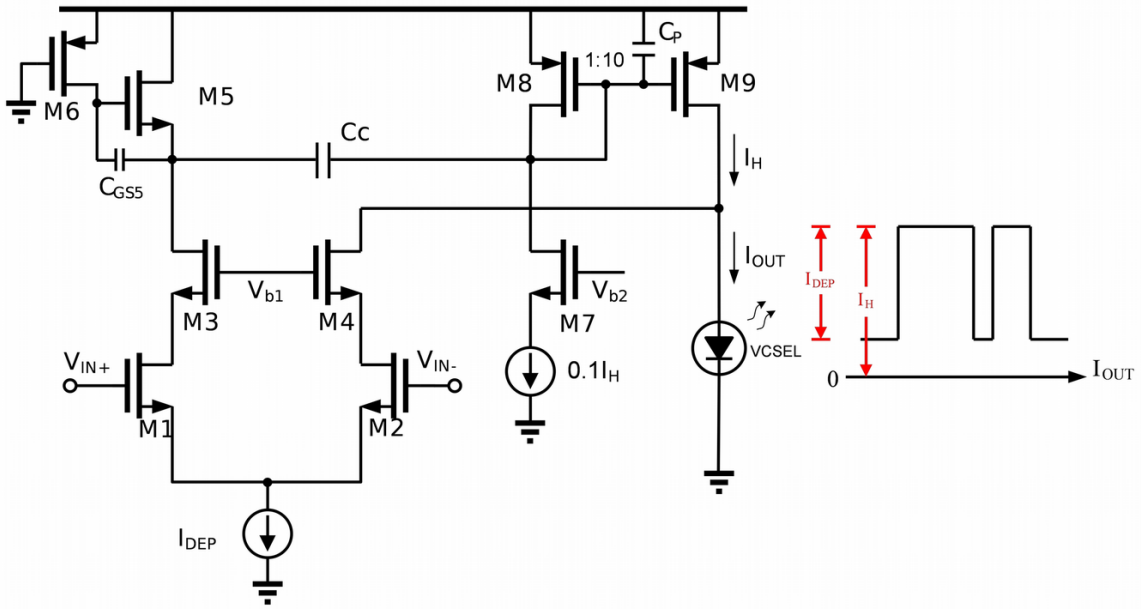



**Figure 4.** Output driver with the feedforward compensation.

which is equivalent to two inductors, has been used during the implementation. Simulations show that a gain of 13.3 dB and bandwidth of 14.8 GHz can be achieved, with a current consumption of 8 mA from 1.2 V supply.

### 2.3 Output driver

#### 2.3.1 Output driver with feedforward compensation

The proposed output driver with feedforward compensation is shown in figure 4. It is suitable for the common-cathode topology with the single-ended output connecting to the anode of the VSCEL. A 1:10 PMOS current mirror consisting of $M_8$ and $M_9$ is added to provide the level high current $I_H$. The modulation function is done by switching ON or OFF $M_2$ so that a modulation depth current $I_{DEP}$ is subtracted from the $I_H$ or not.

Considering the right branch of the output driver (which consists of $M_2$, $M_4$, $M_9$ and the VCSEL), the small-signal output current of the circuit can be expressed as follows:

$$I_{OUT}(s) = \frac{g_{m1,2} V_{IN}}{2 \cdot [1 + s \cdot R_{Dio}(C_{D9} + C_{Dio})]}, \tag{2.1}$$

where $R_{Dio}$ and $C_{Dio}$ are the impedance and parasitic capacitance of the VCSEL diode respectively. $C_{D9}$ is the parasitic capacitance of the drain of $M_9$. Because of the low mobility of PMOS transistor compared to that of NMOS device, the size and thus the parasitics of $M_9$ are relatively large even if implemented with a thin oxide device. Together with the VSCEL parasitics, this is the main limitation the driver speed.

Compared to the right branch of the output driver, the left branch (which consists of $M_1$, $M_3$, $M_5$ and $M_6$) has much less parasitics load. In order to reach a speed of 10 Gb/s, a feedforward path can be built between the two branches by the coupling capacitor Cc [7]. In this design, we

further boost the speed of the left branch by the active inductor load, which consists of $M_5$ and $M_6$, to enhance the feedforward strength at high frequencies. The high-frequency current output loss can be compensated by the compensation current generated by the feedforward path. This compensation current $I_{COM}$ can be represented by

$$I_{COM}(s) = \frac{g_{m1,2}g_{m9}g_{m6}C_C(1 + s\frac{C_{GS5}}{g_{m6}}) \cdot V_{IN}}{2\left[s^2C_CC_PC_{GS5} + sC_{GS5}g_{m6}(C_C + C_P) + g_{m6}g_{m5}(C_C + C_P)\right]}. \tag{2.2}$$

In (2.2), $C_P$ is the parasitic capacitance at the gate of $M_9$. To get an idea on the bandwidth of $I_{COM}$, we can simplify (2.2) by assuming $C_P \ll C_C$,

$$I_{COM}(s) = \frac{g_{m1,2}g_{m9}C_C(1 + s\frac{C_{GS5}}{g_{m6}})}{2g_{m5}C_C(1 + s\frac{C_{GS5}}{g_{m5}})} \cdot V_{IN} \tag{2.3}$$

From (2.3), the bandwidth of $I_{COM}$ is mainly determined by the size and biasing condition of $M_5$ which has much less parasitics than the output of the right branch. Moreover, the zero determined by the size and biasing condition of $M_5$ can further boost the bandwidth. Because the feedforward signal is superimposed to the output node, the overall bandwidth is boosted by the feedforward compensation path.

### 2.3.2 Configurable rising/falling-edge pre-emphasis

One important difference between a VCSEL and the ideal RC load is its asymmetry on the rise time and fall time in the transient response. In order to reduce this asymmetry, we implemented a programmable rising/falling-edge pre-emphasis in the output driver, where the pre-emphasis can be set on either the rising edge, falling edge or both edges. Similar to the GBLD10, the pre-emphasis is realized by generating a high-frequency zero in the frequency domain [4]. As shown in figure 5, the output driver is source-degenerated by a RC network to generate the required zero. To tune the

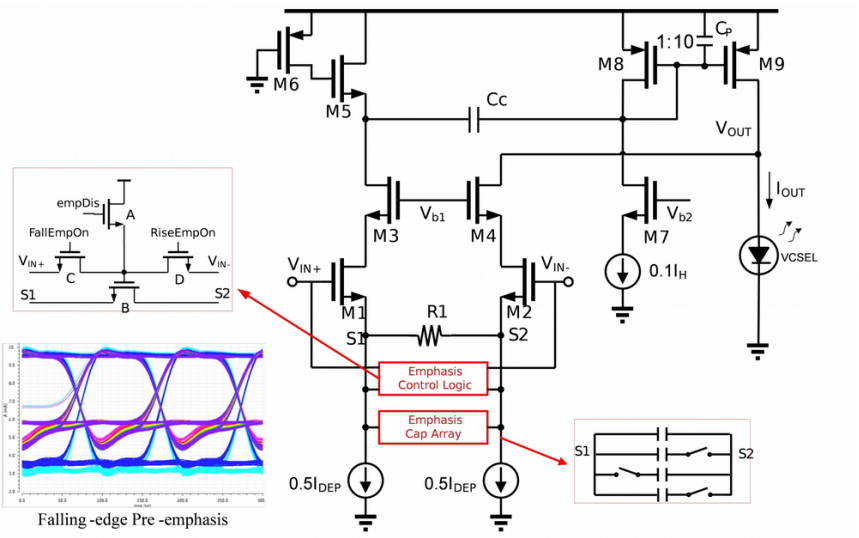



**Figure 5.** Configurable edge pre-emphasis in output driver.

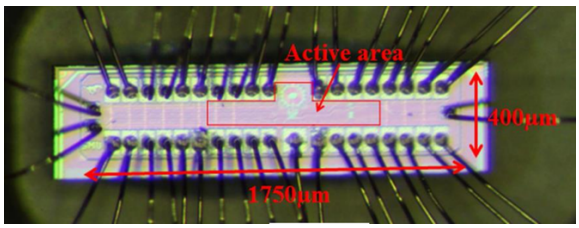
zero location so as to change the pre-emphasis amplitude, an emphasis capacitor array, controlled by a 3-bit DAC, is used in this RC network.

To make the edge pre-emphasis configurable, an emphasis control logic that can sense the input signal edge is implemented. As shown in figure 5, if the pre-emphasis is configured to be falling edge only, switch C is ON while switch A and D are OFF. With this configuration, switch B transits from ON to OFF during the falling edge of $V_{IN+}$ (so as the output current), which makes the RC degeneration effective and generates the emphasis peak in the output current. On the other hand, the pre-emphasis is disabled at the rising edge of $V_{IN+}$ because the RC network is shorted by switch B. Similarly, the rising edge only pre-emphasis or both edge pre-emphasis can be achieved by enabling switch D or both C and D respectively. The pre-emphasis function can be easily turned OFF by setting switch A and B ON so the degeneration network is always disabled regardless of the input signal.

### 2.4 GBLD10+ implementation

The GBLD10+ is implemented in a 9-metal 65-nm CMOS technology. The high-speed signals are routed with the thick top metal layers to reduce parasitics. Figure 6 (a) and (b) show the layout and chip photo of the GBLD10+. A three-terminal octagonal inductor with a diameter of 130 $\mu$m is used in the limiting amplifier. The die size is 1750 $\mu$m $\times$ 400 $\mu$m including PADs and seal-rings, with an active area of only 0.16 mm$^2$.


**(a)**




**(b)**

**Figure 6.** GBLD10+ implementation: (a) layout; (b) die photo.

## 3 Test results

Electrical tests have been carried out to characterize the GBLD10+ performance. An Agilent J-BERT N4903B was used to generate the differential PRBS input signal which is AC coupled to the chip. An Agilent DSA91204A oscilloscope was used to measure the outputs.



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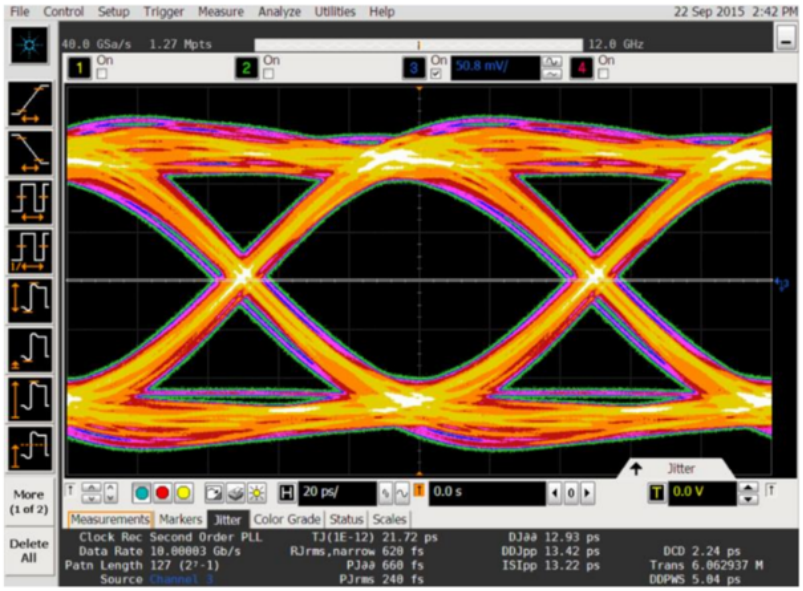
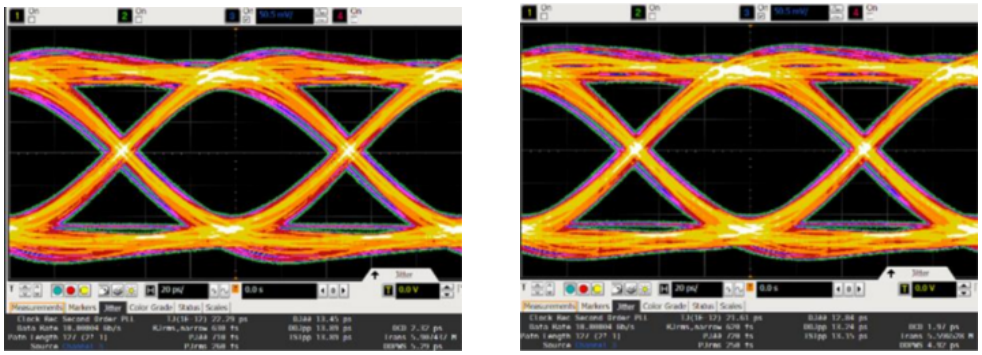



**Figure 7.** 10 Gb/s electrical eye diagram at 400 mV input swing.



**(a)** **(b)**

**Figure 8.** 10 Gb/s electrical eye diagram at different input swings: (a) 200 mV input swing; (b) 1.2 V input swing.

The jitter performance at 10 Gb/s has been measured with PRBS $2^7 - 1$ input data and at a BER of $10^{-12}$. Figure 7 shows the electrical eye diagram with a 4 mA modulation depth with the differential input swing of 400 mV. The total jitter in the electrical eye is 21.72 ps with an RMS random jitter component of 0.62 ps and a data-dependent jitter component of 13.42 ps peak-to-peak.

To test the function of the limiting amplifier, electrical eye diagrams at different input swings were measured. As shown in figure 8, the test results show that the GBLD10+ can accommodate a differential input swing from 200 mV to 1.2 V and maintain the stable modulation amplitude and jitter performance.

The supply current of the GBLD10+ has been measured at the default current settings for modulation height and depth. The measurements show 9 mA current consumption for the 1.2 V supply and 8 mA current consumption for the 2.5 V supply, which makes the total power of only 31 mW.



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A mistake in digital I/O pads prevented the full characterization of the chip. More measurement results on pre-emphasis, radiation tolerance and optical tests are expected after the Focused Ion Beam (FIB).

Table 1 compares the performance of the GBLD10+ with the GBLD10. Operating at the same speed of 10 Gb/s, the GBLD10+ has significant advantages in terms of the power consumption and die size. Moreover, compared to the differential AC coupling approach in the GBLD10 where external components on the PCB are needed, the GBLD10+ uses direct bonding to couple the VCSEL laser diode, greatly simplifying the PCB design and lowering the cost.

**Table 1.** Performance comparison power.

| **Parameters** | **GBLD10** | **GBLD10+** |
|---|---|---|
| Technology | 130-nm CMOS | 65-nm CMOS |
| Speed | 10 Gb/s | 10 Gb/s |
| Total Jitter (Electrical) | 14 ps | 22 ps |
| Power Consumption* | 85 mW | 31 mW |
| Die Size | 2 mm × 2 mm | 1.75 mm × 0.4 mm |
| Laser Coupling Method | differential AC with external components | single-ended direct bonding |

* Power consumption is tested at default register settings after power-on reset operation.

## 4 Conclusion

A 10 Gb/s VCSEL low power laser driver (GBLD10+) has been designed in a 65-nm CMOS technology. To meet the speed requirement within a compact die size, a shared-inductor peaking and a feedforward approach have been used in the limiting amplifier and output driver respectively. A programmable pre-emphasis function, implemented by RC source degeneration technique, has been proposed to balance the rise and fall times of the optical signal. Measurements show that the GBLD10+ is able to achieve the speed of 10 Gb/s with a power consumption of only 31 mW. The whole chip has a compact die size of 1.75 mm × 0.4 mm, allowing users to drive the VCSEL die and choose the transmitter channel count by die-to-die bonding. The direct bonding method of coupling the laser diode used in GBLD10+ eliminates the need for external components on the PCB, which simplifies the board design and lowers the implementation costs.

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