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Received: *October 6, 2015*
Accepted: *November 17, 2015*
Published: *January 8, 2016*

17th International Workshop on Radiation Imaging Detectors
28 June – 2 July 2015,
DESY, Hamburg, Germany

Towards a new generation of pixel detector readout chips

2016 JINST 11 C01007

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Abstract: The Medipix3 Collaboration has broken new ground in spectroscopic X-ray imaging and in single particle detection and tracking. This paper will review briefly the performance and limitations of the present generation of pixel detector readout chips developed by the Collaboration. Through Silicon Via technology has the potential to provide a significant improvement in the tile-ability and more flexibility in the choice of readout architecture. This has been explored in the context of 3 projects with CEA-LETI using Medipix3 and Timepix3 wafers. The next generation of chips will aim to provide improved spectroscopic imaging performance at rates compatible with human CT. It will also aim to provide full spectroscopic images with unprecedented energy and spatial resolution. Some of the opportunities and challenges posed by moving to a more dense CMOS process will be discussed.

Keywords: Solid state detectors; Hybrid detectors; Electronic detector readout concepts (solid-state)

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doi:10.1088/1748-0221/11/01/C01007

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1 Introduction

The Medipix3 Collaboration has undertaken two major ASIC developments since its creation in 2005. The Medipix3 readout chip aims at spectroscopic X-ray imaging at relatively high X-ray fluxes. In order to mitigate the degradation of energy resolution by charge sharing between pixels a novel charge summing and allocation scheme is implemented permitting neighbouring pixels to communicate on an event-by-event basis and allocate each hit with its total deposited energy to one pixel only. The Timepix3 chip, on the other hand, aims to send continuously as much information as possible off chip for data processing. For both chips the peripheral circuitry has been kept to a strict minimum to reduce the dead area in case large surfaces have to be covered. Both chips are also "Through Silicon Via (TSV) ready", that is to say that the design of the wire bonding pads is such that they can be accessed from the rear of the chip for TSV processing. TSV's on the IO pads obviate the need for wire bonds further diminishing the required dead area between chips on a large surface.

This paper highlights recent results obtained using the Medipix3 and Timepix3 chips. It also describes in some detail the results of the TSV processing of wafers composed of these chips. These are so promising that we feel confident to propose new chip architectures which will make full use of TSV's. The basic features of the next generation of chips are outlined.

2 Some highlights from the Medipix3 and Timepix3 ASIC's

The various iterations of the Medipix3 chip are already described in detail in the literature [1–3]. A short reminder of the functionality is provided here for completeness. The chip is composed of a matrix of 256×256 pixels on a pitch of 55 μm. Following the amplification and discrimination process which takes place within each pixel, inter-pixel logic ensures that simultaneous hits in a local region are allocated to one single pixel only (the pixel with the largest charge). While this process is taking place summing circuits at the four pixel corners add up the charge in each 2×2 pixel cluster. It is the corner sum with the highest charge in the allocated pixel which determines the

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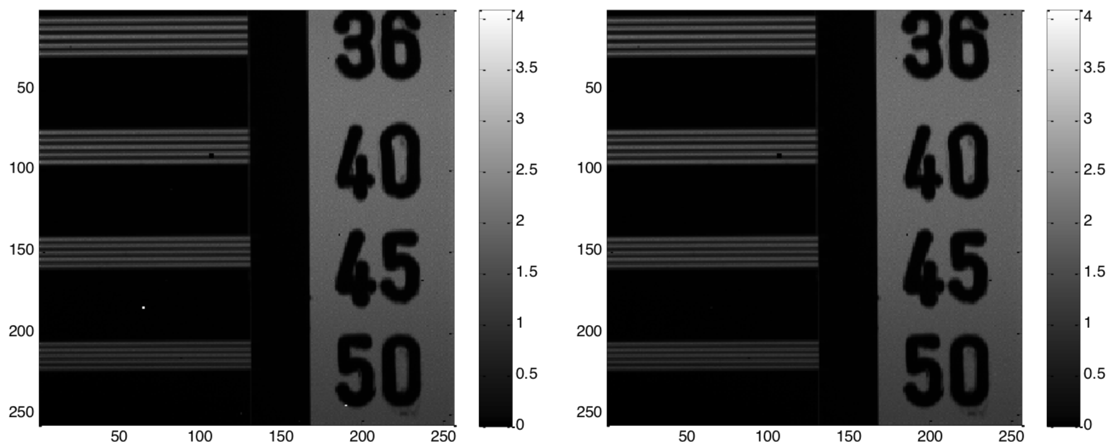

Figure 1. Line pair mask images for the Medipix3RX chip connected to a 300 μm thick Si sensor in single pixel mode (left) and charge summing mode (right) [3].

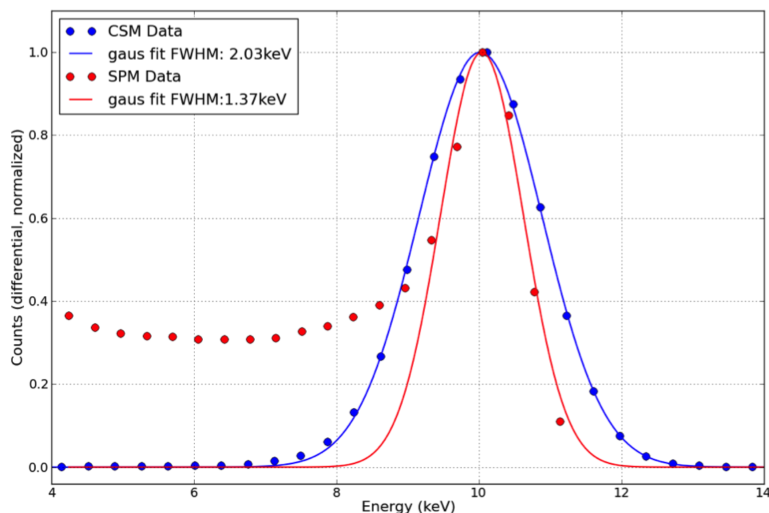

Figure 2. Threshold scans of the Medipix3RX chip connected to a 300 μm thick Si sensor in single pixel mode (SPM) and Charge summing mode (CSM). CSM results in the suppression of the charge sharing tail at the expense of a slightly degraded energy resolution [4].

attribution of a hit to a given energy bin. This process works both at a sensor pixel pitch of 55 μm and 110 μm (whereby only one in 4 corresponding readout pixels is connected to the sensor and each large pixel uses the circuitry of the four 55 μm pixels). Figure 1 [3], which shows line pair mask images for a 55 μm pitch and 300 μm thick Si sensor, proves that the spatial resolution of the system is identical for images taken with the charge summing and allocation scheme switched on or off. Figure 2 [4] shows threshold scans for a similar detector when exposed to a monochromatic beam of 10 keV X-rays. These are generated by plotting the total number of hits in the full chip at different threshold levels and then differentiating the curve with respect to threshold. While the energy resolution in the photo peak in charge summing mode is degraded with respect to single pixel mode

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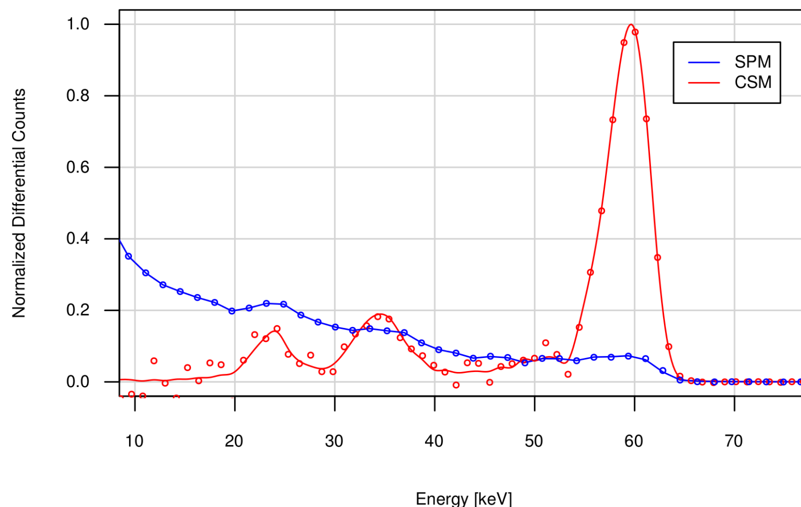

Figure 3. Threshold scans of the Medipix3RX chip connected to a 2 mm thick CdTe sensor at a sensor pixel pitch of 110 μm in single pixel mode (SPM) and charge summing mode (CSM) [5].

the suppression of the charge sharing tail is evident. The impact of the charge summing scheme is even more pronounced for a 2mm thick CdTe detector with a pixel pitch of 110 μm exposed to an ^{241}Am source, see figure 3 [5]. When charge summing and allocation is switched off the energy information is almost completely lost because of charge sharing (due to both fluorescence during charge deposition and diffusion during charge collection) but when charge summing is switched on spectroscopic information becomes again visible. However, a degradation in the dead time of a factor of about 4 has been measured with charge summing and allocation active [5].

The Timepix3 chip [6] takes an approach to signal treatment which is almost orthogonal to the Medipix3 approach; in this case each pixel sends as much information as possible off chip as soon as a hit is detected. Pixel coordinates, Time over Threshold (ToT) and particle arrival time (ToA, measured to a precision of 1.56 ns) are sent off chip. The maximum flux which can be read out correctly is 80Mhits/sec per chip. A global shutter is used to stop or activate detection but, as long as the shutter is open, data is continuously driven off chip as soon as it is generated. Using this mode spectroscopic X-ray imaging is also possible [7], but at a significantly lower flux than that permitted by Medipix3. On the other hand, much more information is available for analysis as the time stamp permits off-line clustering and the number of energy bins used can be chosen a posteriori according to the needs of the application. Moreover, there are many other applications which can take advantage of the data driven architecture and the precise time stamp. For example, if a charged particle crosses more than one pixel at a grazing angle the drift time of the generated charge will be slightly different from pixel to pixel. After careful calibration for timewalk it is possible to reconstruct the charged track effectively providing a vector from a single semiconductor layer. (Of course, it is impossible to determine the arrow of the vector as the charge is deposited at the speed of light.) An example of this is shown in figure 4 where the measured ToT and arrival time (normalised to the hit on the sensor pixel nearest to the readout chip) are plotted for a cosmic particle crossing the sensor at a high incident angle. In figure 5 [7] the reconstructed track is shown where the diffusion of the drifted charge is evident.

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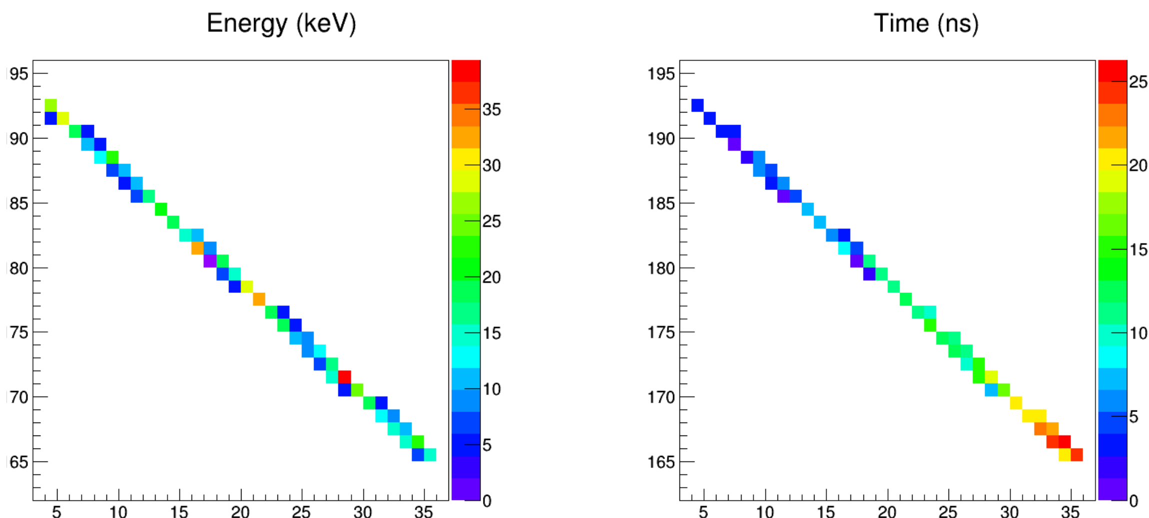

Figure 4. A high energy cosmic track as imaged by the Timepix3 chip. The plot on the left indicates the ToT data showing a uniform deposition of charge throughout the depth. On the right the ToA data indicates the arrival time of the drifted charge at the pixel chip normalised to the charge from the pixel nearest the chip.

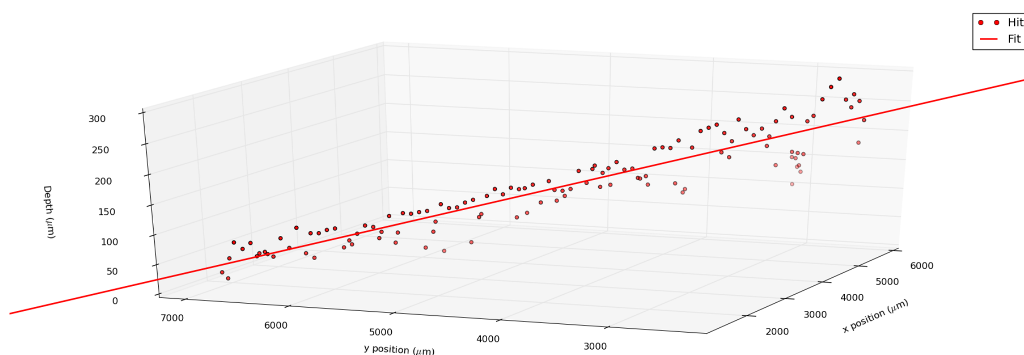

Figure 5. The data shown in figure 4 has been reconstructed to shown the 3D view of the charge in the silicon sensor [7].

3 Tiling larger areas using Through Silicon Vias

Vertex detectors for high energy physics and X-ray detectors for synchrotron light applications require large and preferably contiguous hermetically covered sensitive areas. Vertex detectors at particle colliders are often cylindrical in shape and there is a strict requirement to minimise the material encountered by traversing charged particles. On the other hand large area X-ray detectors are usually composed of flat panels. Pixel detector readout chips are normally limited in size by the dimensions of the reticle used in CMOS processing. In some special cases chip stitching may be permitted but that, in turn, puts a severe restriction on which processes can be used and may lead to low yield. In the case of hybrid pixel detectors until now the chips normally use up most of the reticle and are designed to be abutted on 3 sides. This allows the construction of sensor ladders which are composed of multiple large readout chips which are flip chip bonded to a single

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larger sensor. The sensor pixels at the stitching region between neighbouring readout chips are stretched such that spatial resolution in one dimension is degraded but there is no loss in detection efficiency. However, the area of the sensor guard ring and, in particular, the readout chip periphery both contribute to detector material without being sensitive. In the case of vertex detectors the ladders are typically arranged mechanically such that the chip periphery is in the shadow of an area of sensitive detector, an example is described in [8]. Some large area flat panel X-ray detectors use edgeless sensors and a roof tile geometry to avoid dead areas between single chip assemblies or ladders [9] but for synchrotron light applications some dead area can usually be tolerated [10–13].

TSV readout promises to help in reducing dead area. Three separate projects have been undertaken with CEA-LETI in order to develop TSV processing on the IO pads of Medipix3 and Timepix3 wafers. Although TSV-last processing was deemed to be mature in 2011 quite some refinement and tuning of the LETI process was necessary to make it fully compatible with these ASICs which are intended for use in pixel detector readout.

In a first project launched in 2011, 10 low yield Medipix3 wafers were provided to LETI. The wafers contain around 100 chips and each chip has around 100 wire bonding pads which were prepared for TSV processing; the metallisation layers under the pads extended all the way down to the bottom metal layer and gate and poly filling structures were excluded under the pads. The necessity to omit the filling structures was a lesson learnt from a prior effort at TSV processing with Medipix2/Timepix devices in the context of the RELAXd project [14]. TSVs should connect these pads to an array of BGA-compatible pads on the rear of the chip. Since the chips are to be bump bonded to sensors after TSV processing, a unique requirement for these wafers was that Under Bump Metallisation (UBM) had to be deposited on the front side passivation openings (about 25 μm diameter) prior to rear side processing. Another complication is that in the ASIC process used for these chips the top metal layer is not planarised and therefore the surface of the wafers had steps of 4 μm corresponding to the pattern of the top metal. This imposes restrictions on lithography and led to challenges during post dicing de-bonding of chips. The results of that project are summarised in [15]. The TSV diameter chosen was 60 μm (to match a wire bond pad pitch of roughly 100 μm) and the wafers were thinned to 120 μm to provide an optimised aspect ratio of 2. Figure 6 shows an

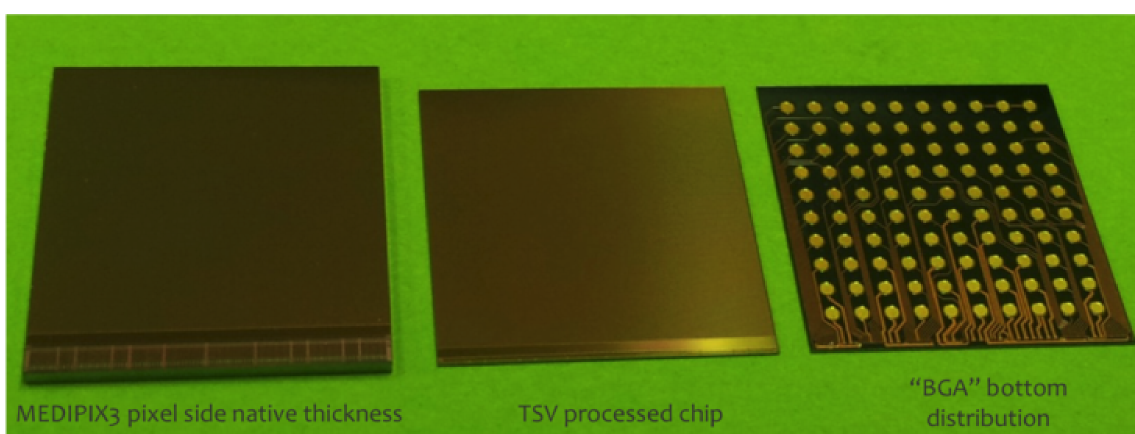

Figure 6. A chip diced from a native thickness wafer is compared with the front and rear faces of chips which have been TSV processed.

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Figure 7. Image of a dried fish taken using a TSV processed Medipix3 chip connected to a 300 μm thick Si sensor

image of 3 die. On the left is shown a Medipix3 chip which has been diced from a wafer with native thickness (~ 725 μm). The front and rear views of chips following TSV processing and dicing are in the middle and on the right of the image. The redistribution layer and the BGA compatible array of pads are clearly evident on the chip on the right hand side. A small number of these were flip chip connected to standard silicon sensors. Figure 7 shows an X-ray image of a small fish taken with one of these assemblies and read out through the TSVs. The bump bonding quality is excellent even if there is a spot of unexplained insensitive area at the bottom of the image.

In a second project which was launched in 2013, 6 high yield Medipix3RX wafers were made available to LETI. The same masks and processing steps which had been established during the first run were used. Once again UBM was deposited on the front of the wafers and the IO pads were connected using TSVs to the array of BGA compatible pads on the rear side of the chip. The aim of this project was to evaluate the yield of the TSV processing. Due to equipment limitations a number of chip failures around the edge of the wafer were foreseen. Wafers were tested prior to TSV processing and diced chips were tested after processing. Since each chip has a unique identifier it was possible to reconstruct wafer maps from the measurements of the diced chips. An example of one wafer is shown in figure 8. One can clearly observe the expected loss of components around the edge of the wafer. However, the yield is otherwise good. Table 1 quantifies the yield of all wafers processed. We concluded from this project that the TSV yield is adequate for small scale production.

A third project was devised aimed at producing ‘ultra-thin’ TSV-processed readout chips ready for flip-chip assembly. We aimed at thinning the wafers to 50 μm in order to permit the production of extremely thin assemblies primarily for vertex detector applications in high energy physics. 2 Medipix3RX wafers and 2 Timepix3 wafers were provided to LETI. In order to optimise the aspect ratio of the TSV’s the diameter was reduced to 40 μm. New masks were prepared for the Timepix3 wafers and one mask was changed for the Medipix3RX wafers in order to accommodate the smaller TSV diameter. All wafers were processed successfully. Only the Medipix3RX components have been tested until now and the results are consistent with those of the 2nd run. The dice appear to be

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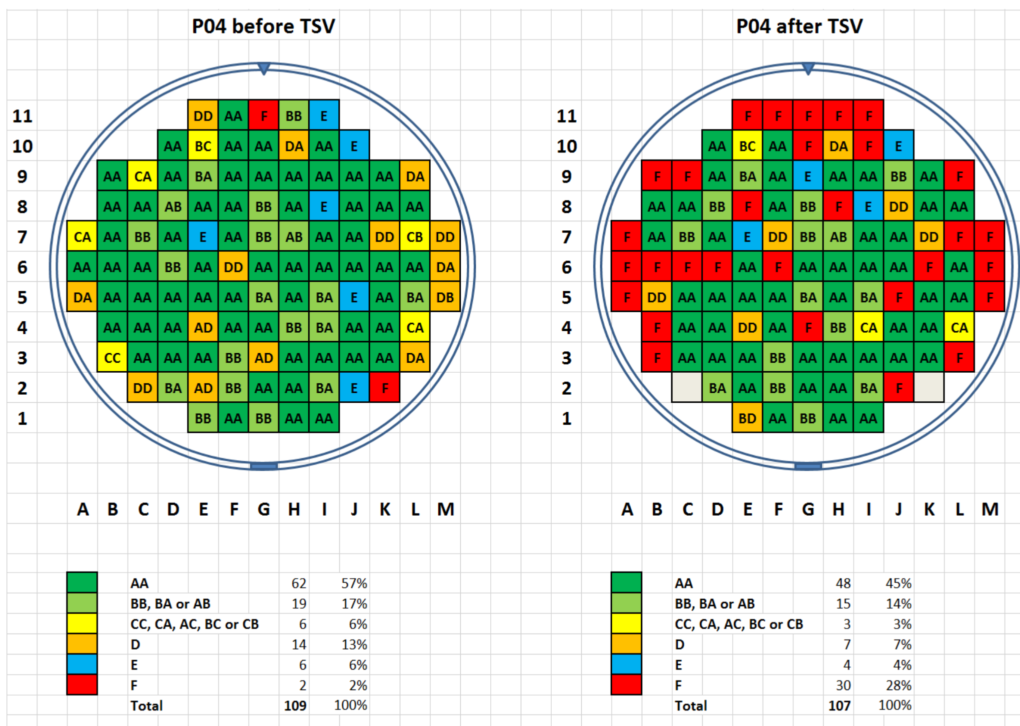

Figure 8. A typical wafer map from the 2nd run at LETI using Medipix3RX wafers. Class AA means perfect chip, Class Bx are with one bad column over 256, Class Cx are with two, Class Dx with more than two, Class E with bad internal DAC(s) and class F not functional (bad communication and or power failure).

Table 1. Yield measured on all Medipix3RX wafers of the 2nd run before and after TSV processing.

	Lot no. uSA999P			Lot no. uSB254P		
Wafer number	P04	P05	P06	P01	P02	P03
%KGD before TSV	57	51	50	50	60	53
%KGD after TSV	45	41	rework	20	41	38

flat visually and are mechanically robust. Figure 9 is a side view image comparing 2 TSV-processed die; one from the second lot (120 μm thick) and one from the third lot (50 μm thick). Flip chip assembly is planned in the near future.

4 Medipix4 and Timepix4

Moore's law continues to govern progress in microelectronics and provides the semiconductor detector community with new opportunities and challenges. On the side of opportunities it is possible to implement a higher number of transistors in a given area providing designers with the option of packing new functionality into a pixel of a given size. Alternatively, the pixel size may be reduced. The challenges are partly technical and partly organisational. On the technical side the only available wafer size is 300 mm and this may pose problems for some wafer post processing steps, in particular bump bonding. Wafer size, however, is not considered to be an issue for TSV-last

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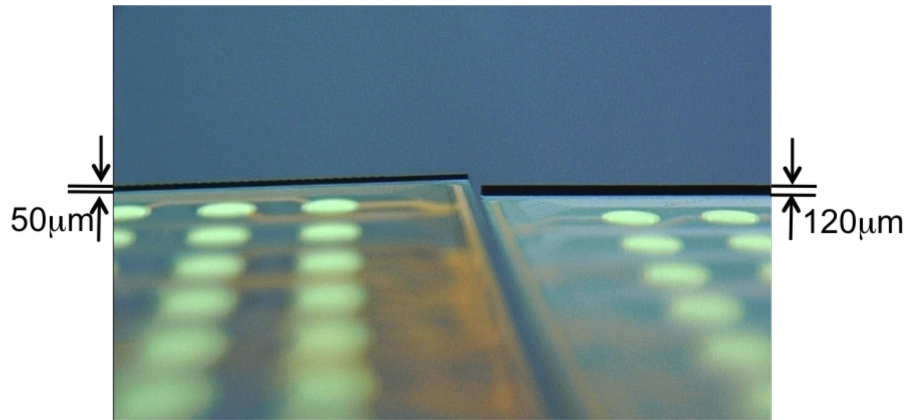

Figure 9. Microscope photo of two TSV processes Medipix3RX die. The die on the left has been thinned to 50 μm on the right to 120 μm. The rear side redistribution layers and BGA compatible pads are also visible

processing as most modern semiconductor back-end equipment is designed for 300 mm wafers. Cost and mainly the cost of prototyping, on the other hand, represents a major organisational challenge. As an example, the cost of a mask set for a 65 nm CMOS process is approximately double that of a 130 nm process. This implies that efforts must be grouped and full use should be made of a given reticle. We propose to address these organisational issues by developing 2 large chips, Medipix4 and Timepix4, implementing them together on the same reticle.

The detailed characteristics of the chips will be determined and agreed upon by those institutes who become collaboration members. However, some of the main features can already be identified.

In the case of Medipix4 a particular emphasis will be placed upon providing spectroscopic X-ray images at rates which are compatible with applications in human CT. The exact number of thresholds etc. will be determined by the space available. Like Medipix3 the pitch of the sensor pixels can be adapted to match the sensor material and the readout chip will be compatible with various sensor pixel pitches. Timepix4 will aim at improved time stamping (sub-ns) and a reduced pixel pitch. For both chips we will aim to implement the functions normally associated with the chip periphery throughout the pixel matrix taking full advantage of the opportunities provided by the TSV process. As the readout logic is no longer confined to one chip edge there is more flexibility in the choice of readout architectures. The chips should be abuttable on 4 sides. This, however, will impose a design based on slightly smaller ASIC pixel dimensions with respect to the sensor pixels.

5 Conclusions

The Medipix3 architecture has been proven to provide an effective solution to the issue of charge sharing in spectroscopic X-ray imaging. Spectral fidelity is restored at the expense of energy resolution in the peak and count rate. The Timepix3 chip has a fully data driven architecture and can be used for spectroscopic X-ray imaging at lower fluxes than Medipix3. However, it is probably most useful in applications where data is sparse and where the ability to tag hits with a precise time stamp is required. Both chips are prepared for TSV processing and wafers have been processed with good yield down to thicknesses of 50 μm. This gives us the confidence to propose a new generation

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of pixel detector readout chips which can be tiled on 4-sides eliminating one of the barriers to covering large sensitive areas

Acknowledgments

This work was carried out in the context of the Medipix3 Collaboration. We are especially grateful for the fruitful collaboration with the team in CEA-LETI, Grenoble which was led initially by David Henry and later by Gabriel Pares. The work on TSV's was also supported by CERN-LCD, the AIDA project and the ALICE ITS collaboration.

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