The Prototype Design of gFEX – A Component of the L1Calo Trigger for the ATLAS Phase-I Upgrade

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***Abstract*—The ATLAS experiment will follow the upgrade steps of the Large Hadron Collider (LHC), which will undergo a series of upgrades to increase the luminosity in the next ten years. During the Phase-I upgrade, a new component will be designed for the ATLAS Level-1 calorimeter trigger system to maintain the trigger acceptance against the increasing luminosity - the global feature extractor (gFEX). The gFEX is intended to identify patterns of energy associated with the hadronic decays of high momentum Higgs, W & Z bosons, top quarks and exotic particles in real time at the LHC crossing rate. A prototype v1 with one System-on-Chip Xilinx ZYNQ FPGA, and one Vertex-7 FPGA for technology validation has been designed and tested in 2015. With the lessons learned from the prototype v1, a prototype v2 with three UltraScale FPGAs and one ZYNQ FPGA is implemented on an ATCA module. This board will receive coarse-granularity information from the entire ATLAS calorimeter on 276 optical fibers at the speed up to 12.8 Gb/s synchronous to the 40 MHz LHC clock. The test results of the prototype v2 show that the main gFEX functionalities are working well. Currently it is being used as the test platform for trigger algorithm development and integration with other detector systems. Based on the prototype v2 design, a prototype v3 design, the final prototype before production, has been started. This features a ZYNQ UltraScale+ FPGA and more fiber optical links to provide compatibility for the High-Luiminosity upgrade of the LHC (HL-LHC).**

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I. Introduction

THE Large Hadron Collider (LHC) will undergo a series of significant upgrades during the next ten years, which allow both collision energy and luminosity to increase. The ATLAS experiment [1] will follow the same upgrade schedule. During the Phase-I upgrade [2], the ATLAS first-level trigger (Level-1) will be updated with the Feature Extractors in the calorimeter trigger system (called L1Calo) against increasing luminosity: the Electron Feature Extractor (eFEX) [3], the Jet Feature Extractor (jFEX) [4], and the Global Feature Extractor (gFEX). The gFEX receives all calorimeter data in a single module and thus enables the use of full-scan algorithms.

The gFEX is used to select large-radius (large-R) jets, typical of Lorentz-boosted objects, by means of wide-area jet algorithms refined by subject information. It is intended to identify patterns of energy deposition in the calorimeter associated with the hadronic decays of high momentum Higgs, W & Z bosons, top quarks, and exotic particles in real time at the LHC crossing rate. The high-p_T bosons and fermions are a key component of the ATLAS physics program. The current ATLAS Level-1 trigger system (L1Calo) was designed for narrow jets with limited acceptance for large objects. The acceptance for large-R jets will be greatly enhanced by the inclusion of the gFEX in the L1Calo system.

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II. Prototype Design of gFEX

The gFEX is a single ATCA (Advanced Telecommunications Computing Architecture) module with several large Field Programmable Gate Arrays (FPGAs) for data processing, and a combined FPGA & CPU System-on-Chip ZYNQ FPGA for control and monitoring. A special feature of the gFEX is that it receives data from the entire calorimeter enabling the identification of large-R jets and the calculation of whole-event observables. Each processor FPGA has 2π azimuthal (ϕ) coverage for a slice in pseudorapidity (η) and executes all feature identification algorithms. The processor FPGAs communicate with each other via low-latency GPIO (General-Purpose Input/Output) links while input and output to the board are via Multi-Gigabit Transceivers (MGTs). The gFEX is a customized ATCA module based on the PICMG® 3.0 Revision 3.0 specification [5]. The gFEX module will likely be placed in a sparsely populated ATCA shelf so that it can occupy two slots if needed: one for the board and one for cooling (e.g., large heat sinks), fiber routing, etc.

A. Prototype V1

The gFEX prototype v1 has been designed to verify all the functionalities of the chosen technical solutions: the power on sequence, power rails monitoring, clock distribution, MGT link speed and high-speed parallel GPIO links. One ZYNQ FPGA and one processor FPGA, Xilinx Virtex-7, are included on this prototype. There are also several MiniPODs [6], MicroPODs [7], power modules and high-speed parallel GPIOs between two FPGA implemented on the board.

The gFEX prototype v1 was tested in the lab in 2015 to verify all functionalities suceessfully. All the 80 channels of GTH transceivers of the Virtex-7 FPGA and 16 channels of GTX transceivers of the ZYNQ FPGA have been tested at 12.8 Gb/s with Bit Error Rate (BER) $< 10^{-15}$. The 50-bit parallel GPIO data bus has been tested running stably at 960 Mb/s in 480MHz DDR mode with good margin ($> 65\%$) .

The gFEX prototype v1 was used in the link-speed test between LAr (Liquid Argon Calorimeter) and L1Calo in January 2016. The LAr-L1Calo link-speed test was to determine the link speed between two systems in the Phase-I upgrade. The test results show that the links between the LDPB (Liquid Argon Digital Processing Blade) and gFEX are stable at both 6.4 Gb/s and 11.2 Gb/s without any error data observed, except

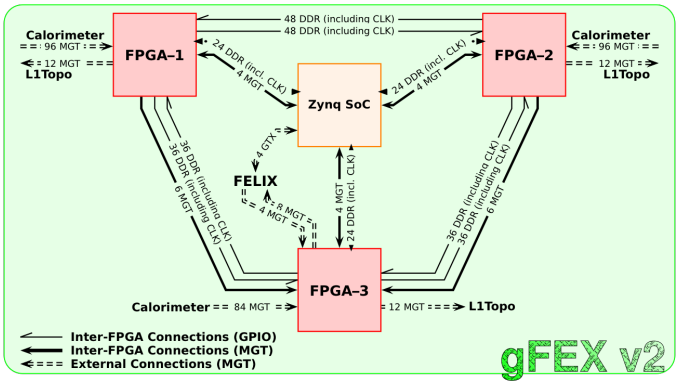

Fig. 1. Architecture of gFEX prototype v2

two links that have known issues at the LDPB TX side [8]. The link speed test between LDPB and eFEX was carried out in April 2016. Based on the successful LAr-L1Calo link speed test, it was agreed to use 11.2 Gb/s as the baseline link speed, with options of 9.6 Gb/s and 12.8 Gb/s.

B. Prototype V2

The gFEX prototype v2 is a full functional prototype. As shown in Fig. 1, there are a total of four FPGAs implemented on the module. Three Virtex UltraScale FPGAs are used as processor FPGAs, and one ZYNQ FPGA is for control and monitoring.

Processor FPGAs receive data from the electromagnetic and hadronic calorimeters via optical fibers. There are a total of 276 MGTs signals from the calorimeters. The core trigger algorithms are implemented in the firmware of the processor FPGAs. After the trigger processing, the real-time data to the L1 Topological Trigger (L1Topo) [9] are sent by three processor FPGAs respectively with 12 MGTs per FPGA.

MGT links and GPIO links running in DDR mode are used among FPGAs to share information during the trigger processing. One processor FPGA and ZYNQ also interface to FELIX (Front End LInk eXchange) [10] for triggered data readout. The ZYNQ FPGA receives TTC (Timing, Trigger and Control) information through the FELIX link. The recovered TTC clock goes through a high-performance clock generator (Si5345) with jitter-cleaning capability to improve the clock quality, which is crucial to ensure the links run stably above 10Gb/s.

The floor plan of the gFEX prototype v2 design is shown in Fig. 2. It includes detailed interconnections between FPGAs, between FPGAs and MiniPODs, and between the ZYNQ FPGA and other peripheral components, such as GbE, SD card, DDR3 memory and IPMC (Intelligent Platform Management Controller) [11]. The gFEX prototype v2 is a 26 layers board with 28 MiniPODs mounted. It is designed and manufactured with low-loss material (Megtron-6), and back drilling technology is adopted in its fabrication to reduce the influence of stubs on high-speed links performance.

1) Lab Test of Prototype V2: The assembled gFEX v2 prototype shown in Fig. 3 was received in June 2016, and evaluation has been carried out at BNL. The basic functionalities of the four FPGAs have been verified successfully,

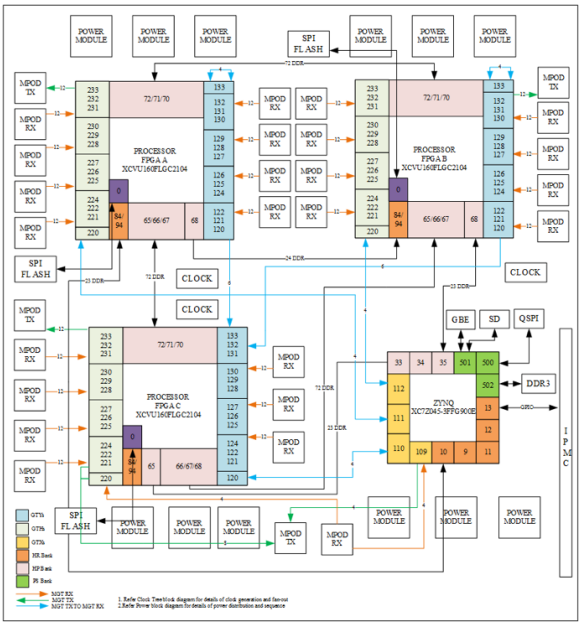

Fig. 2. Floor plan of gFEX prototype v2 design

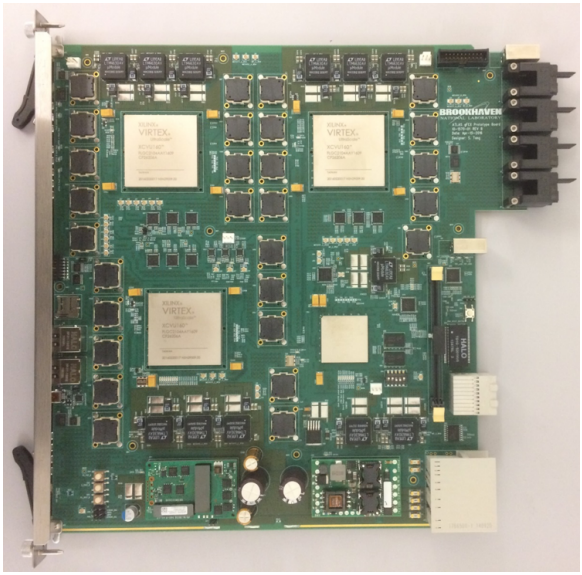

Fig. 3. Full assembly of gFEX prototype v2 board

including the on-board power and clock distribution circuit, FPGA configuration over JTAG and SPI flash, ZYNQ FPGA interface to DDR3 memory, GbE, SD card and I2C slaves, voltage, current and temperature monitoring.

Power consumption and thermal management has been studied on the gFEX prototype v2. With all the MGTs of the four FPGAs turned on and running at 12.8Gb/s, the power consumption except power input module is ∼300W with 28 MiniPODs populated. Taking into account the efficiency of the power input module, the total power consumption is ∼350W, which is well within the 400W power limit for a single ATCA module. The measured temperature of the FPGA is $\sim 67^{\circ}C$, and the temperature of the power module is $\sim 79^{\circ}C$, both are within the specified operating temperature range of the

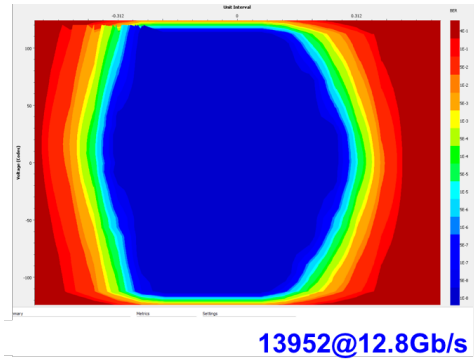

Fig. 4. Eye diagram of the optical link from processor FPGA transmitter to receiver going through MiniPODs and fiber

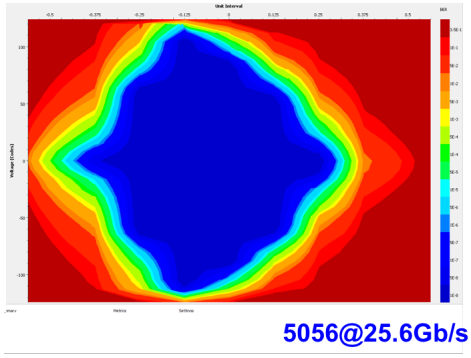

Fig. 5. Eye diagram of the electrical link from processor FPGA transmitter to receiver going through on board traces

components.

The parallel GPIO data bus has been tested running stably at 1.12 Gb/s in 560 MHz DDR mode with good margin ($>50\%$). The IBERT test has been used to characterize the high-speed link performance, including both fiber-optical links over MiniPODs, and also electrical links between FPGA MGTs on board. All links are stable at 12.8Gb/s with BER $< 10^{-14}$.

The eye diagram shown in Fig. 4 is measured on the optical link from the processor FPGA transmitter to receiver going through MiniPODs and optical fiber. The eye opening is 13952 at 12.8Gb/s. The one shown in Fig. 5 is measured on the electrical link from the processor FPGA transmitter to receiver going through on board traces, the eye opening is 5056 at 25.6Gb/s. Both eye diagrams are obtained from GTY transcievers on the FPGA, which perform better than GTH and GTX transceivers as reported in [12].

2) Integration Test of Prototype V2: The integration test between gFEX and FELIX was carried out at BNL in the fall of 2016, to prepare for the final design review of the gFEX. The integration test stand is shown in Fig. 6. The gFEX prototype v2 is on the test bench at the near end, while the FELIX is installed in the PC at the far end. gFEX uses the recovered TTC clock from the FELIX link as its system clock, and the jitter cleaner Si5345 is used to improve the clock quality. The GBT link from FELIX to gFEX is in low fixed-latency GBT mode, running at 4.8Gb/s, while the GBT link from gFEX to FELIX is in FULL mode running at 9.6Gb/s.

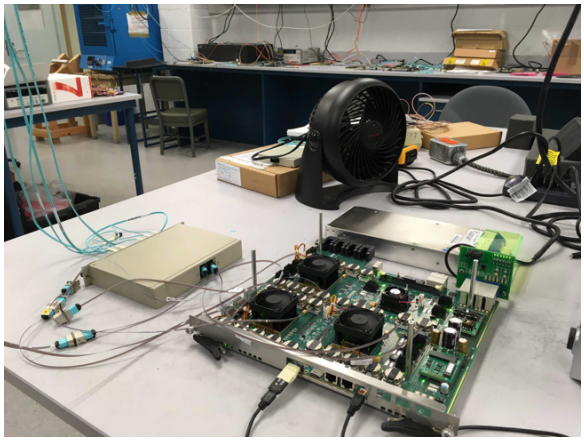

Fig. 6. Test stand of the gFEX and FELIX integration test. The gFEX prototype v2 is on the test bench at the near end, while the FELIX is installed in the PC at the far end

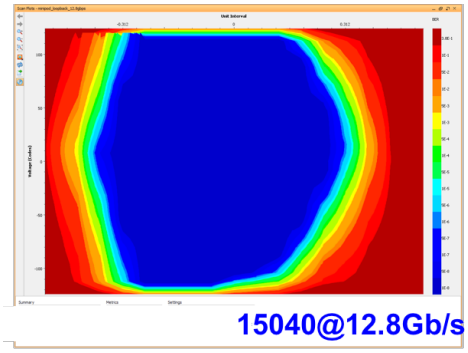

Fig. 7. Eye diagram of the electrical link from processor FPGA transmitter to receiver going through on board traces with recovered clock from FELIX

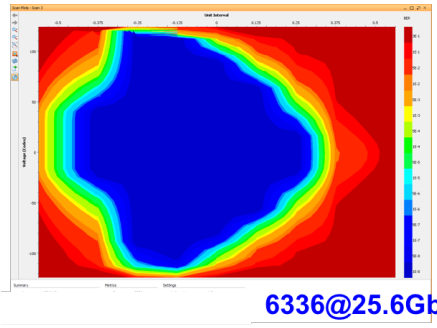

Fig. 8. Eye diagram of the electrical link from processor FPGA transmitter to receiver going through on board traces with recovered clock from FELIX

Links in both directions have been established between FELIX and gFEX successfully.

With the recovered TTC clock from FELIX, the GTH works well at a link speed of 12.8 Gbps, and the GTY works well at 25.6 Gbps. The eye diagram shown in Fig. 7 is measured on the optical link from the processor FPGA transmitter to receiver going through MiniPODs and fiber, the eye opening is 15040 at 12.8Gb/s. The one shown in Fig. 8 is measured on the electrical link from processor FPGA transmitter to receiver going through on board traces, the eye opening is 6336 at 25.6Gb/s. Both eye diagrams are measured with recovered

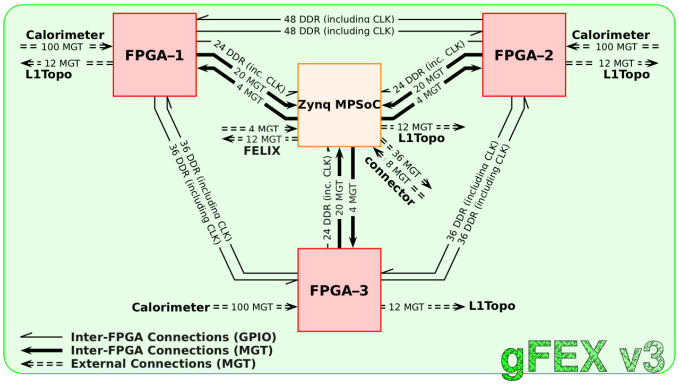

Fig. 9. Architecture of gFEX prototype v3

TTC clock, and they are comparable to the ones shown in Fig. 4 and 5.

The TTC clock can be distributed from FELIX to gFEX to establish stable high-speed links, which shows that the integration test between gFEX and FELIX is successful. Currently gFEX prototype v2 is being used as the test platform for trigger algorithm development and integration with other detector systems.

C. Prototype V3

Based on the experience of the gFEX prototype v2, the development of the prototype v3 has been started. The prototype v3 serves as the pre-production board: it will be the final prototype before the production and installation on detector. The architecture of the gFEX prototype v3 is shown in Fig. 9. As with prototype v2, there are in total four FPGAs on the module. Besides three Virtex UltraScale FPGAs as processor FPGAs, the ZYNQ FPGA is replaced by a ZYNQ UltraScale+ FPGA.

The gFEX prototype v3 can accomodate up to 300 input links from calorimeters. The ZYNQ UltraScale+ FPGA will be the only interface to FELIX, while all four FPGAs will send data to L1Topo, via 12 links each. All of these will provide better compatibility for gFEX to be used in in the High-Luiminosity LHC (HL-LHC) [13].

The floor plan of the gFEX prototype v3 design is shown in Fig. 10. It includes detailed interconnections among FPGAs, between FPGAs and MiniPODs, and between ZYNQ UltraScale+ FPGA and other peripheral components, such as GbE, SD card, DDR4 memory module and IPMC. The prototype v3 will be a 30-layer board with 34 MiniPODs mounted. It will be designed and manufactured with low-loss material (Megtron-6) with back-drilling technology. It is planned to have the prototype v3 design finalized by Spring 2017.

III. Summary

Two gFEX prototypes have been developed and evaluated successfully. The gFEX prototype v1 has been used in the LAr-L1Calo link speed test, to determine the baseline link speed of 11.2Gb/s. The prototype v2 has been designed and tested in the lab. High-speed fiber-optic links are stable at 12.8 Gbps, and on-board electrical links are stable at 25.6 Gbps. Parallel

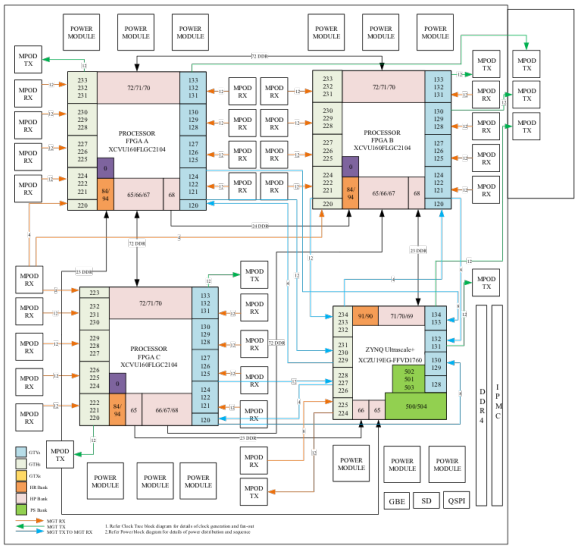

Fig. 10. Floor plan of gFEX prototype v3 design

buses operate at 1.12 Gb/s with good margin. The integration test with FELIX has been successful, and now the prototype v2 is being used as firmware development platform.

The gFEX prototype v3 design has been started with a new ZYNQ UltraScale+ on board. More input links from calorimeters and output links to L1Topo will be implemented for compatibility in HL-LHC. The design of prototype v3 is planned be finalized in Spring 2017.

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