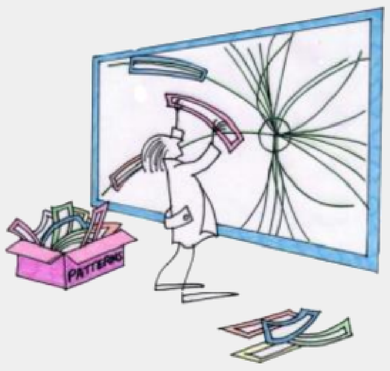

Design, Characterization and Test of the Associative Memory Chip AM06 for the Fast TracKer System

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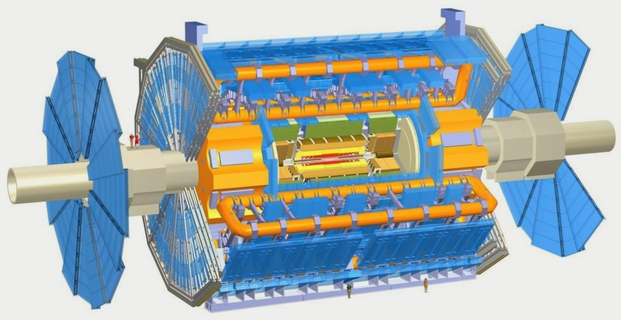
Abstract

The AM06 is a large Associative Memory chip specifically designed in 65 nm CMOS technology. It will be massively used in the Fast TracKer system, which is a part of the ATLAS detector upgrade.

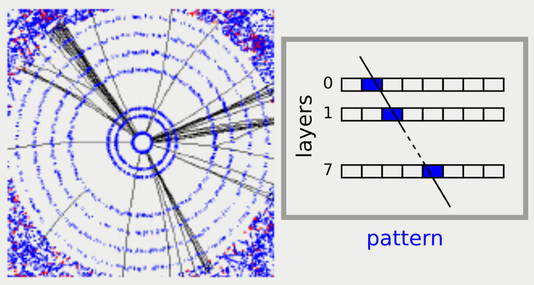
The Fast TracKer in the ATLAS experiment upgrade



The ATLAS detector

The Phase I LHC will reach a luminosity up to $3 \cdot 10^{34}$ cm^{-2} s^{-1} and the experiments will produce a huge amount of data. For this reason, a **tight selection of events** will be required to choose data to be transferred to the mass storage system.

Tracking information is indispensable to perform the selection of events.
The **Fast TracKer (FTK)** system has been designed to find charged particle tracks, by comparing data from silicon detectors with a set of pre-calculated patterns.



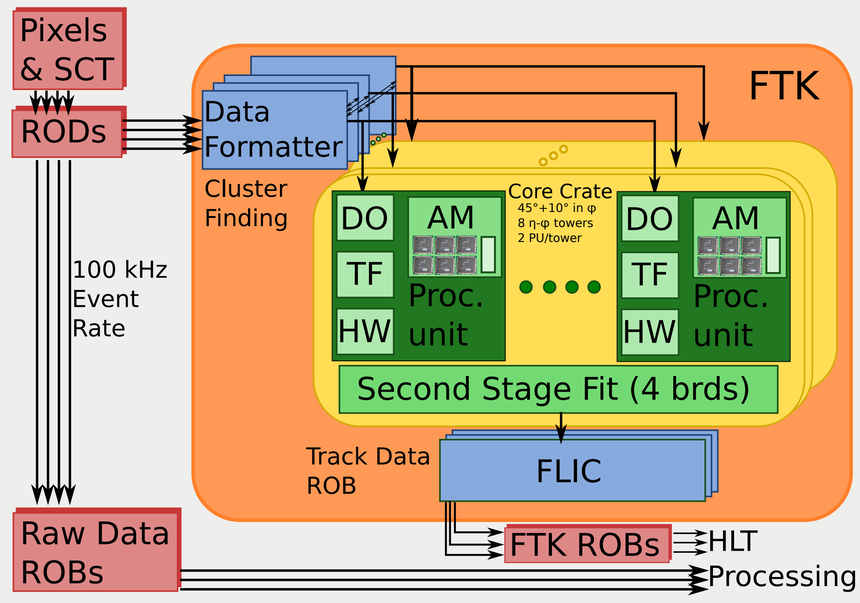
A charged particle striking through the detector layers produces a "pattern"

Overview of the Fast TracKer system

The Fast TracKer system is made of:
- 32 Data Formatters (DF)
- 128 Processing Units
- 32 Second Stage Fitting Boards
- Interface towards the High-Level Trigger

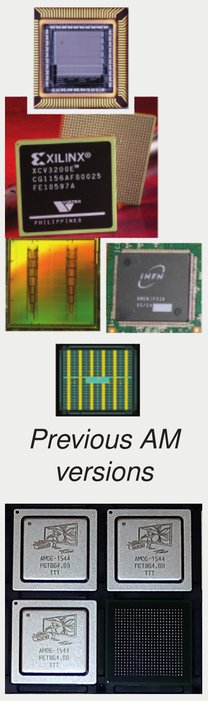
Each Processing Unit is composed of:
- an **AM Board** for pattern matching
- a rear card (AUX Board) with Data Organizer (DO), Track Fitter (TF), and Hit Warrior (HW)

The **Associative Memory (AM)** system is the core of the FTK.
- Inside the AM chip, the memory is organized in blocks of 2048 patterns; each pattern contains the spatial coordinates of 8 layers (18 bits per layer).
- The AM chip contains 64 blocks, for 18.8 Mbit of total memory capacitance (128 k patterns).
- 64 AM chips are assembled on an Associative Memory Board, for a total capacitance of 8 M patterns.
- The whole FTK system is made of 128 AM Boards, for an overall memory capacitance of 1 G patterns (one billion patterns).



Architecture of the FTK system

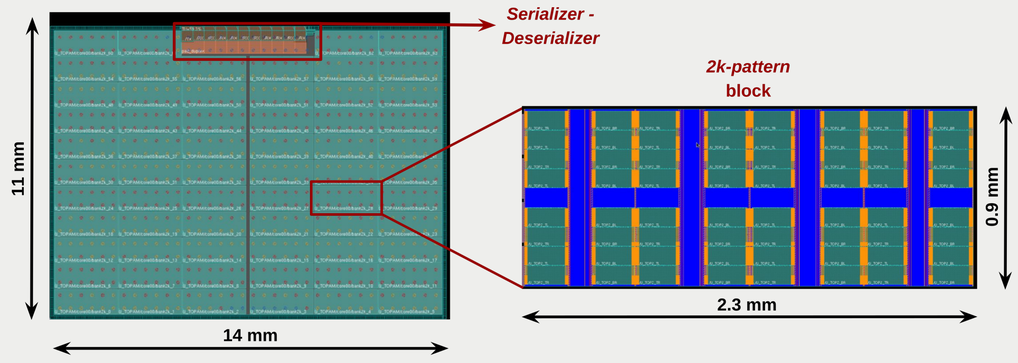
The Associative Memory chip



Previous AM versions

AM06 chips in flip-chip BGA package

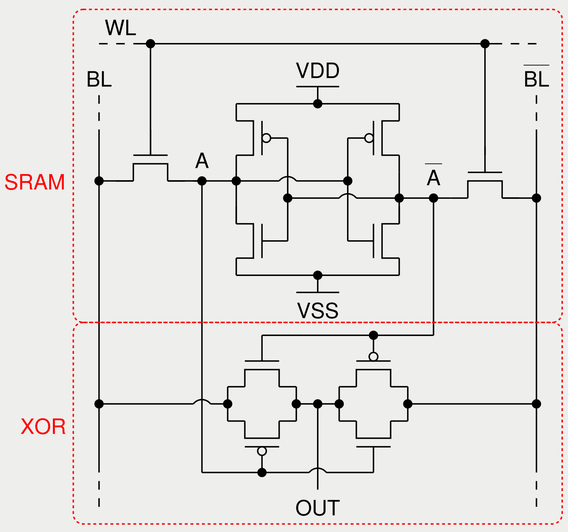
The AM06 is a 65 nm CMOS device, designed with mixed approach:
- **full-custom** design for the memory array;
- **standard cell** design from **VHDL description** for glue logic and JTAG interface;
- **IP blocks** for the I/O serializers and deserializers.



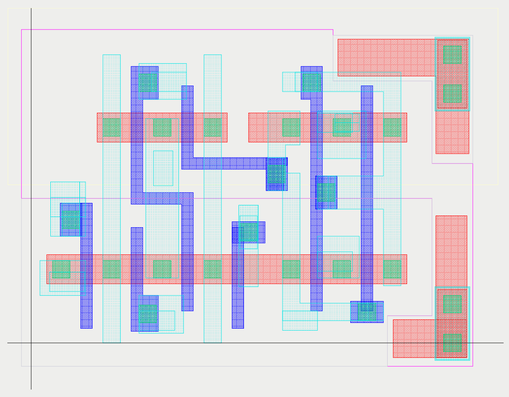
AM06 layout and detail of a memory block

The AM06 is a large chip with an area of 168 mm^2 and 421 million transistors. It has:
- 64 arrays, with 18 Mbit of total memory;
- 20 million standard cells;
- 10 deserializers for the inputs and 1 serializer for the output, at 2 Gbit/s;
- 7 separate supply voltages;
- 14 clock domains;
- JTAG interface for programming and testing.

The AM chip employs a new type of associative memory cell, specifically designed for this purpose, and called XORAM (= XOR + RAM).



Schematic diagram of the XORAM cell



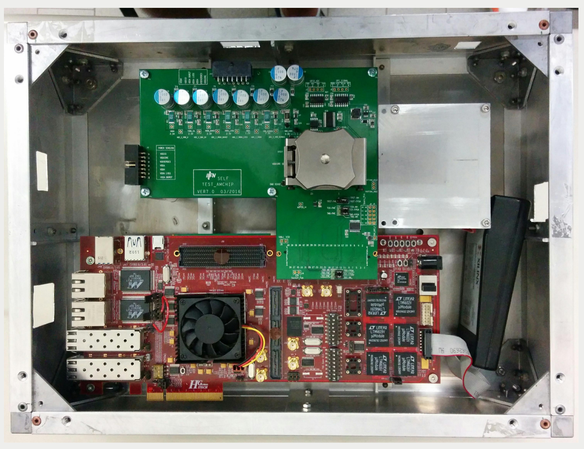
Layout of the XORAM cell in 65 nm CMOS

The AM cells are arranged in "words" of 18 bits, corresponding to the coordinates of the clusters of pixels (15 bits for the coordinates + 3 'don't care' bits to implement variable resolution).

The XORAM cell has a low power consumption: ≈ **1 fJ/bit per comparison**.

Layout of the 18-bit AM cell, made of 18 XORAM cells and a 18-bit NOR gate

AM06 test setup

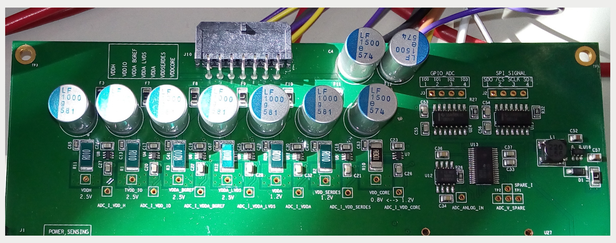


The AM06 test setup

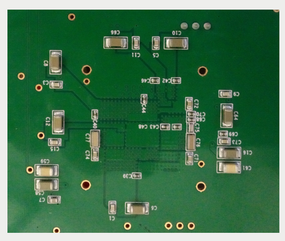
The test setup includes:
- a **Xilinx FPGA evaluation board** from HiTechGlobal (the **red board**), and
- a **custom board** equipped with a ZIF socket (the **green board**).

The boards are placed into a box with a cover that leaves only the ZIF socket accessible to the operator, to prevent accidentally changing the configuration switches.

The AM06 has a large current consumption: **up to 2.5 A** per chip in normal operation mode.
The AM core average current rises from 0.1 A to 2.5 A in about 0.1 ns, and current peaks are synchronous with the 100 MHz clock rising edge.
To overcome problems due the current consumption, the test board has been carefully designed, adding **decoupling capacitors**:
- large electrolytic capacitors on the top side, close to the power cables; and
- small ceramic capacitors with different capacitance values and low ESR and ESL on the bottom side, below the ZIF socket.



Electrolytic capacitors on the top side of the board

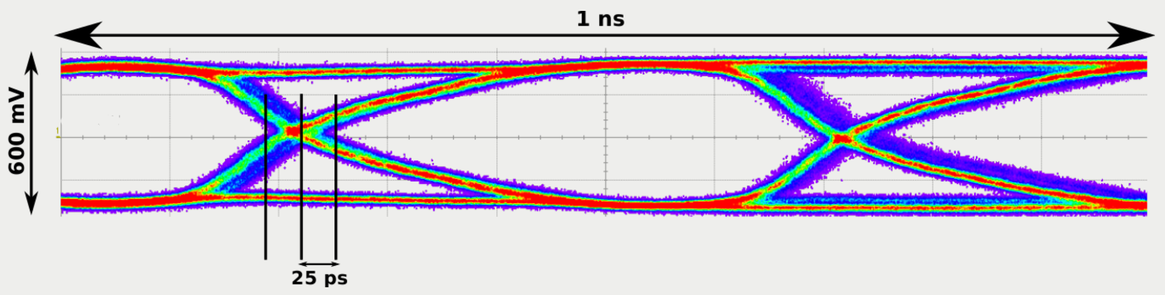


Ceramic capacitors on the bottom side

AM06 characterization and volume test

The AM06 chip has been characterized with the test system at the INFN laboratories in Milan and Frascati, and at the LPNHE laboratory in Paris.

From the eye diagram, the jitter of one of the AM06 serial links at 2 Gbit/s is about 25 ps.
The same result has been obtained for all the serial links, thus confirming the good quality of the serial communication.



Eye diagram of AM06 serial link at 2 Gbit/s

Shmoo plot

The test sequence exploits the **JTAG interface** and the **self-testing capabilities** integrated in the associative memory arrays, which can be tested with a CRC procedure with on-chip test pattern generator and signature analysis.
The test procedure has **100 % coverage against single faults** in the AM core blocks, in the readout, and in the main functions used to configure and run the AM chip.
The test setup has been assembled and used at the Microtest company in Altopascio, Italy.
The test takes about **2 min per chip**. The test procedure is very user-friendly and does not require a specialized training of the operator.

The shmoo plot indicates that the optimal supply voltage for the AM core is ≈ 1.1 V when the clock frequency is equal to 100 MHz.

Conclusion

The 6th version of a large Associative Memory chip for the FTK system has been designed in 65 nm CMOS technology.
The laboratory characterization shows a fully functionality of both the AM06 and the test system.
The test setup has been implemented successfully at the company and the operator is capable to perform the test of a large number of AM06 chips without any interaction with test setup developers.

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