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Silicon pixel R&D for the CLIC detector

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Abstract

The physics aims at the future CLIC high-energy linear e^+e^- collider set very high precision requirements on the performance of the vertex and tracking detectors. Moreover, these detectors have to be well adapted to the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of a few microns, ultra-low mass (~0.2% X_0 per layer for the vertex region and ~1% X_0 per layer for the outer tracker), very low power dissipation (compatible with air-flow cooling in the inner vertex region) and pulsed power operation, complemented with ~10 ns time stamping capabilities. A highly granular all-silicon vertex and tracking detector system is under development, following an integrated approach addressing simultaneously the physics requirements and engineering constraints. For the vertex-detector region, hybrid pixel detectors with small pitch (25 µm) and analogue readout are explored. For the outer tracking region, both hybrid concepts and fully integrated CMOS sensors are under consideration. The feasibility of ultra-thin sensor layers is validated with Timepix3 readout ASICs bump bonded to active edge planar sensors with 50-150 µm thickness. Prototypes of CLICpix readout ASICs implemented in 65 nm CMOS technology with 25 µm pixel pitch have been produced. Hybridisation concepts have been developed for interconnecting these chips either through capacitive coupling to active HV-CMOS sensors or through bump-bonding to planar sensors. Recent R&D achievements include results from beam tests with all types of hybrid assemblies. Simulations based on Geant4 and TCAD are used to validate the experimental results and to assess and optimise the performance of various detector designs. The R&D project also includes the development of through-silicon via (TSV) technology, as well as various engineering studies involving thin mechanical structures and full-scale air-cooling tests. An overview of the R&D program for silicon detectors at CLIC will be presented.

Talk presented at the 25th International Workshop on Vertex Detectors, Isola d'Elba, Italy, 26–30 September 2016
This work was carried out in the framework of the CLICdp collaboration

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The physics aims at the future CLIC high-energy linear e^+e^- collider set very high precision requirements on the performance of the vertex and tracking detectors. Moreover, these detectors have to be well adapted to the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of a few microns, ultra-low mass (~0.2% X_0 per layer for the vertex region and ~1% X_0 per layer for the outer tracker), very low power dissipation (compatible with air-flow cooling in the inner vertex region) and pulsed power operation, complemented with ~10 ns time stamping capabilities. A highly granular all-silicon vertex and tracking detector system is under development, following an integrated approach addressing simultaneously the physics requirements and engineering constraints. For the vertex-detector region, hybrid pixel detectors with small pitch (25 µm) and analogue readout are explored. For the outer tracking region, both hybrid concepts and fully integrated CMOS sensors are under consideration. The feasibility of ultra-thin sensor layers is validated with Timepix3 readout ASICs bump bonded to active edge planar sensors with 50-150 µm thickness. Prototypes of CLICpix readout ASICs implemented in 65 nm CMOS technology with 25 µm pixel pitch have been produced. Hybridisation concepts have been developed for interconnecting these chips either through capacitive coupling to active HV-CMOS sensors or through bump-bonding to planar sensors. Recent R&D achievements include results from beam tests with all types of hybrid assemblies. Simulations based on Geant4 and TCAD are used to validate the experimental results and to assess and optimise the performance of various detector designs. The R&D project also includes the development of through-silicon via (TSV) technology, as well as various engineering studies involving thin mechanical structures and full-scale air-cooling tests. An overview of the R&D program for silicon detectors at CLIC will be presented.

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*Speaker.

1. The CLIC accelerator and detector

1.1 The CLIC accelerator and experimental conditions

The Compact LInear Collider (CLIC) is a proposed CERN-based linear e^+e^- collider [1], capable of operation with a centre-of-mass energy of up to 3 TeV. The accelerator is currently envisaged to be constructed in 3 stages, shown schematically in figure 1 [2], and is based upon a novel two-beam acceleration method. The central concept of the CLIC acceleration scheme is the use of high frequency RF to achieve high accelerating gradients (of order 100 MV/m). Given the low efficiency for klystron power generation at such high frequencies, the RF power is instead extracted from a high frequency (low energy) *drive beam*. This beam is accelerated using klystrons at low frequency, with the bunch frequency subsequently increased using a series of delay loops and combiner rings. High frequency RF power can then be extracted by decelerating this beam, which is used in conjunction with normal conducting cavities to accelerate the main colliding beam.

Due in part to this acceleration scheme, the bunch structure at CLIC has some particular features which strongly impact the detector design. Colliding bunches are arranged into *trains*, 156 ns long and with a repetition rate of 50 Hz, which allows the use of power-pulsing in the front-end electronics. Additionally, in order to produce the high luminosities of order 6×10^{34} cm^{-2} s^{-1} required for physics analyses, each bunch in the CLIC machine contains a large number of particles (10^9) over a very small physical area ($\sigma_x \times \sigma_y \times \sigma_z \approx 40$ nm$\times 1$ nm$\times 44$ µm). Such a high bunch density leads to strong electromagnetic interactions between opposing bunches, even in the absence of a hard interaction. This *Beamstrahlung* reduces the collision energy and produces a large number of background particles. These beam-induced backgrounds are peaked in the forward directions, and add a significant number of hits which must be removed in order to perform the track reconstruction. For this purpose, it is assumed that a 10 ns window around the hard physics event will be used for the track reconstruction (requiring sufficient time-stamping on the detector level), with a further 1 ns time window imposed by the calorimeters in order to reduce the physics-level contamination.

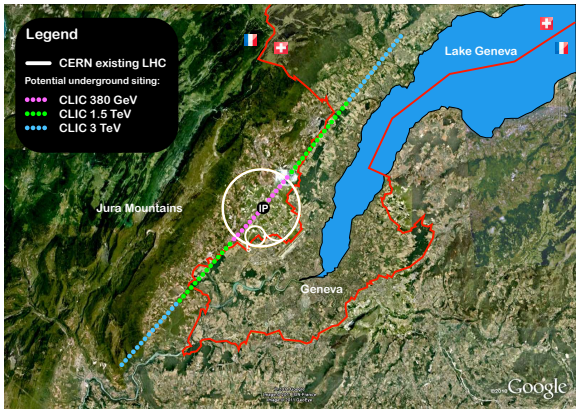

Figure 1: Proposed layout of the CLIC accelerator, showing the staged construction at several centre-of-mass energies.

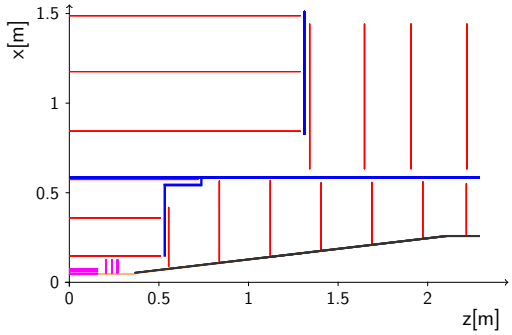

Figure 2: Current layout of the vertex and tracking detectors (pink and red respectively), showing a single quadrant as seen in the *xz*-plane. The conical beam pipe can be seen in the centre (black), as well as the support shell separating the inner and outer tracking detectors (blue), and the positions of interlink structures (blue).

1.2 Current detector layout

A new detector model for CLIC is currently under development, based on an all-silicon vertex and tracking system with high-granularity calorimeters and a 4 T solenoid field. The layout of the tracking system is shown in figure 2. The vertex detector consists of six barrel layers, arranged in three double-layers containing modules mounted on opposing sides of the mechanical substrate. This sharing of the mechanical support between two layers aids in reducing the material budget to the ~0.2% X_0 per layer required (0.4% X_0 per double-layer). In addition, it is foreseen not to have any cooling pipes/material inside the vertex detector: cooling will instead be achieved by a forced air flow through the detector. Such an approach has been shown to work in previous experiments [3] using barrel-only geometries, as well as in mechanical mockups produced for CLIC [4]. To accommodate this, the vertex forward disks (also consisting of double layers) will be constructed in a spiral geometry, in order to improve the efficiency of the heat extraction. Power-pulsing of the front end electronics will additionally keep the mean power consumption below 50 mW/cm^2. For the desired impact parameter resolution to be reached (important for flavour tagging) the detector should be capable of providing a single hit resolution of 3 µm.

The tracking detector is designed to provide a momentum resolution of $< 2\times10^{-5}\ \Delta p_T/p_T^2$ for high-momentum particles, within the 4 T solenoid field currently planned. The material budget for each layer is less than ~1.5% X_0, with an assumed single point resolution of 7 µm in the bending plane of the magnet. In the longitudinal direction the cell size is limited by occupancies from beam-beam interactions, with maximum values of between 1 mm and 10 mm.

2. HV-CMOS sensor studies

High Voltage (HV-) CMOS is a commercial CMOS process where the electronics are shielded within a deep *n*-well. In recent years, detectors for particle physics have been proposed around this concept [5], which allow for some degree of on-pixel functionality without compromising fast signal collection (since the *n*-well shielding allows the application of a moderate bias voltage to deplete the sensing layer underneath). Such *active* sensors may contain an amplification stage

which would allow the signal transfer to the readout chip to proceed via capacitive coupling despite the small pixel area, removing the need for bump-bonding. Such detectors are currently considered as possible sensors for the CLIC vertex detector.

2.1 CLIC ASICs

In order to prove that the requirements on the CLIC vertex detector can be met, a series of custom ASICs have been developed. A dedicated readout chip, CLICpix [6], has been designed and fabricated in a commercial 65 nm CMOS process, containing a matrix of 64×64 square pixels with 25 µm pitch. Each CLICpix pixel contains a Charge Sensitive Amplifier (CSA), discriminator, and digital logic to record the arrival time and charge deposited of each hit. The pixel logic can be seen schematically on the right hand side of figure 3. The chip is operated in a shutter-based acquisition mode, well suited to the bunch structure of the CLIC accelerator, and additionally supports power-pulsing of the analogue and digital circuitry in order to reduce power consumption between bunch trains.

For the HV-CMOS sensor studies, a dedicated ASIC has further been produced in order to match the footprint of the CLICpix. This device, fabricated in a commercial 180 nm HV-CMOS process, again contains a matrix of 64×64 square pixels with 25 µm pitch, with each pixel containing a charge sensitive amplifier and a second inverting amplifier stage. The chip, termed Capacitively Coupled Pixel Detector version 3 (CCPDv3) [7], has limited standalone readout capabilities, intended for use solely as an active sensor for the CLICpix. The pixel schematic of the CCPDv3 can be seen on the left hand side of figure 3.

2.2 Proof of concept

An initial study to gauge the feasibility of using capacitively coupled devices for charged particle tracking has been carried out (results documented in [8]). The CCPDv3 and CLICpix were connected together using a flip-chip machine with placement accuracy of order 1-2 µm, using only a thin layer of glue placed on one of the ASICs. A cross section of such an assembly is shown on the left hand side of figure 4, with the CLICpix on the upper part of the photograph and the CCPDv3 underneath. The pads on each chip which together form the coupling capacitance for the signal transfer can be clearly seen, with the CLICpix electronics separated by the copper power distribution layer. A single hit efficiency of $> 99\%$ was measured in testbeam for thresholds of around 1000 electrons, with little sensitivity to the bias voltage applied (the technology is rated to

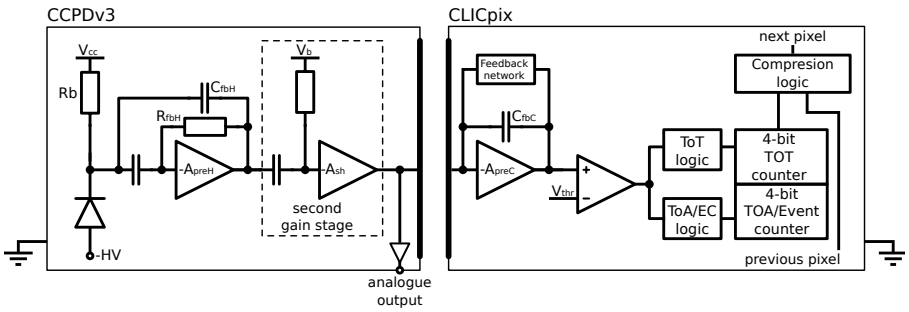

Figure 3: Schematic of the CCPDv3 and CLICpix pixels.

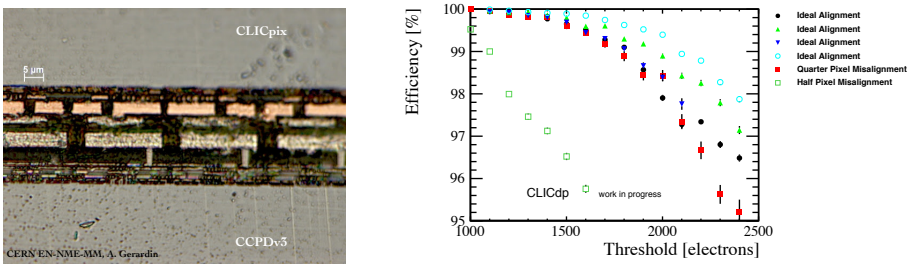

Figure 4: Cross-section photograph of a CLICpix-CCPDv3 assembly (left) and single hit efficiency versus threshold for CLICpix-CCPDv3 assemblies with differing degrees of misalignment (right).

60 V). The single hit resolution was measured to be 6 µm, with a degree of cross-coupling observed between the HV-CMOS pads and neighbouring CLICpix pixels.

2.3 Fabrication studies

Having demonstrated the successful use of capacitively coupled HV-CMOS devices as active sensors, subsequent studies have focussed on the production of assemblies and concerns which might arise for large scale uses. Given the signal transfer through the capacitance generated between the ASIC bonding pads, the distance between the chips and quality of the glueing across the matrix are of principal importance. Different glue viscosities, drop sizes, bonding pressures and alignments have been used to produce a range of assemblies, some of which have been characterised by physical dicing in order to obtain cross-section photographs, while others have been placed in testbeams to evaluate their performance. In most assemblies produced, the dominant factor behind the chip separation was observed to be the passivation layers applied to the chips by the foundry. The most prominent features of the surface, the metal coupling pads, were separated by only this layer and a thin (0.3 µm) layer of glue, with the majority of the glue instead occupying the surrounding gaps. For small pitch devices such as those under investigation by CLICdp, the alignment precision during glueing could be expected to have a large impact on the capacitance between the small coupling pads; on the contrary this was observed to be robust. Figure 4 shows the single hit efficiency versus threshold for a range of samples produced; it can be seen that only in the case of extreme misalignment (where the pixels of the HV-CMOS sensor are perfectly misaligned with respect to the readout chip, i.e. half-pixel misalignment) is any significant drop in performance observed.

3. Planar sensor studies

3.1 Small pitch sensors

Due to the production of the CLICpix ASIC on multi-project wafers, post-processing of the chips at the wafer level has not been possible. This has serious consequences for the bump-bonding of the chips to sensors. Several assemblies have been produced at the Stanford Linear Accelerator laboratory (SLAC) [9], using a custom process involving the deposition of indium bumps on both the sensor and readout chip. Given the small dimensions of the CLICpix (the active matrix is 1.6 mm by 1.6 mm) and the pitch of 25 µm, a large variability between assemblies has been

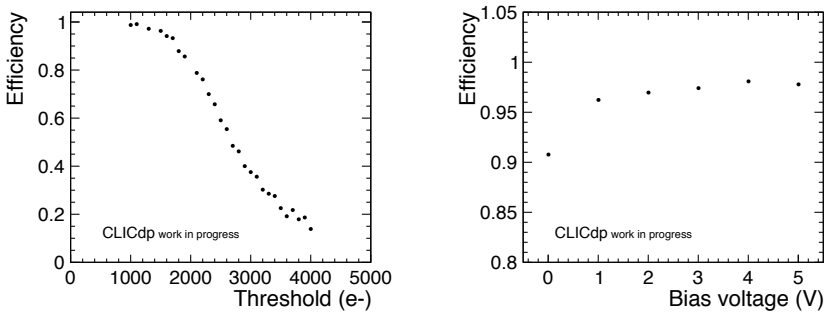

Figure 5: Efficiency versus threshold for a CLICpix ASIC bump-bonded to a 50 µm thick planar sensor at 5 V bias (left) and efficiency versus bias voltage for the same assembly with a threshold of 1200 electrons (right).

observed, with some showing successful bumping in only half of the matrix. Nonetheless, samples have been produced with slim-edge 200 µm thick planar sensors and active-edge sensors of 50 µm thickness, allowing measurements to be made of their performance. It should be noted that large-scale bump-bonding of 25 µm pitch detectors has already been demonstrated [10], where access to the ASIC wafers is possible.

Some testbeam performance plots of a CLICpix bump-bonded to a 50 µm thick active-edge sensor can be seen in figure 5. The efficiency versus threshold is shown in the left hand plot, reaching an efficiency of around 99% at a threshold of 1000 electrons. A known issue exists within the CLICpix layout, where an overlap of the discriminator output and the CSA input leads to an unwanted feedback loop. This results in an operating threshold higher than the design value of 600 electrons; should this issue be alleviated in future chip submissions, it would seem feasible to reach even higher efficiencies. On the right hand plot of figure 5 the efficiency versus bias voltage can be seen (for a threshold of 1200 electrons). The depletion voltage of the sensor is around 2 V, while the built-in potential and offset of the pixel ground level due to biasing of the CMOS circuitry leads to an effective applied voltage of 1 V independent of the external bias voltage. The detector is thus observed to be very efficient even in the absence of external biasing, with the efficiency rising quickly to 98%.

3.2 Active-edge sensors

To facilitate the testing of new sensor designs, the Timepix [11] and Timepix3 [12] ASICs have been used. Active-edge sensors [13] have been under development for several years, but have yet to be employed in a large scale detector for high energy physics. These sensors typically involve an extension of the back-side implant to the sensor cut edge, significantly reducing the distance between the last pixel implant and the physical edge of the sensor. Guard rings may still be used in this region, and may affect the electric field (and therefore charge collection properties) towards this cut edge. Several guard ring designs have been tested with active edge sensors, produced by Advacam. In the most conservative configuration, the guard ring is connected to an additional row of bump bonds, which keep the guard rings at zero potential via dedicated pads on the ASIC side. In a second design, these guard rings are left unconnected, such that the potential is floating.

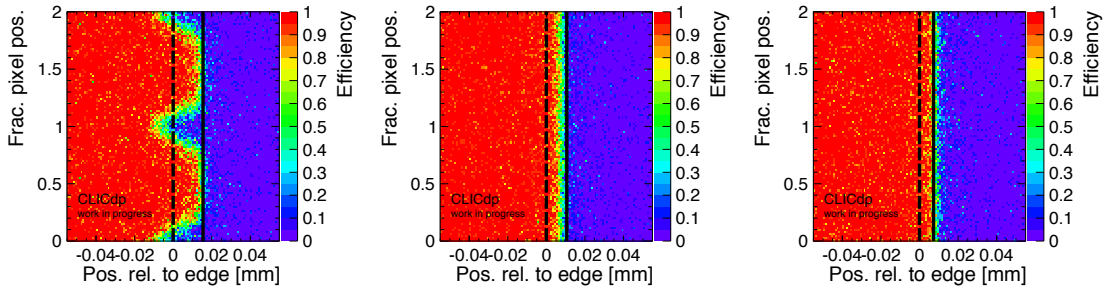

Figure 6: Single hit efficiency over a two-pixel region, (left) for a grounded guard ring, (centre) for a floating guard ring and (right) in the absence of a guard ring. In each case the distance from the last implant to the physical cut edge is 28 µm, 23 µm and 20 µm respectively. The dashed line represents the end of the regular pixel grid, while the solid line represents the cut edge.

Finally, sensors have been produced where the guard ring has been removed entirely.

Testbeam results are shown in figures 6 and 7 for active-edge sensors in all three of these configurations; in each case the sensor thickness is 50 µm, matching the expected sensor thickness for CLIC. The efficiency over a two-pixel cell is shown in figure 6. It can be seen that when the guard rings are grounded a significant amount of charge is lost, due to field line termination on the rings themselves. When the potential of the guard rings is left floating (centre plot) then this is not the case: only a very marginal drop in efficiency close to the physical edge is observed. The best results, in terms of charge collection and single hit efficiency, are however seen with the complete removal of the guard rings. The losses observed with floating guard ring are further highlighted in figure 7, where the mean cluster charge is shown over the same two-pixel cell. The drop in charge collected for tracks passing close to the corners of the pixel cell at the physical edge can be seen, which are absent when the guard rings are removed completely (right hand plot).

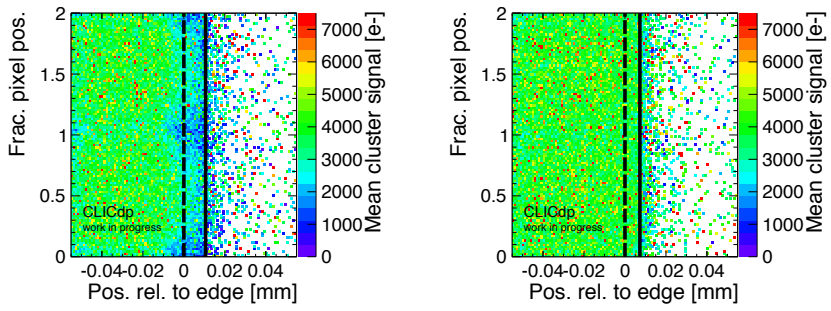

Figure 7: Mean cluster signal over a two-pixel region, (left) for a floating guard ring and (right) in the absence of a guard ring. The distance from the last implant to the physical cut edge is 23 µm and 20 µm respectively. The dashed line represents the end of the regular pixel grid, while the solid line represents the cut edge.

4. Integrated technologies

For the tracker, where the requirements on power consumption and cell size are more relaxed than for the vertex detector, a number of technology options are under consideration. Given the large area currently foreseen (of order 100 m^2), silicon strip detectors and integrated CMOS devices are both of interest. The relatively small cell lengths, necessary to keep the occupancy low in the face of beam-induced backgrounds, lead to short strips/long pixels of between 1 mm and 10 mm length (while the pitch in the bending plane of the magnet is expected to be around 50 µm). For this reason, effort has been directed more towards integrated CMOS options, including technologies not yet employed on a large scale in the community.

4.1 Monolithic Active Pixel Sensors (MAPS)

The development of quadruple-well processes, where both p- and n-type transistors are shielded from the (p-type) substrate, allows the placement of full CMOS circuitry inside the active region of the chip. Recently, as part of the ALICE Inner Tracking System (ITS) upgrade [14], a chip has been developed in such a technology with 180 nm feature size, containing a large number of small test matrices to better understand the effects of sensor geometry on the device performance. This *Investigator* chip contains many small matrices of pixels with differing diode layouts, transistor size, pixel pitch, etc., allowing detailed studies concerning the influence of the physical pixel layout. Some preliminary results from a recent testbeam are shown in figure 8, where a spatial resolution of around 5 µm has been measured, along with a timing resolution of approximately 7 ns. This fast timing is possible due to the High Resistivity (HR) epi-layer, which allows a significant amount of charge collection via drift.

4.2 SOI

Another emerging technology being considered for CLIC is Silicon-on-Insulator (SOI) [15], so-called due to the separation of the bulk HR silicon from the layer containing the CMOS readout electronics via a thick insulating layer (connected by *vias*). This layer can thus be operated under full depletion, and arbitrarily complex circuitry can be included in the upper layer(s). While the simplest such scheme contains only a single Buried OXide (BOX) layer, more complicated

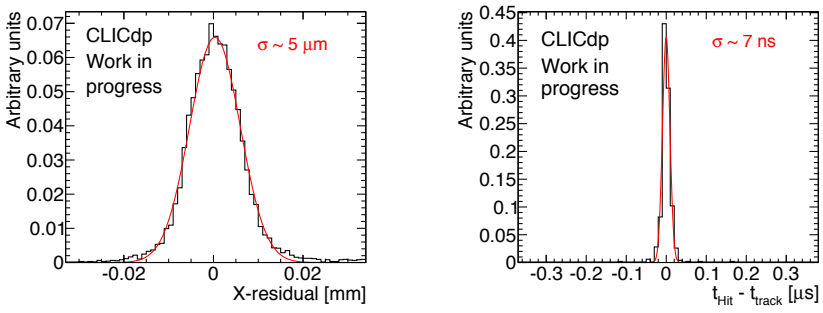

Figure 8: Spatial (left) and timing (right) residuals for 28 µm pitch pixels within the *Investigator* chip. An external bias voltage of 6 V is applied.

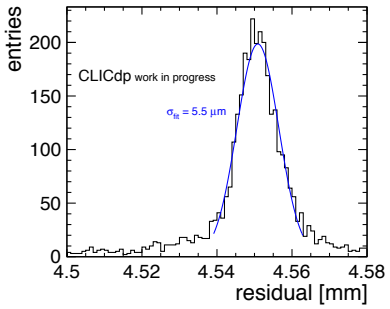

Figure 9: Track correlation plot for an SOI detector with 30 µm pitch. The sensor thickness is 200 µm, with a 30 V applied bias voltage.

schemes such as double-SOI have been proposed, intended to overcome some of the initial problems observed with this technology (in particular the sensitivity to charge build-up in the insulating layer during irradiation). An initial test chip has been produced with several pixel architectures containing variations on the electronics (source follower versus charge pre-amplifier) and pixel layout. The analysis of recent testbeam measurements is currently underway, with an initial correlation plot (figure 9) showing a spatial resolution of 6 µm, for pixels of 30 µm pitch.

5. Outlook

The result of the studies and investigations detailed above have led to the design of a new generation of ASICs, designed to come closer to meeting the performance required for the CLIC detector. A new version of the CLICpix readout chip, featuring a larger matrix (128×128 pixels), longer on-pixel counters and the correction of the discriminator feedback issue has been designed, shortly to be submitted for production. Similarly, a new HV-CMOS sensor, the CLIC Capacitively Coupled Pixel Detector (C3PD) has recently been received and has shown excellent performance. The new sensor contains a redesign of the amplifier layout, removing the second stage and providing a much faster signal (with a peaking time of order 25 ns). Analysis of the data obtained with devices for the tracker is still on-going, with the aim of a future chip which satisfies the CLIC requirements. In parallel, many developments not mentioned above will continue: the mechanical layout of the tracker, including services and cooling layout; a more detailed description of what the tracker electronics will look like; and a finalised detector model to be used for future full-simulation physics studies.

6. Acknowledgements

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References

[1] M. Aicheler et al. (eds), *A Multi-TeV linear collider based on CLIC technology: CLIC Conceptual Design Report*, CERN-2012-007.

[2] P.N. Burrows et al. (eds), *Updated baseline for a staged Compact Linear Collider*, CERN-2016-004.

[3] H.H. Wieman et al., *STAR PIXEL detector mechanical design*, JINST 4 (2009) P05015.

[4] F. Duarte Ramos et al., *Experimental tests on the air cooling of the CLIC vertex detector*, CLICdp-Note-2016-002.

[5] I.Peric, *A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology*, Nucl. Instrum. Meth. A 582 (2007) 876

[6] P. Valerio, R. Ballabriga and M. Campbell, *Design of the 65 nm CLICpix demonstrator chip*, CLICdp-Conf-2013-003.

[7] I. Peric et al., *High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments*, Nucl. Instrum. Meth. A 731 (2013) 131.

[8] N. Alipour et al., *Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector*, Nucl. Instrum. Meth. A 823 (2016) 1.

[9] A. Tomada et al., *Flip chip assembly of thin substrates, fine bump pitch, and small prototype die*, SLAC-PUB-16168.

[10] S. Cartier et al., *Micrometer-resolution imaging using MONCH: towards G2-less grating interferometry*, J. Synchrotron Rad. 23 (2016) 1462.

[11] X. Llopart et al., *Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements*, Nucl. Instrum. Meth. A 581 (2007) 485.

[12] T. Poikela et al., *Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout*, JINST 9 (2014) C05013.

[13] X. Wu et al., *Recent advances in processing and characterization of edgeless detectors*, JINST 7 (2012) C02001.

[14] ALICE Collaboration, *Technical Design Report for the Upgrade of the ALICE Inner Tracking System*, CERN-LHCC-2013-024.

[15] B. Dierickx et al., *Integration of CMOS-electronics and particle detector diodes in high-resistivity silicon-on-insulator wafers*, IEEE Trans. Nucl. Sci. 40 (1993) 753.