The VeloPix ASIC for the LHCb VELO Upgrade

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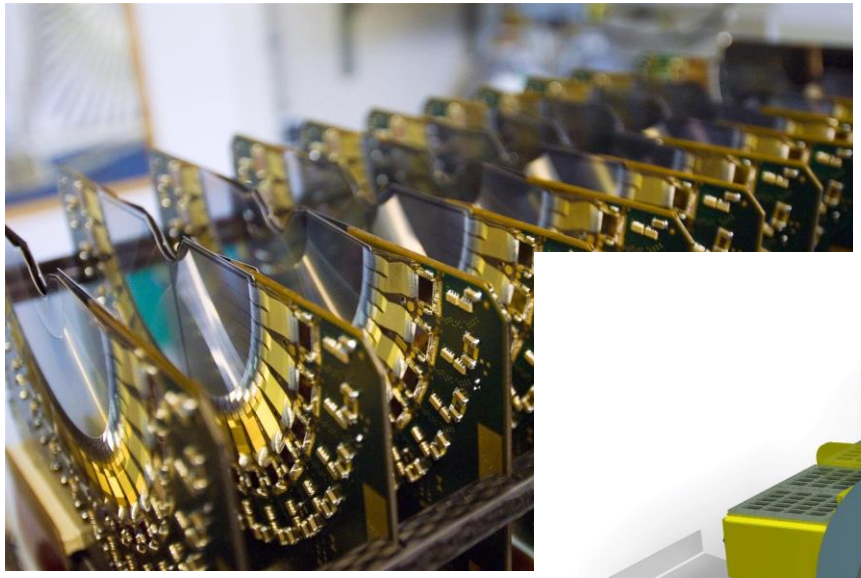
On behalf of the LHCb and Medipix3 Collaboration

with the support of CLIC DP group

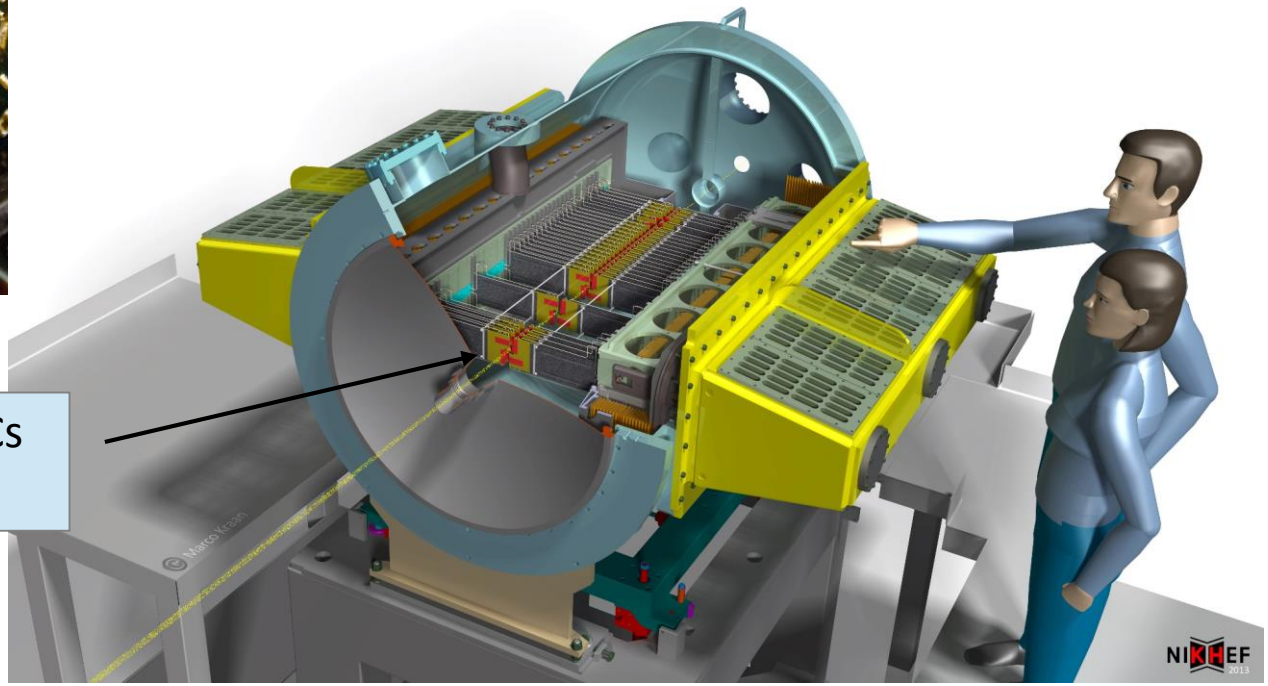
Outline

- Introduction to the VELO upgrade
- The VeloPix chip
- Measurements
- Conclusion

The LHCb VELO upgrade

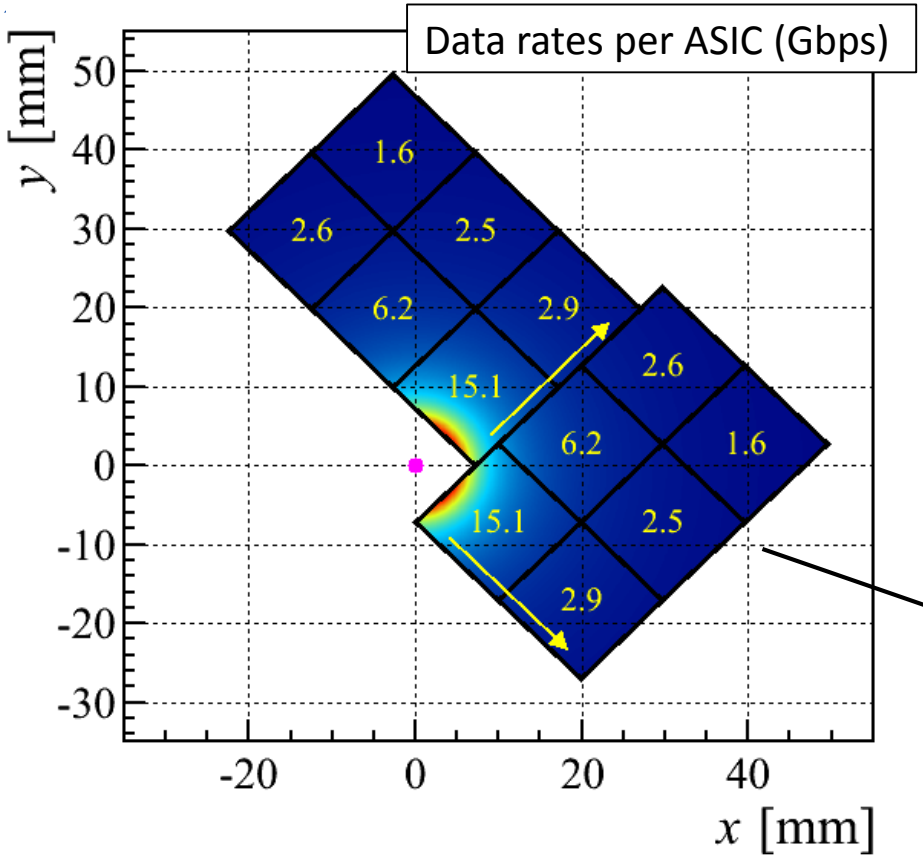


- Trigger readout @ 1 MHz
- Radial strip detector + Beetle ASIC
- During physics data-taking, the silicon sensors @7 mm

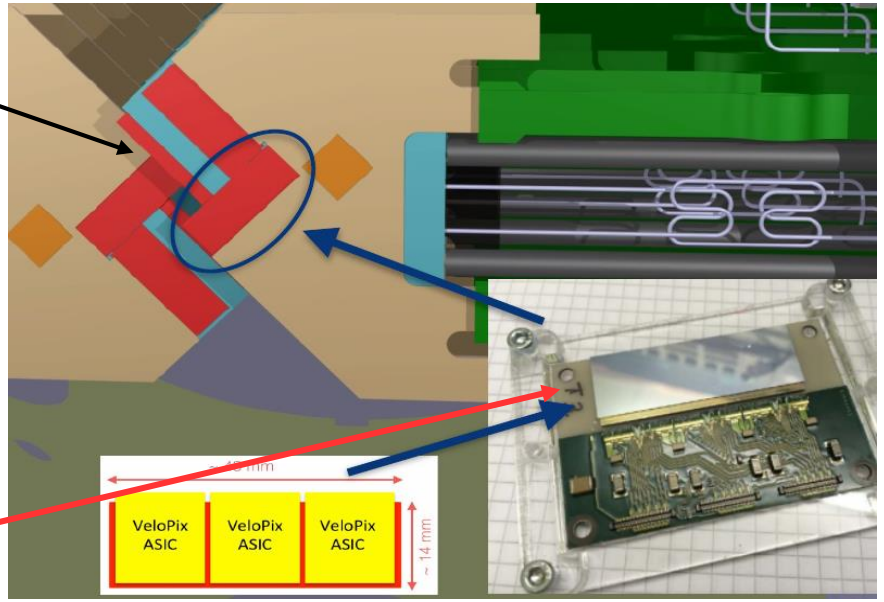


N07-17: P. Collins: ”The LHCb VELO Upgrade”
N12-3: P. Collins: “The Timepix3 Telescope and Sensor Development for the LHCb VELO Upgrade”

VeloPix ASIC module



- Trigger-less readout @ 40MHz
- The hottest chips 5.1 mm from the beam
- Expected integrated radiation 10 years:
  - TID: From 50 to 400 Mrad (non-uniform)
  - 8.5 x 10^{15} neq cm^{-2}
- Data per chip: ~15.1 Gbps, 2.9 Tbps for VELO
- The module installation during the CERN Long Shutdown 2 (LS2) 2019/2020.



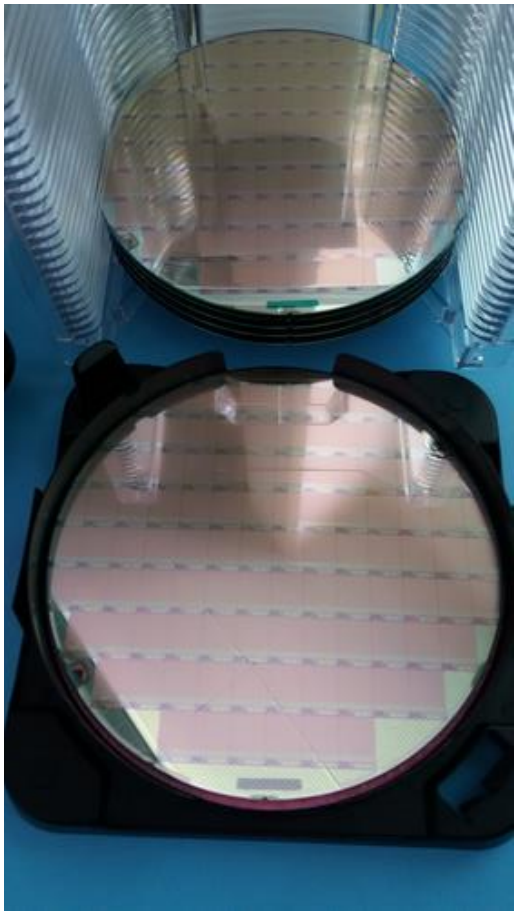
Hybrid pixel readout chip:
Bonded to a sensor.

From Timepix3 → Velopix

	Timepix3 (2013)	VeloPix (2016)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 µm²	
Peak hit rate	80 Mhits/s/ASIC	800 Mhits/s/ASIC 50 khits/s/pixel
Readout type	Continuous, trigger-less, TOT	Continuous, trigger-less, binary
Timing resolution/range	1.5625 ns, 18 bits	25 ns, 9 bits
Total Power consumption	<1.5 W	< 3 W
Radiation hardness		400 Mrad, SEU tolerant
Sensor type	Various, e- and h+ collection	Planar silicon, e- collection
Max. data rate	5.12 Gbps	20.48 Gbps
Technology	IBM 130 nm CMOS	TSMC 130 nm CMOS

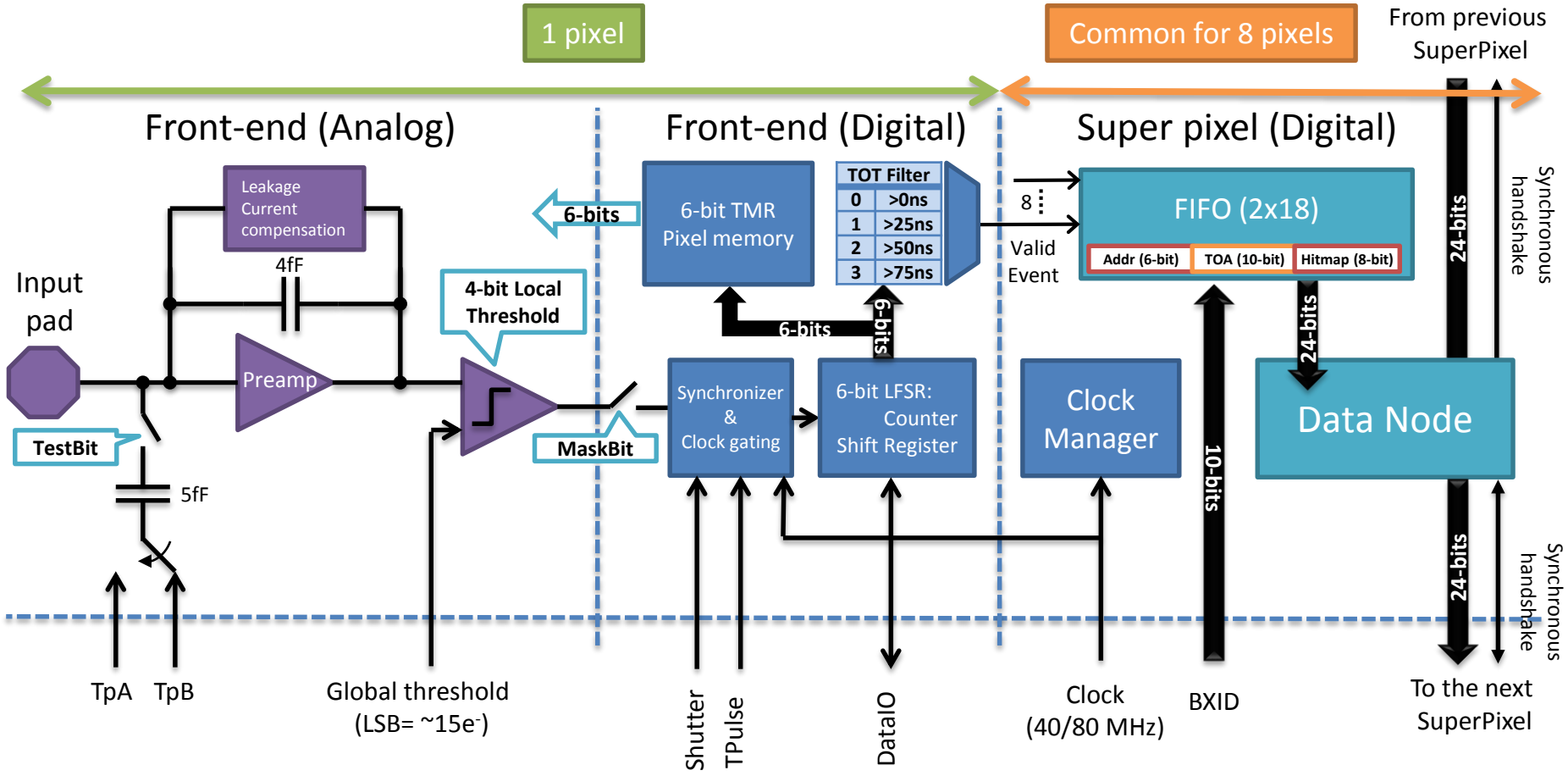
VeloPix Project Overview

- Design started in June 2013 (after Timepix3 submission)
- Change of technology (IBM 130nm → TSMC 130nm)
- The chip was submitted as an engineering run on May 2016
- First wafers received on 31st August
- Fabricated (and diced) chips back at CERN on 7th September
- Production testing later this year (624 chips)
- Irradiation campaign in the future with sensors bonded



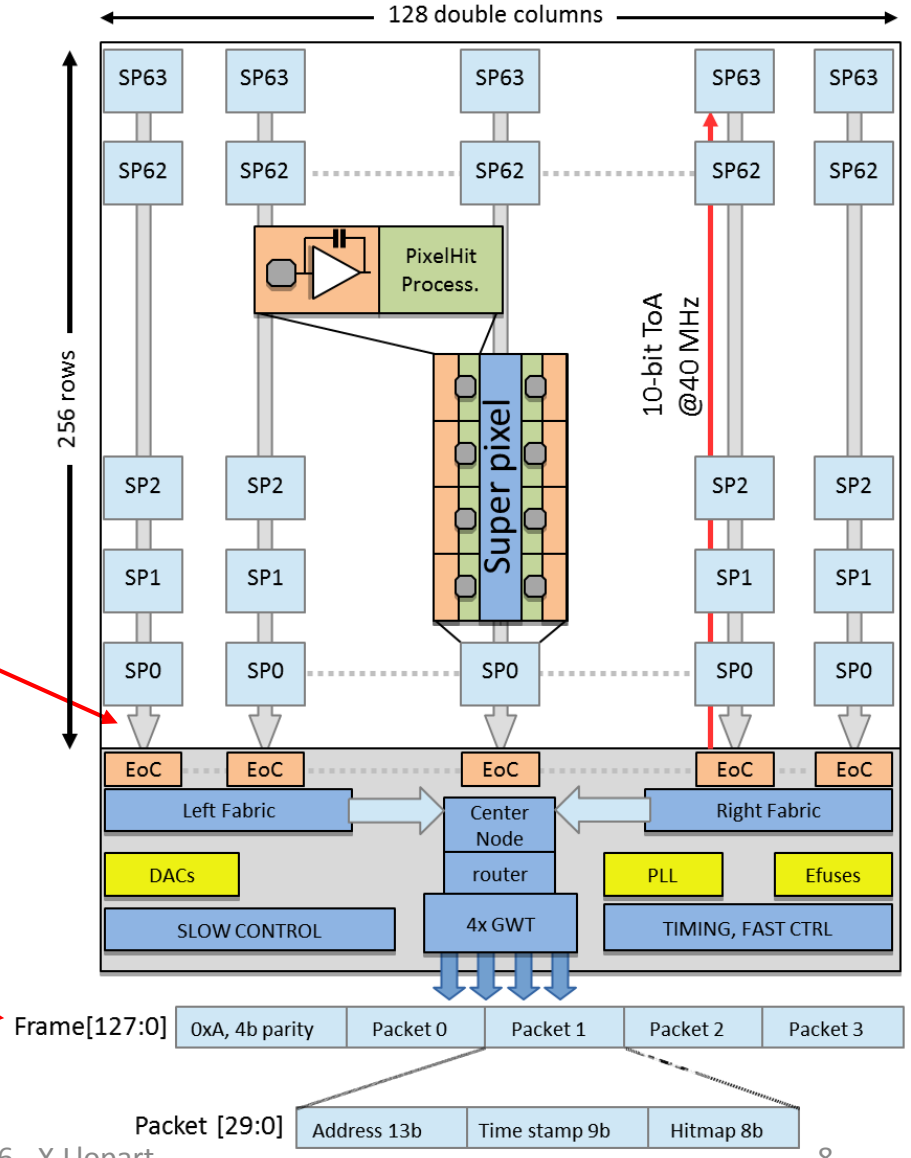
VeloPix wafers

VeloPix pixel schematic



Velopix Chip Architecture

- Pixel matrix:
  - 256 x 256 pixels
  - 128 x 64 super pixels (2x4 pixels each)
  - @40MHz
- Packet-based architecture:
  - 8 pixels/packet + 9 bit time stamp → 30% reduction in data rate
- Data-driven readout:
  - 20 Mpackets/s/double column
- 40, 80, 160 and 320 MHz TMR clock domains in the periphery
- 1 to 4 configurable serializers (GWT)
- GBT frame compatible



Velopix: TMR/RadHard design

- Pixel Matrix (<400Mrad):
  - Only NMOS ELT transistors used in analog front-end
  - Full TMR in FSM & configuration FFs:
    - Pixel configuration → Asynchronous self correcting TMR latch
  - Pixel data flip-flops (FF) unprotected
  - Custom made HD Standard cell library (74 cells) with HVT NMOS HVT and regular PMOS:
    - Standard cell library characterized at 400 Mrad, High-Vt NMOS + Std PMOS

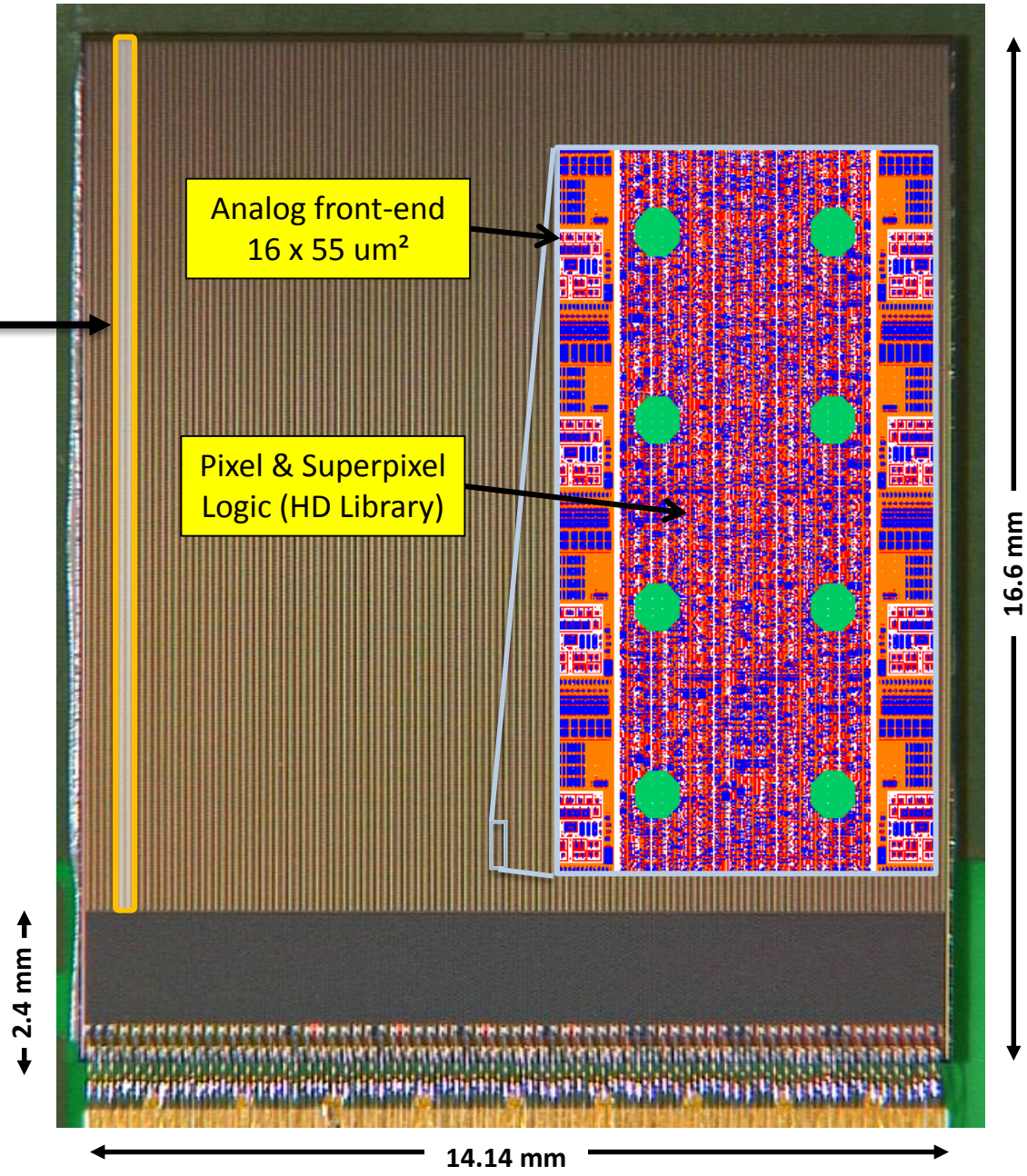
- Periphery (<50Mrad):
  - Full TMR in FSM & configuration FFs
  - Data path unprotected

VeloPix

Double column:
512 pixels
64 super pixels

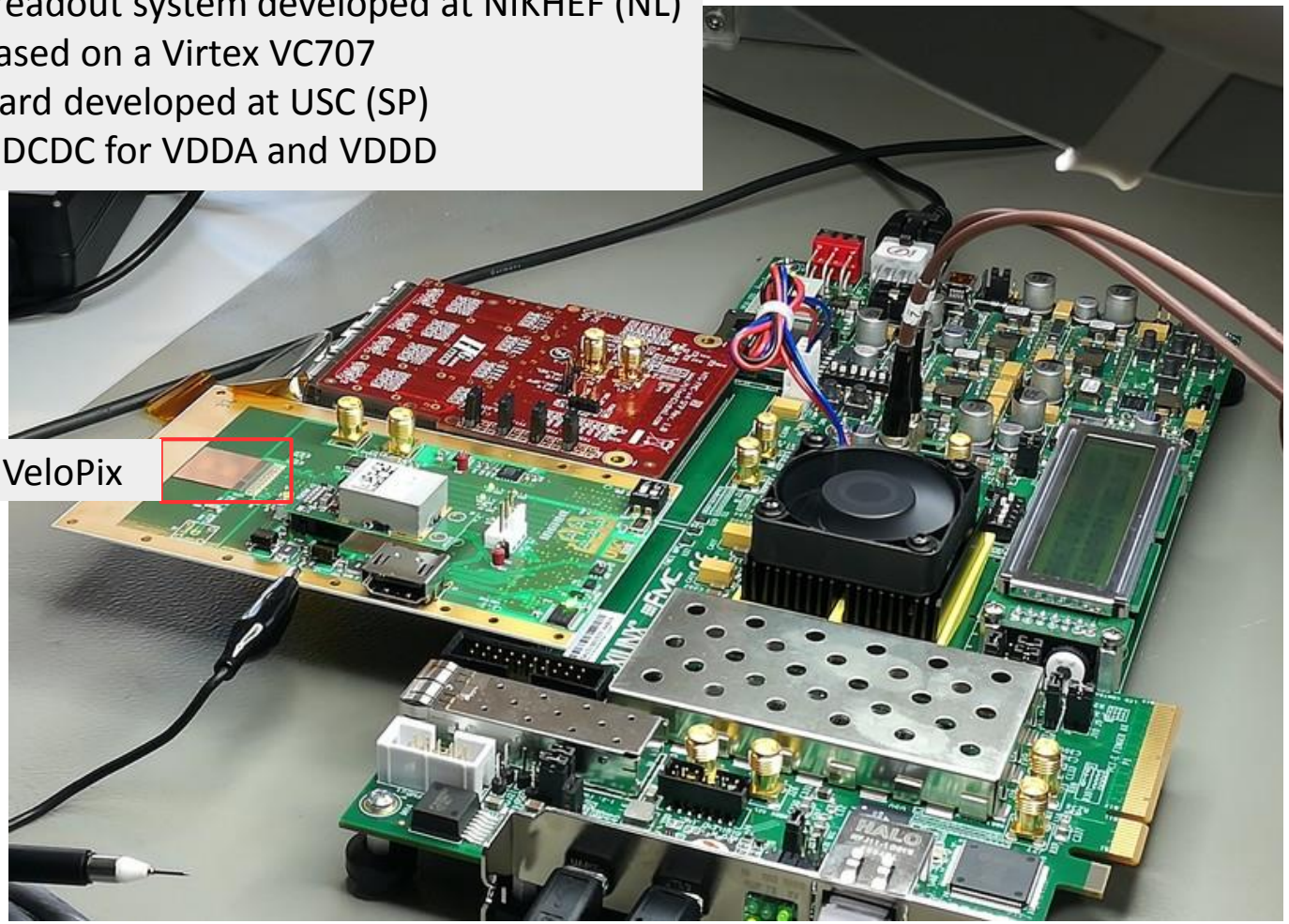
Full matrix:
128 Double columns
~190 Mtransistors

Active Periphery



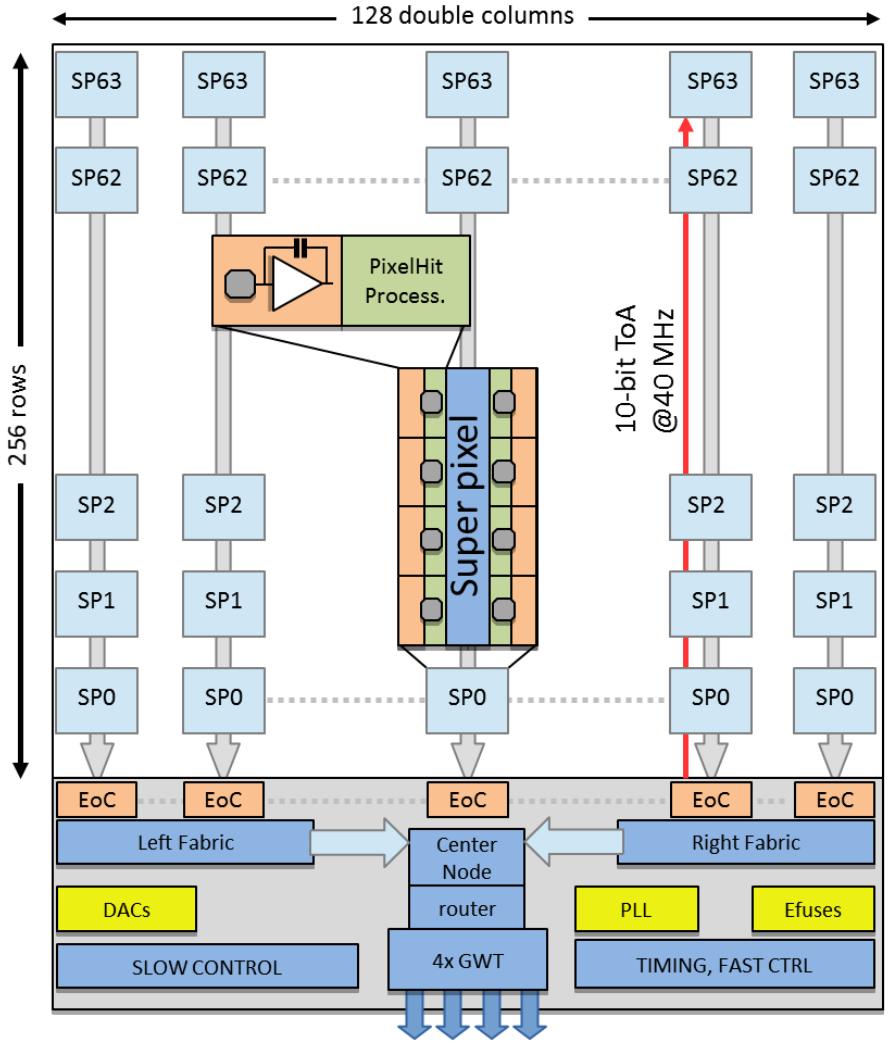
VeloPix debug readout

- SPIDR-readout system developed at NIKHEF (NL)
  - Based on a Virtex VC707
- Chipboard developed at USC (SP)
  - 1 DCDC for VDDA and VDDD

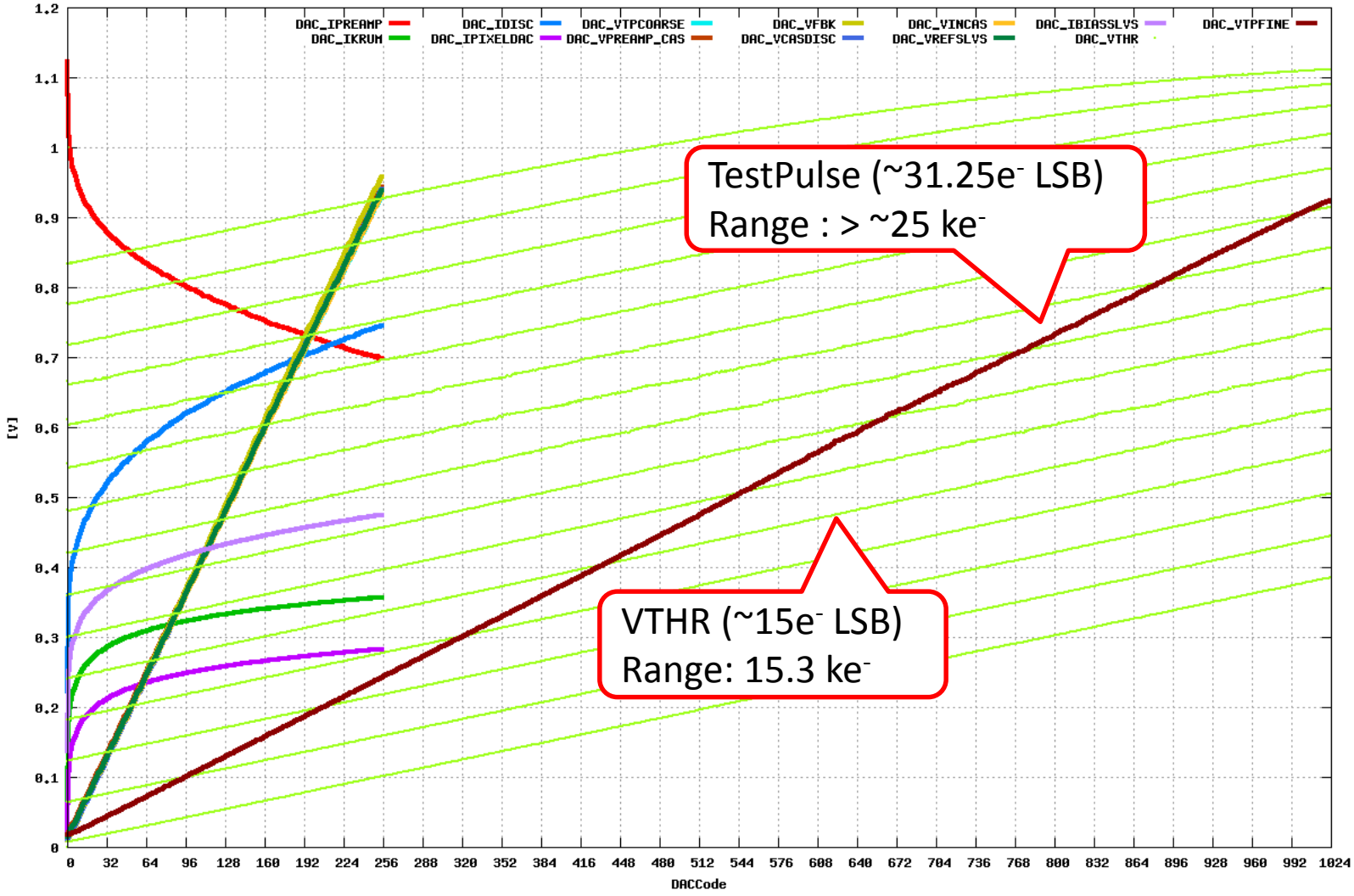


VeloPix: General Measurements

- ✓ Measured power consumption (@nominal settings):
  - ✓ Analog < 480 mW
  - ✓ Digital:
    - ✓ Periphery < 380mW
    - ✓ Pixel Matrix <350mW (idle)
    - ✓ @High rate ~+300mW (simulated)
  - ✓ Total= ~1.5W @High rate
- ✓ Slow and Fast control fully functional
- ✓ Pixel Configuration and readout
- ✓ On-chip biasing DACs (next slide)
- ✓ Internally measured packet latency (@low rate)
- ✓ eCDRPLL (CERN) total jitter @320MHz <6ps$_{rms}$

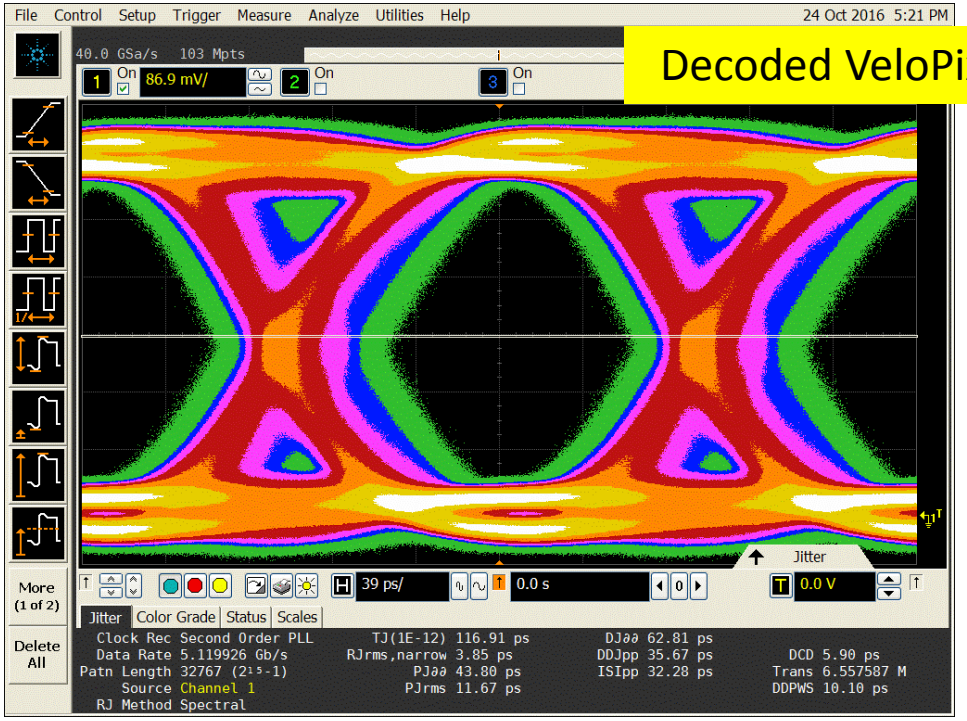


VeloPix on-chip biasing DACs



VeloPix Serializers (GWT)

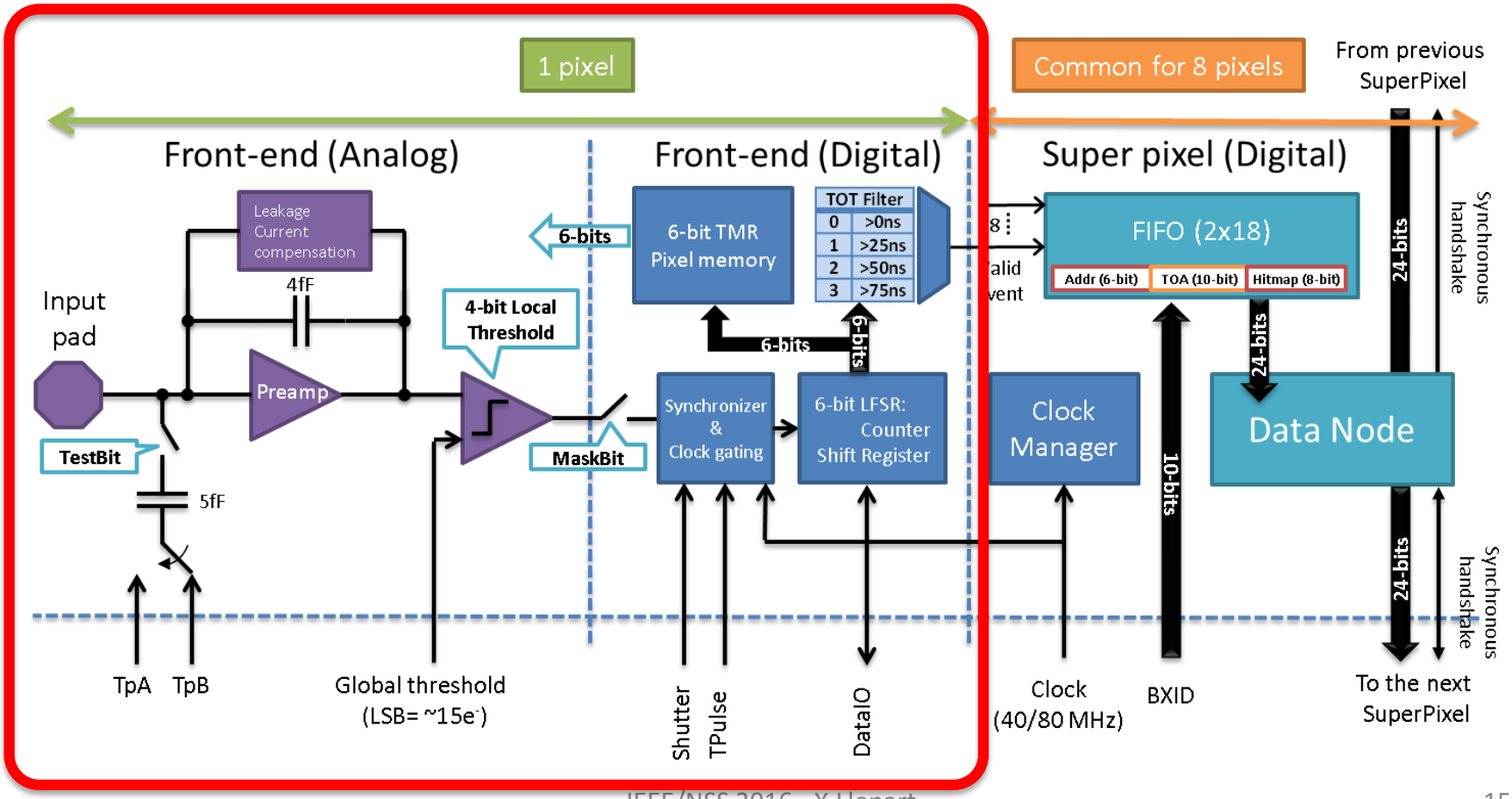
- A low power (~20mW) 5.12 Gbps byte-interleaved serializer and wireline transmitter (NIKHEF)
- Full readout data chain not ready yet but check internally generated PRBS15 signal with scope → Measured BER<10^{-12}



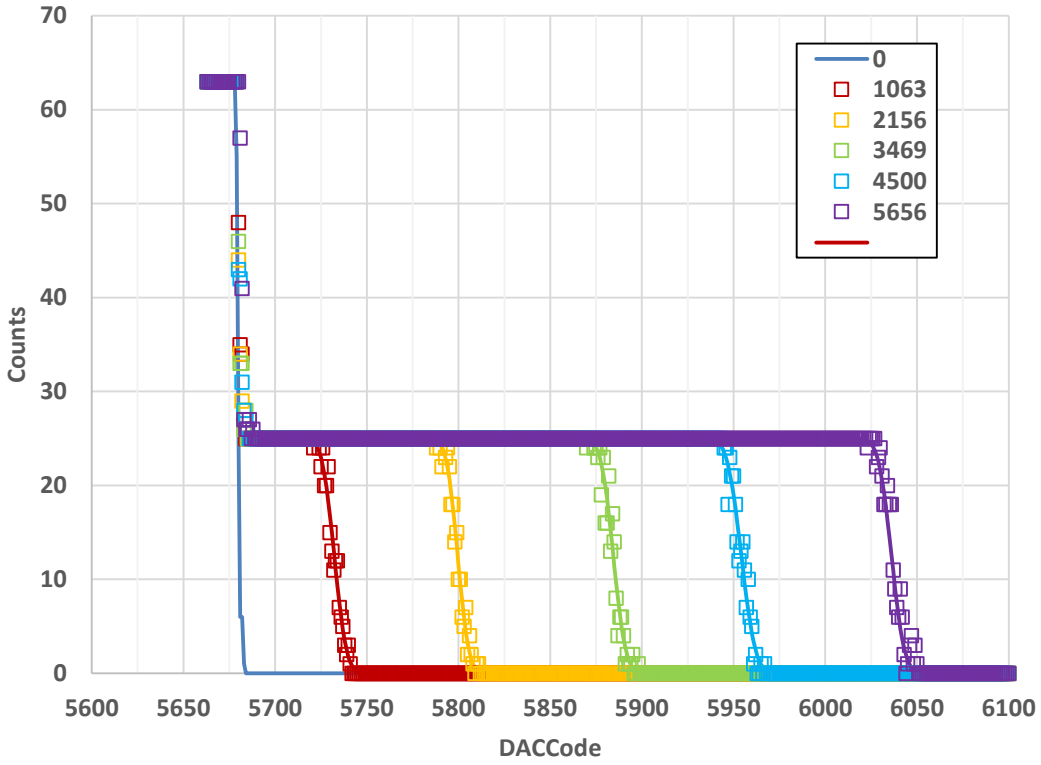
Decoded VeloPix PRBS15 stream

FE Measurements

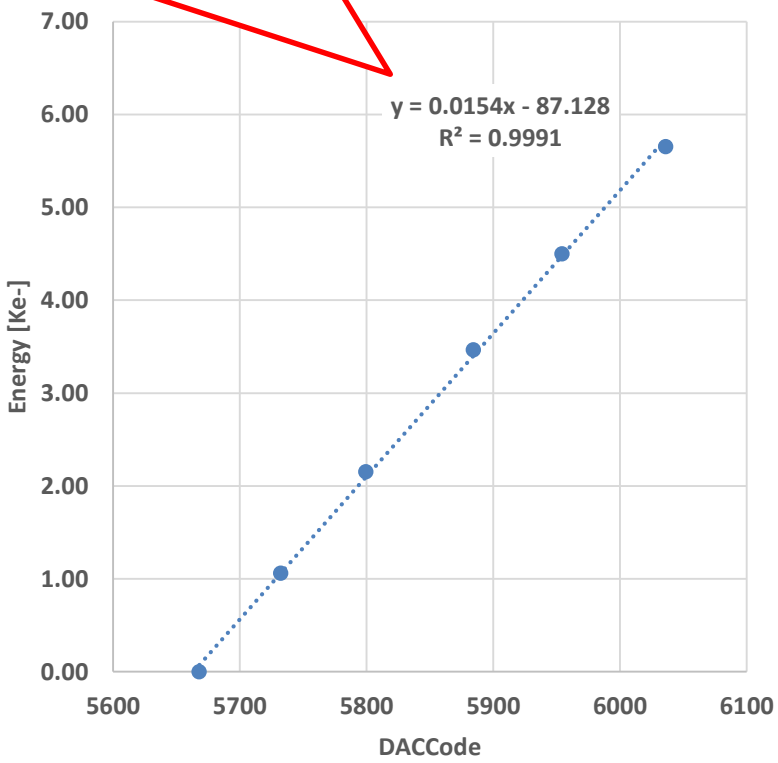
- Front end characterization measurements done through the slow control readout



Test Pulses in one pixel

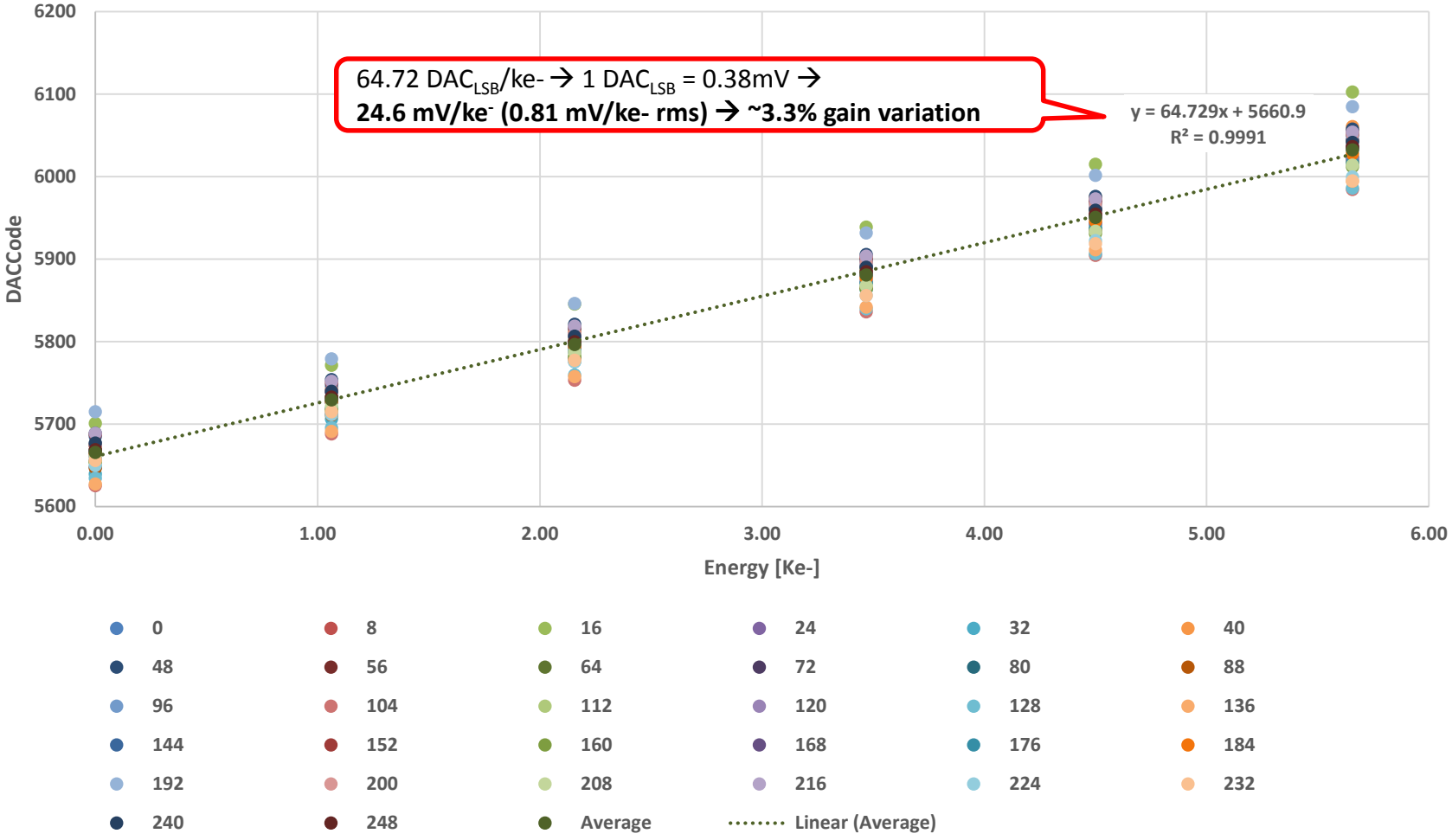


0.0154 e^-/DAC_{LSB}* → 1 DAC_{LSB} = 0.38mV → **24.6 mV/ke^-**



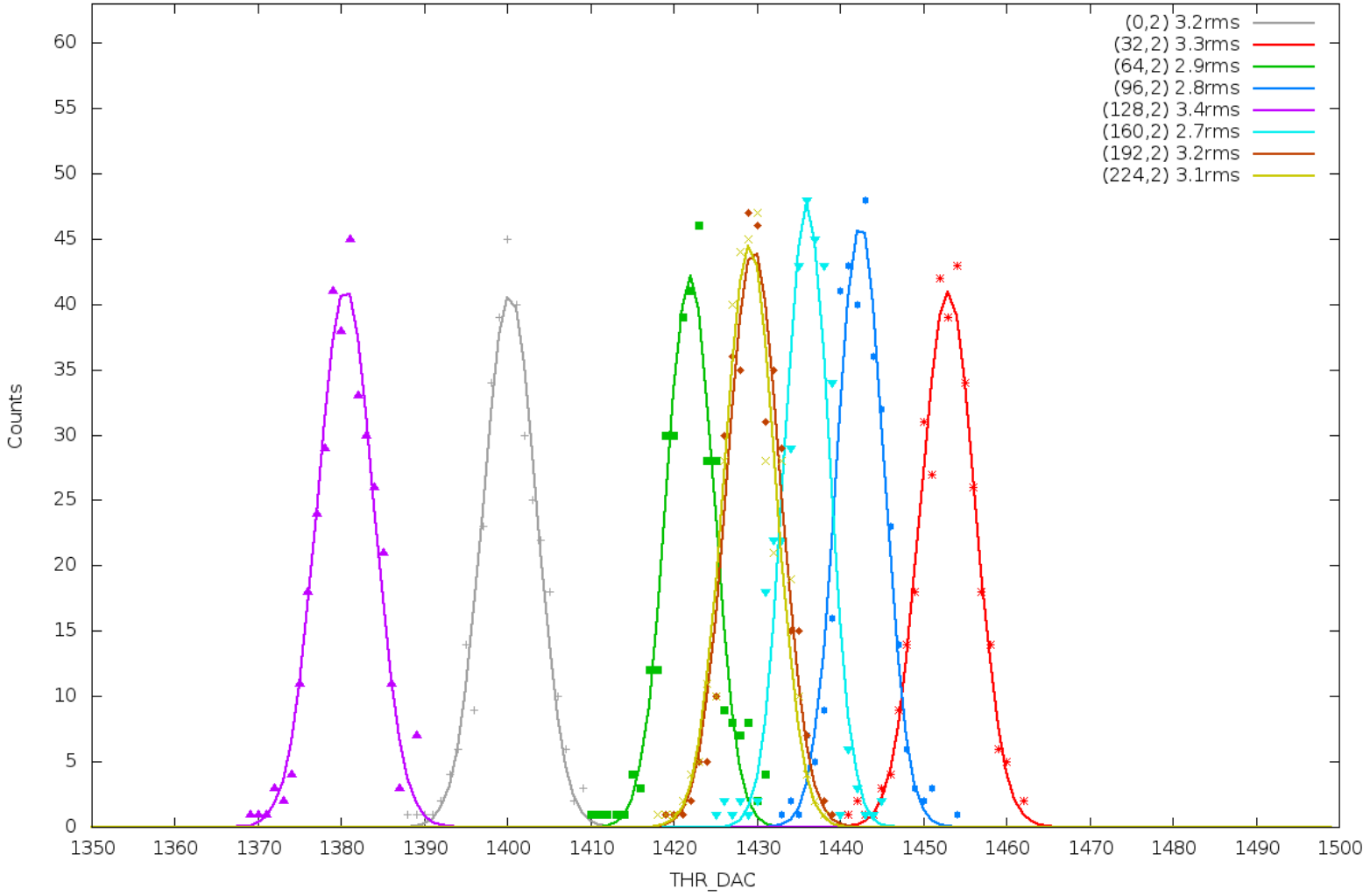
*Assuming Ctest=5fF

Test Pulses in 32 pixels

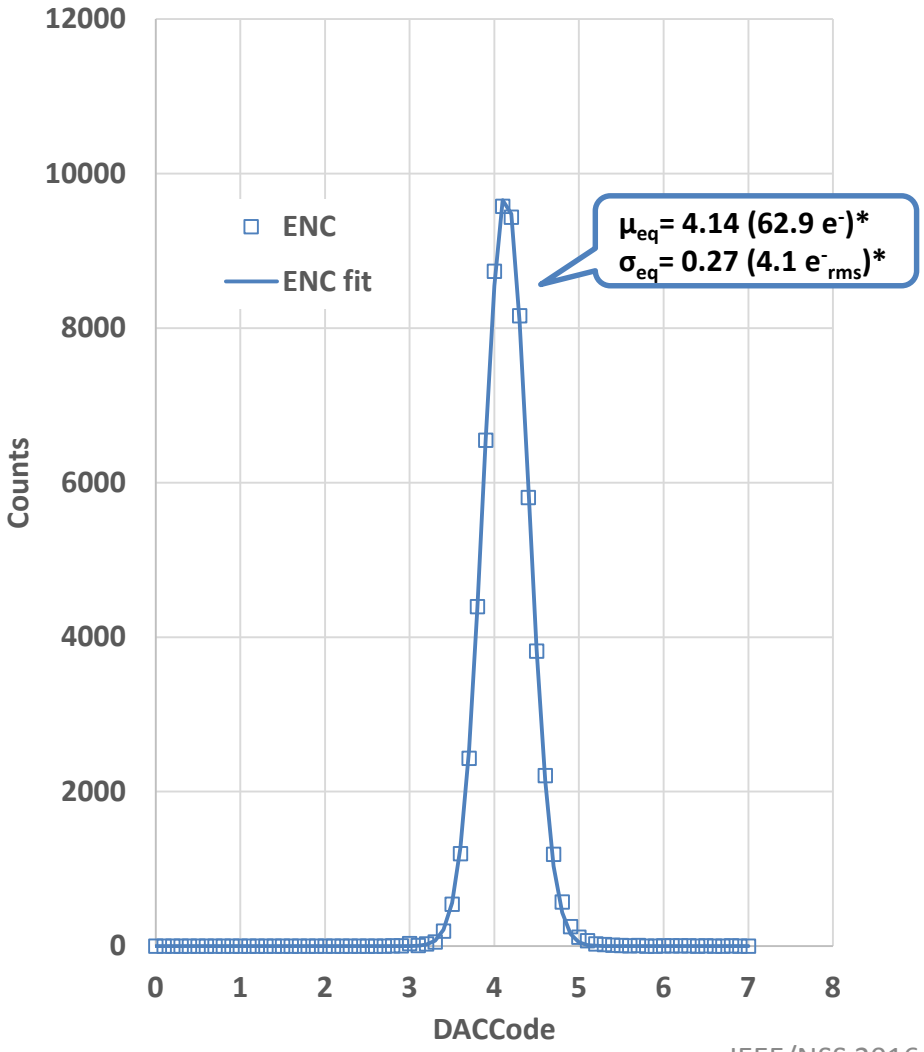


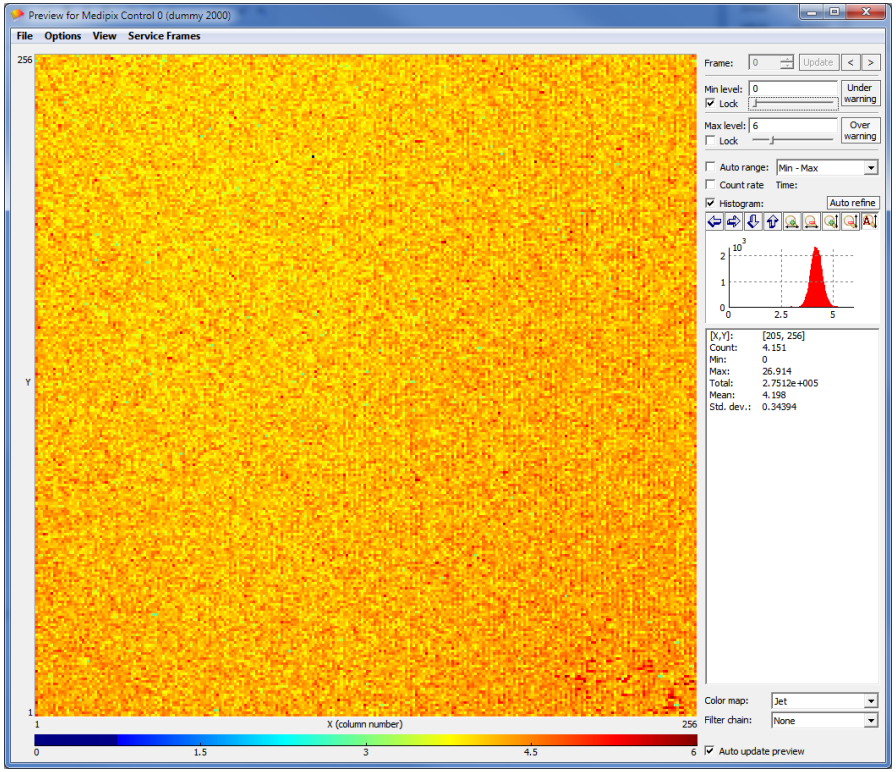
Pixel ENC

[Threshold scan over noise floor in PC mode]



Electronic Noise

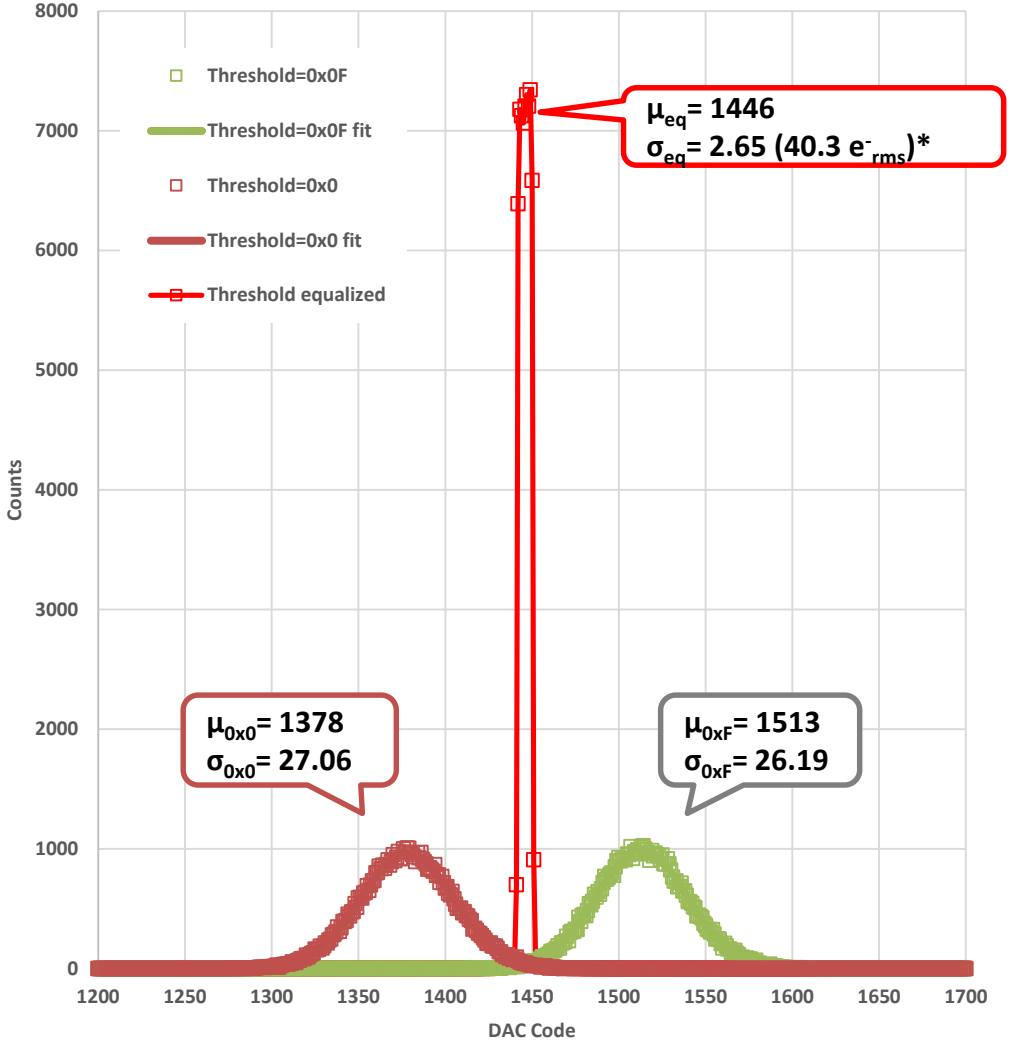


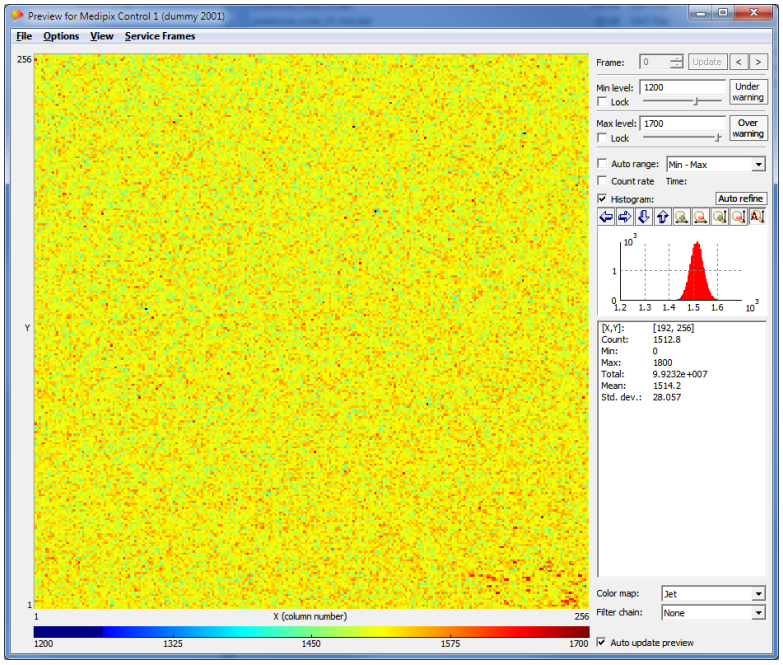


Measured ENC of all pixels
- **Threshold scan over noise floor**
- **All pixels at code 0xF**

*@gain of 25mV/ke$^-$

Threshold Equalization





Unequalised Threshold distribution:
- **All pixels at code 0x0**

*@gain of 25mV/ke$^-$

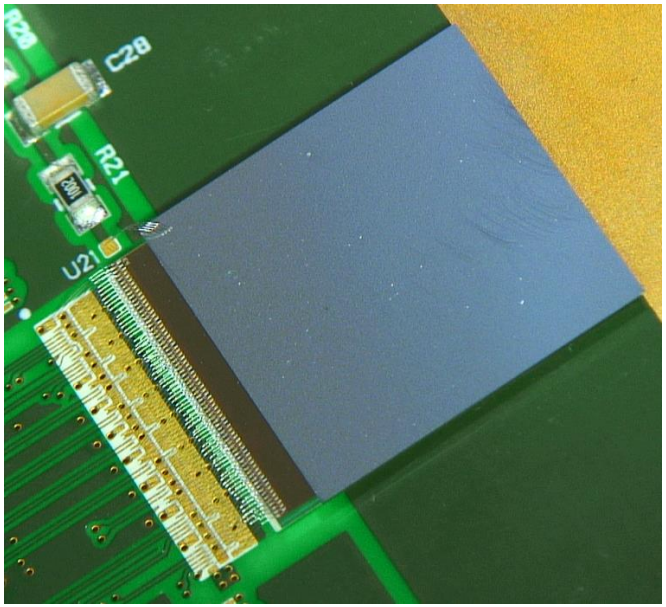
Summary of pixel measurements

Pixel gain	~24.6 mV/Ke$^-$
Pixel to pixel gain variation	~3.3%
Pixel ENC	62.9 e$^-$
Pixel to pixel threshold mismatch	410 e$^-$rms
Pixel to pixel threshold mismatch calibrated (Threq)	40.3 e$^-$rms
Expected minimum threshold	> 450 e-

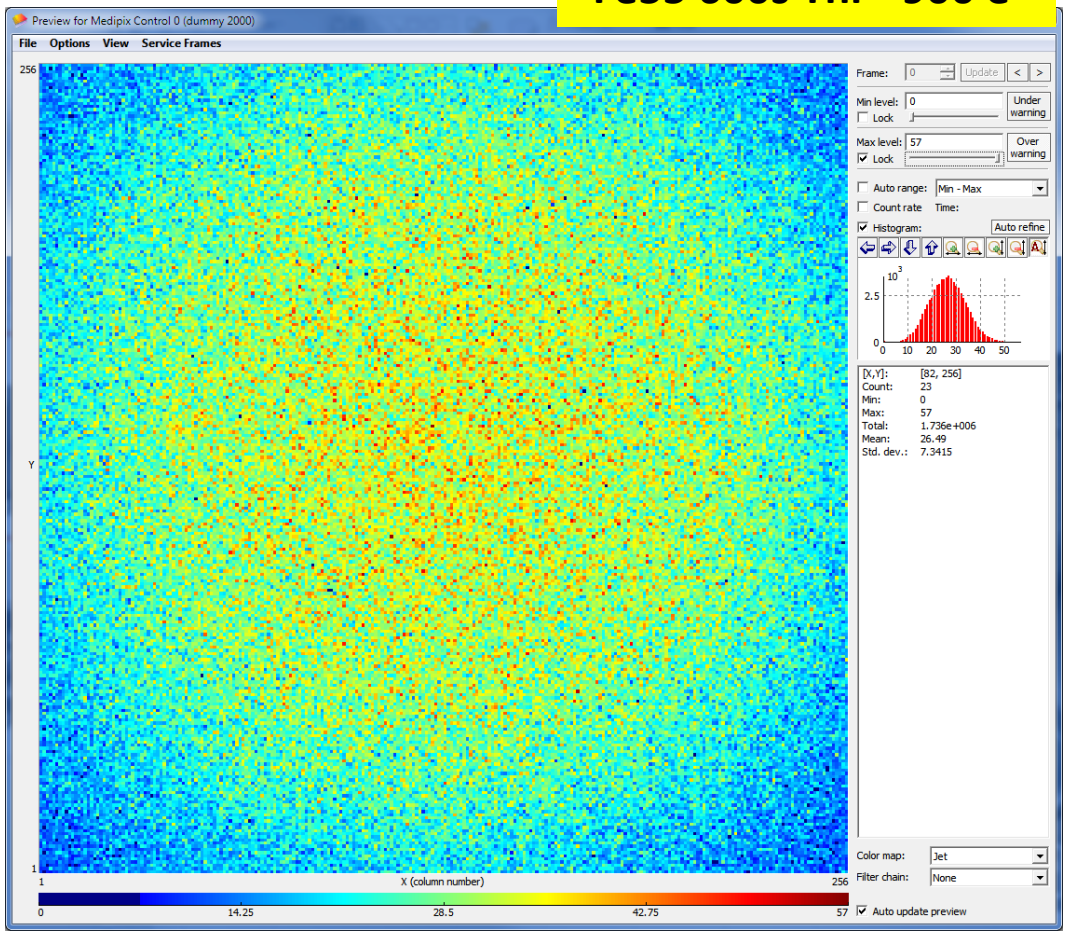
Threshold equalization only calculated not measured on chip
All measurements assuming Ctest=5fF

First source measurements

- First single chip assemblies available since last week at CERN



Fe55 600s Thr ~900 e-



Conclusions

- VeloPix ASIC designed in 130nm CMOS
- First results show the chip is alive and eyes open:
  - Power < 2 W/ASIC, DACs working, pixels functional
  - Pixel: Gain ~25 mV/Ke- and ENC 63 e- (no sensor)
  - GWT serializer working
- All measurements, so far, indicate that the Velopix chip is fully functional as designed:
  - First source images taken in photon counting mode : Slow Control
  - Still to test the full binary readout chain
  - Scheduled TID and SEU campaigns to validate design robustness
- Production testing later this year at CERN