ICECAL: a 4 channel ASIC for the Upgrade of the LHCb Calorimeter

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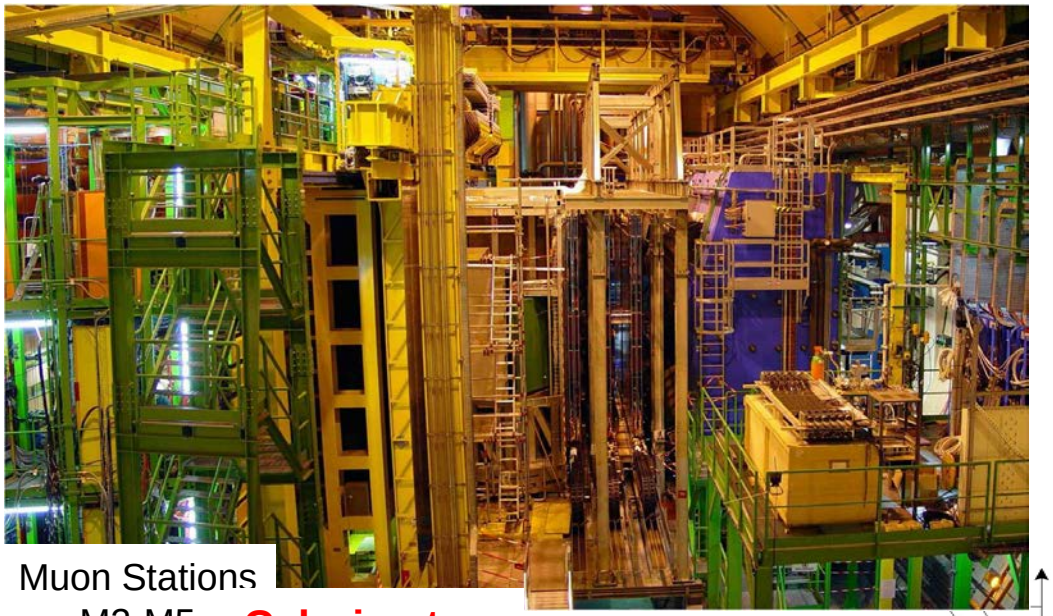
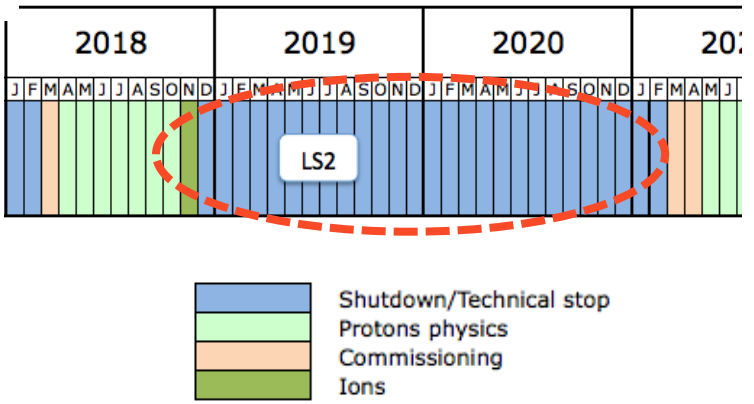
I. Introduction: LHCb upgrade

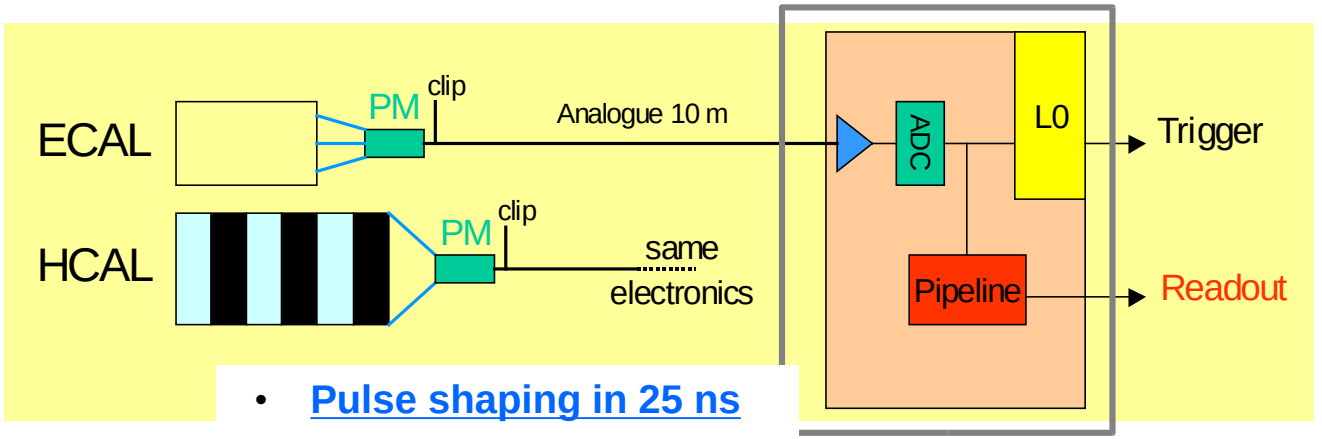


- Increase luminosity by factor 5
  - Instantaneous: $2 \cdot 10^{33}$ $cm^{-2}s^{-1}$
- Major changes:
  - VELO and tracking detectors
  - RICH detectors
  - All FE @ 40 MHz: SW trigger
- LHCb Collaboration intends to upgrade the detector during the long LHC shutdown 2.

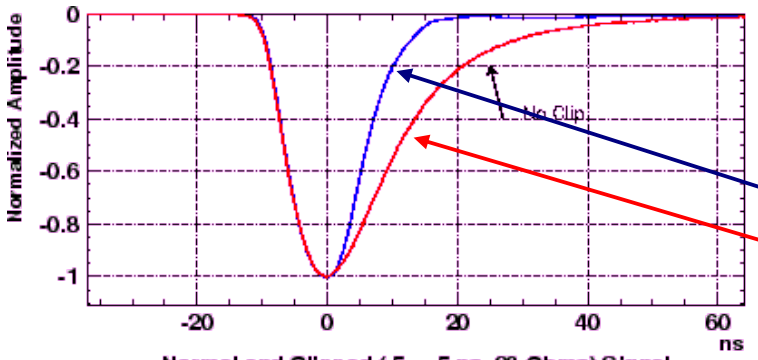


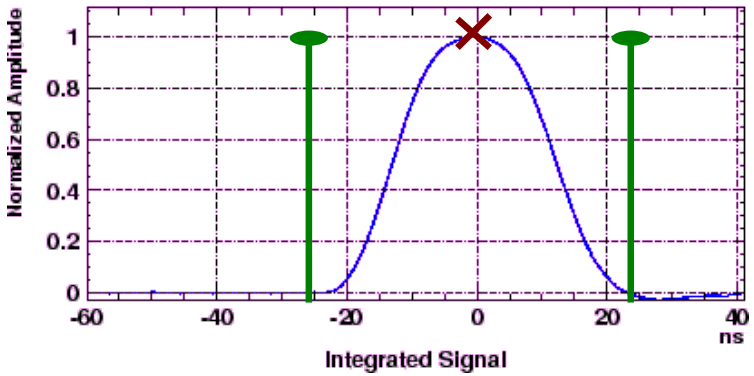
I. Introduction: current ECAL/HCAL FE

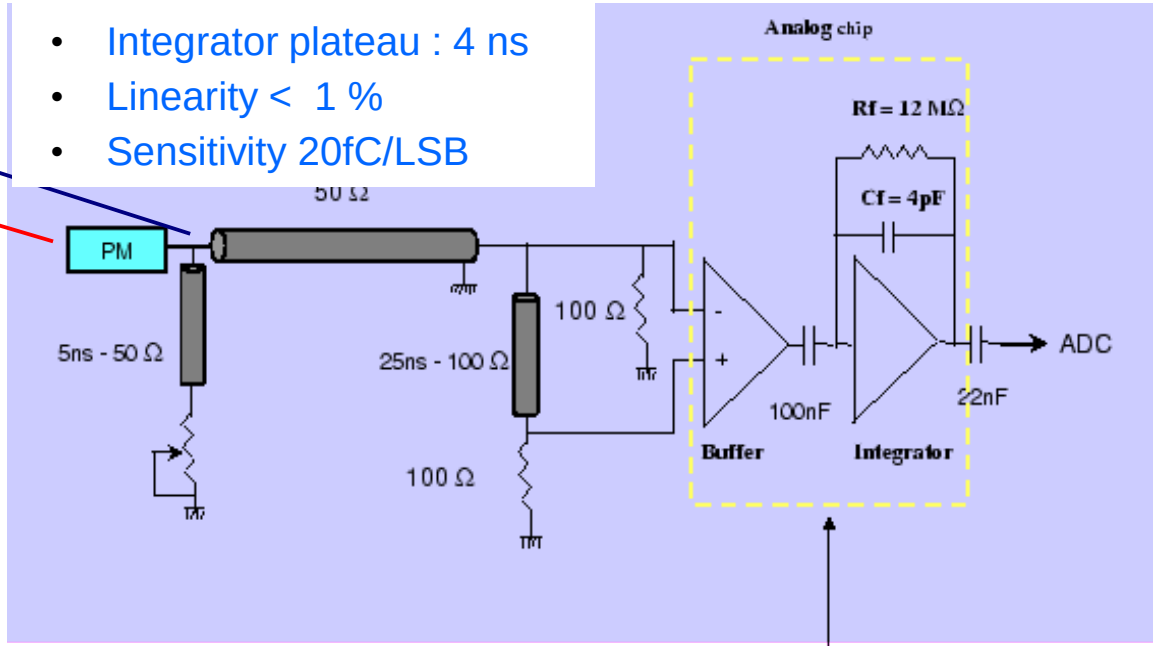
LAL-Orsay



- **Pulse shaping in 25 ns**
- Residue < 1% after 25 ns
- Integrator plateau : 4 ns
- Linearity < 1 %
- Sensitivity 20fC/LSB







BiCMOS 0.8um Integrated Circuit
4 Channels per chip

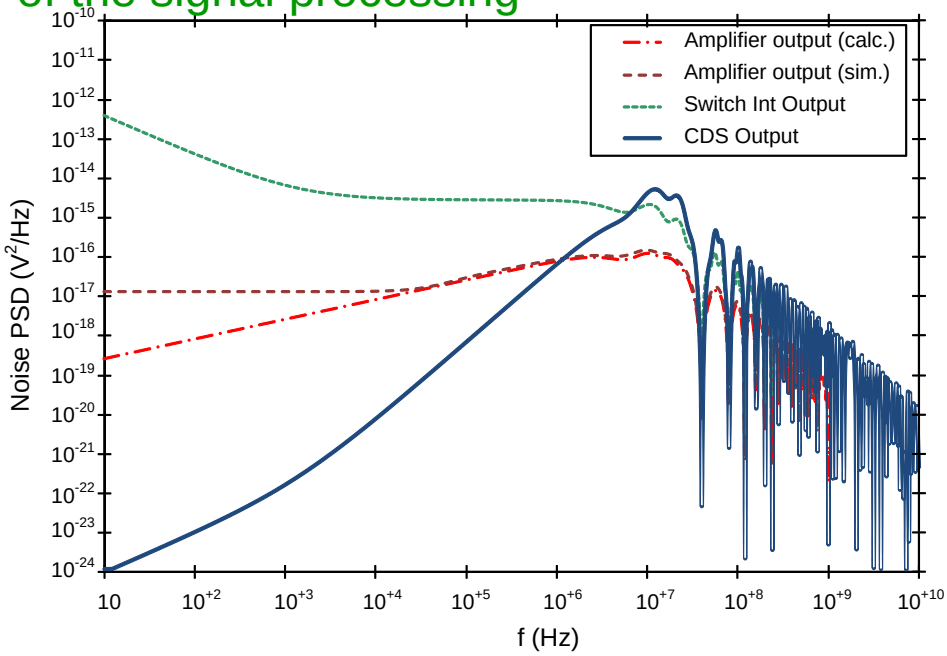
I. Introduction: requirements

- New front end board is required:
  - Low noise analog electronics:
    - ASIC (ICCUB and URL)
  - Digital signal processing and GBT for data readout @ 40MHz (LAL)

- PM current has to be reduced by factor ~ 5:
  - FE gain increases to 4 fC/LSB
    - LSB is kept at 2.5 MeV
  - FE input equivalent noise should reduce from 20 fC to 4fC

- Signal processing elements (analog):
  - Amplification
  - Integration / shaping
- Dynamic pedestal subtraction (or CDS):
  - Needed to correct baseline shift
  - And to filter LF noise (pick-up)
    - **Has proven to be crucial in LHCb**
  - Noise PSD in signal increases by ~ sqrt(2)

Noise PSD at different stages of the signal processing



II. Circuit design: channel architecture

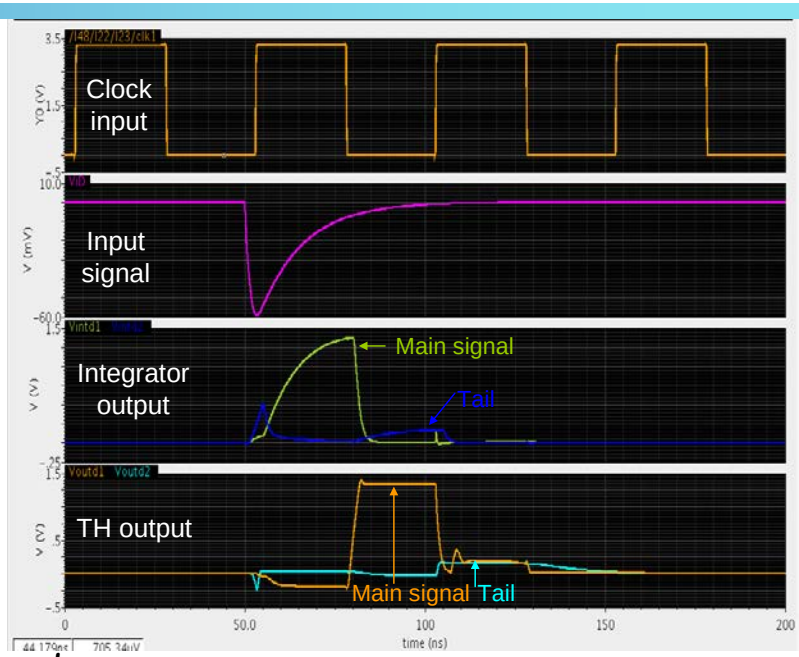
Very difficult to integrate HQ analog delay lines

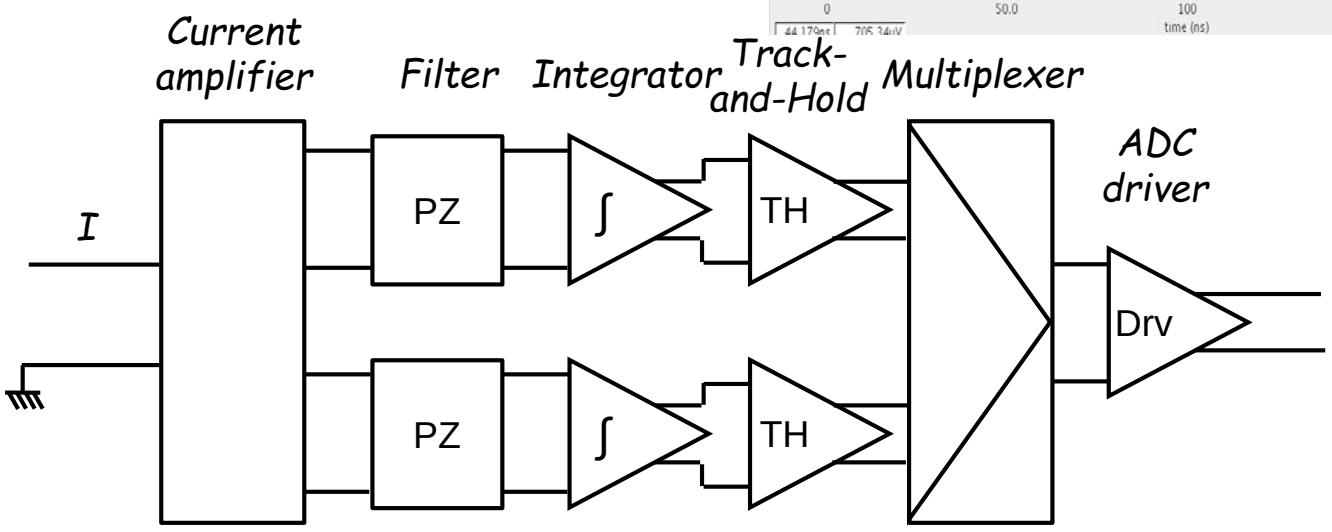
2 switched alternated paths

Switching noise !

Fully differential ASAP

- Current mode amplifier
- Pole-Zero cancellation
- Switched integrator
- Track and hold
  - 12 bit: flip-around architecture
- Analog multiplexer
- ADC driver
  - To match ADC input impedance





More demanding: e_n increases by sqrt(2): active termination

II. Circuit design: input stage: current output / current feedback

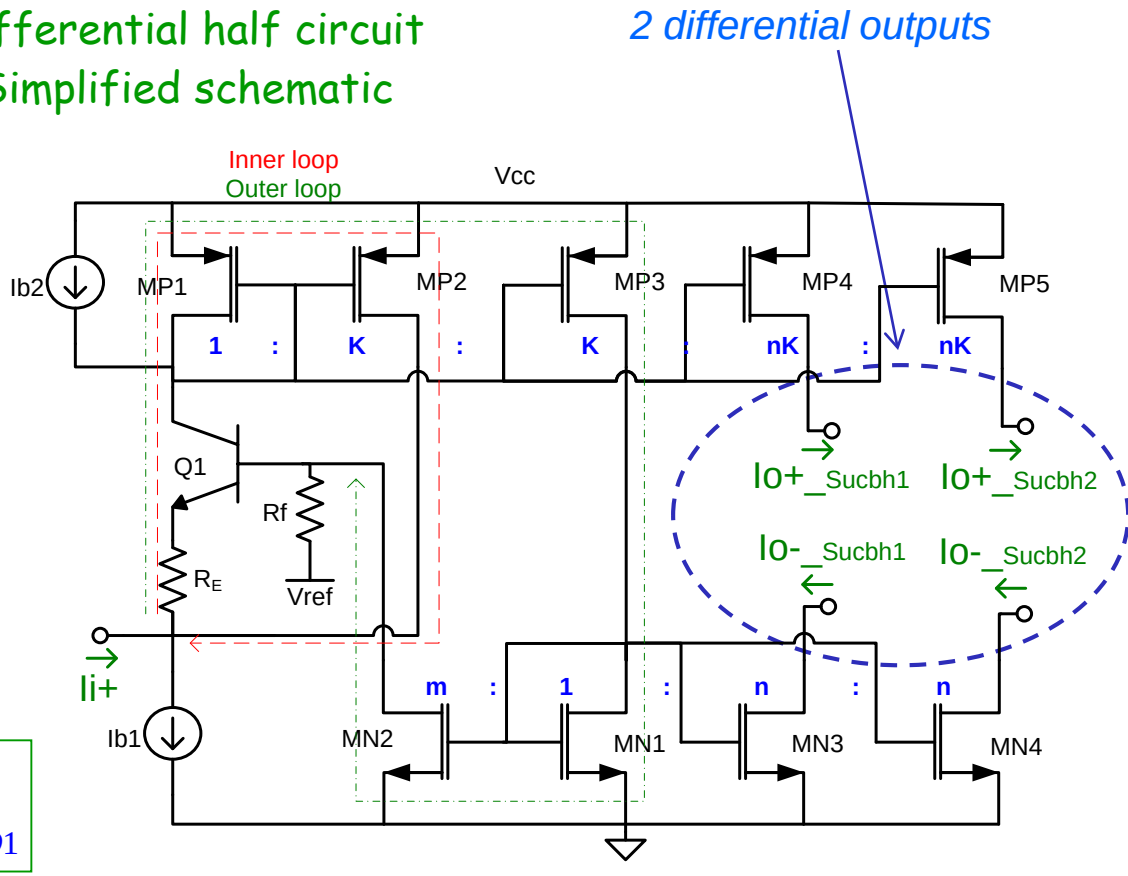
- **Double current feedback:**
  - Inner loop: lowers input impedance
    - Current feedback gain: K
  - Outer loop: controls input impedance
    - Current feedback gain: Km
- **Current gain:** 2n
- **Input impedance**

Open loop input impedance

$$Z_{i_{OL}}^{0} = R_E + \frac{1}{g_{mQ1}}$$

$$Z_i \approx \frac{1/g_{m1} + R_E}{1+K} + \frac{K}{1+K} mR_f$$

Differential half circuit
Simplified schematic



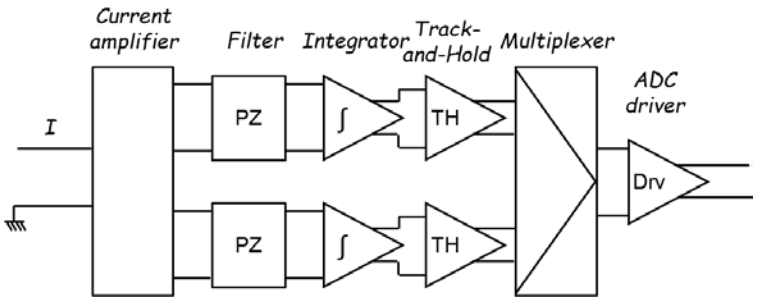
POWER < 10 mW

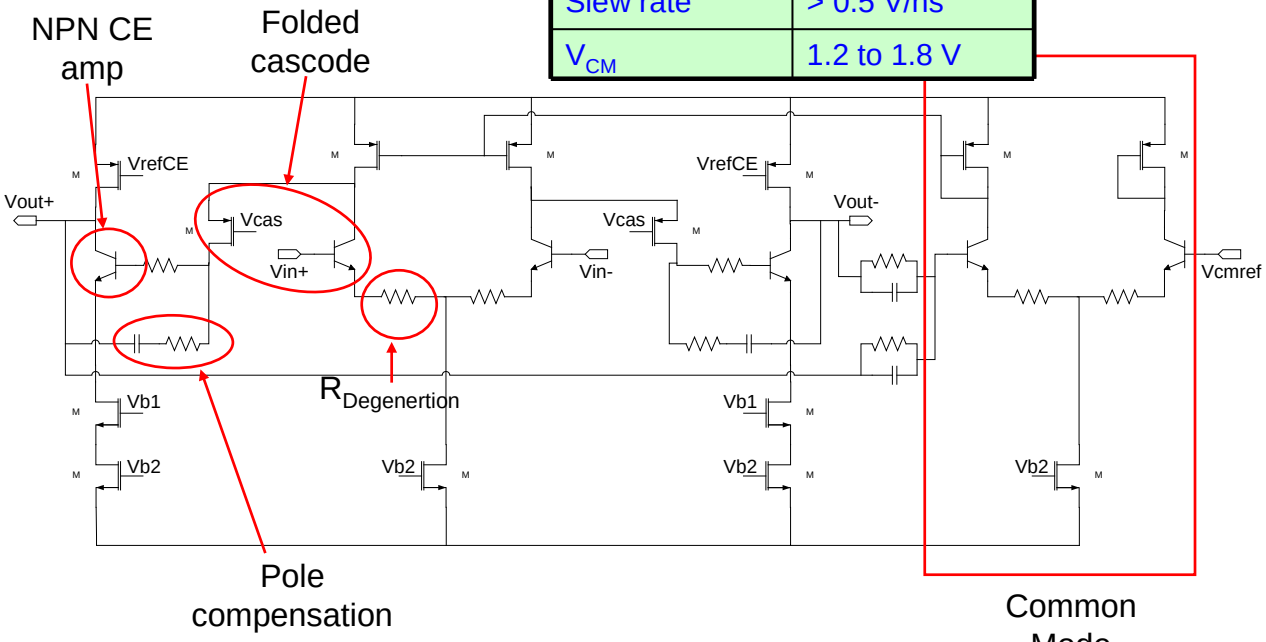
D. Gascon., E. Picatoste et al., "Low Noise Front End ASIC with Current Mode Active Cooled Termination for the Upgrade of the LHCb Calorimeter", IEEE Transactions on Nuclear Science, 59, 5, 2471-2478 (2012).

II. Circuit design: the channel

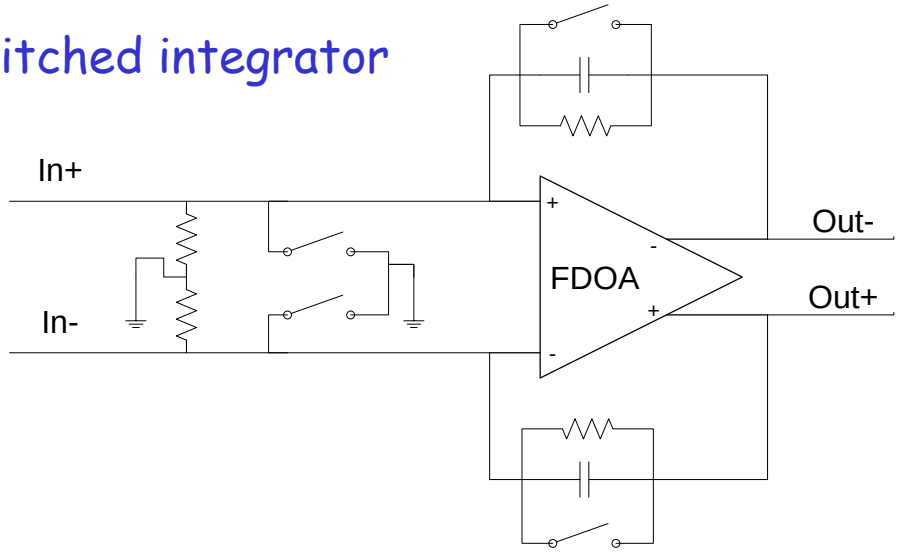
Fully Diff. OpAmp

FDOA specifications	
Parameter	**Value**
Gain bandwidth	500 MHz
Phase margin	> 65º
Slew rate	> 0.5 V/ns
V_{CM}	1.2 to 1.8 V

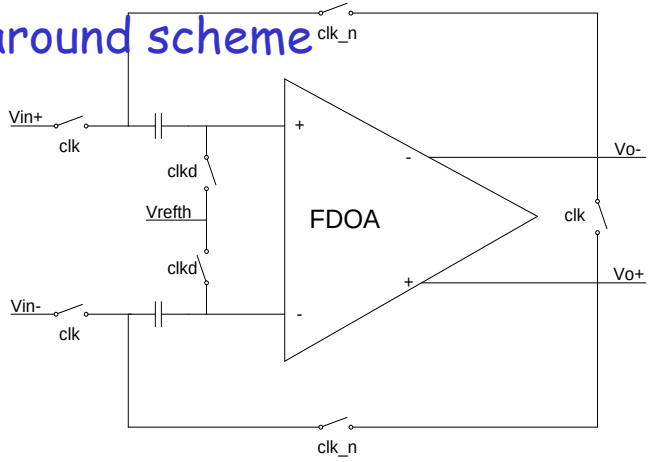




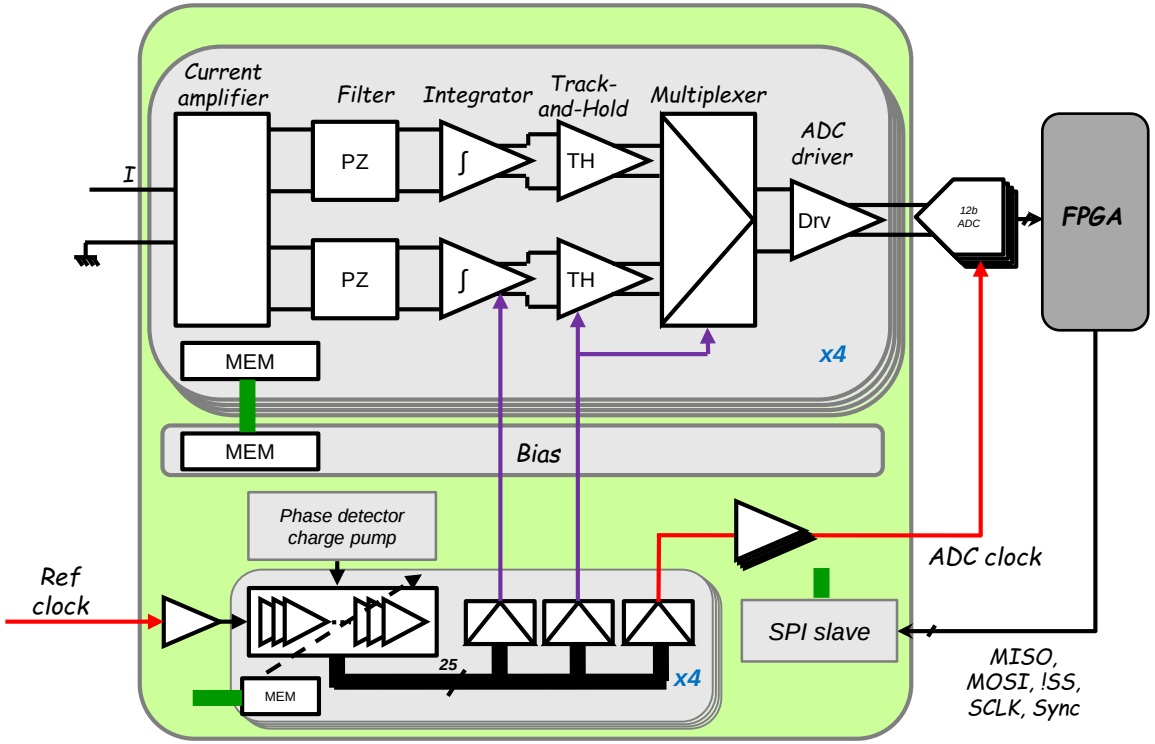
Switched integrator



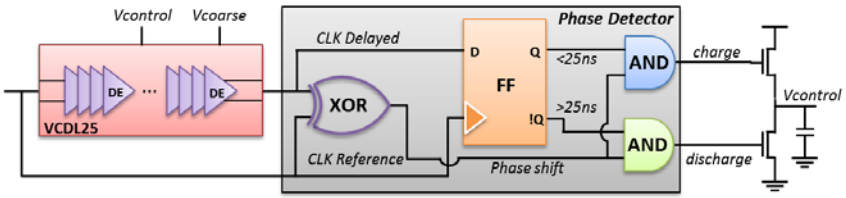
Track and hold
Flip around scheme

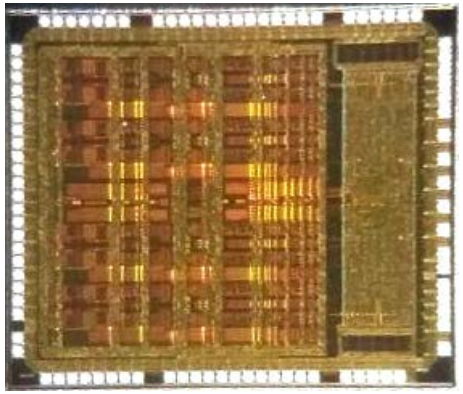


III. ICECALv3: 4 ch ASIC



- Complete 4 analog channels
- Tunable parameters
  - Input impedance
  - Filter parameters
  - Gain
  - Offset
  - Bias currents
- SPI interface
- On-chip DLL to generate synchronous clocks





ICECALv3 chip:

SiGe BiCMOS 0.35um
AMS 10.5 mm^2
Received: July 2014

Radiation hard programmable delay line for LHCb calorimeter upgrade
J. Mauricio et al. 2014 JINST 9 C01016

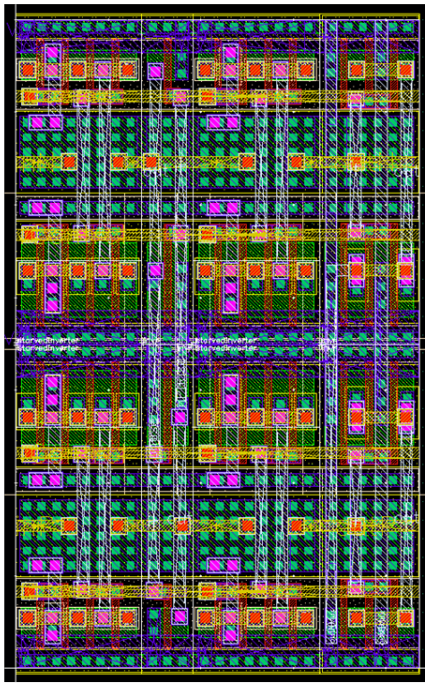
III. ICECALv3: radiation tolerant techniques

- SEL avoidance: guard rings
  - Analog blocs
  - Custom digital library

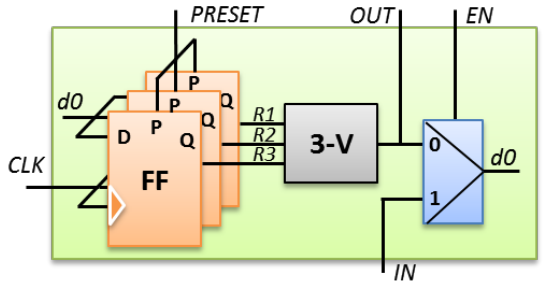
Extra Design Rules:

1. ≥ 5um between N-DIFF layer and NWELL.
2. Guard rings between PMOS and NMOS.

P+ ring
NMOS
P+ ring
N+ ring
PMOS
N+ ring
PMOS
N+ ring
P+ ring
NMOS
P+ ring



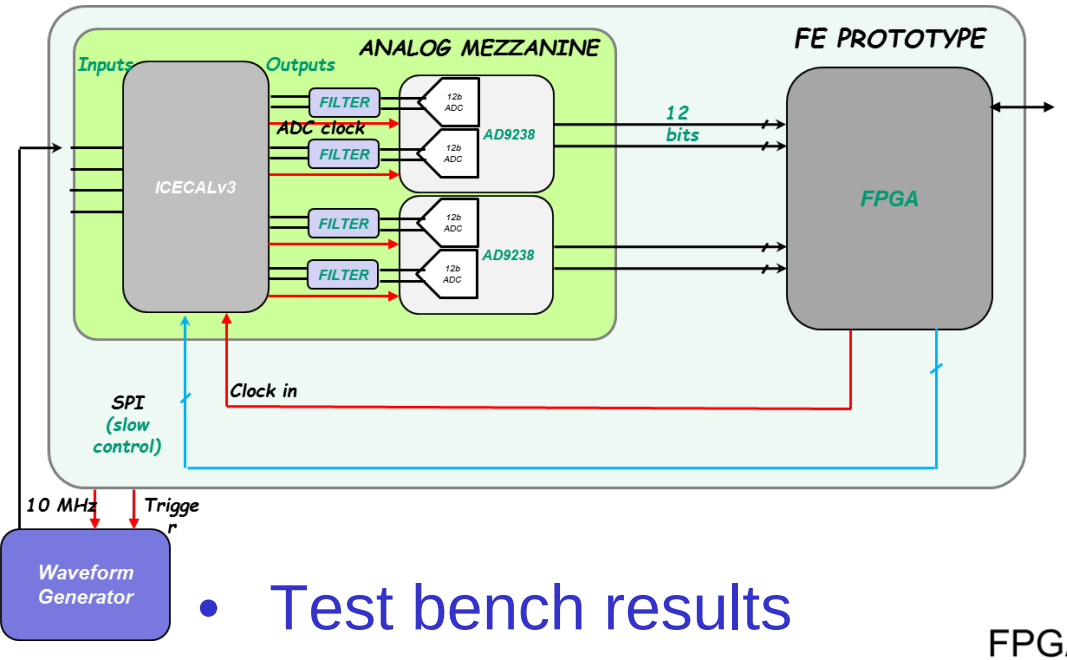
- 16-bit TMR registers:
  - Each bit is stored in 3 flip-flops.
  - Majority is computed.
  - SEUs are automatically corrected.

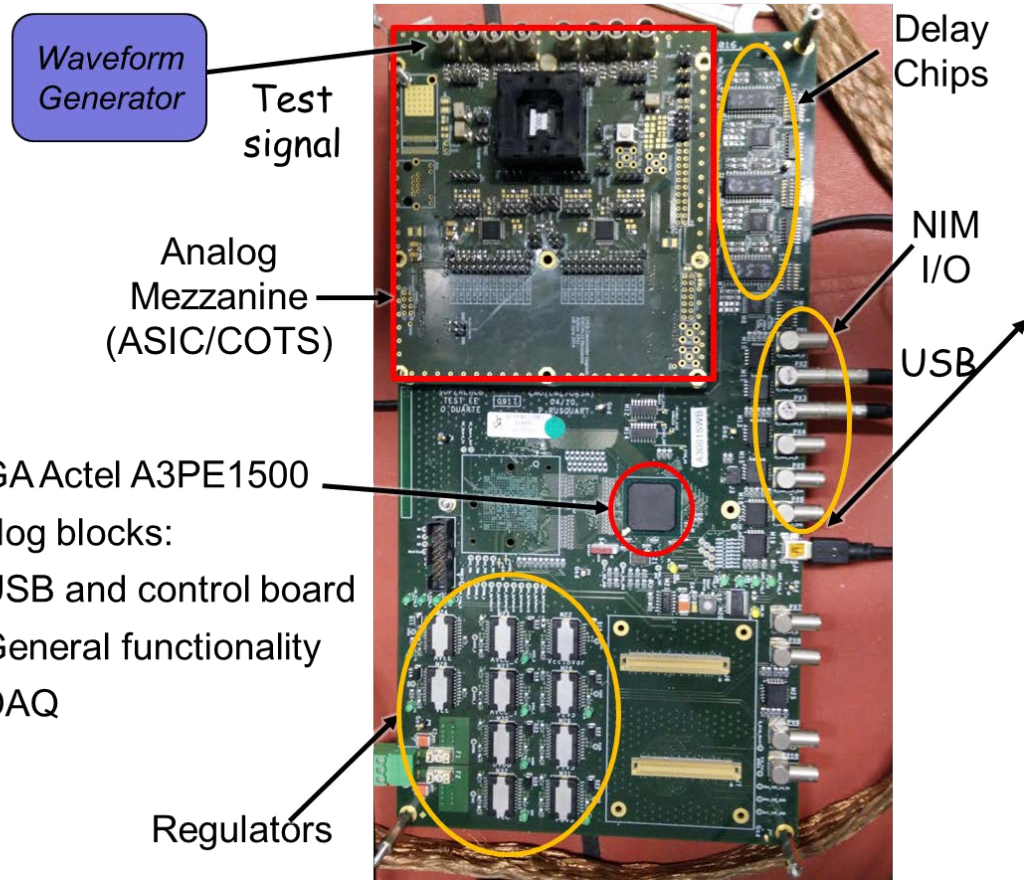


- SPI Slave control unit FSM:
  - SEU tolerant.

Example: Delay Element

IV. Test results: lab test bench with FEB prototype



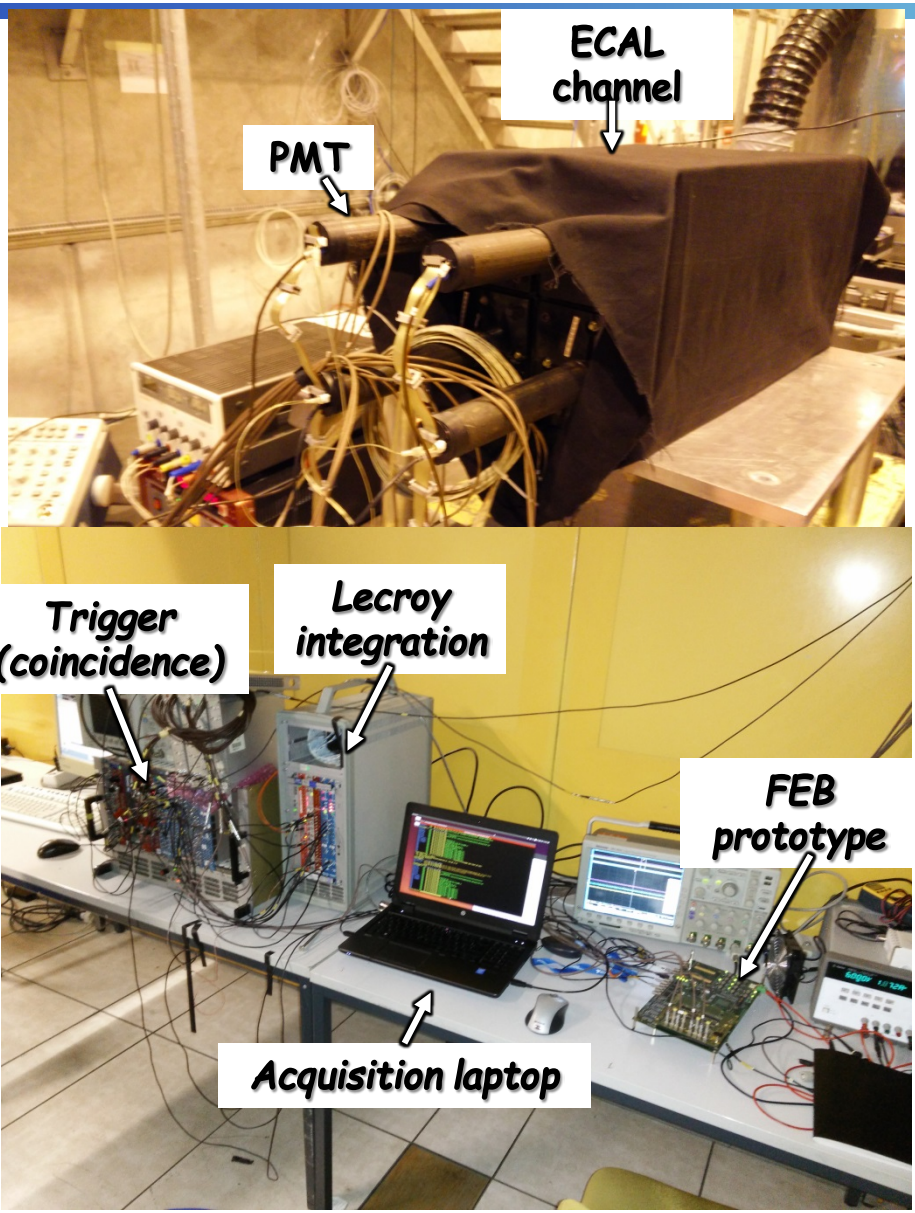


- Test bench results
  - Calibration is 4.5 fC/LSB
  - Linearity is within 1%
  - Crosstalk is below 0.5%
  - Plateau is about 4 ns
  - Spill over is below 1%
    - Except T2 (~2%)
  - Noise w/o pedestal subtraction: 1.4 LSB
  - Noise w pedestal subtraction: 1.7 LSB

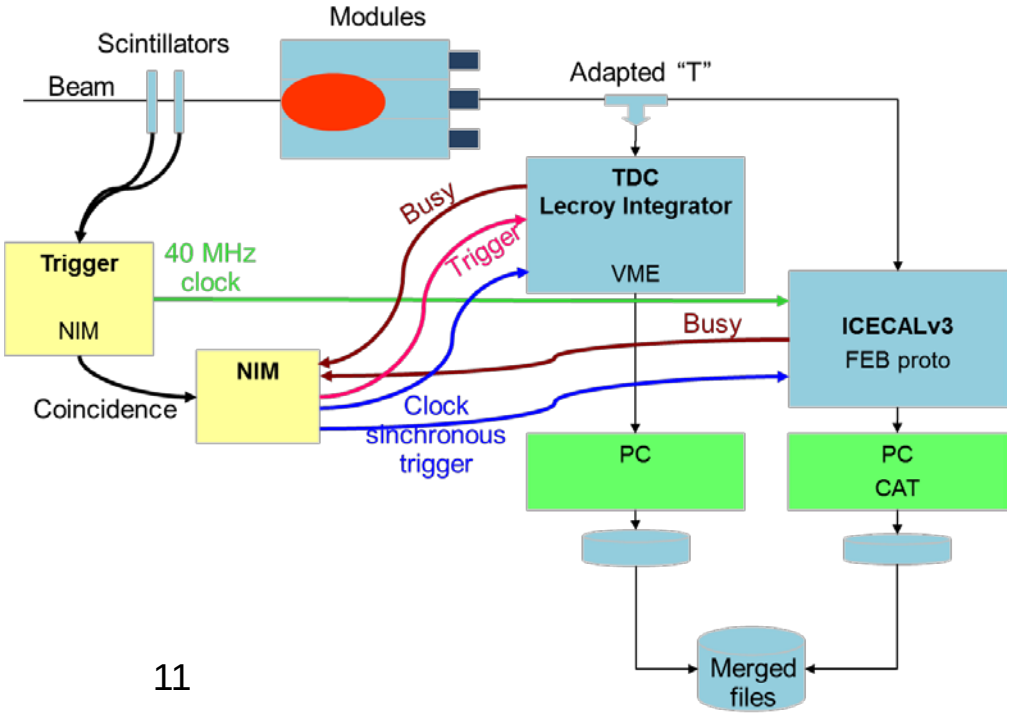
Verilog blocks:

- USB and control board
- General functionality
- DAQ

IV. Test results: test beam with FEB prototype



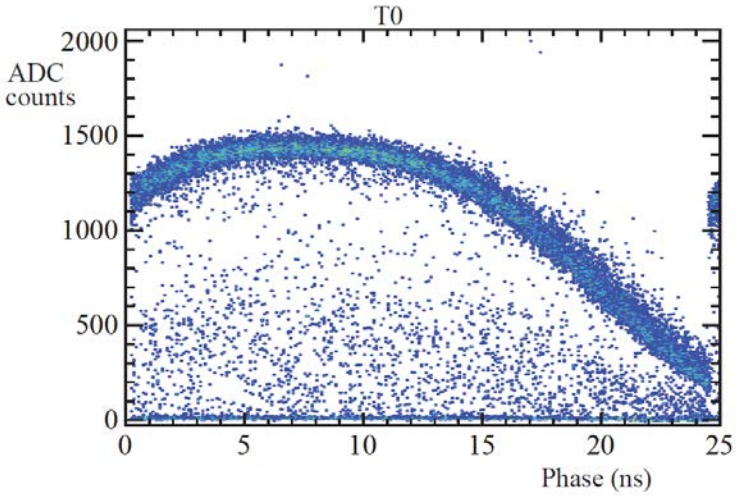
- When: April/November 2015
- Test beam at CERN Prevessin
- Beam: e^- with energy ranging from 20 to 120 GeV
- Elements used:
  - 4x(ECAL module+PMT+12m cable)
  - FEB prototype
  - Lecroy integrator
  - Time-to-Digital Converter (TDC)
  - ICECALv3 ASIC



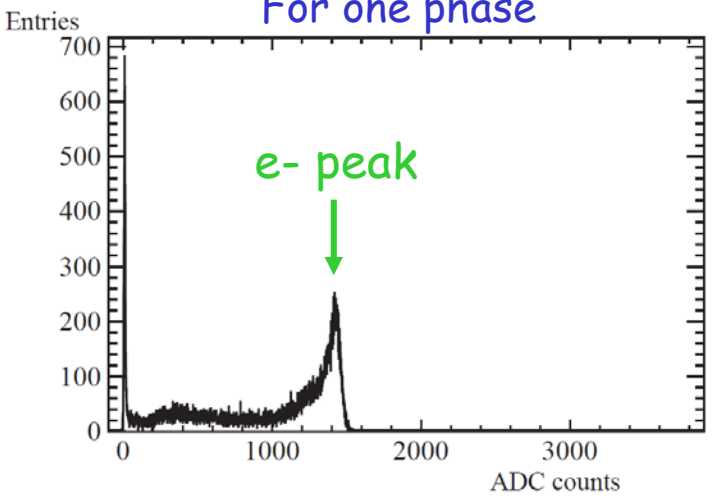
IV. Test results: test beam with FEB prototype

Typical measurement

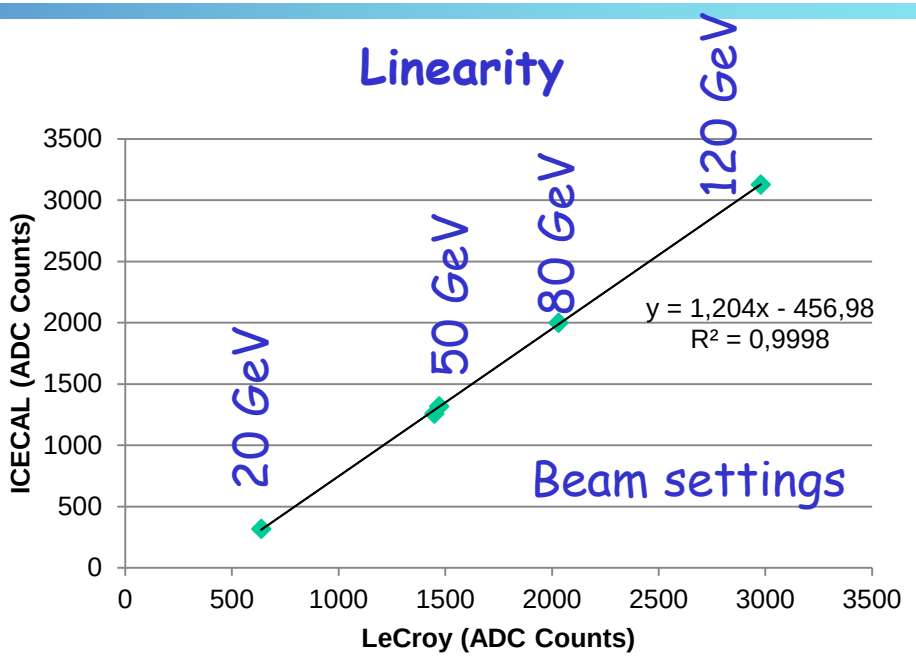
TDC provides time of arrival of particles wrt clock



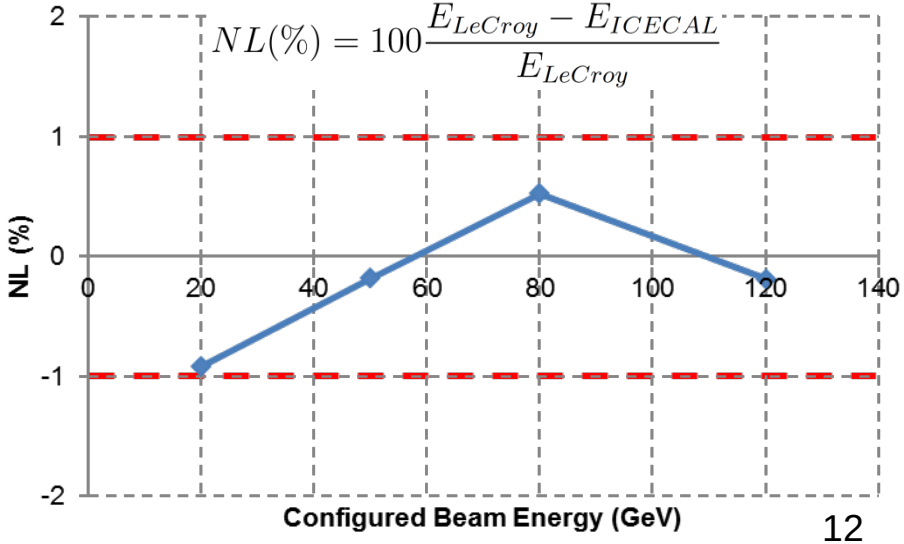
For one phase



Linearity

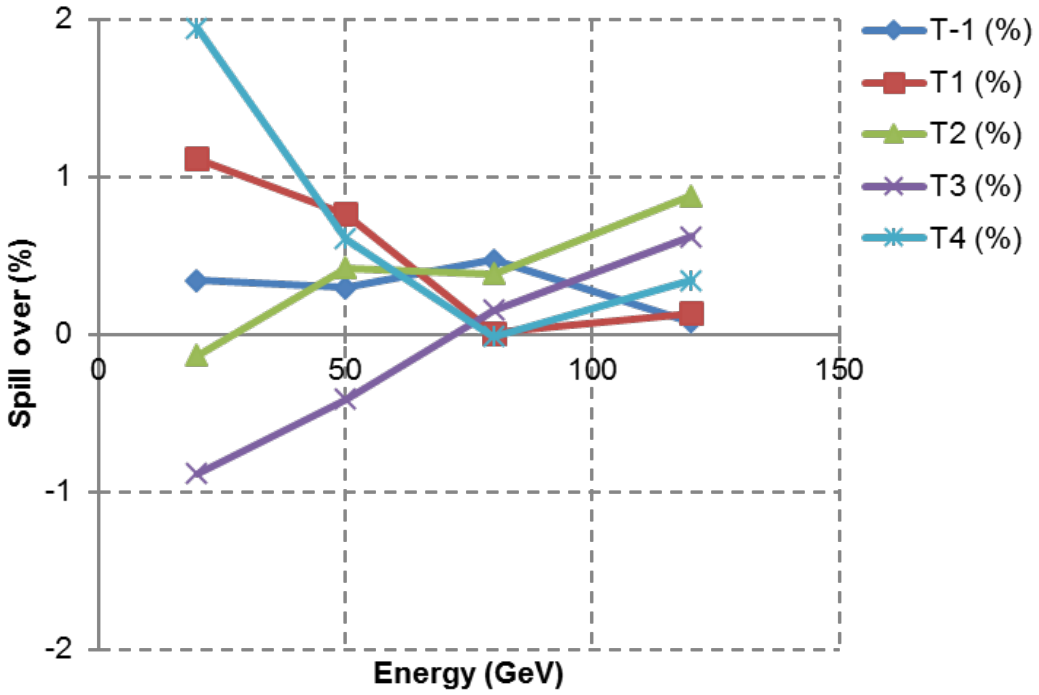


$$NL(\%) = 100\frac{E_{LeCroy} - E_{ICECAL}}{E_{LeCroy}}$$

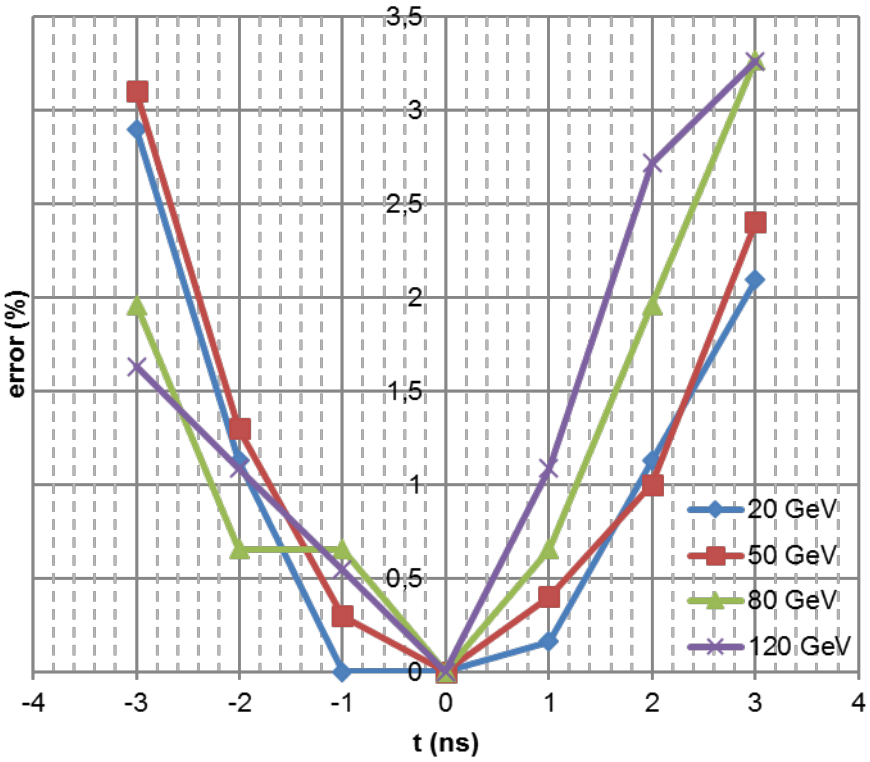


IV. Test results: test beam with FEB prototype

Spill-over vs energy



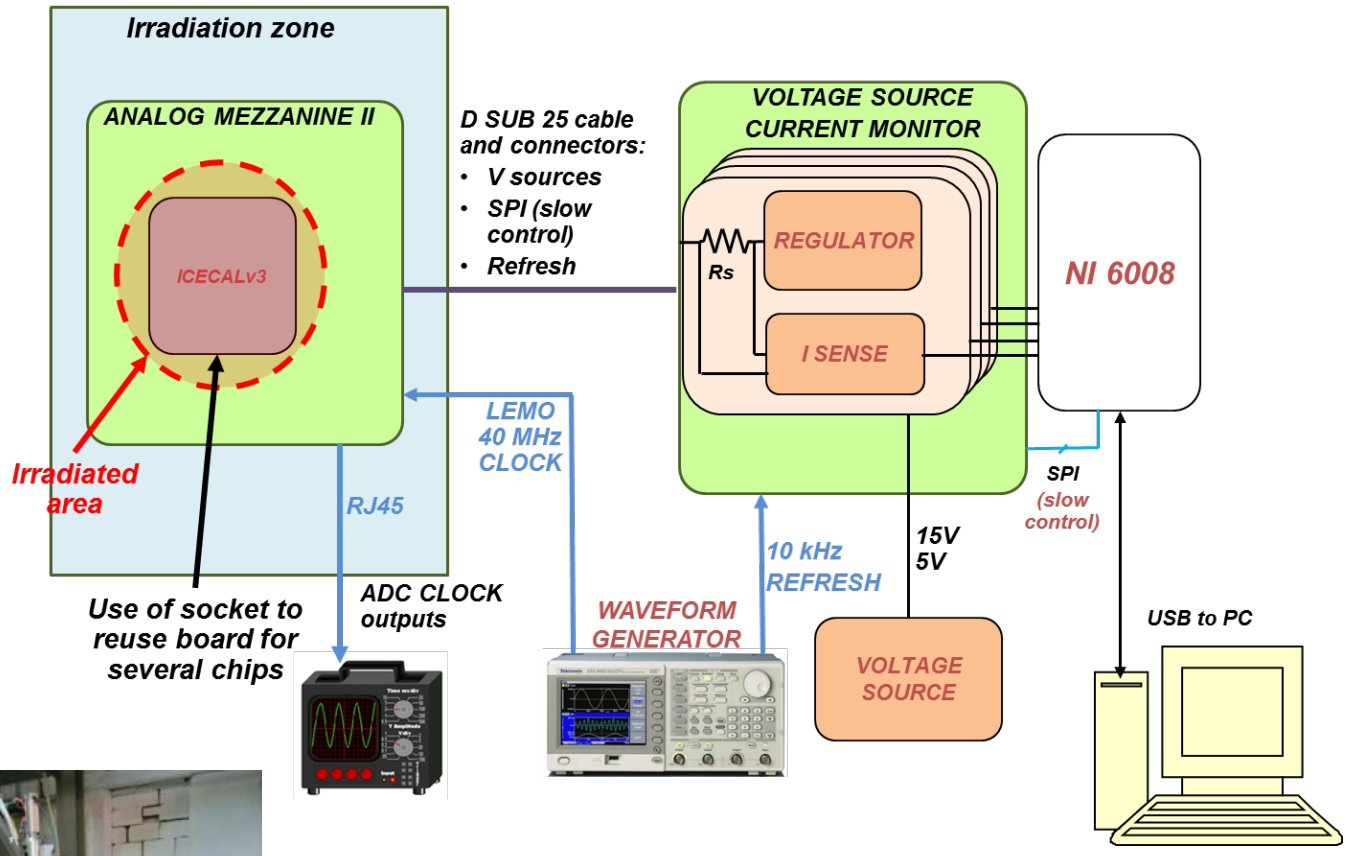
Plateau vs energy

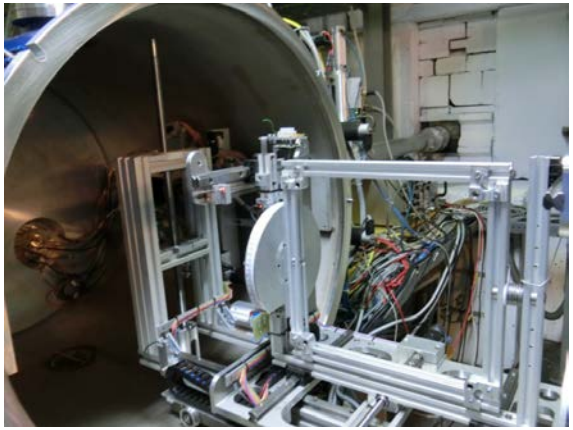


- Noise is higher than in the lab
  - 12 LSB without pedestal subtraction
  - 2.7 LSB with pedestal subtraction
  - It is caused by switching noise of CW HV supply in PMT base

V. Radiation qualification

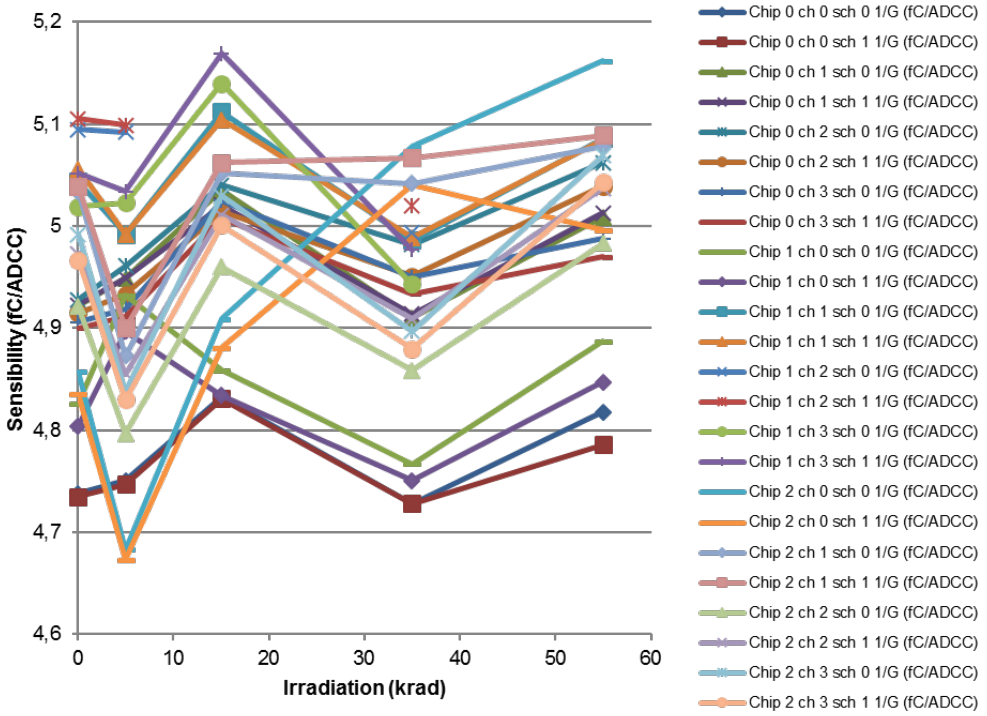
- Expected radiation levels for 50fb^{-1}:
  - Dose: 5krad
  - Total neutron fluence: 2.55·10^{12} cm^{-2}
- Tests:
  - TID with 61 MeV protons
  - SEE with Heavy Ion
- Louvain-la-Neuve
  - 13-14 July 2016

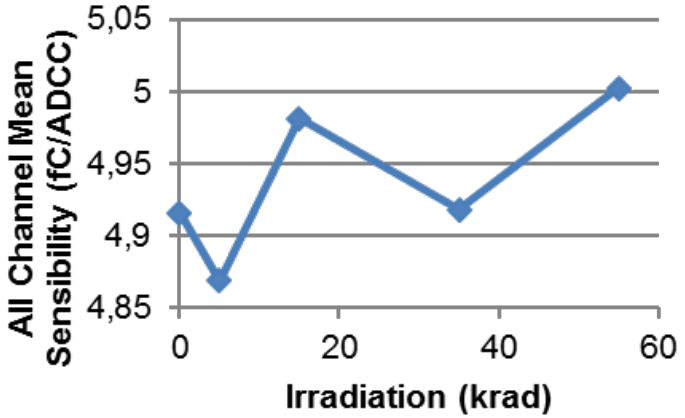




V. Radiation qualification: TID

- General procedure:
  1. Characterize chip
  2. Irradiate
  3. Characterize chip
- Characterization
  - Gain (linearity)
  - Plateau and spill over
  - Noise
- Use beam of 61 MeV protons
  - 55 krad for 3 chips
  - 40 krad for 1 chip
  - Several irradiation steps
- During irradiation no SEU or SEL was detected
- No effect on noise, linearity or timing (spill-over and plateau)
- Possible variation in sensitivity (< 2%)



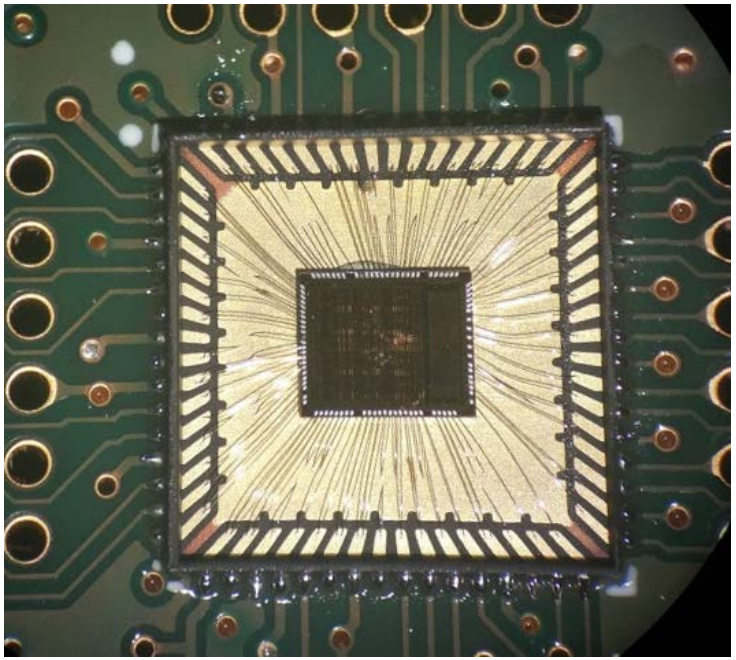


V. Radiation qualification: heavy ions

- Irradiate with heavy ions: expected max LET is 15 MeV/mg/cm^2

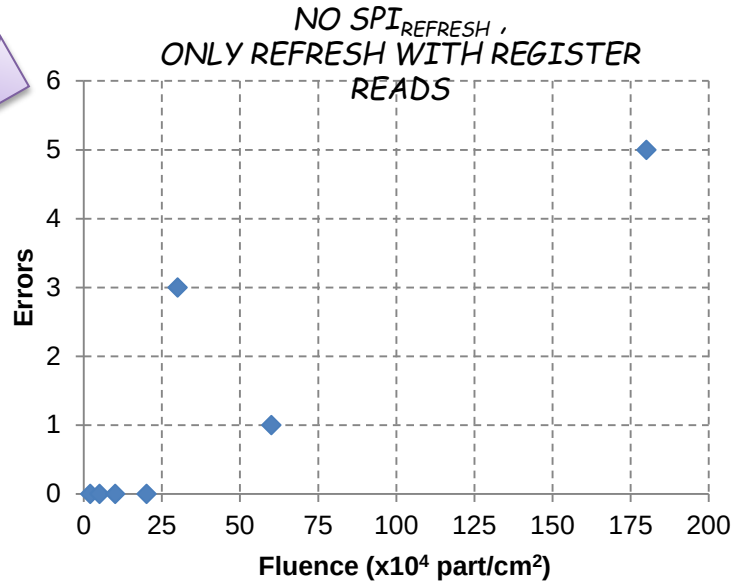
M/Q	Ion	DUT energy [MeV]	Range [μm Si]	LET [MeV/mg/cm^2]
3.25	$^{13}C^{4+}$	131	292	1.1
3.14	$^{22}Ne^{7+}$	235	216	3
3.33	$^{40}Ar^{12+}$	372	117	10.2
3.22	$^{58}Ni^{18+}$	567	100	20.4
3.32	$^{83}Kr^{25+}$	756	92	32.6
3.54	$^{124}Xe^{35+}$	995	73	62.5

- Beam homogeneity of 10% on a 25 mm diameter
- Irradiations are done in vacuum
- Naked chips: soldered chips without lid cover
- Two chips were irradiated:
  - 1st chip up to 2.087·10^8 part/cm^2
  - 2nd chip up to 1.008·10^8 part/cm^2



V. Radiation qualification: SEU

- SEU without triple voting
  - No SEU detected if fluence < $3 \cdot 10^5$ part/cm^2
- SEU with triple voting
  - No SEU detected after a fluence of $9.45 \cdot 10^7$ part/cm^2
- SEU limit with triple voting
  - From simulations:
    - 420 part/s at $5 \cdot 10^{32}$ cm^{-2}s^{-1}
    - ~1680 part/s at the upgrade maximum instantaneous luminosity ($2 \cdot 10^{33}$ cm^{-2}s^{-1})
    - Total fluence: $4.2 \cdot 10^{10}$ part/cm^2
  - Protons vs. Ions: 10^6 factor to break Si nucleous
  - Expected limit for all the detector and experiment life: 1.3 SEU

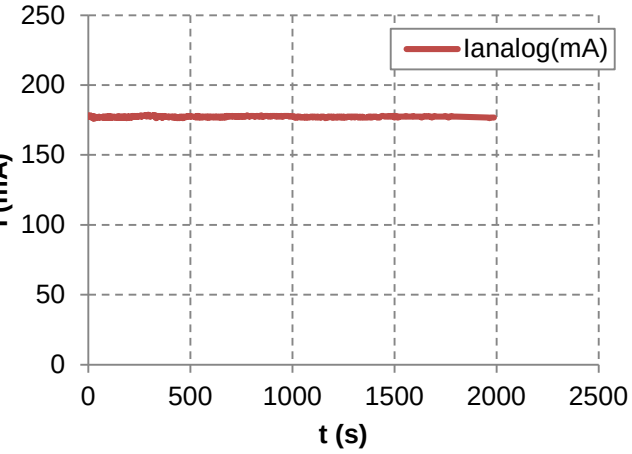


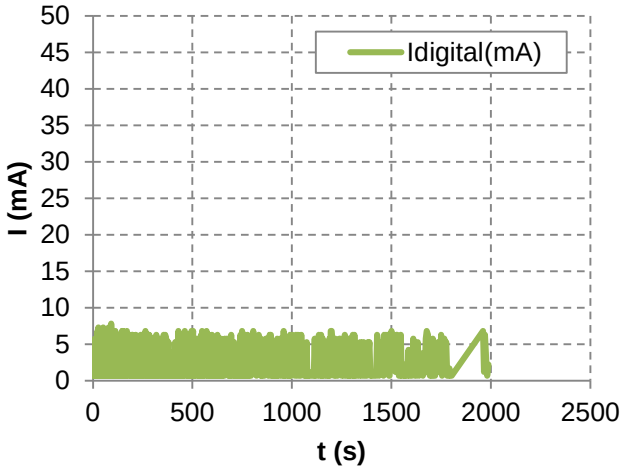
$$N_{SEU,\,LIMIT} = \frac{\Phi_{test}}{\Phi upgrade} \times N_{chips}$$

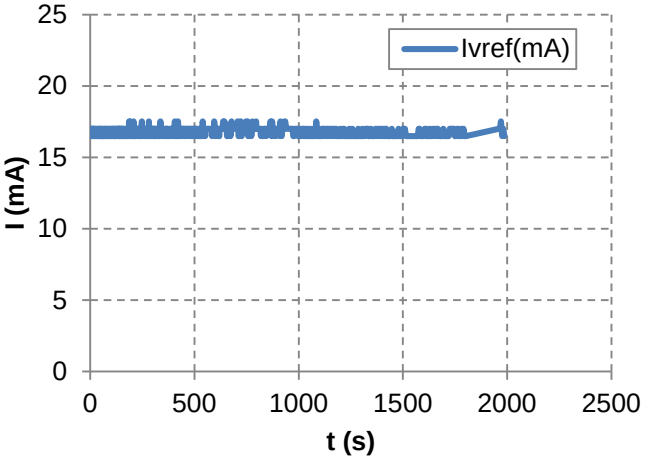
V. Radiation qualification: SEL

- No SEL detected during all irradiations
  - Proton beam
    - Fluence = $1.48 \cdot 10^{12}$ part/cm^2
    - Expected limit for all the detector and experiment life: 57
  - Ion beam
    - Fluence = $9.71 \cdot 10^{7}$ part/cm^2
    - Expected limit for all the detector and experiment life: 0.9

Current measurement examples







VI. Conclusions and outlook

- ICECAL is a 4 ch ASIC for the upgrade of the LHCb calorimeter
  - 12 bit dynamic range
  - Signal processing in 25 ns
- ICECAL has been validated both in lab test benches and dedicated test beams
- Basic requirements are met
  - Higher noise is measured when connected to CW PMT bases
  - No modification of CW bases is required
    - Noise introduced by pile-up at high luminosity will mask the effect
    - A gain reduction in ICECAL is considered to increase dynamic range
- ICECAL has been qualified to operate at the radiation level expected for the upgrade with ample safety margin

Thanks for your attention !

Contact: dgascon@fqa.ub.es

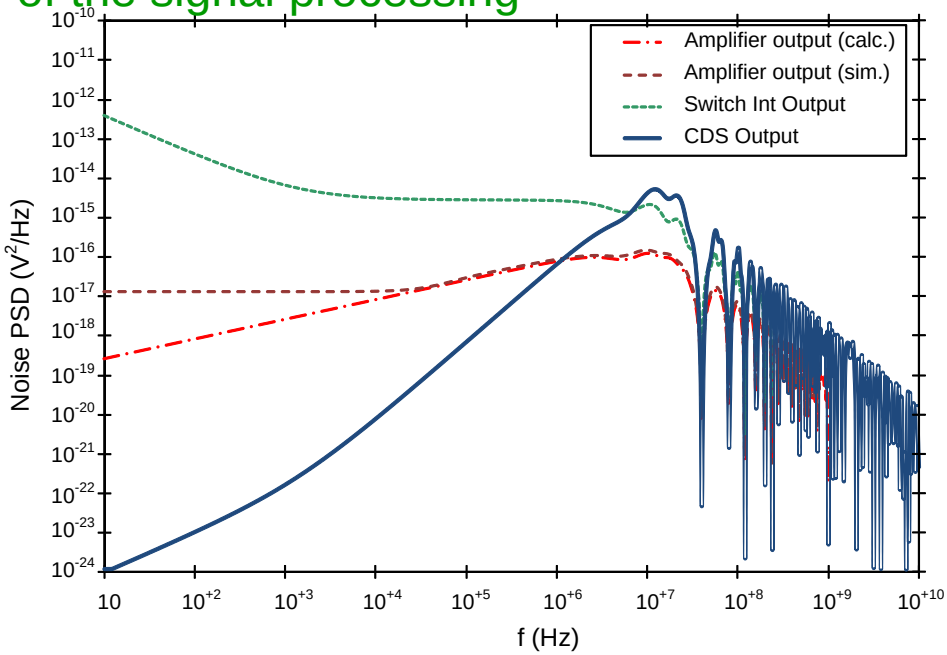
I. Introduction: requirements

- New front end board is required:
  - Low noise analog electronics:
    - ASIC (ICCUB and URL)
  - GBT for data transmission @ 40MHz (LAL)
- PM current has to be reduced by factor ~ 5:
  - FE input equiv. noise should still be ~ 1 LSB

Energy range	0-10 GeV/c (ECAL) Transverse energy
Calibration	4 fC /2.5 MeV / LSB
Dynamic range	4096-256=3840 :12 bit
Noise	<≈1 LSB or ENC < 4 fC
Termination	50 ± 5 Ω
Shaping	25 ns (99 % of the charge)
Spill-over noise	< LSB
AC coupling	5-20 μs
Baseline shift Prevention	Dynamic pedestal subtraction (CDS) Pedestal is the smallest of 2 prev. samples
Max. peak current	4-5 mA (clipped)
Spill-over correction	Clipping
Linearity	< 1%
Crosstalk	< 0.5 %
Timing	Individual (per channel)

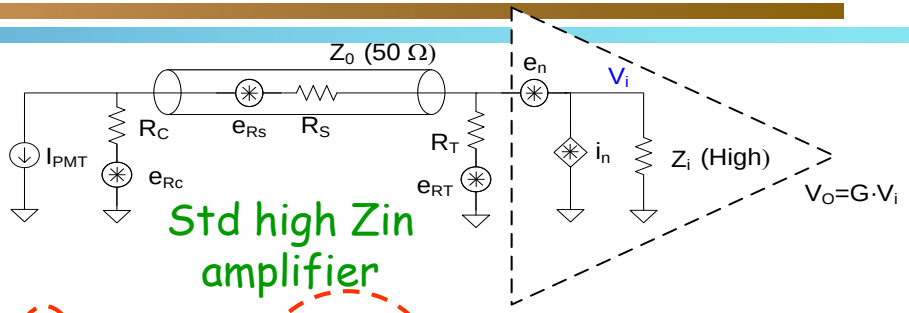
- Signal processing elements (analog):
  - Amplification
  - Integration / shaping
- Dynamic pedestal subtraction (or CDS):
  - Needed to correct baseline shift
  - And to filter LF noise (pick-up)
    - **Has proven to be crucial in LHCb**
  - Noise PSD in signal increases by ~ sqrt(2)

Noise PSD at different stages of the signal processing



I. Introduction: noise requirements: why cooled termination ?

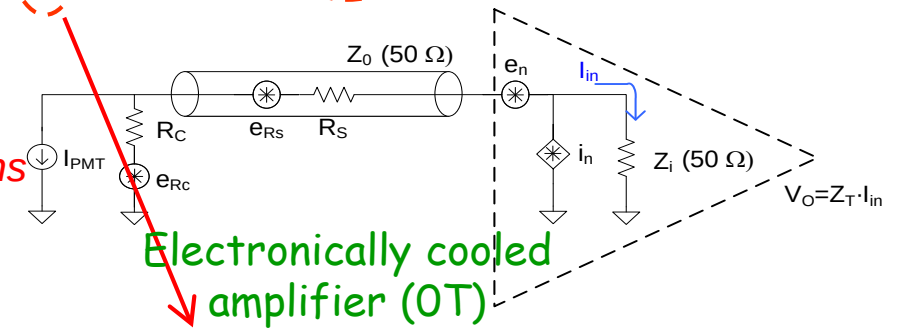
- Noise contributions of
  1. Std. high Zin voltage preamplifiers
  2. Current amplifier with cooled termination
- Referred to the clipped PMT current i_{nCLIP}
- ENC: amplifier + integrator (time T) + CDS:
  - White noise
    - Resistive source imp. $ENC^2_{A+I} \approx \frac{1}{2} i^2_{CLIP} T$
  - Amp BW >> 1/T $ENC^2_{A+I+CDS} \approx i^2_{CLIP} T$
- Assumptions:
  - Cable modelled as lumped element*
  - Cable seen as Z_0 at HF from amp. side*
  - $R_T=Z_0$ (V amp) and $Z_i=Z_0$ (I amp)
  - Uncorrelated noise for CDS



Std high Zin amplifier

$$i^2_{nCLIP} = \frac{e_n^2}{|Z_0|^2} + i_n^2 \left|\frac{1}{2}\right|^2 + \frac{4KT}{R_T}\left|\frac{1}{2}\right|^2 + \frac{4KT}{R_C}\left|\frac{R_C}{Z_0+R_C}\right|^2 + \frac{4KTR_S}{|R_S+Z_0|^2}$$

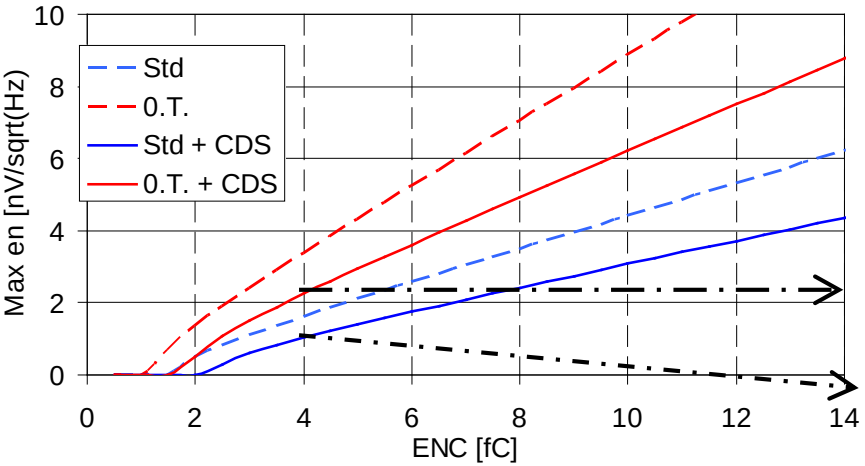
Typically dominant contributions



Electronically cooled amplifier (OT)

$$i^2_{nCLIP} = \frac{e_n^2}{|2Z_0|^2} + i_n^2 \left|\frac{1}{2}\right|^2 + \frac{4KT}{R_C}\left|\frac{R_C}{Z_0+R_C}\right|^2 + \frac{4KTR_S}{|R_S+Z_0|^2}$$

Total input referred series noise requirement



R_C=21 Ω
R_S=18 Ω
i_n neglected

OT with e_n< 2 nV/sqrt(Hz) fulfils requirements,
Whereas std amp should have e_n< 1 nV/sqrt(Hz) !

* R.L. Chase, C. de La Taille et alt., NIM A330, 1993

II. Circuit design: input stage: current output / current feedback

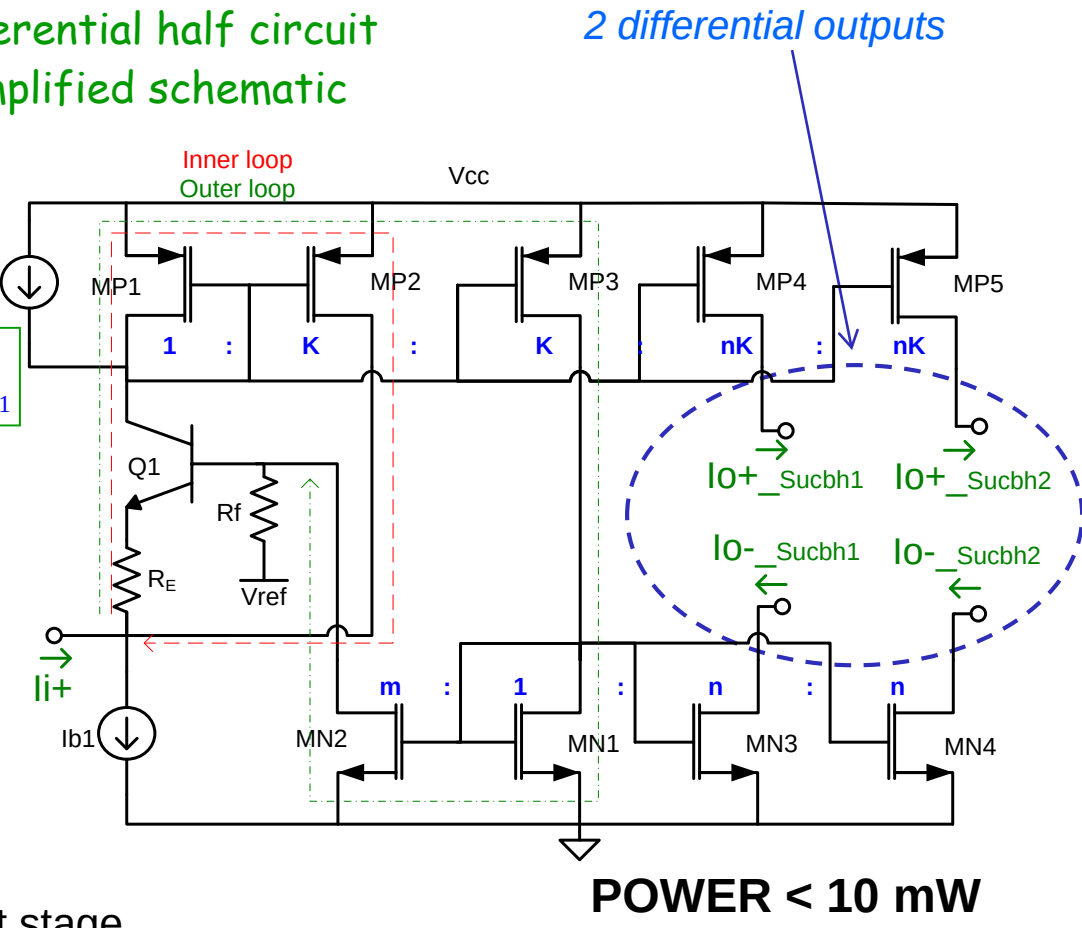
- Double current feedback:
  - Inner loop: lowers input impedance **
    - Current feedback gain: K
  - Outer loop: controls input impedance
    - Current feedback gain: Km
- Current gain: 2n
- Input impedance

Open loop gain $Z^0_{i_{OL}} = R_E + 1/g_{mQ1}$

$$Z_i \approx \frac{1/g_{m1} + R_E}{1+K} + \frac{K}{1+K} mR_f$$

- No external components
  - No additional pads
  - Can easily go to multichannel chip
    - Even with pseudo differential input
- Low voltage (large dynamic with 3.3 V)
  - Only 1 Vbe for the super common base input stage
- Good in terms of ESD:
  - No input pad connected to any transistor gate or base

Differential half circuit
Simplified schematic



POWER < 10 mW

D. Gascon., E. Picatoste et alt.," "Low Noise Front End ASIC with Current Mode Active Cooled Termination for the Upgrade of the LHCb Calorimeter ", IEEE Transactions on Nuclear Science, 59, 5, 2471-2478 (2012).

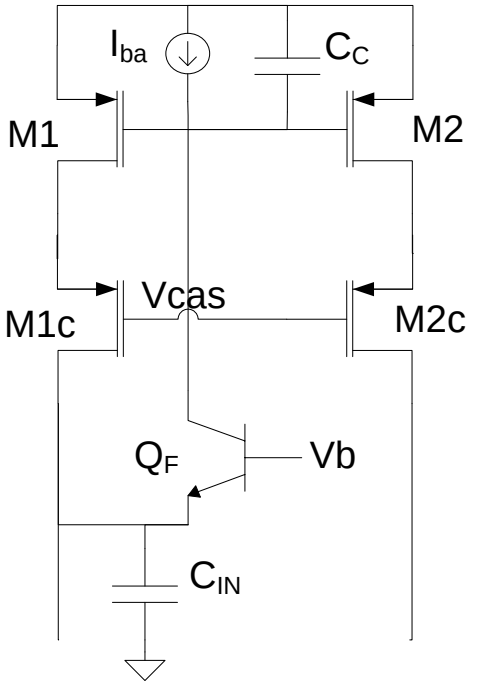
II. Circuit design: HF LV current mirrors: cascode + CB amplifier

- Cascode with common base (CB) or common gate (CG) amplifier
  - Additional degree of freedom: Vb
    - Vd of M1c can be low for small signals!
      - Vd of M1c not linked to Vg of M1
    - Vcas can be lowered
      - Higher swing for Vgs of M1
      - Higher dynamic range
- Low input impedance
  - Low voltage
  - Good linearity

$$Z_{in} = \frac{1}{g_{mF}\left(Z_{cF} g_{mM1} + 1\right)}$$

- But, feedback system:
  - Compensation !
  - Two main poles:
    - M1 gate
      - Add Cc for dominant pole comp: Limits BW
    - Input node
      - Effect of Cin

Cascode with common base amplifier



$$T_{fb}(s) = \frac{g_{mM1} R_{cF}}{\left(sR_{cF}C_{cF} + 1\right)\left(s\,C_{IN}/g_{mF} + 1\right)}$$

$$C_{cF} = C_C + C_{gsM1} + C_{gsM2} + \ldots$$

II. Circuit design : small signal analysis

Cable included in simulation: mtline model

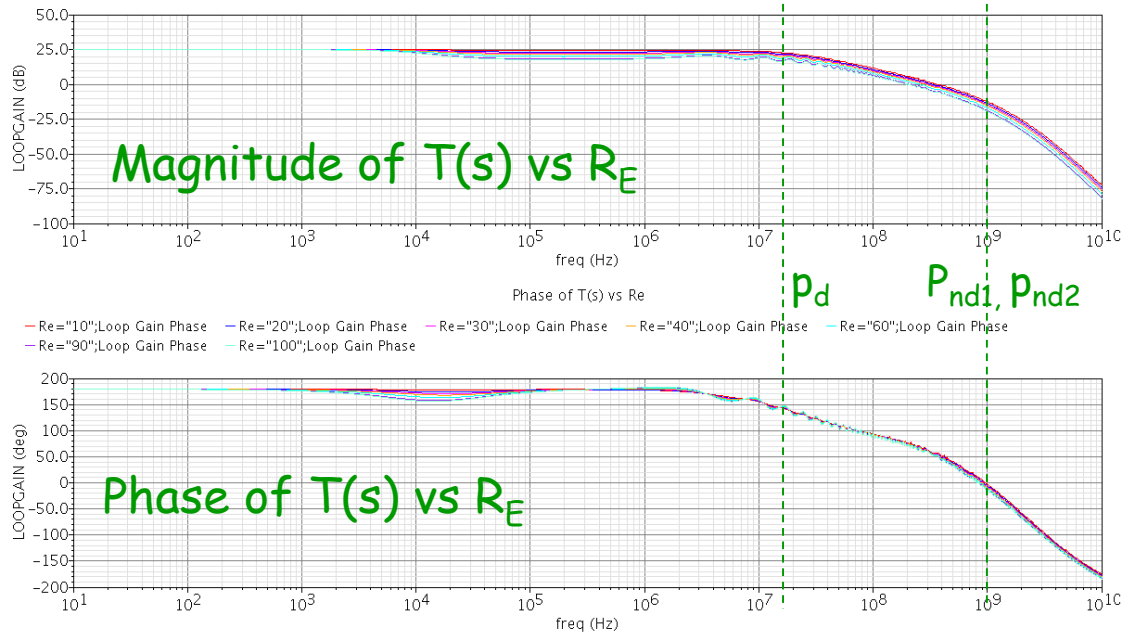
- Return ratio technique to evaluate stability
  - Single breakpoint for 2 loops (C of Q1)

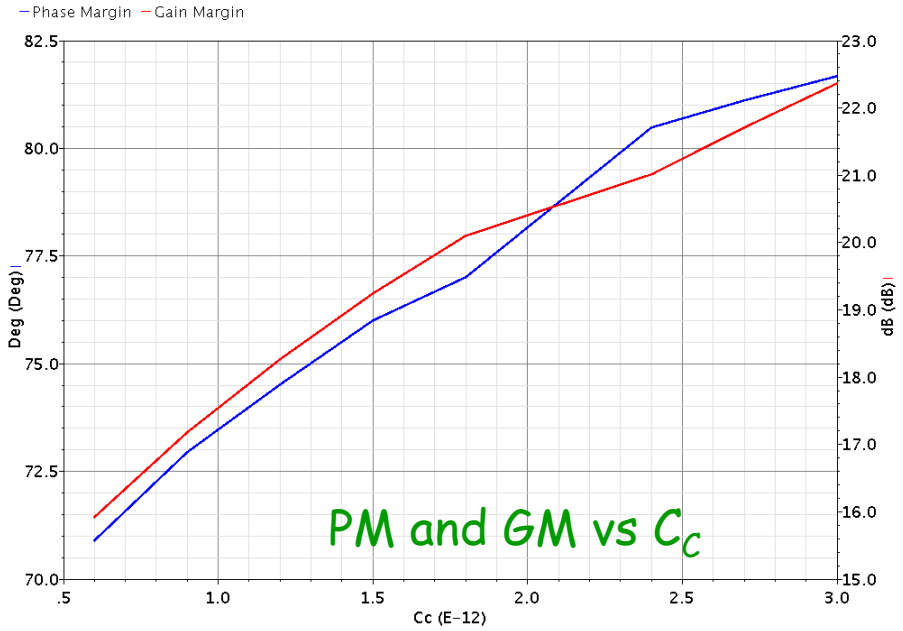
$$T(s) \approx T(0)\frac{(sz+1)}{(sp_d+1)(sp_{nd1}+1)(sp_{nd2}+1)} \qquad T(0) \approx 2K\alpha$$

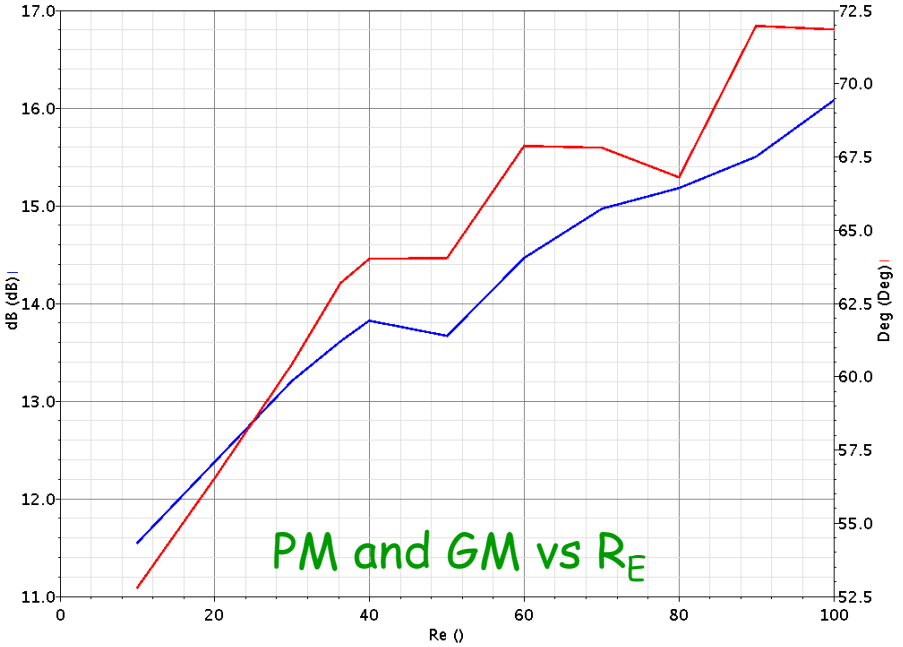
PMOS mirror NMOS mirror $\frac{1}{\alpha Z^0_{i_{OL}} C_{IN}}$

$$\alpha = \frac{\mathrm{Re}(Z_{cable})}{\mathrm{Re}(Z_{cable}) + R_E}$$

- Compensation
  - NMOS mirror BW >> PMOS MIRROR BW
  - Dominant pole comp. (increase C_C, but smaller signal BW)
    - Signal BW is p_d*(K+1)
  - Decreasing loop gain (increase R_E, but higher noise)







II. Circuit design : small signal analysis

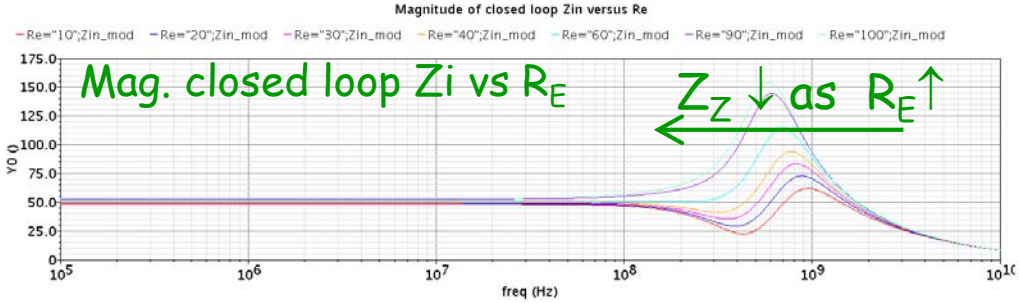
* G. Battistoni et alt., NIM A424, 1999

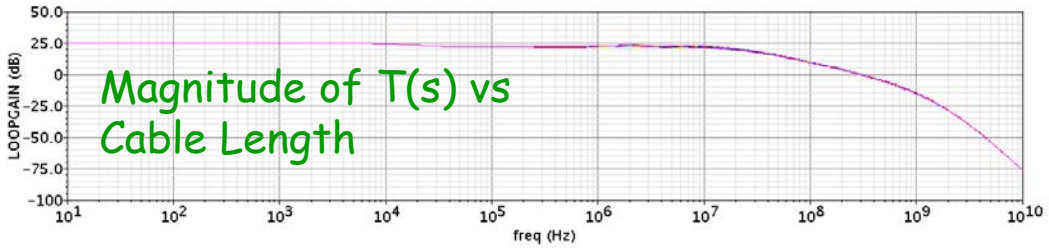
- Input impedance (Blackman`s formula)

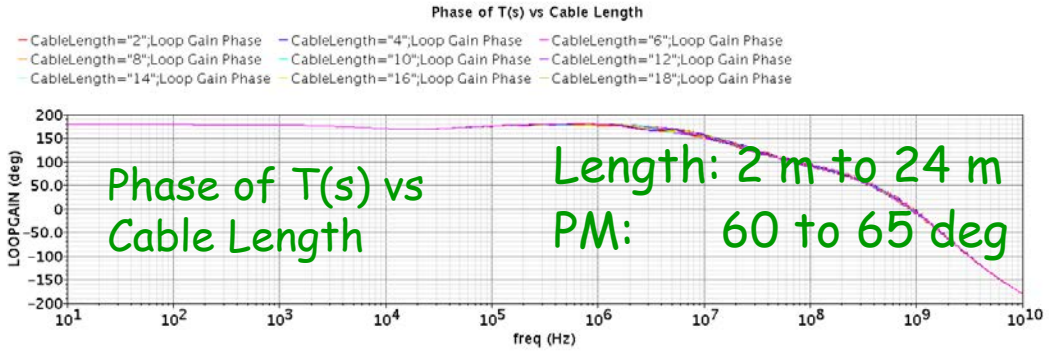
$$Z_{i_{CL}}(s) \approx Z^0_{i_{CL}} \frac{p_d\left(1+{KmR_R}/{Z^0_{i_{OL}}}\right)}{\left(sp_{z1}+1\right)\left(sp_{z2}+1\right)} \qquad Z^0_{i_{CL}} \approx \frac{Z^0_{i_{OL}}}{K+1}+\frac{K}{K+1}mR_R$$

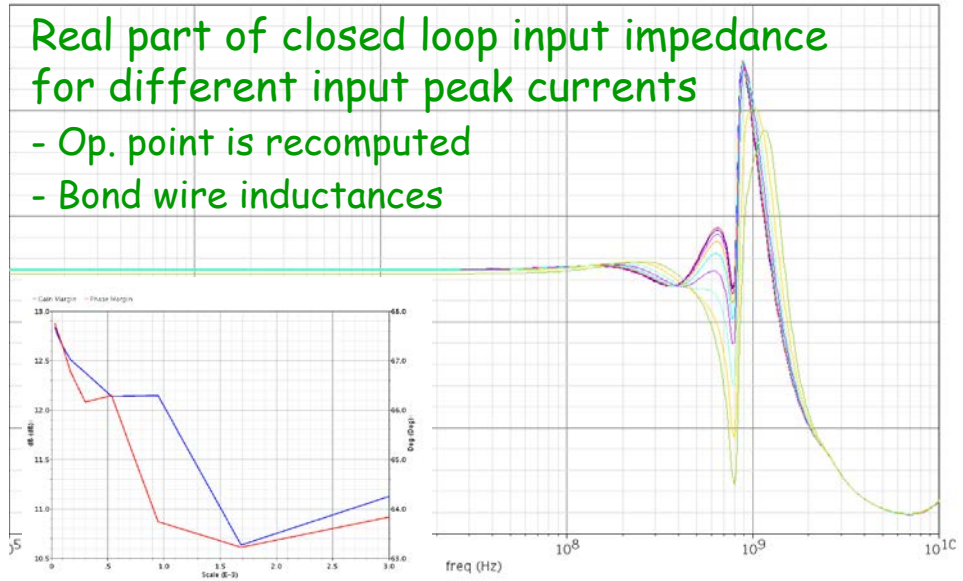
$$p_d K \,//\, p_{nd1} \qquad \frac{p_d K + p_{nd1}}{Z^0_{i_{OL}} C_{pad}}$$

- No inductive effect at p_d
- 2nd look to stability: Re(Zin)>0 (for BW) *
  - Increasing p_{z1}(p_{nd1}>p_d·K)
  - Decreasing z_z by increasing R_E



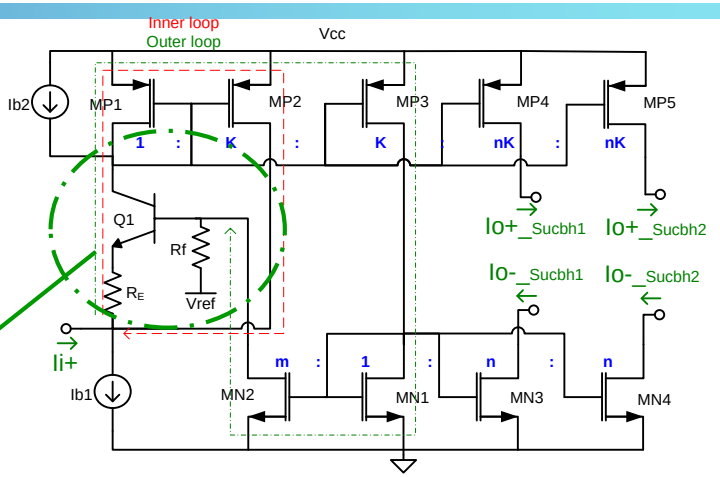




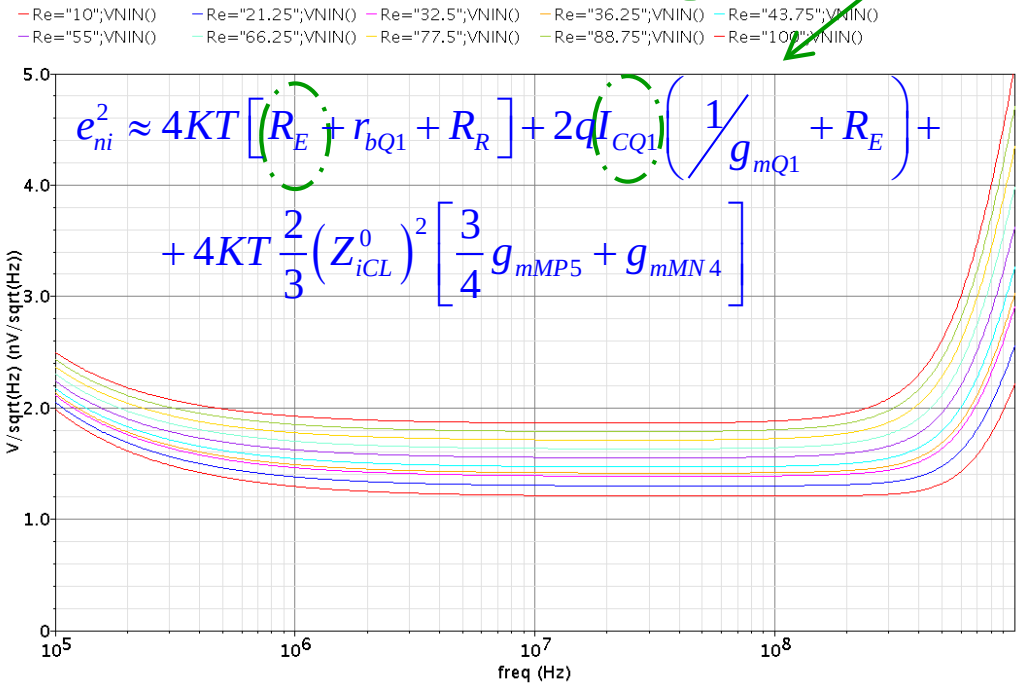


II. Circuit design: noise analysis

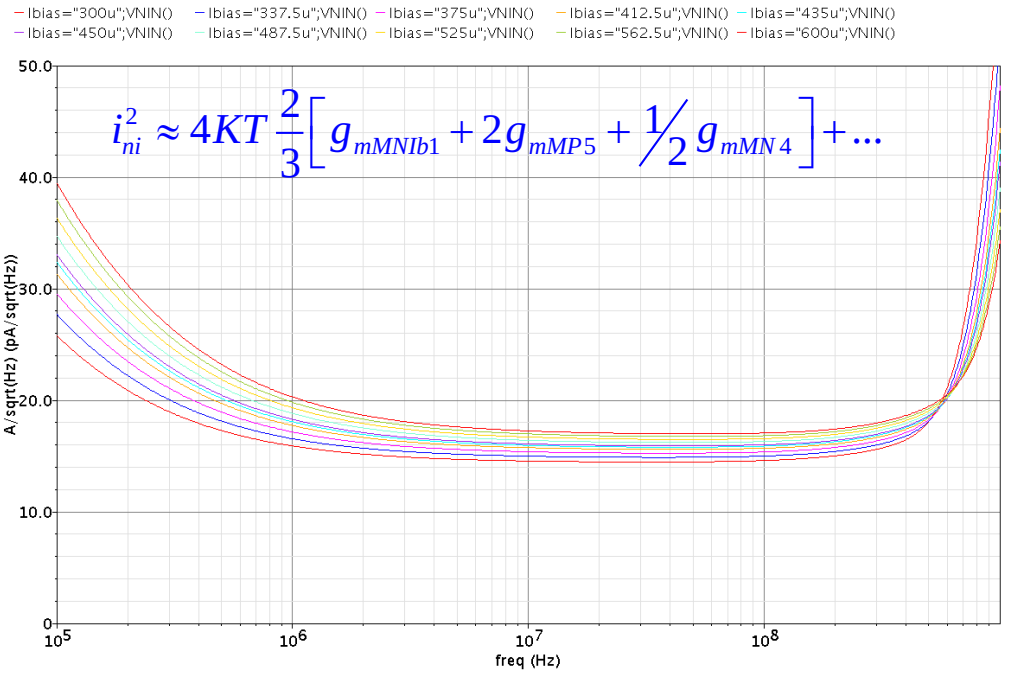
- Series and parallel noise for half circuit
  - Series noise will dominate (low source impedance)
- R_E dominates series noise is in practice
  - Relevant noise sources: R_E and I_{CQ1}
    - Not divided by inner loop gain
  - Trade-off: linearity/stability versus noise
  - Use the largest R_E possible so e_n=1.4 nV/sqrt(Hz)
    - 2 nV/sqrt(Hz) for pseudodifferental config



Series noise PSD vs R_E

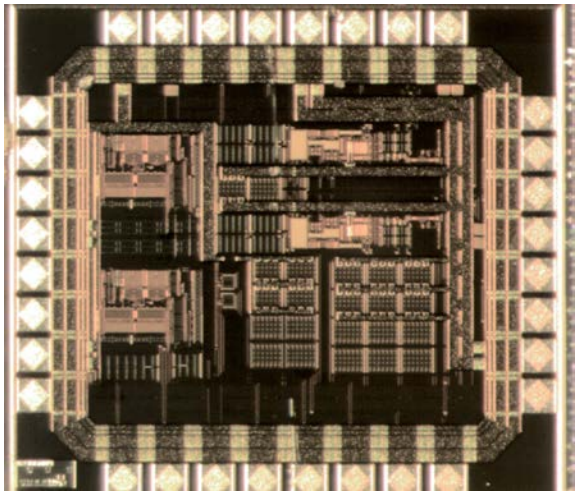


Parallel noise PSD vs I_{b1}

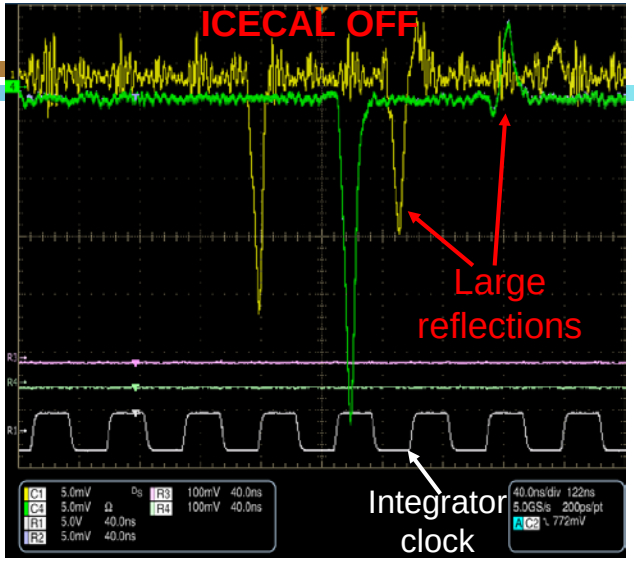


III. ICECAL prototype test results

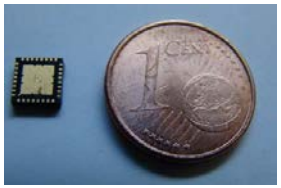
- Two ICECAL prototype submitted:
  - V1 preamp and integrator
  - V2 preamp, integrator and track and hold (1 ch)
    - Received 2 weeks ago

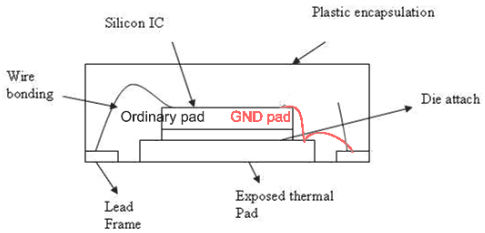


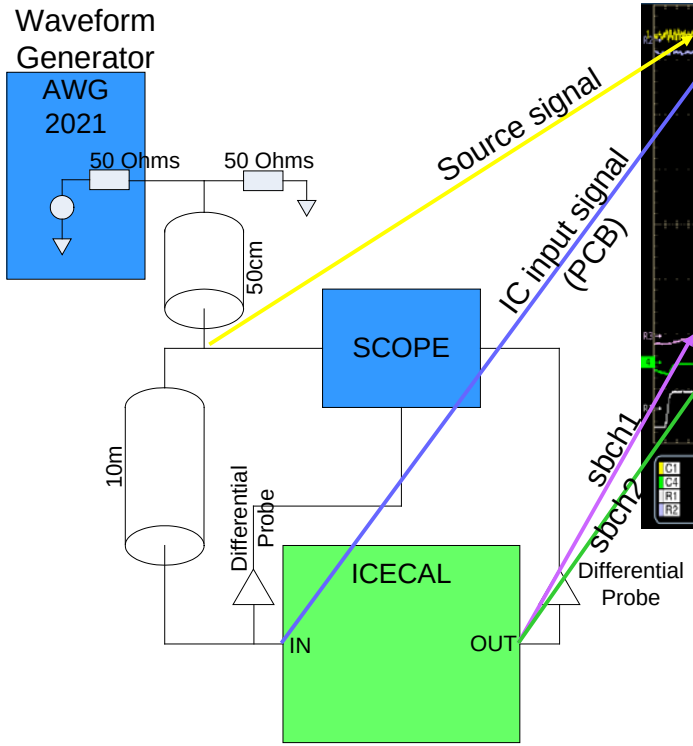
ICECALv1 chip:
SiGe BiCMOS 0.35um
AMS 2 mm²
3.3 V

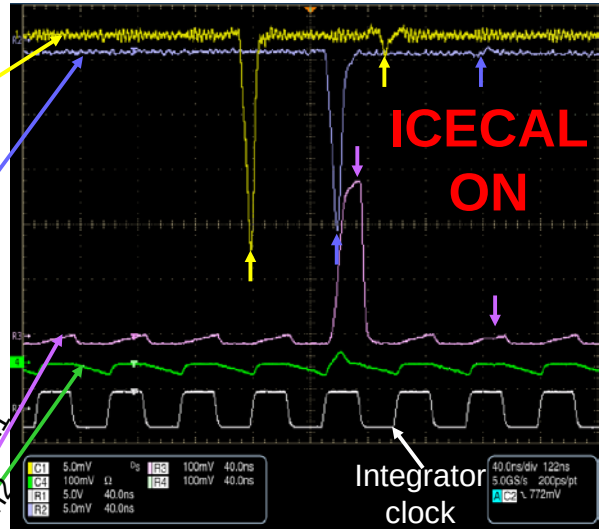


QFN32:
Downbonds









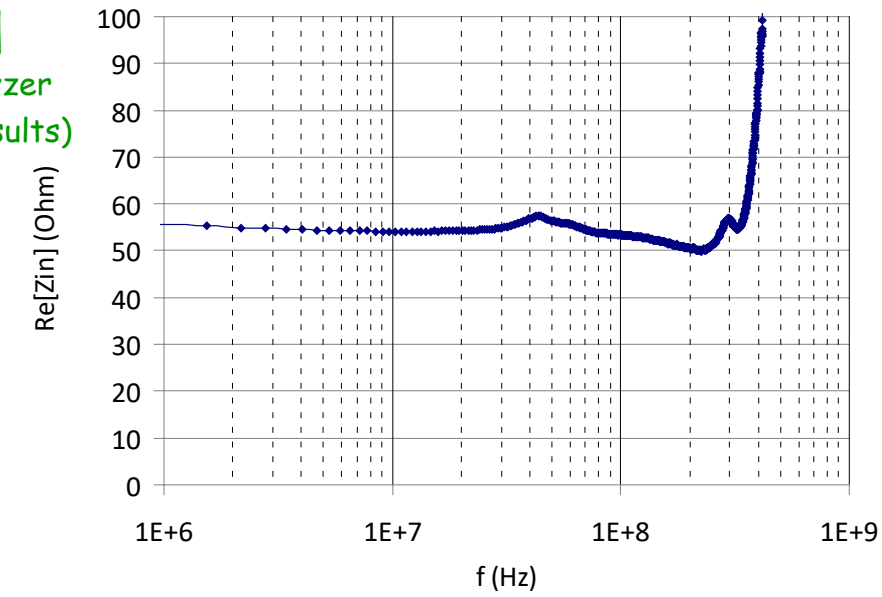
Reflection Coefficients for source, IC input, and output signals:

Refl. Coeff. = 1st pulse integral / 2nd pulse integral

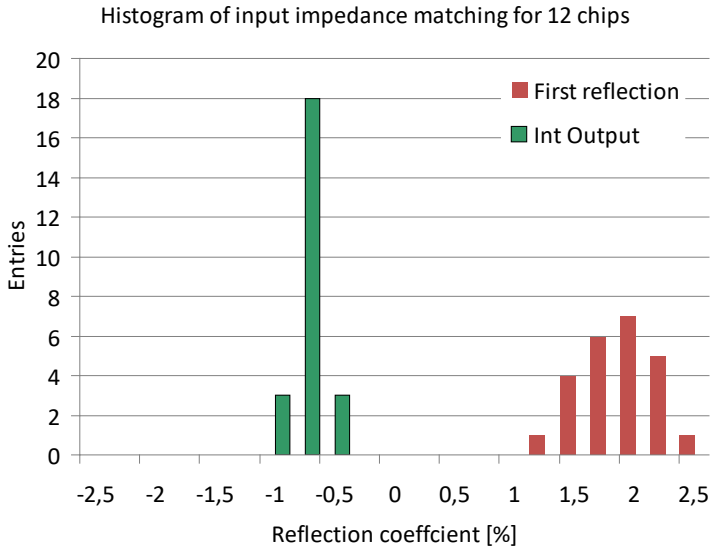
III. ICECAL prototype test results: input impedance

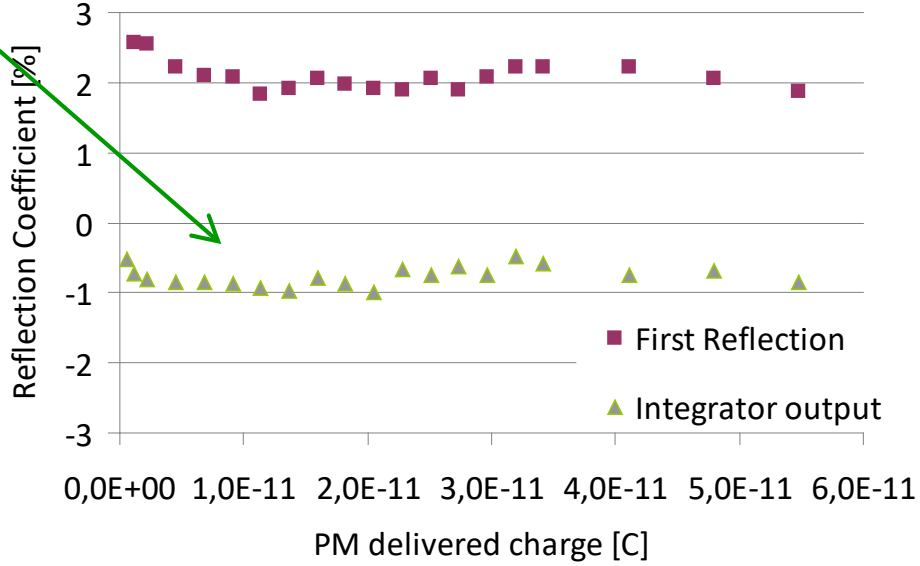
- Reflection coefficient measured:
  - First reflection: measured on input cable
  - Second reflection
    - Source imped. is 25 Ohm)
    - Measure integrator output 50 ns after
- No ringing/oscillation observed
  - Different cable lengths, opens, etc
- Good line termination:
  - Reflection coefficient:
    - 1 -2 % systematic (can be corrected)
    - ***Less 0.5 % variation over full dynamic !***
  - Low dispersion (12 chips measured)

Re[Zin]
Network analyzer
(Preliminary results)



Impedance adaptation



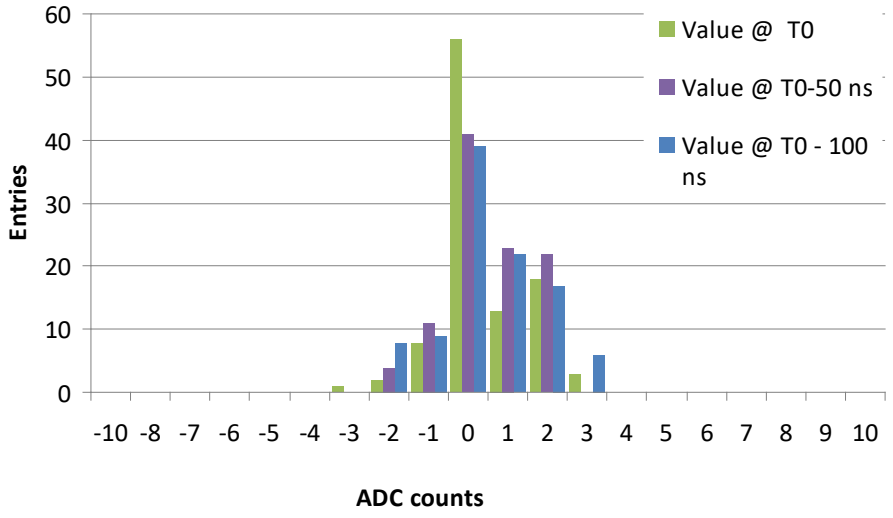


III. ICECAL prototype test results: noise

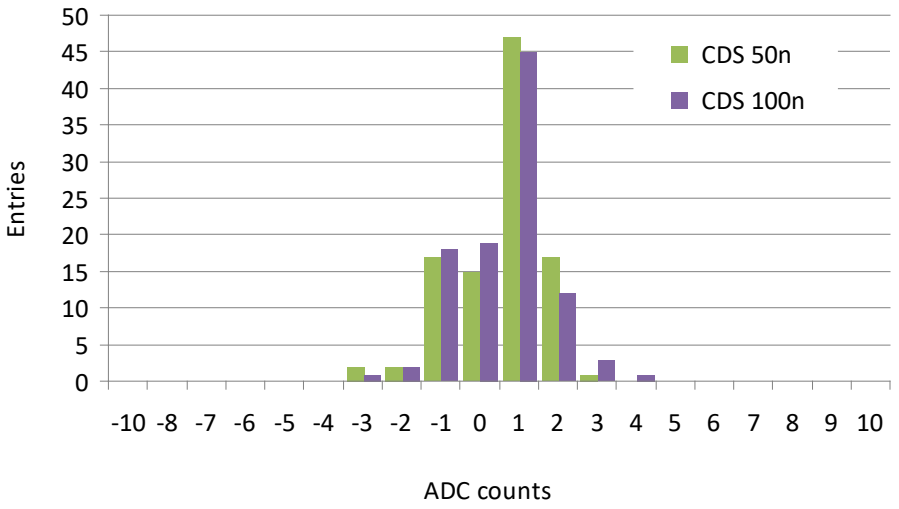
- Noise measured as pedestal rms:
  - For 3 consecutive clock cycles
- Then CDS is applied (50 and 100 ns)
  - Noise is significantly reduced
    - LF noise present (pick up)
    - Tested on pogo pin socket
  - Negligible differences for 50 and 100 ns

Noise [LSB]	Calculation	Simulation	Measurement
P+I	0.62	0.8	1.8
P+I+CDS	0.9	1	1.2
P+I+TH	-	0.8	1.8
P+I+TH+CDS	-	1	1.2

Pedestal for 3 consecutive cycles

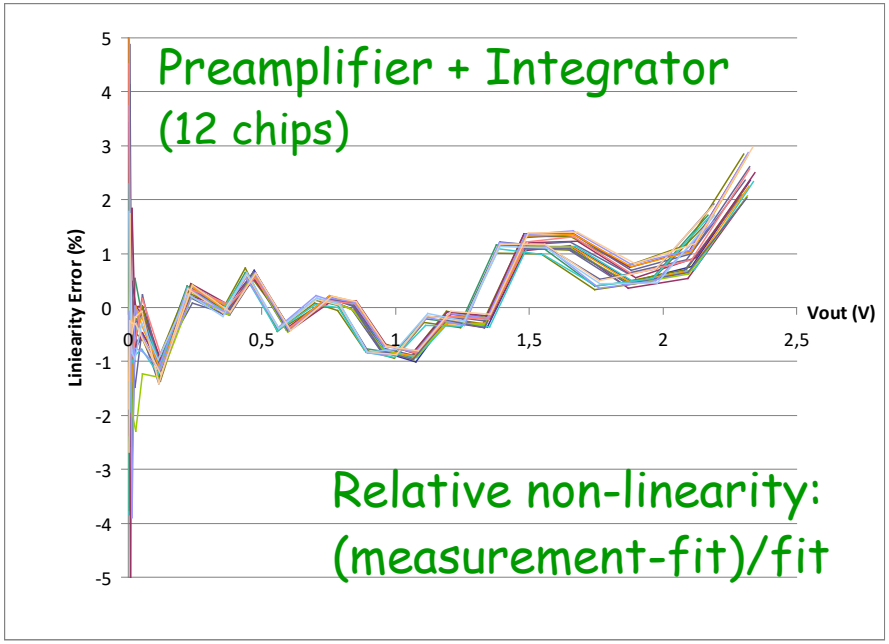


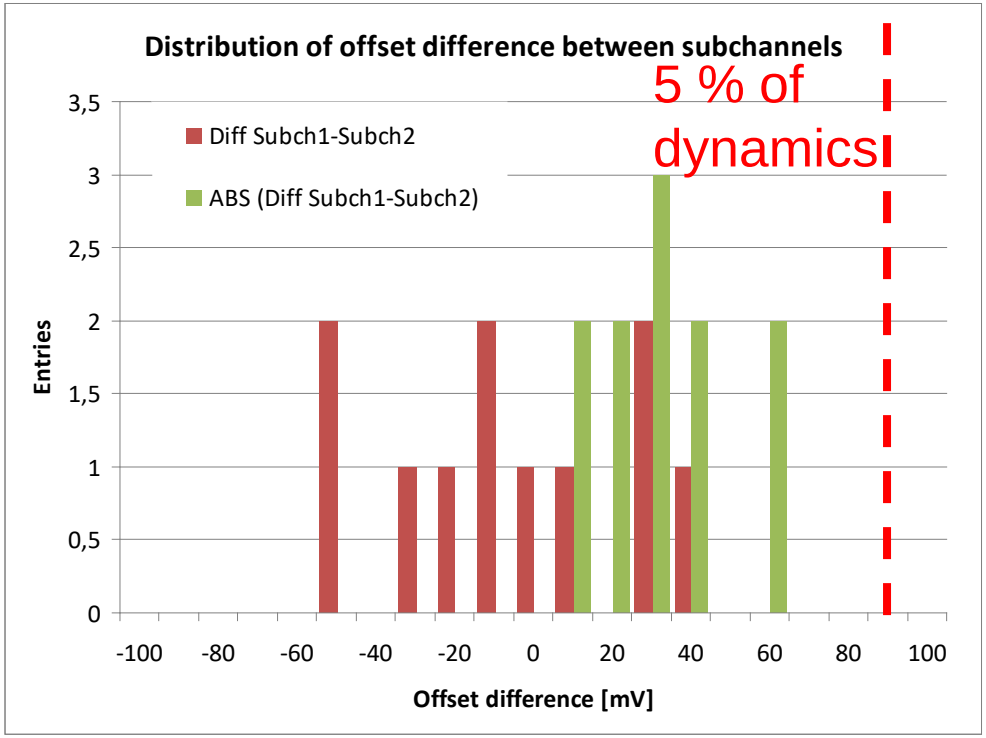
Pedestal applying CDS

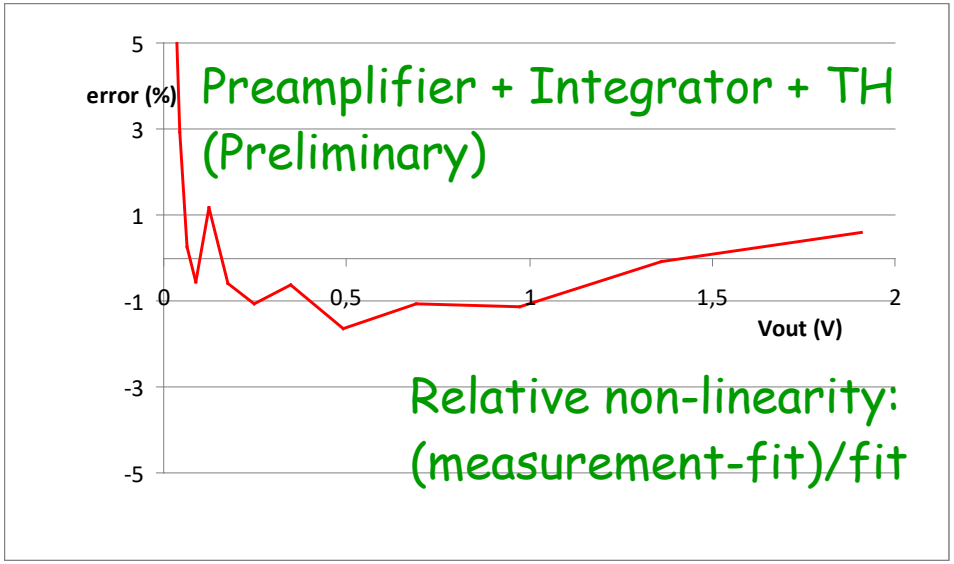


III. ICECAL prototype test results: linearity and offset

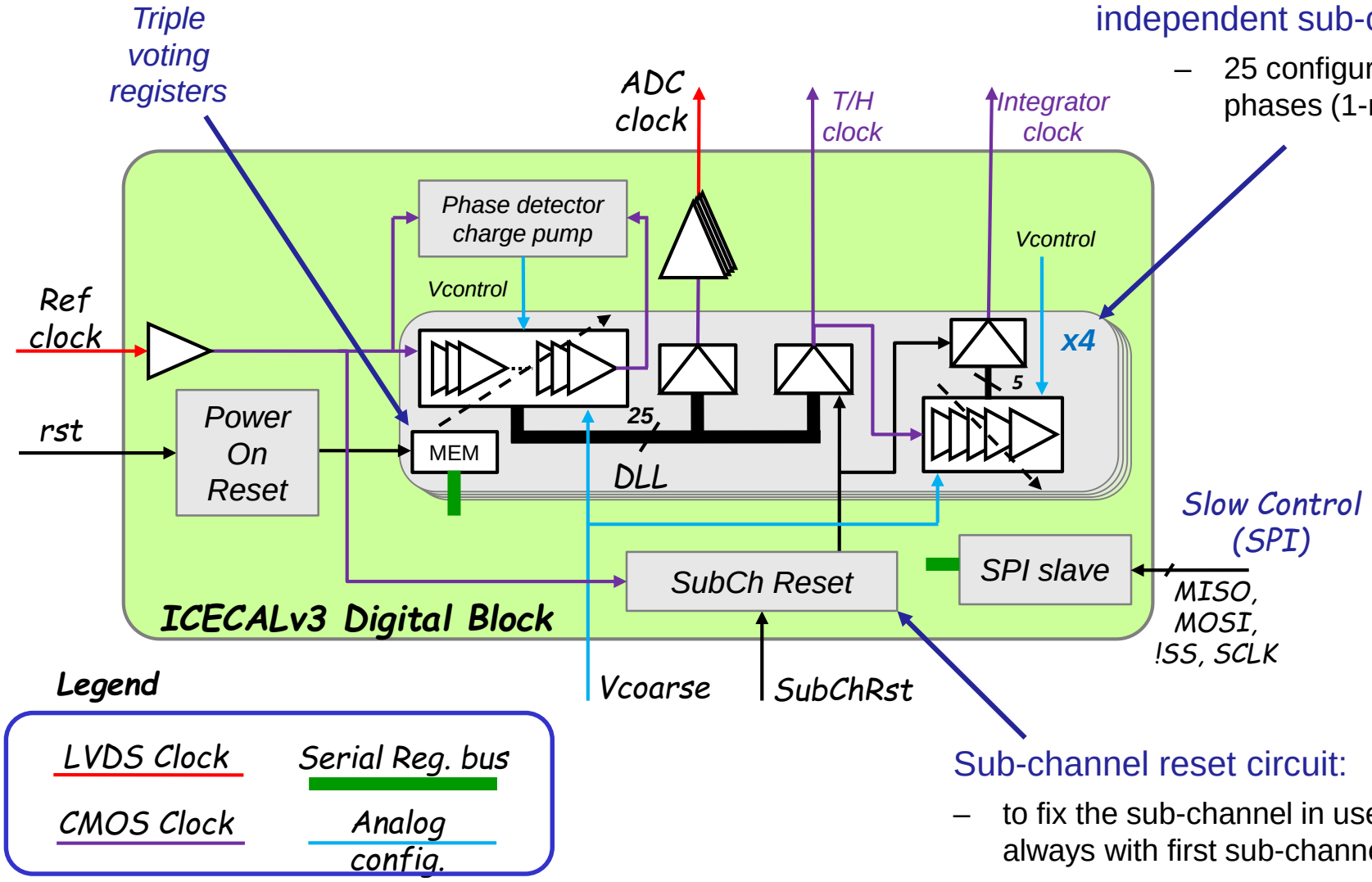
- Relative linearity error:
  - < 1% for full dynamic range
- Offset
  - Good matching
  - Less than 5 % of the dynamic range







ICECALv3 Digital Block overview



4 DLL channels (4x3 = 12 independent sub-channels):

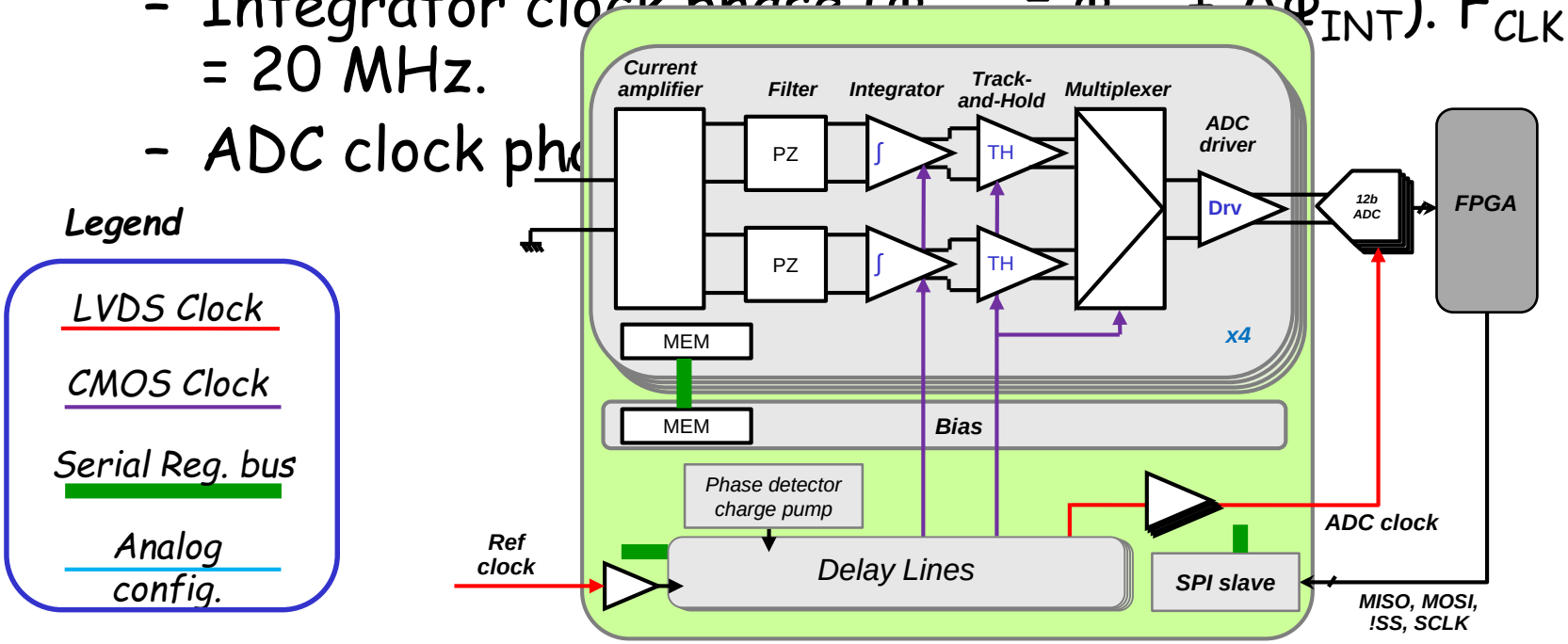
- 25 configurable clock phases (1-ns step).

Sub-channel reset circuit:

- to fix the sub-channel in use (e.g start always with first sub-channel)

ICECALv3 Digital building blocks: delay line

- Clock management is internally done by the ICECAL Chip:
  - Three clock phases are generated from an input reference (REF_CLK):
    - Track & Hold clock phase (Φ_{TH}). F_{CLK} = 20 MHz.
    - Integrator clock phase ($\Phi_{INT} = \Phi_{TH} + \Delta\Phi_{INT}$). F_{CLK} = 20 MHz.
    - ADC clock ph



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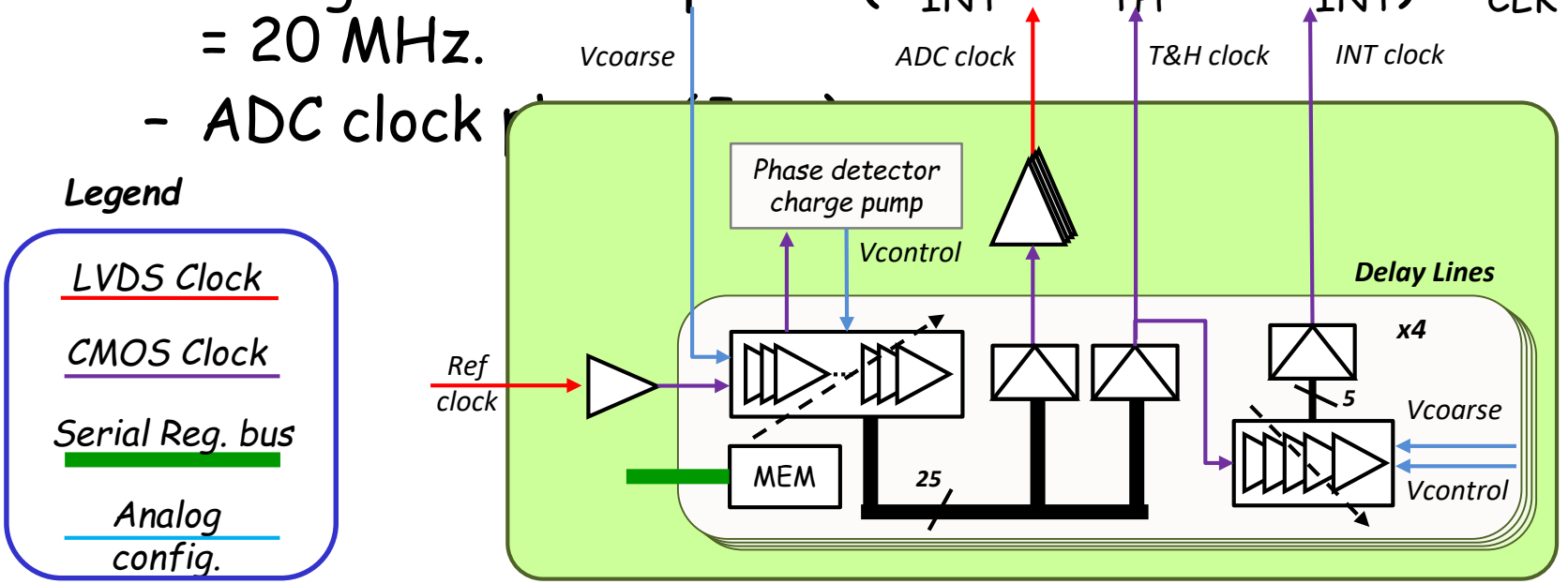
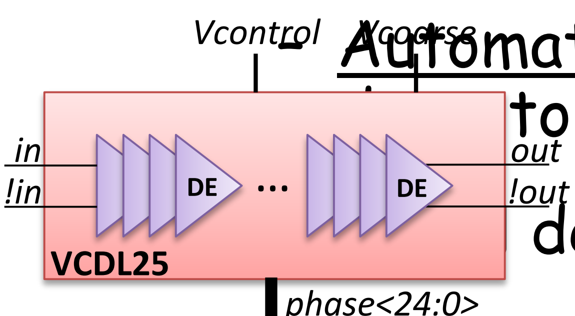
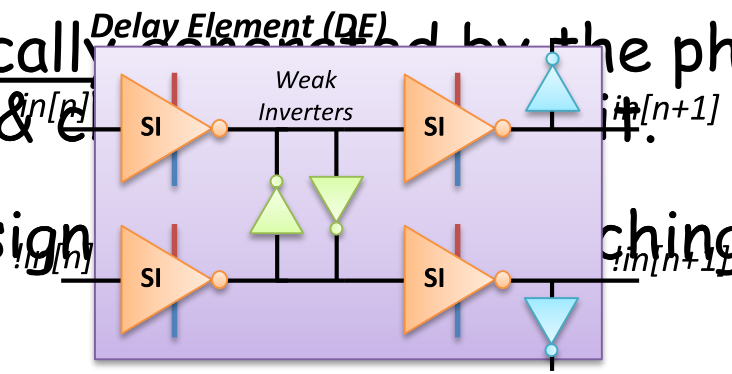
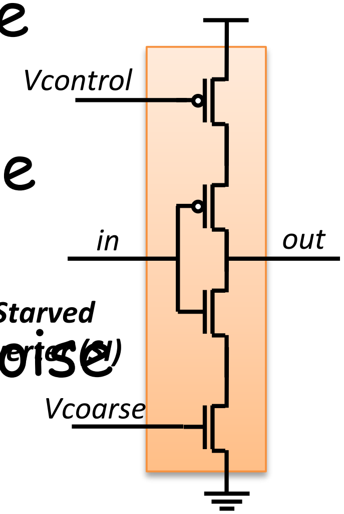


ICECALv3 Digital building blocks: delay line

- Voltage Controlled Delay Line (VCDL):
  - Provides 25 clock phase samples of the LHC clock (1-ns steps).
  - Two control voltages:
    - **Vcoarse**: external. Compensates process variations.
    - **Vcontrol**: internal. Compensates run-time variations.
  - Automatically [illegible] the phase [illegible]tor & e[illegible]it.
  - [illegible] design [illegible]ching noise contribution.

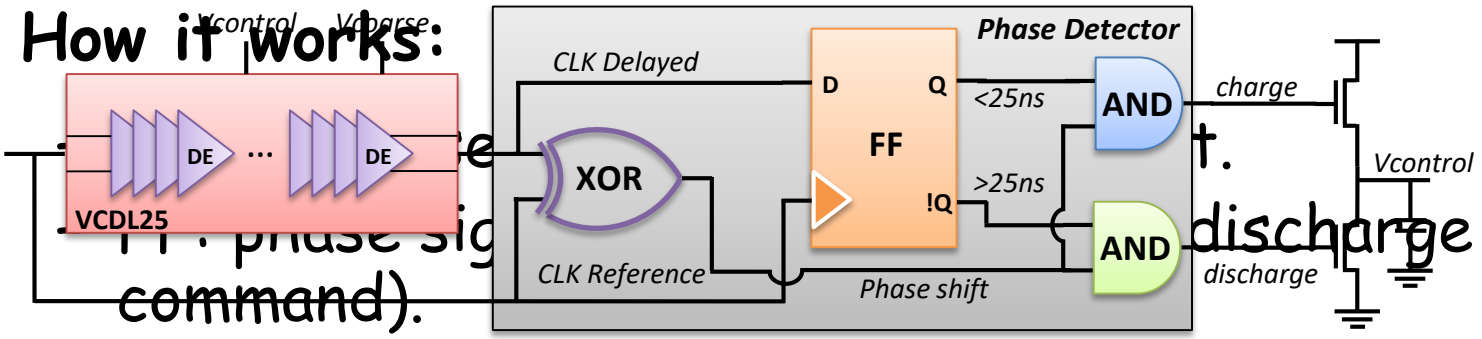






ICECALv3 Digital building blocks: delay line

- Phase Detector & Charge Pump (PD+CP):
  - Converts clock delay variations into a control voltage.
    - Ensures that end-to-end delay is always 25 ns.
  - One PD+CP per chip:
    - No substantial Vcontrol differences between channels (prototype delay chip measurements).
  - How it works:



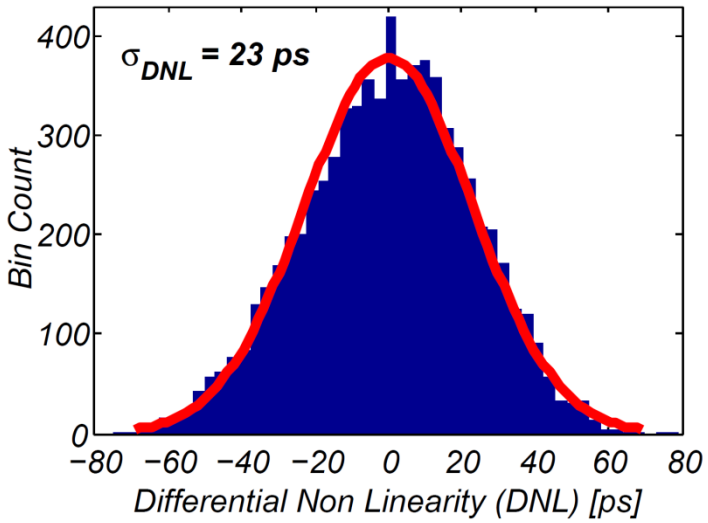
ICECALv3 Digital building blocks: delay line

- Measurements from a standalone prototype (25 chips tested).

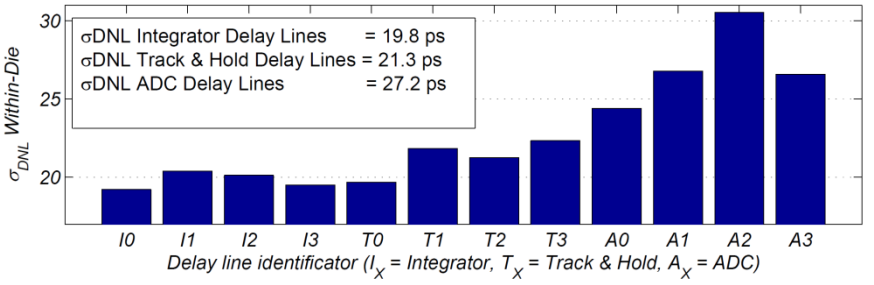
- Linearity:
  - $DNL_i = Delay_i - Delay_{i-1} - 1\ ns$
  - Target: $\sigma_{DNL} < 100\ ps$.
  - Measured $\sigma_{DNL} = 23\ ps$.

- Noise & Jitter:
  - Vcontrol Noise: $\sigma_{Vcontrol} = 6.64\ mV$.
  - Output clock Jitter: $\sigma_{Jitter} \leq 5\ ps$.

Delay Element DNL:

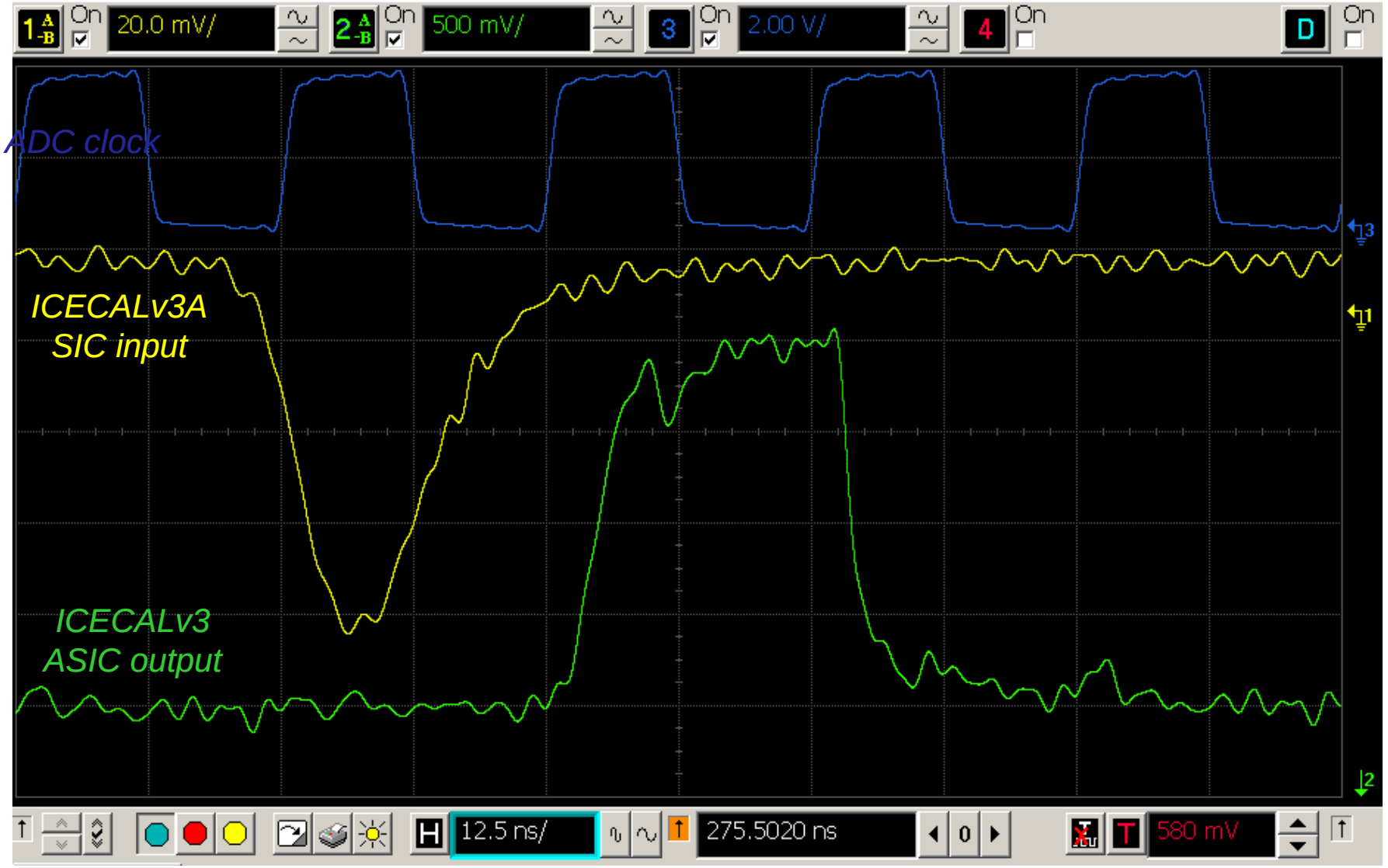


Within-Die variations measurements:



Radiation hard programmable delay line for LHCb calorimeter upgrade
J. Mauricio et al. 2014 JINST 9 C01016

Measurements: analog I/O example

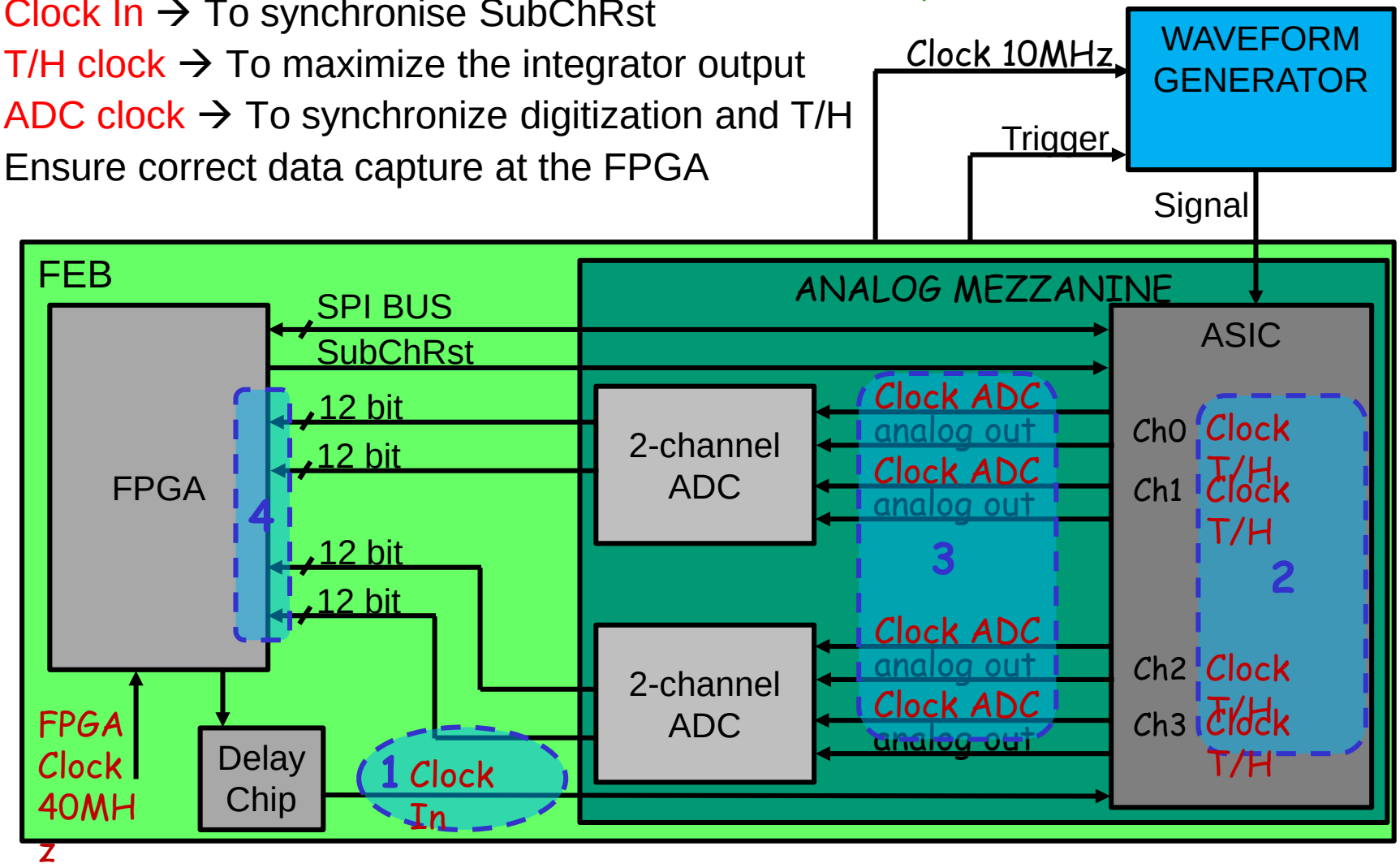


ICECALv3 time alignment

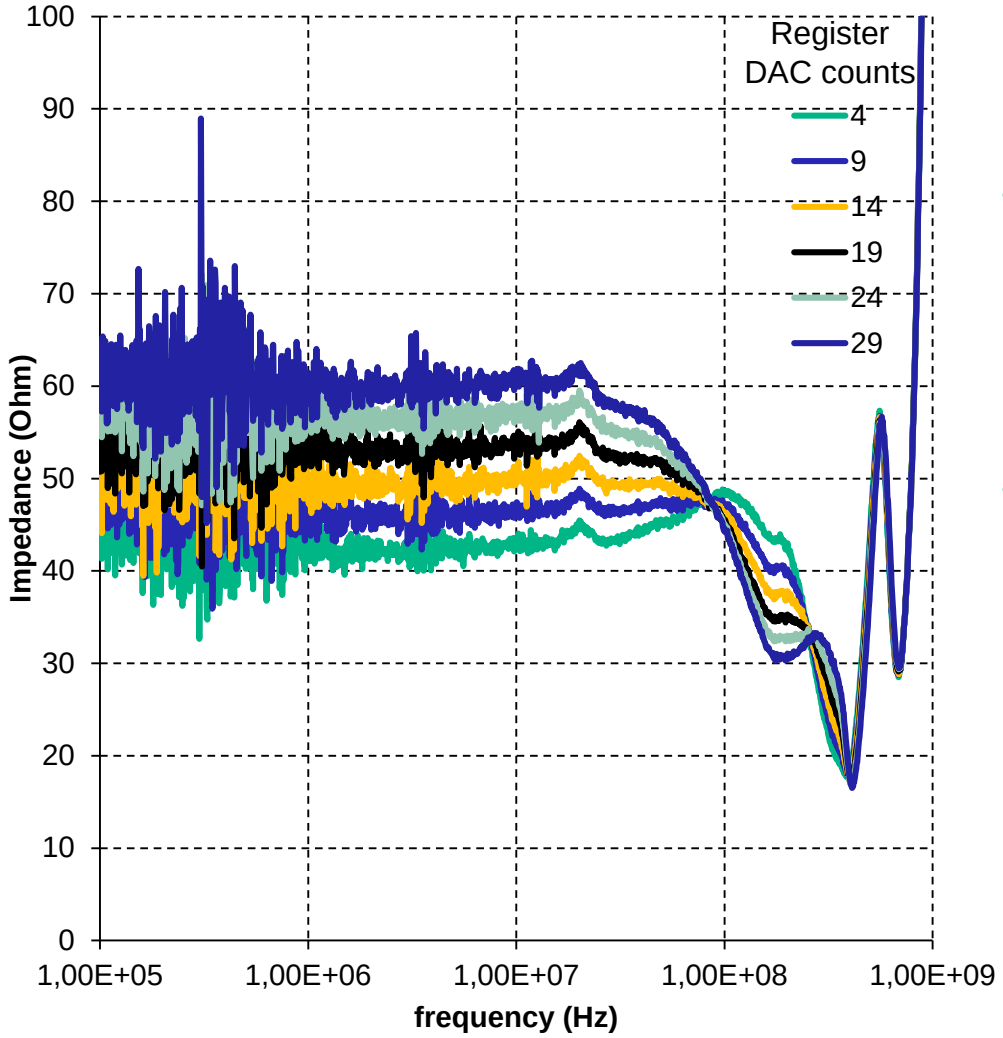
Clock phases to be adjusted:

1) Clock In → To synchronise SubChRst
2) T/H clock → To maximize the integrator output
3) ADC clock → To synchronize digitization and T/H
4) Ensure correct data capture at the FPGA

(Synchronization in prototype is equivalent to the final detector)



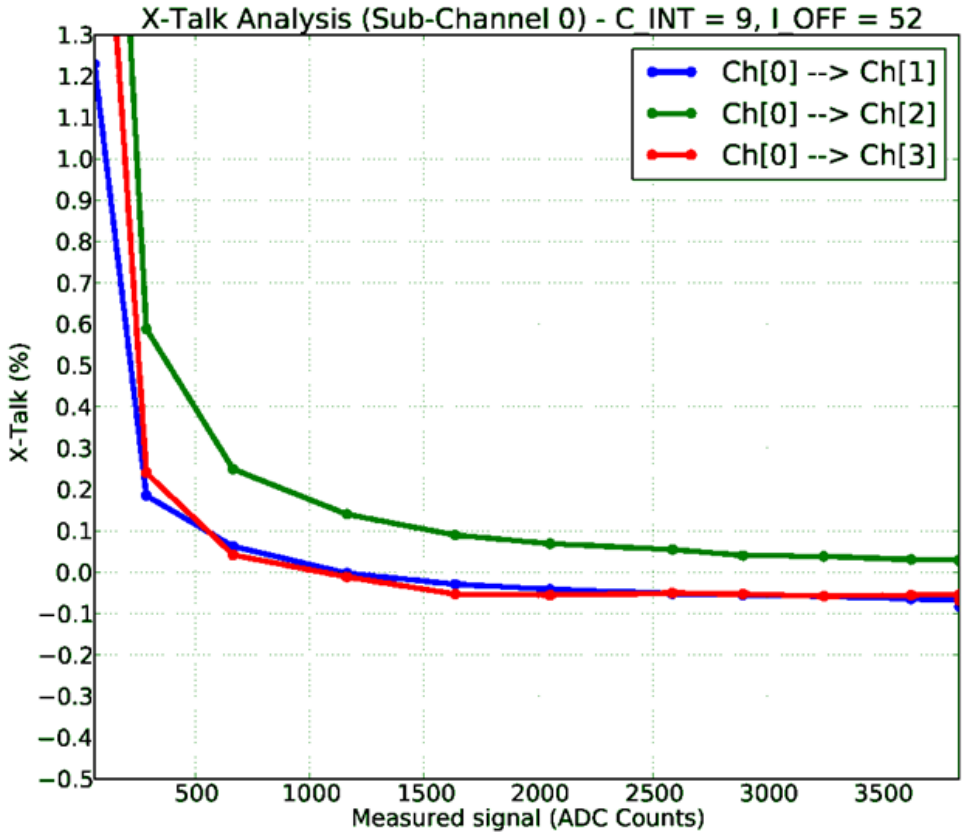
Input Impedance



- Measurement setup
  - Network analyzer at the input (Rohde&Schwarz ZVL)
  - Approximate results due to not-optimal connectivity
- Plot:
  - Input impedance for different configurations
  - Range: ~40 to 60 Ω
  - 50Ω corresponds to 14 DAC counts

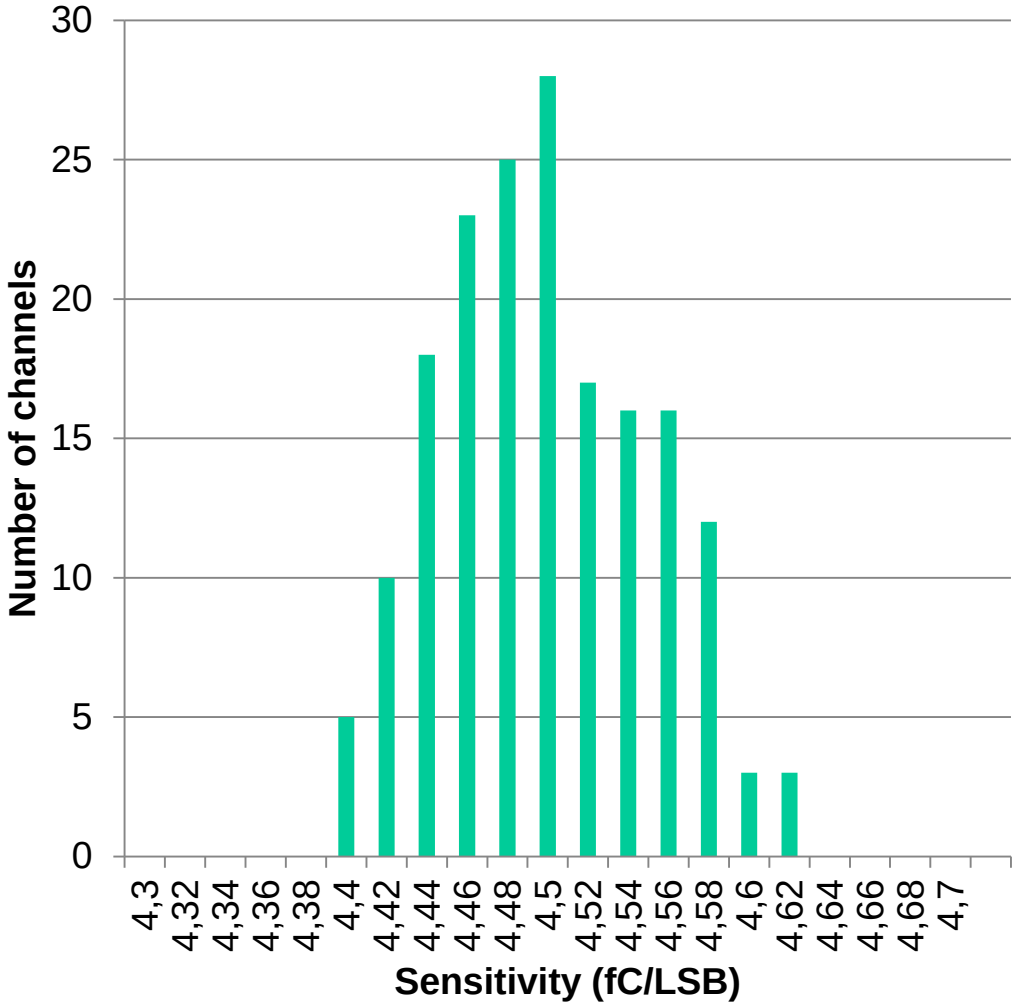
Crosstalk

Measurement example

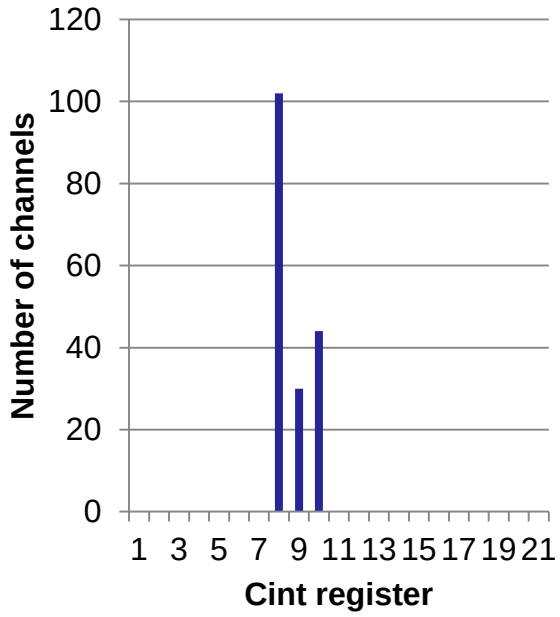


- Crosstalk between channels < 0.5%
- Relative error for low output values is much higher than the crosstalk value

Sensitivity

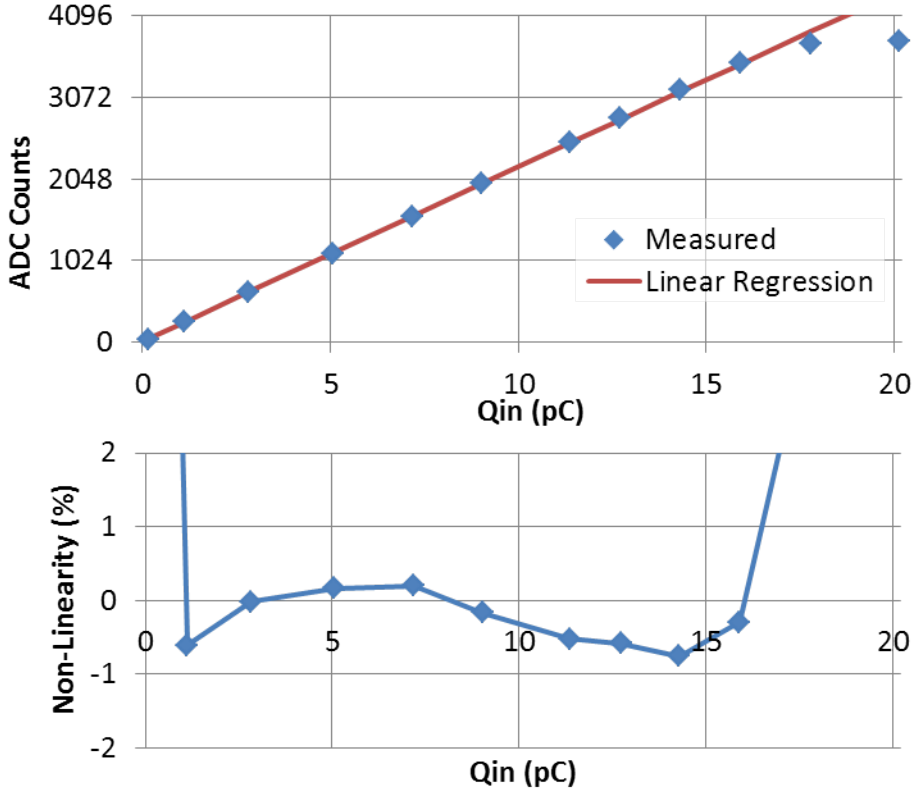


- Sensitivity histogram:
  - Both subchannels for all first 3 channels for 30 chips
  - Specification: 4.5 fC/LSB
  - Sensitivity = 4.488 ⌖ 0.051 fC/LSB



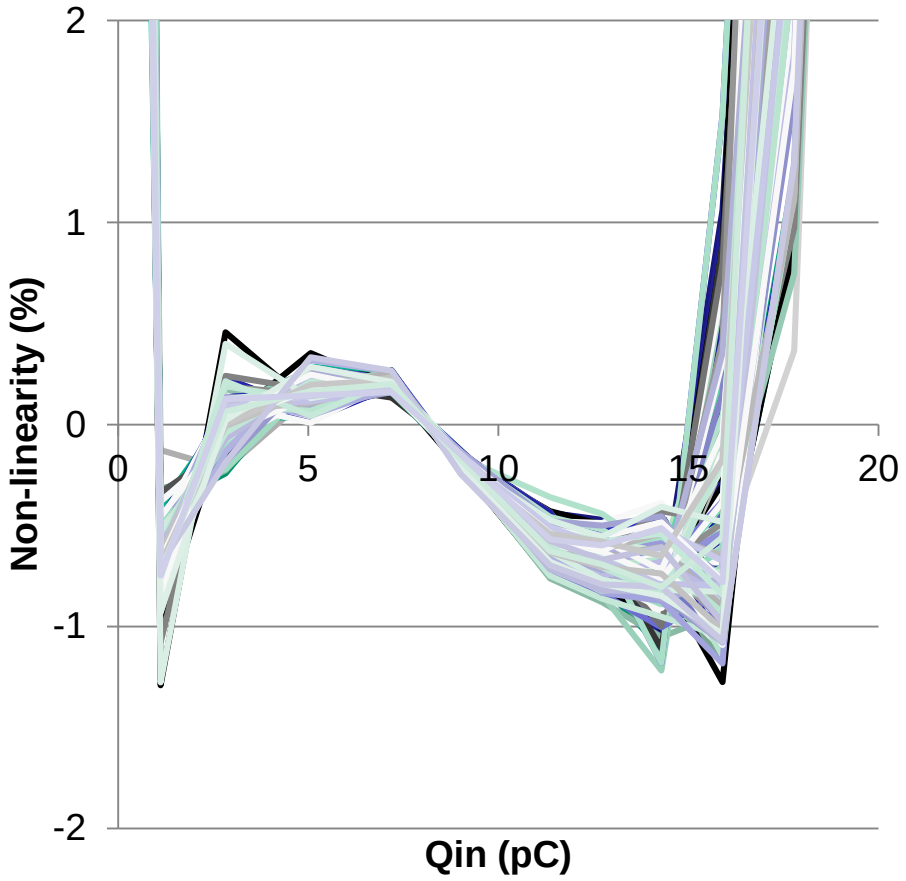
Linearity

Measurement example

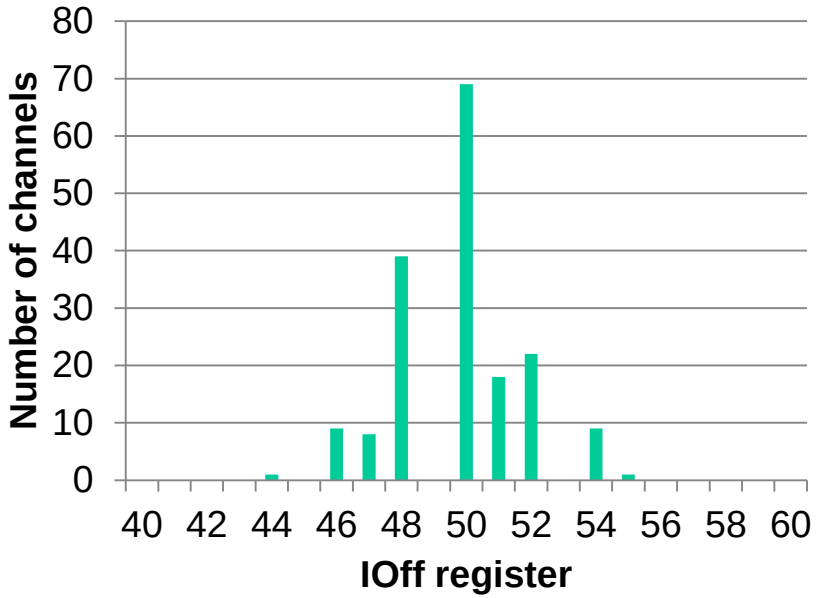


$$NL = 100\frac{V_{expected} - V_{meas}}{V_{expected}}$$

Linearity



- Linearity OK up to ~16 pC for all channels
- High relative error for output low values
- Offset current value adjusted as the minimum offset with correct linearity



Spill over

- Spec: less than 1% for all previous and next clock cycles
- Need to adjust the PZ filter for final configuration of all the chips

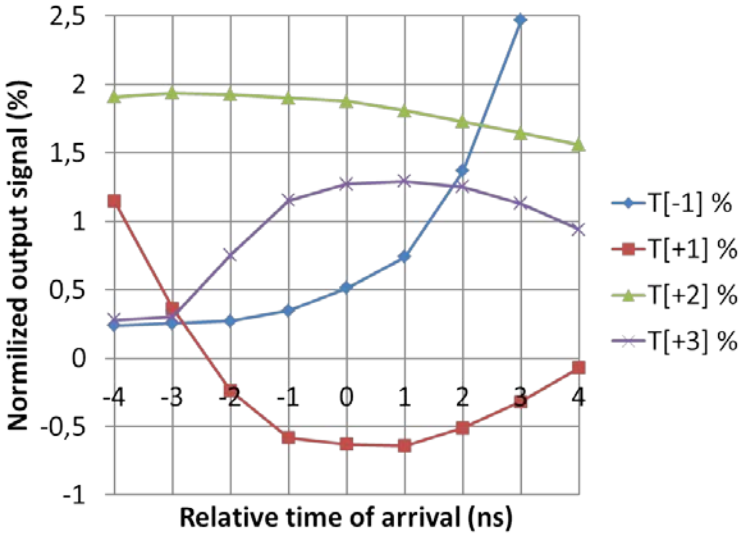
Spill over:

T-1 = 0.50 ⊕ 0.15 %

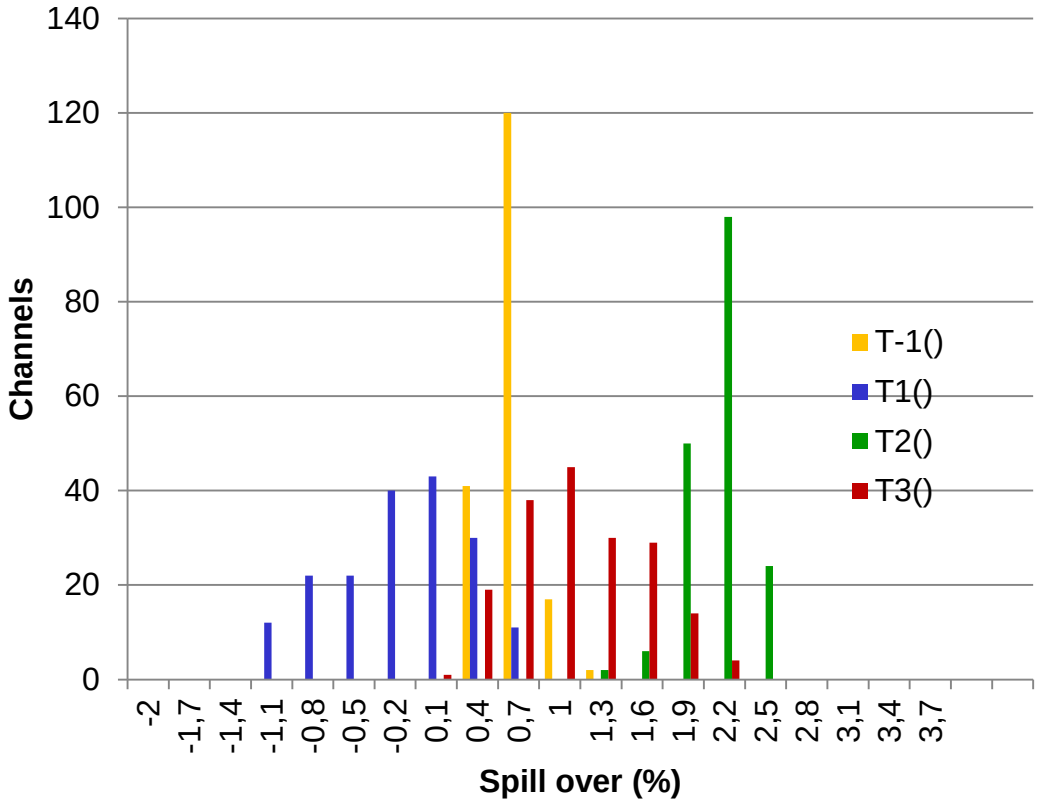
T1 = -0.30 ⊕ 0.47 %

T2 = 1.97 ⊕ 0.19 % ← To be compensated in the digital domain?

T3 = 0.96 ⊕ 0.45 %

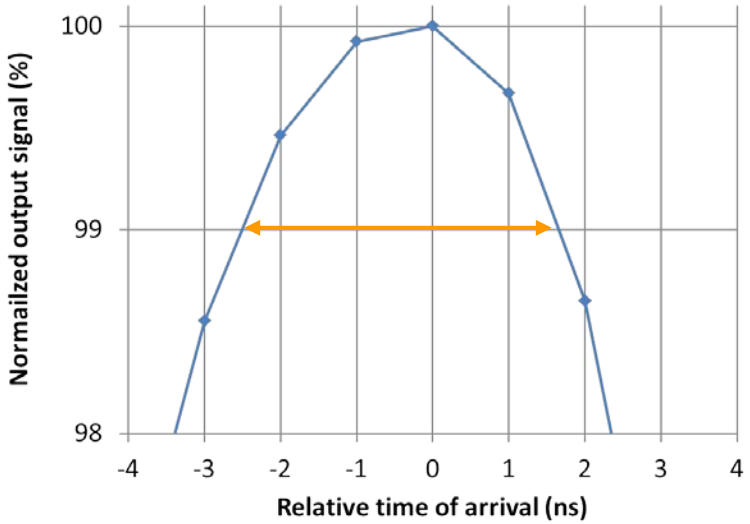


Measurement example

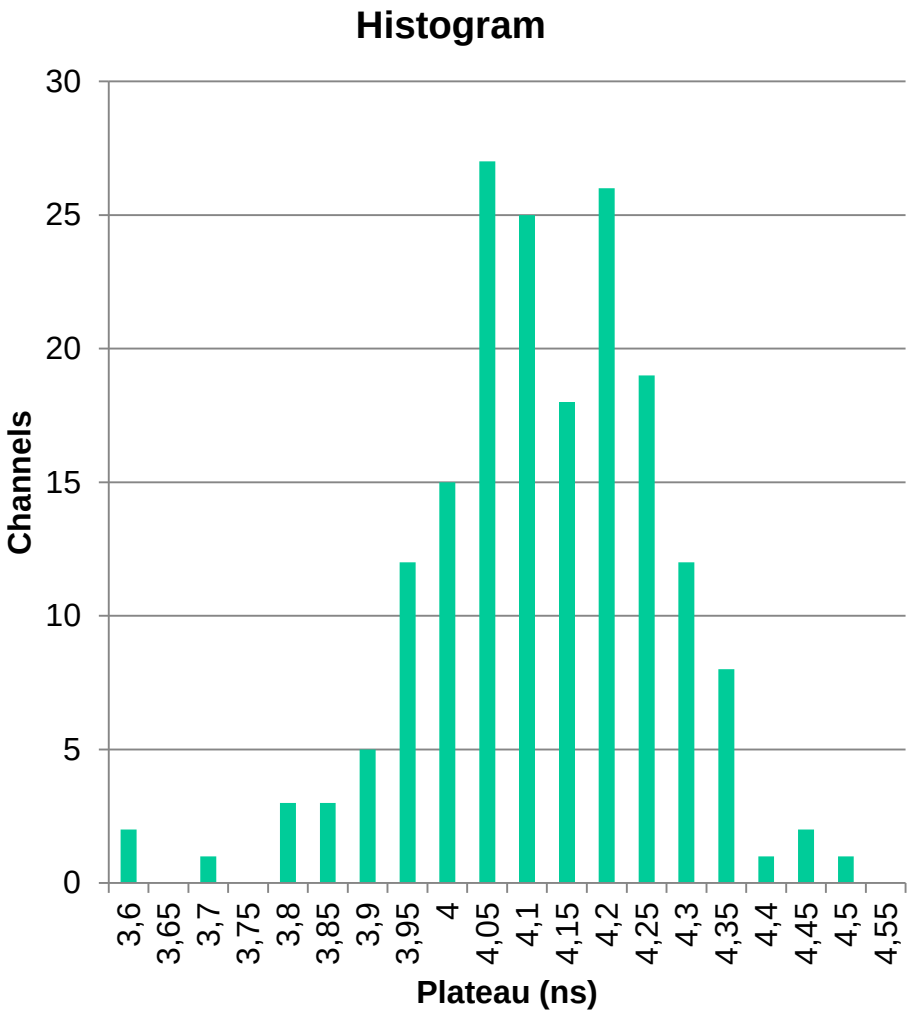


Plateau

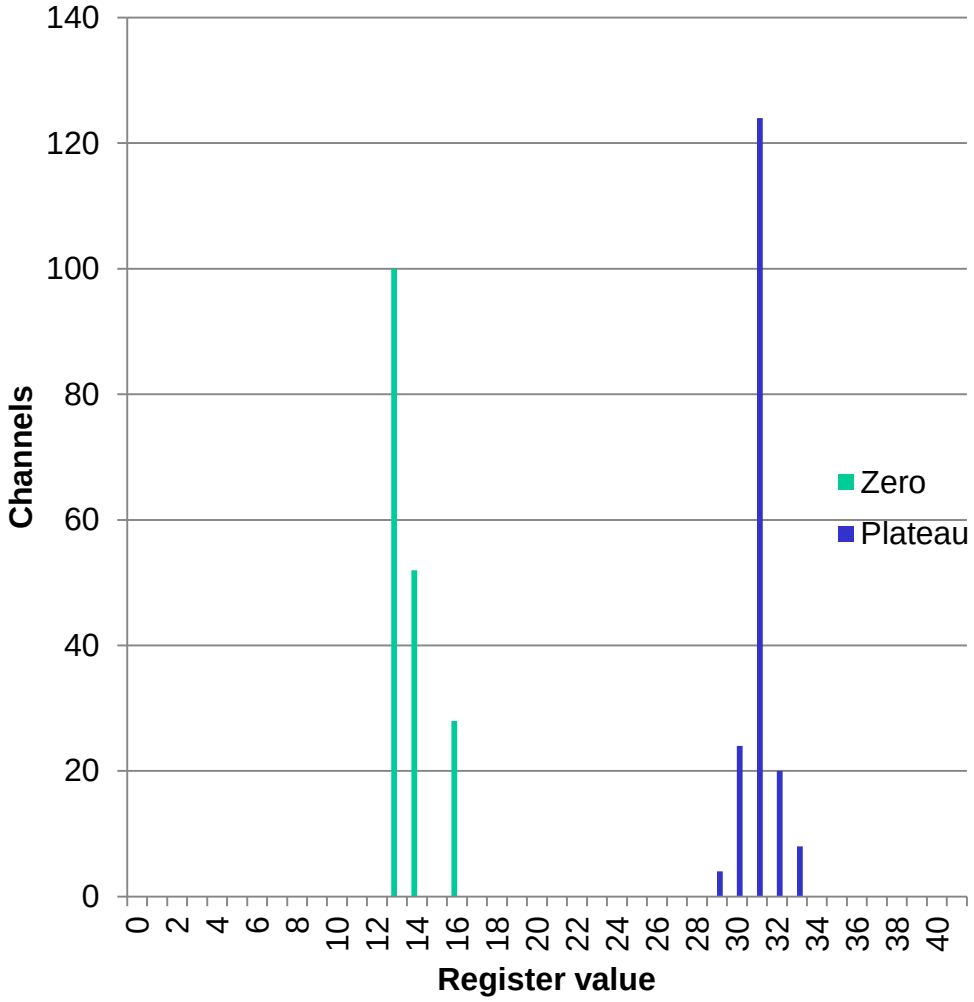
- Spec: less than 1% variation in ⌖2ns
- PZ filter default configuration is enough
- Both subchannels for all first 3 channels for 30 chips
- Plateau = 4.09 ⌖ 0.16 ns



Measurement example



Results: pole zero



- Spill-Over and plateau are a trade-off:

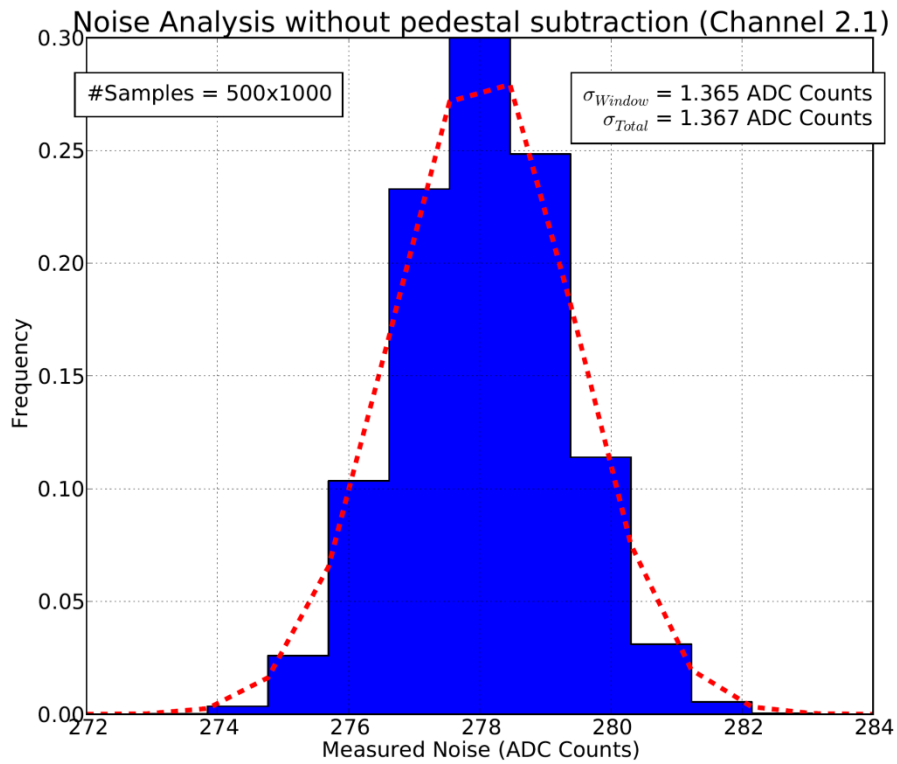
Better spill over ↔ worse plateau

- Pole and zero are adjusted to minimize the spill over standard deviation

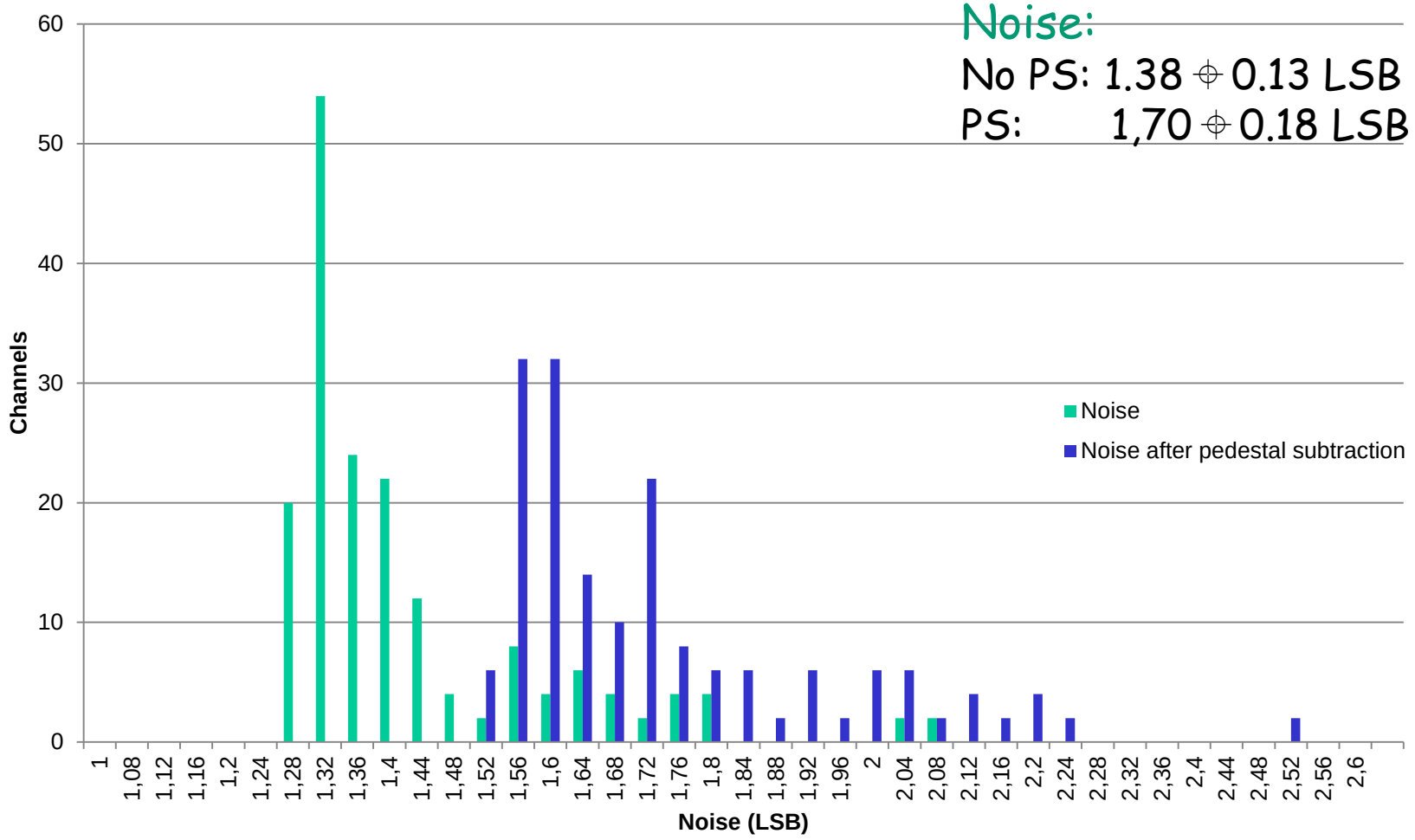
Noise

- Spec: ~1 ADC count
- Measured noise without cable at the input:
  - 1.4 ADC counts
  - 1.7 ADC counts with pedestal subtraction
- If the gain or offset configuration varies, the noise will be affected.

Measurement example



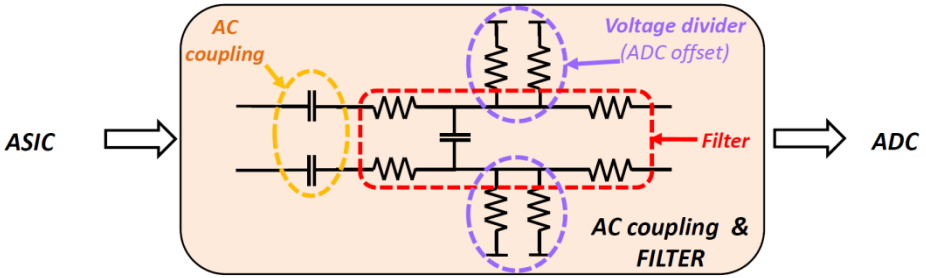
Noise


Noise:
No PS: 1.38 ⌖ 0.13 LSB
PS: 1,70 ⌖ 0.18 LSB
Channels
Noise (LSB)
Noise
Noise after pedestal subtraction
0
10
20
30
40
50
60
1
1,08
1,12
1,16
1,2
1,24
1,28
1,32
1,36
1,4
1,44
1,48
1,52
1,56
1,6
1,64
1,68
1,72
1,76
1,8
1,84
1,88
1,92
1,96
2
2,04
2,08
2,12
2,16
2,2
2,24
2,28
2,32
2,36
2,4
2,44
2,48
2,52
2,56
2,6

TH error and ADC input

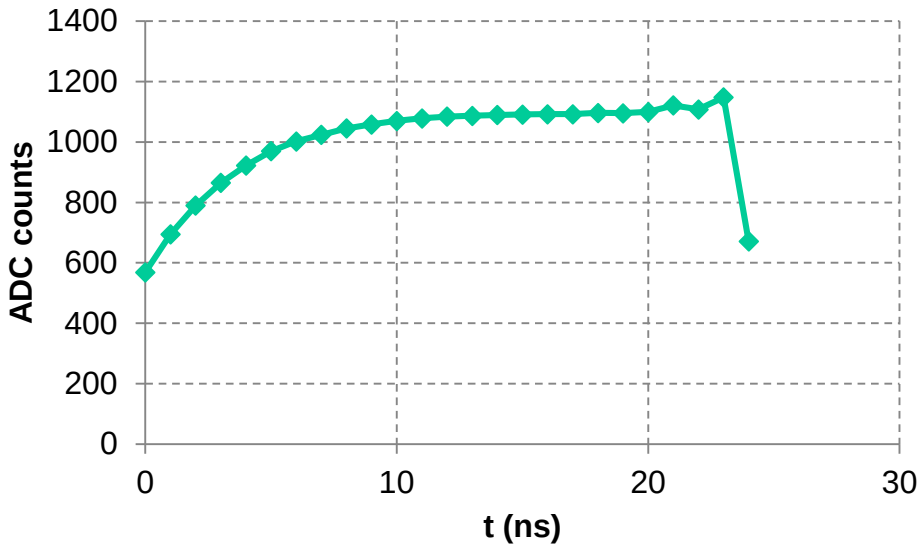
Output impedance of the channel vs. ADC input capacitance

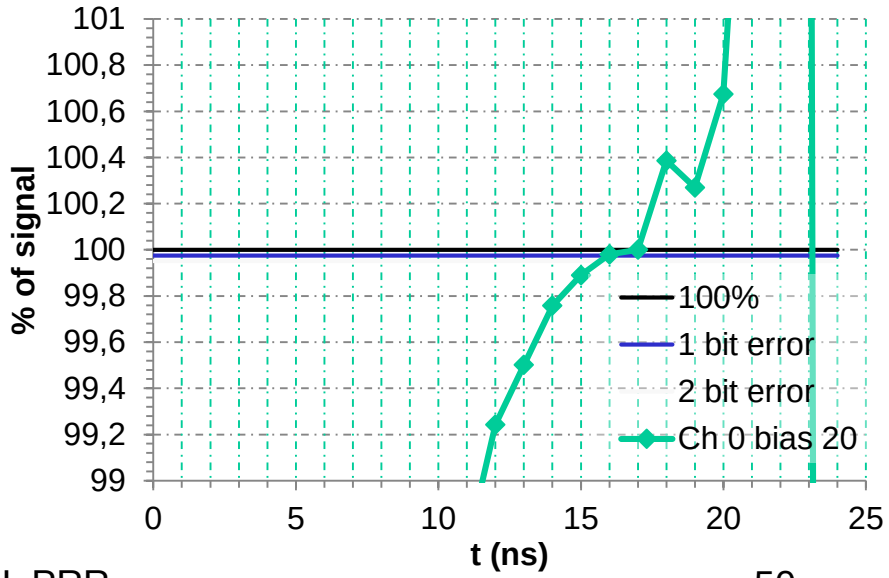
- Simple RC model
- Condition: to settle within 1 LSB of the final value
- Maximum error: 1 bit (12 bits full scale) → 0,024% → 8,3 time constants (RC)
- Known C=10pF → R_{out} = 300Ω
- Simulations show R_{out} = 290 to 450Ω (depending on bias current)



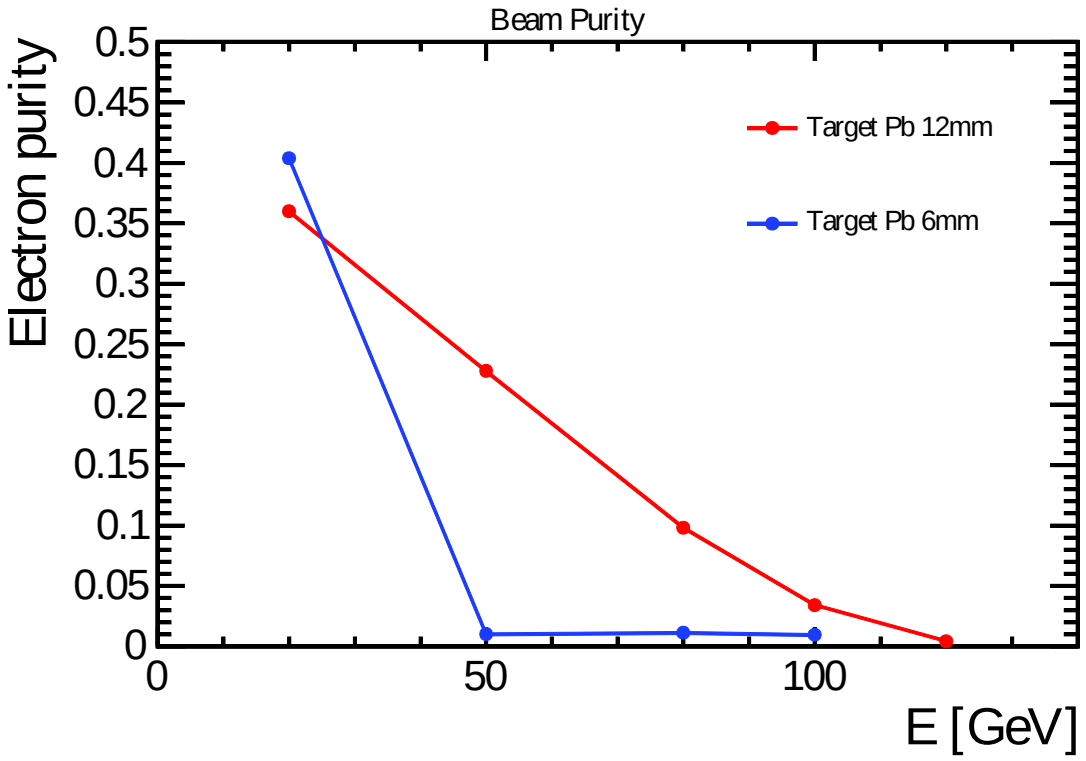
Measurements:

- Trade-off between noise filter capacitor and output precision.





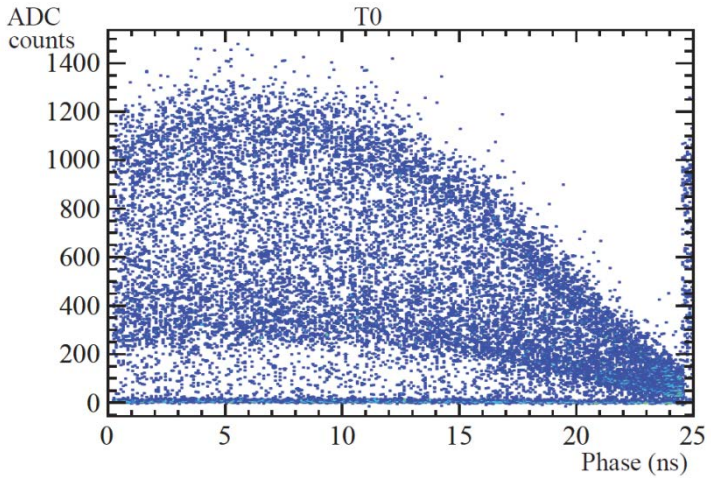
Purity of the electron beam



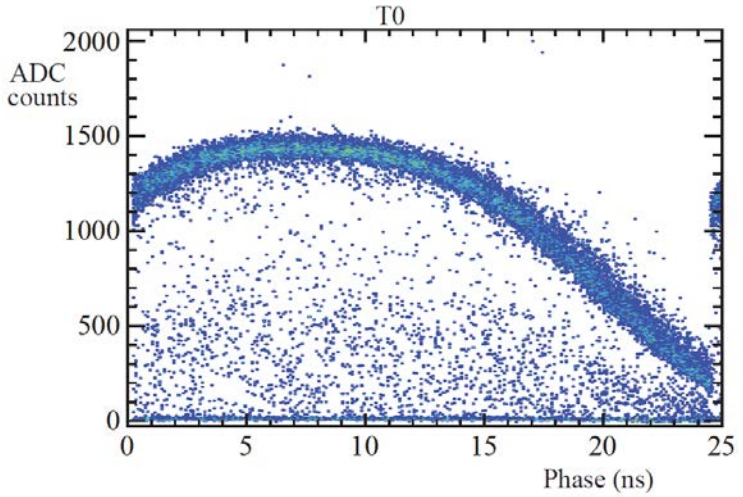
- Targets used:
  - Pb 6mm (initial configuration)
  - Pb 12mm (final configuration)
- Electron purity improved after changing target
- Low electron purity affected measurements
  - Difficult to analize for higher E

Electron purity

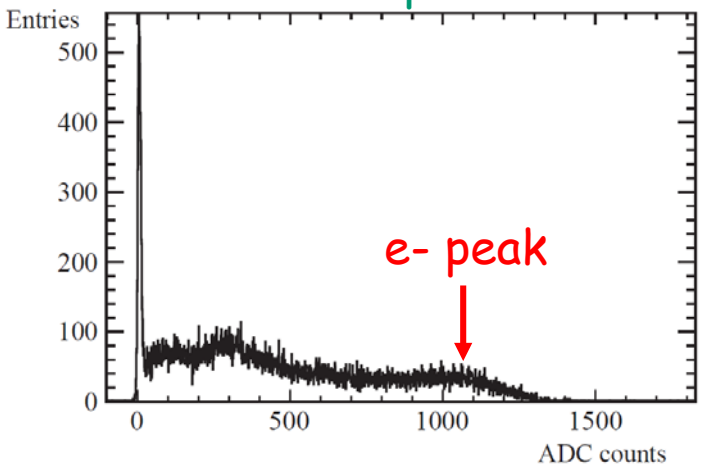
Low e- purity



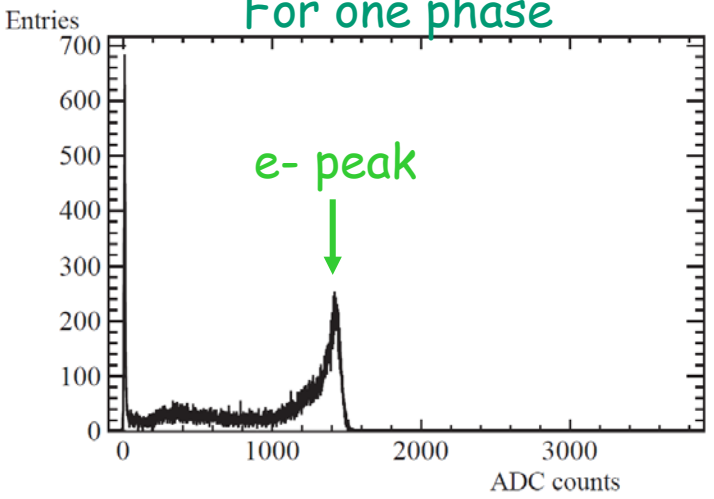
Higher e- purity



For one phase

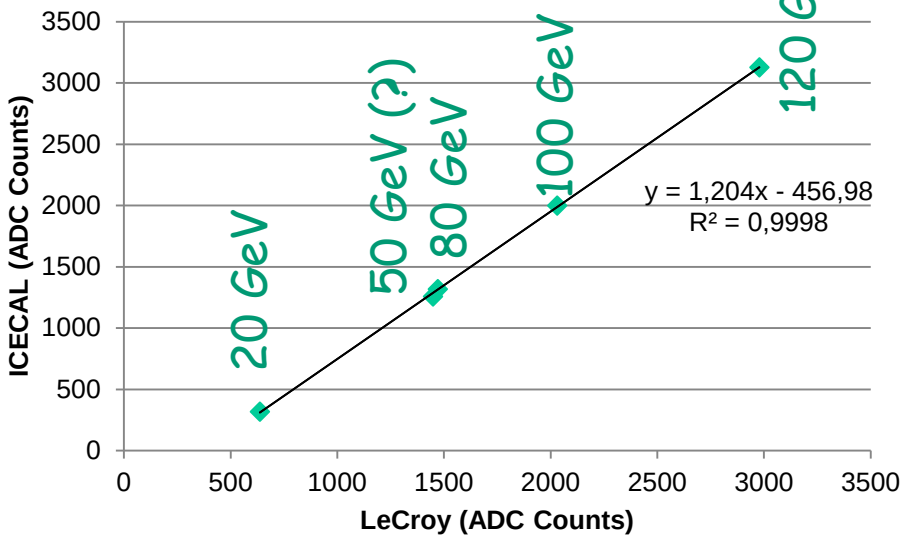


For one phase

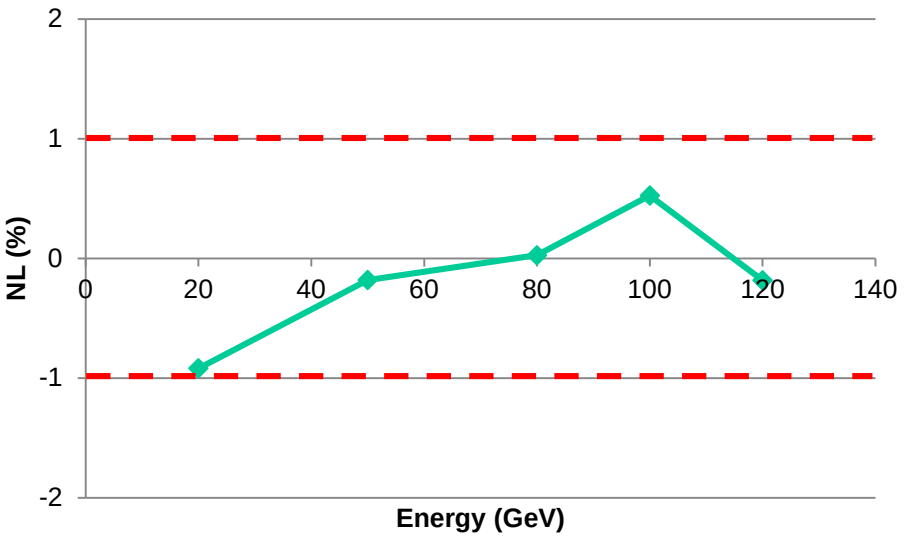


Linearity

- Linearity:
  - Mean max value on the ICECAL output
  - Mean value of the LeCroy

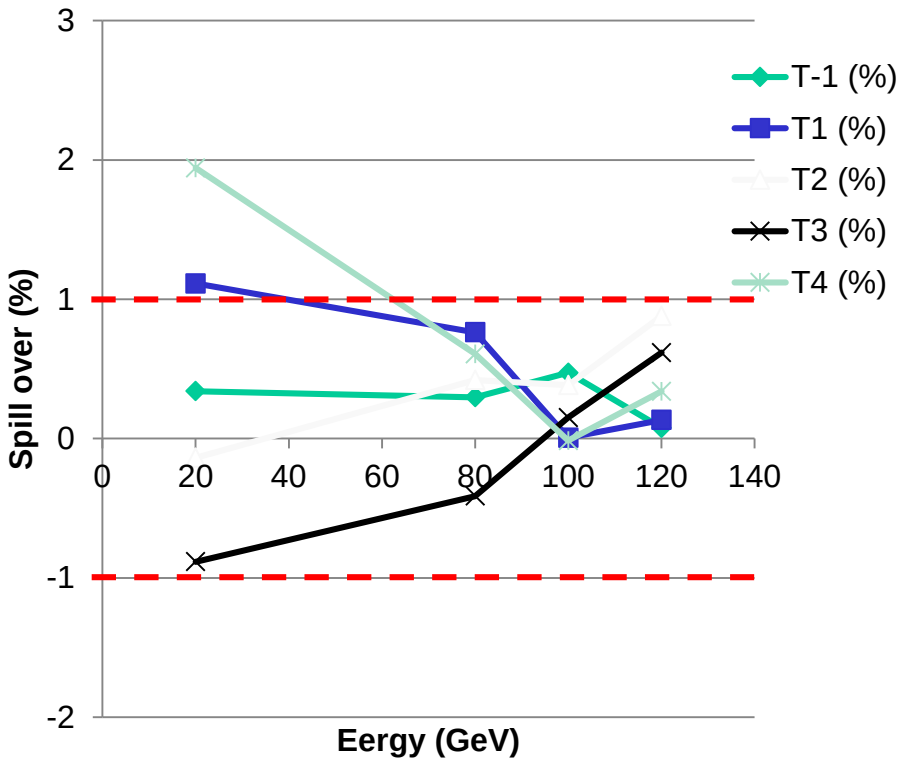


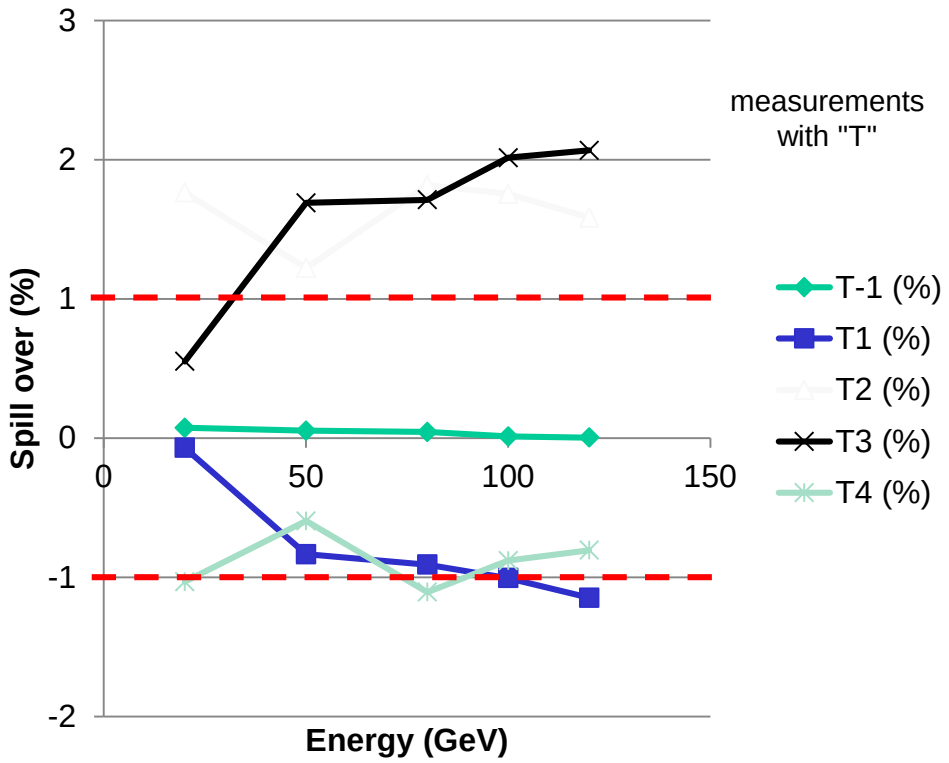
$$NL(\%) = 100\frac{E_{expected} - E_{measured}}{E_{expected}}$$



Spill over

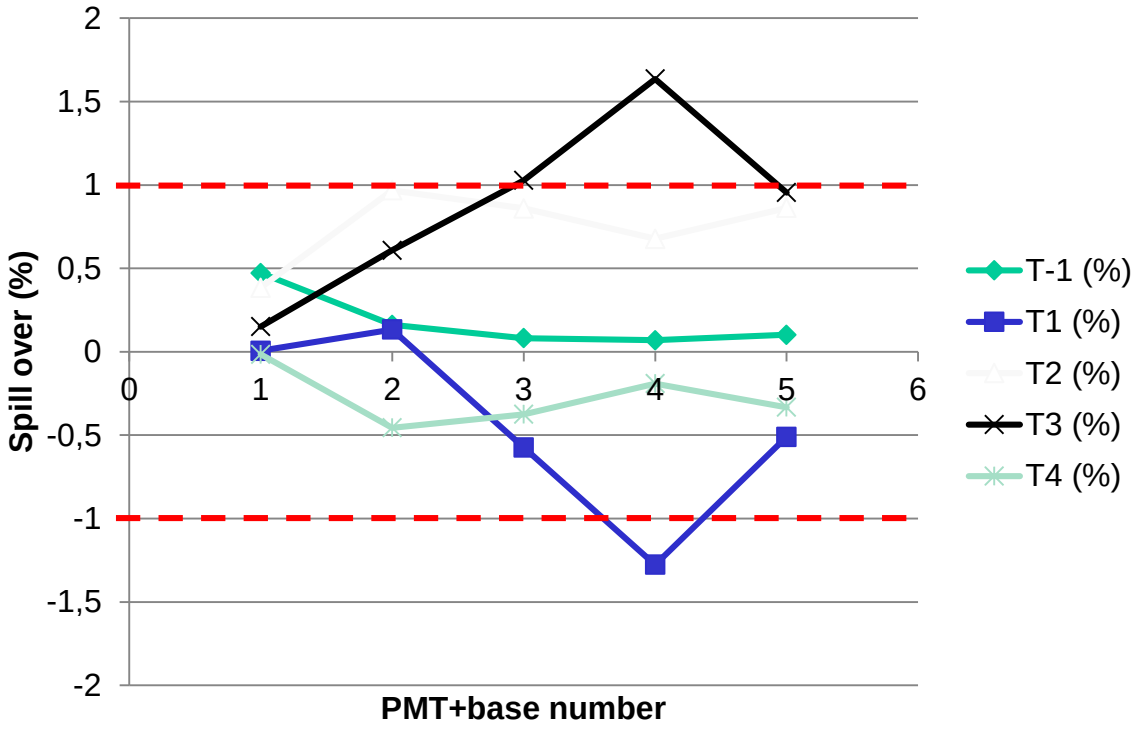
- For different energies





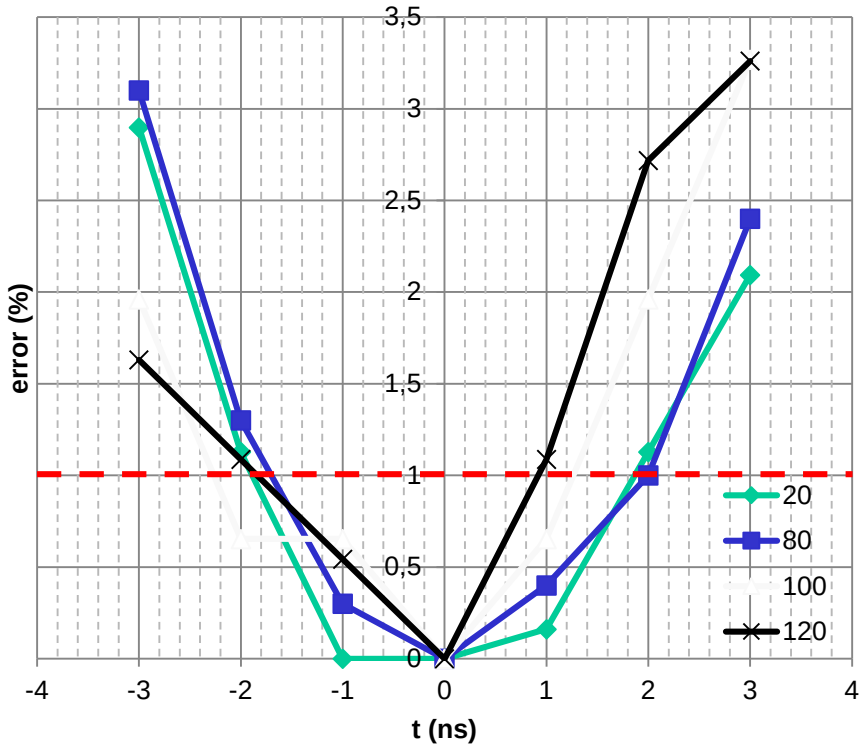
Spill over

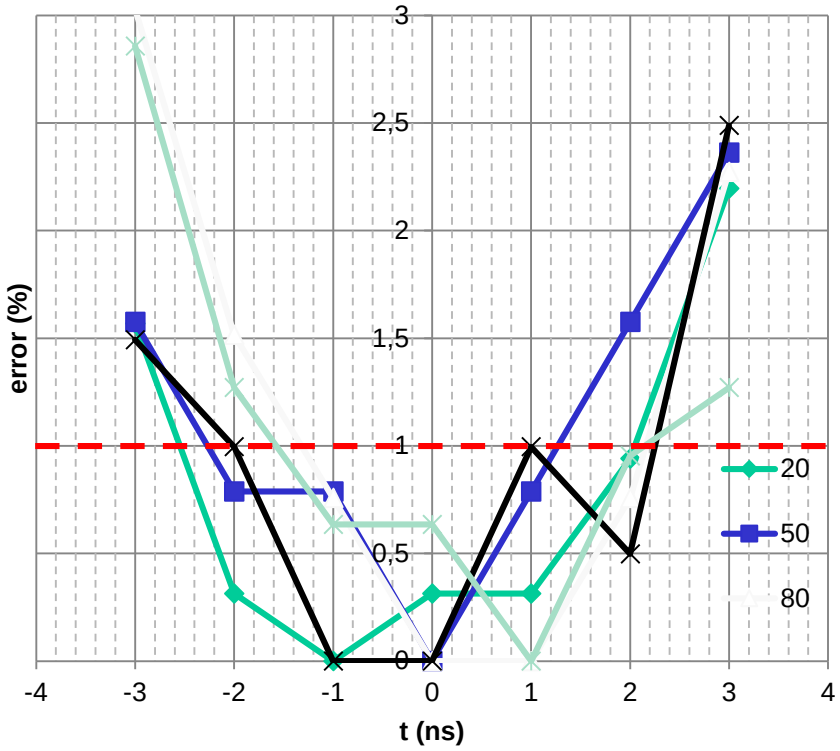
- For different PMT and base



Plateau

- For different energies

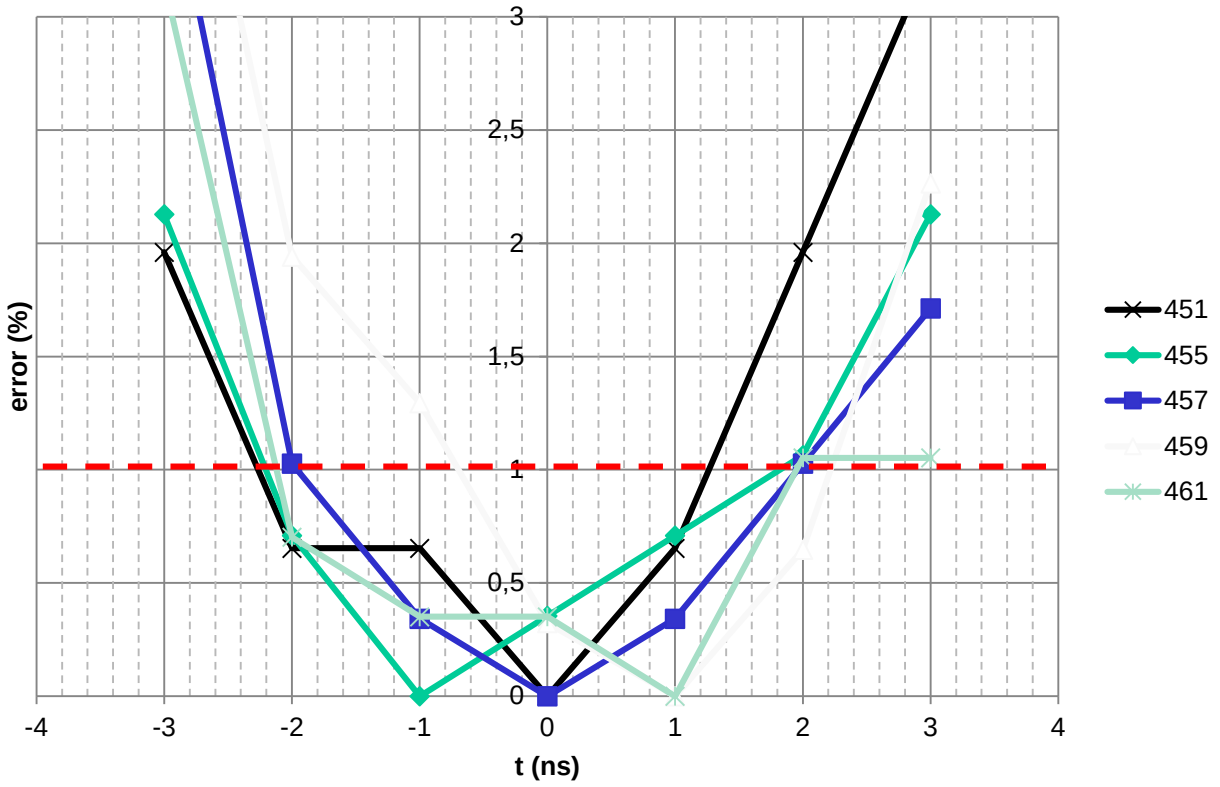




Measurements with "T"

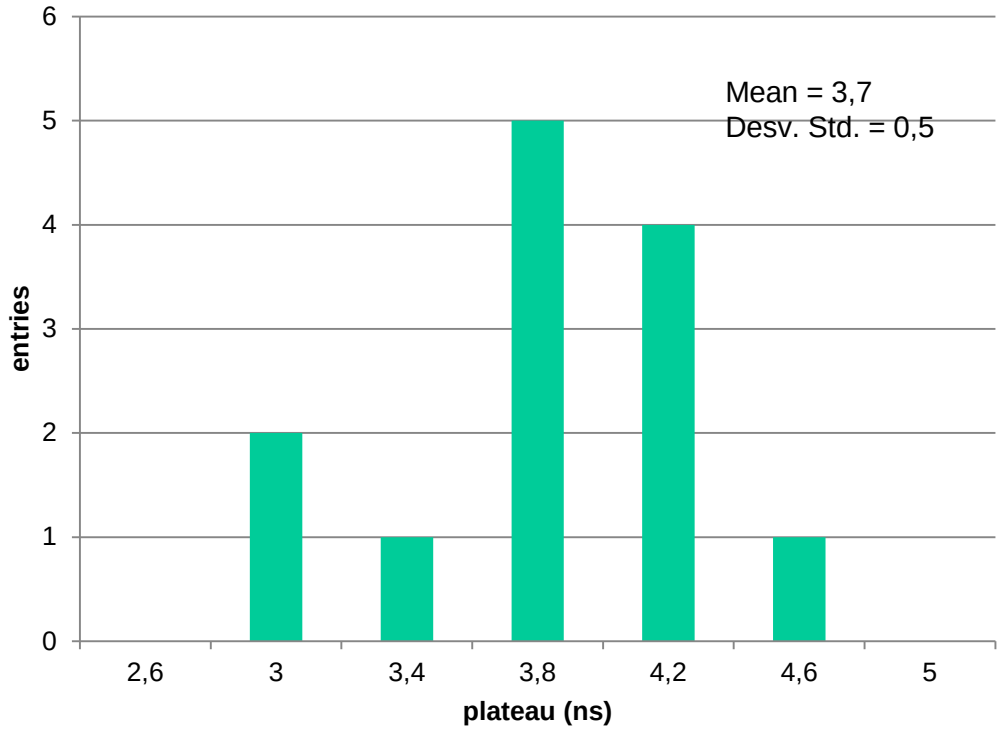
Plateau

- For different PMT and base



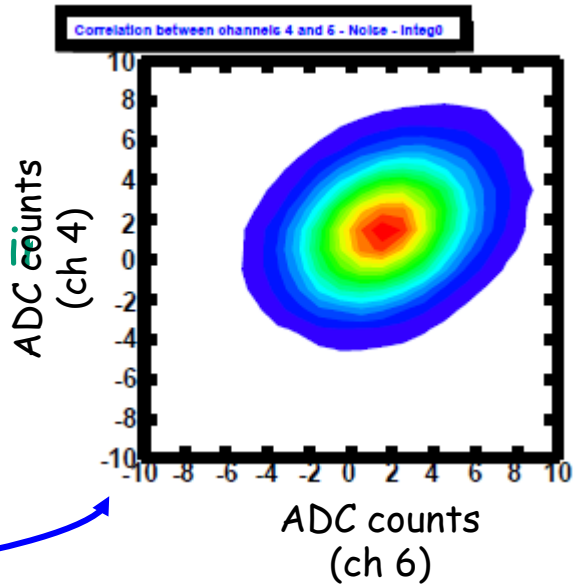
Plateau

- Different plateau results toghether:
  - At different energies, with “T” and changing the PMT+base



Noise

- Check noise in different conditions:
  - With “T”
  - No “T”
  - Clip
  - No clip
- Noise levels:
  - 12 LSB
  - 2.7 LSB (pedestal subtraction)
- Spec: ~1 ADC count
- Measured noise at lab without cable at the i
  - 1.4 ADC counts
  - 1.7 ADC counts with pedestal subtraction
- CW switching noise?
  - Noise levels:
    - 12 LSB
    - 2.7 LSB (pedestal subtraction)
  - Not correlated noise
  - Need to measure at detector level



Noise at the detector

- Measured noise at the detector:
  - PM at nominal conditions of gain ("Present") vs. upgraded
  - Effects of Cockcroft-Walton HV sources and cables increase noise

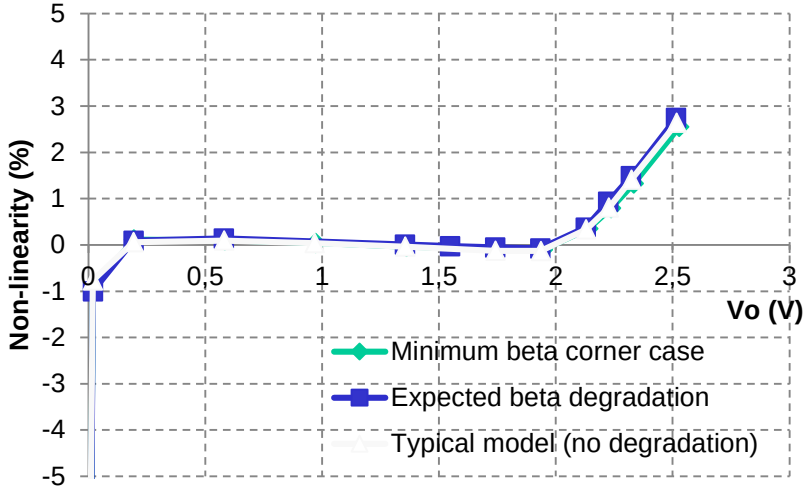
	Channel	PM biasing	Copper braid	Noise (LSB)	PS Noise (LSB)
Not connected			No	1,32	1,59
Not connected			Yes	1,34	1,61
ECAL	200904	Upgrade	Yes	5,83	2,63
ECAL	200904	Present	Yes	6,22	2,69
ECAL worst case	210100	Present	Yes	7,14	2,91
HCAL typical	251726	Present	Yes	2,25	2,20
HCAL worst case	240609	Present	Yes	3,28	2,91

Outlook (II)

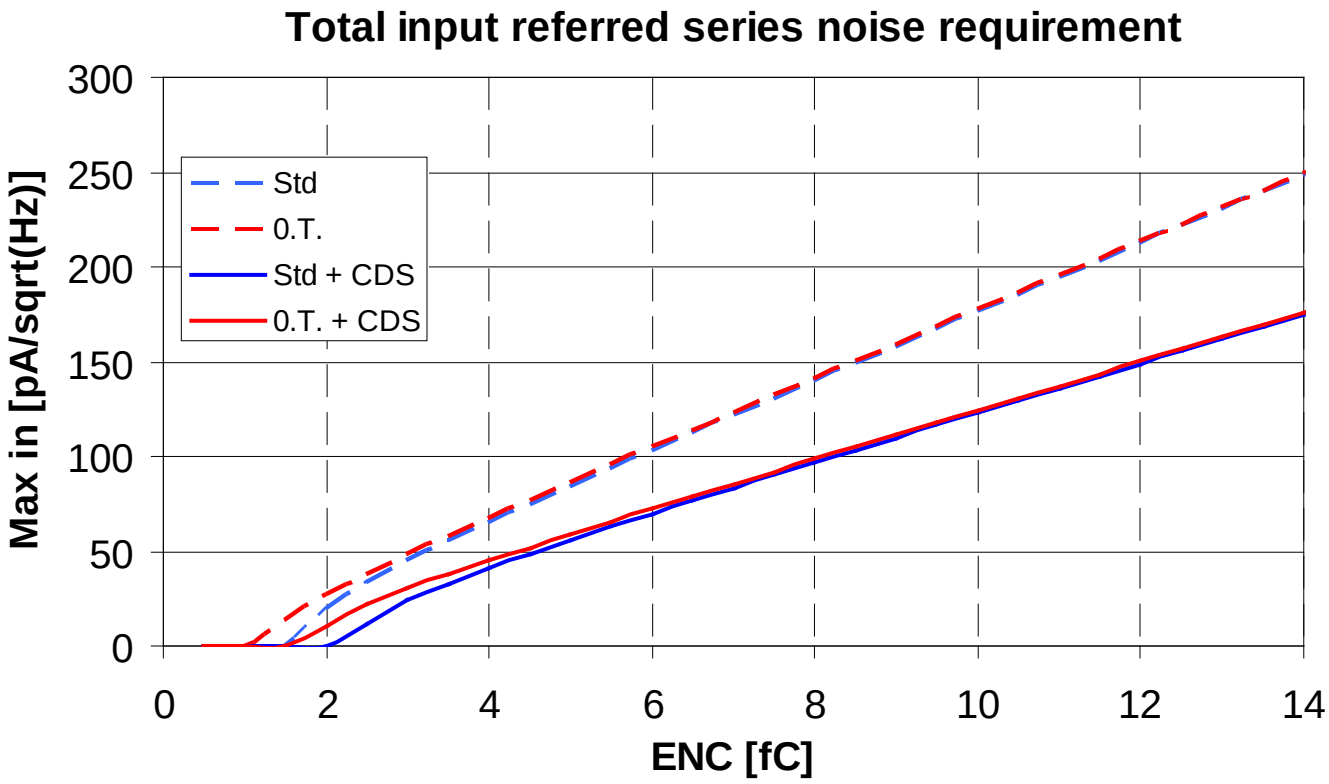
- Test beam
  - Tests performed with real detector signal
  - Statistics:
    - Low e- purity → difficult curve fits for measurements
    - Merged run data files analyzed
  - Linearity OK
  - Plateau and spill over
    - Checked for different conditions
    - Plateau is over 4 ns
    - Spill over below 1% except T2 and T3 with 1.5%
  - Noise levels:
    - Looks like CW noise is high: 12 LSB and 2.7 LSB (ped sub)
    - Measurements at the detector show lower values: 2,2 to 2,9 LSB (ped sub)

Neutron effects

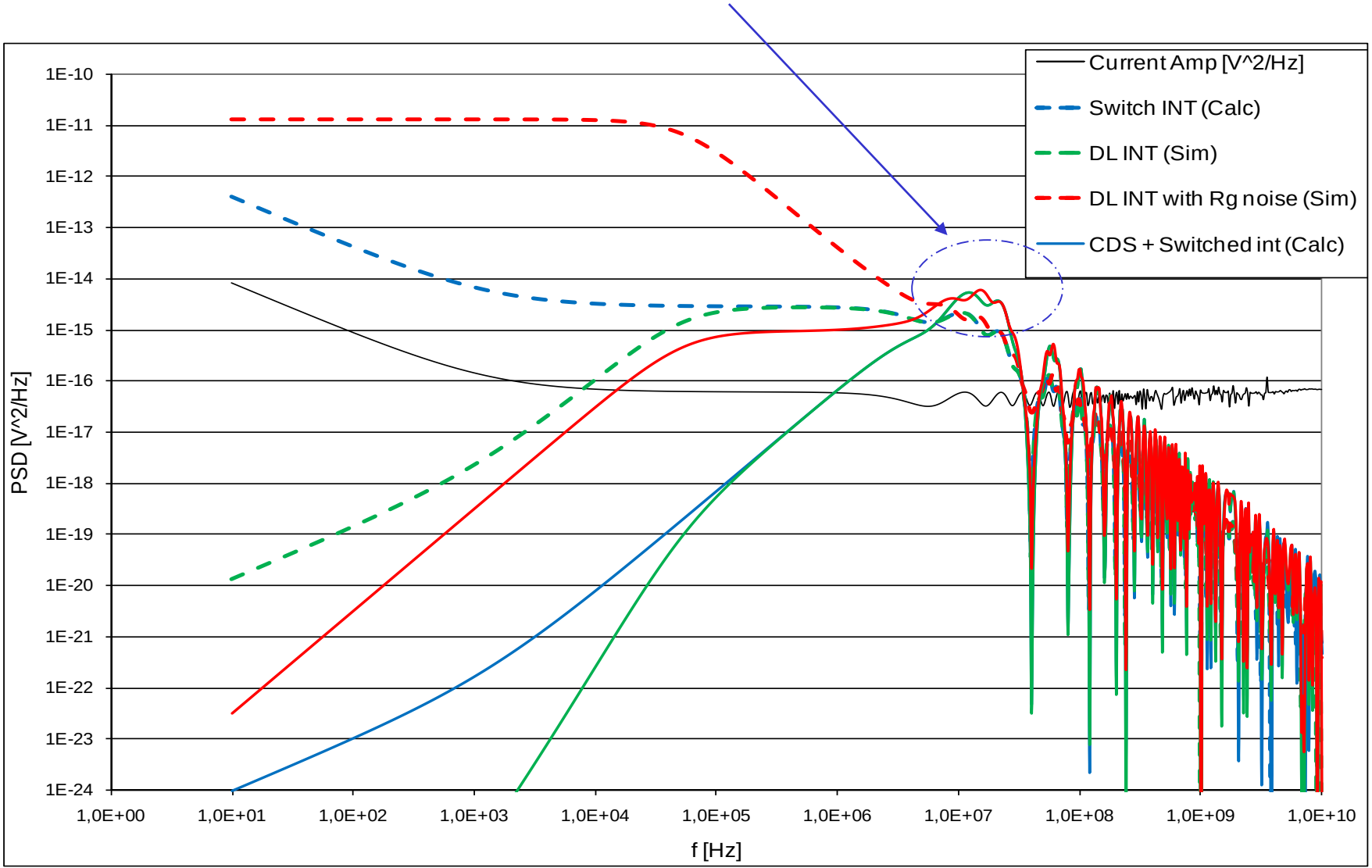
- Expected thermal neutron fluence $2{,}02 \cdot 10^{11}$ cm^{-2} for $50fb^{-1}$
- Effects on BJT described by $\frac{1}{\beta} = \frac{1}{\beta_0} + k_{eq}\Phi_{eq} + k_T\Phi_T$
  - where k_{eq} is 1MeV equivalent factor and k_T is thermal neutron damage factor
    - G. Kramberger and others. Radiationdamage in bipolar transistors caused by thermal neutrons. Nuclear Science Symposium Conference Record, Vol. 1:429-433, 2003.
    - I. Mandic, and others. Bulk damage in dmill npn bipolar transistors caused by thermal neutrons versus protons and fast neutrons. IEEE Trans. Nucl. Sci., 51:1752-1758, 2004.
- Beta degradation: 15,3%
  - Far from degradation due to process variations.
  - Limited effect because at design: closed loop amps (local feedback).



I. Cable impedance and noise



- Reduces LF noise (correlated for t>>T)
- BUT increases uncorrelated noise!

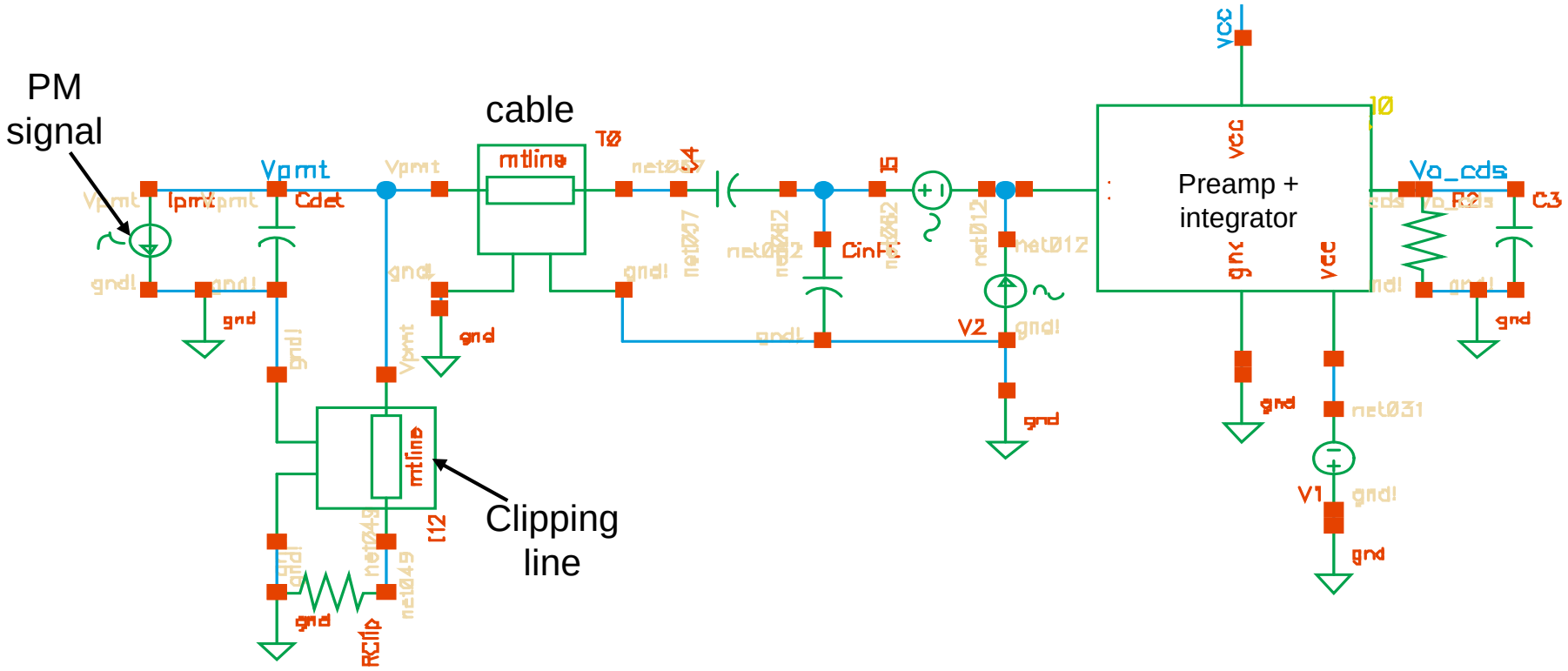


- Current amplifier
- Noise for voltage amplifier is about factor 1.5 – 2 higher
- Numbers may have 10-20 % error
  - Effect of lumped resistor modeling skin effect
  - Systematic for all (comparison does not have this error)

	Integrated noise [uV rms] (10 Hz to 1 GHz)	Noise in ADC counts
Switch INT (Calc)	210	0.5
Switch INT (Tran Sim)	200	0.63
DL INT (Sim)	210	0.5
DL INT with Rg noise (Sim)	1100	3
CDS + Switched int (Calc)	300	0.75
CDS + Switched int (Tran Sim)	300	0.75
CDS + DL Int (Sim)	300	0.75
CDS + DL Int With Rg noise (Sim)	330	0.82

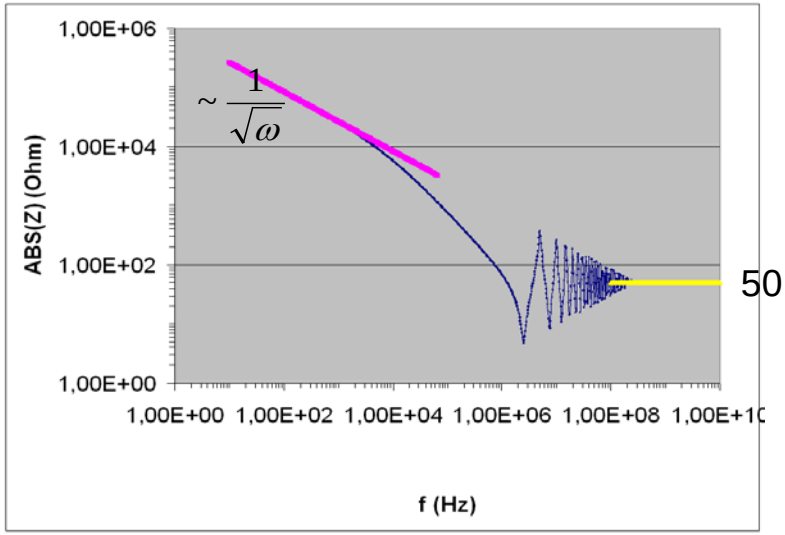
Front End simulations (Preamp+integrator)

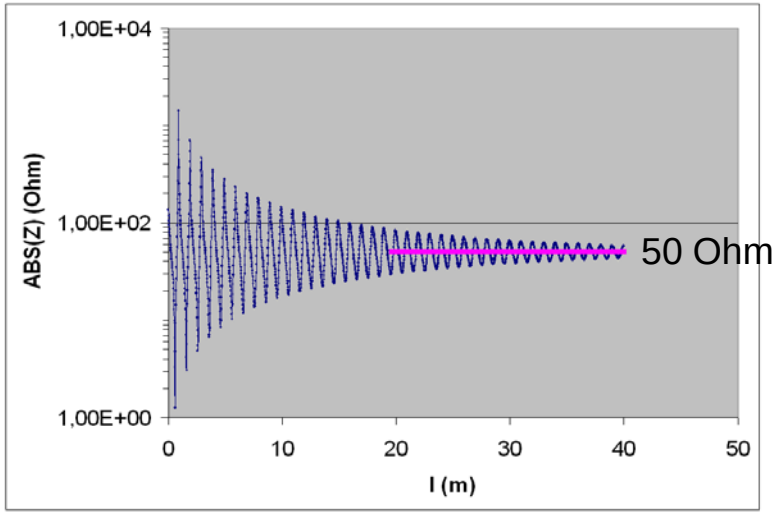
- Simulations based on extracted RC of complete IC
- Includes PM signal and cable effects



Skin effect: impedance after the cable

- Impedance seen after x m of cable towards the detector when **Z_d=1/jCw**:





$$Z(x,\omega) = R_0 \frac{\frac{1}{j\omega C_d} + R_0 tgh(\gamma x)}{R_0 + \frac{1}{j\omega C_d} tgh(\gamma x)}$$

$$Z(x,\omega) \xrightarrow{\omega \to 0} \frac{R_0}{\alpha l} \sim \frac{1}{\sqrt{\omega}}$$

$$Z(x,\omega) \xrightarrow{\omega \to \infty} R_0$$

$$Z(x,\omega) \xrightarrow{x \to 0} \frac{1}{j\omega C_d}$$

$$Z(x,\omega) \xrightarrow{x \to \infty} R_0$$

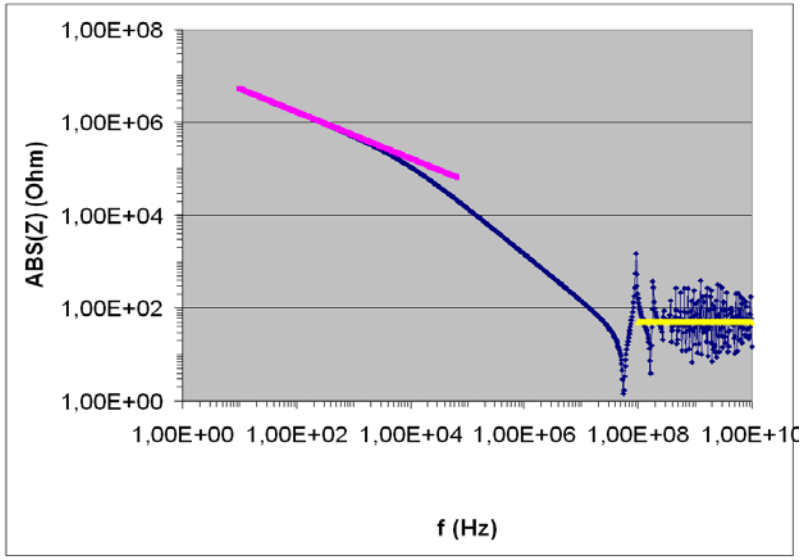
$$Z(x,\omega) \xrightarrow[\omega \to \infty]{x \to 0} \frac{1}{j\omega C_d}$$

$$Z(x,\omega) \xrightarrow[\omega \to 0]{x \to \infty} R_0$$

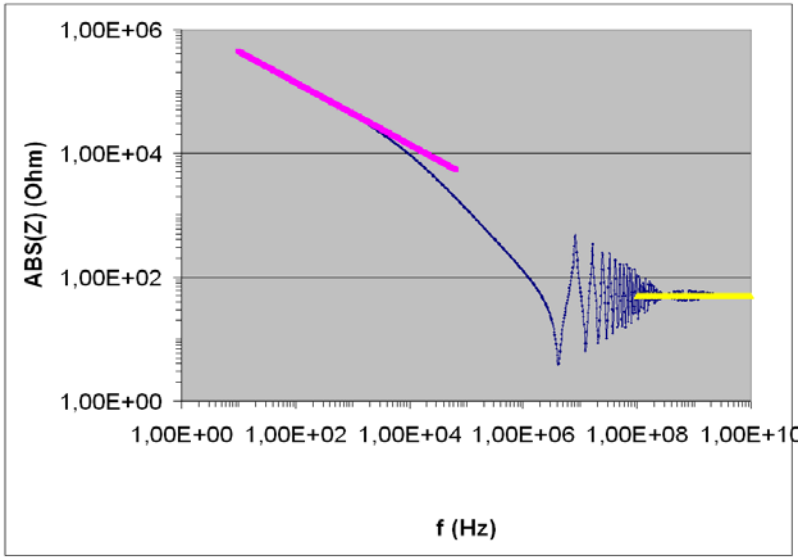
Skin effect: impedance after the cable

- Impedance seen after x m of cable towards the detector when $\mathbf{Z_d=1/jCw}$:

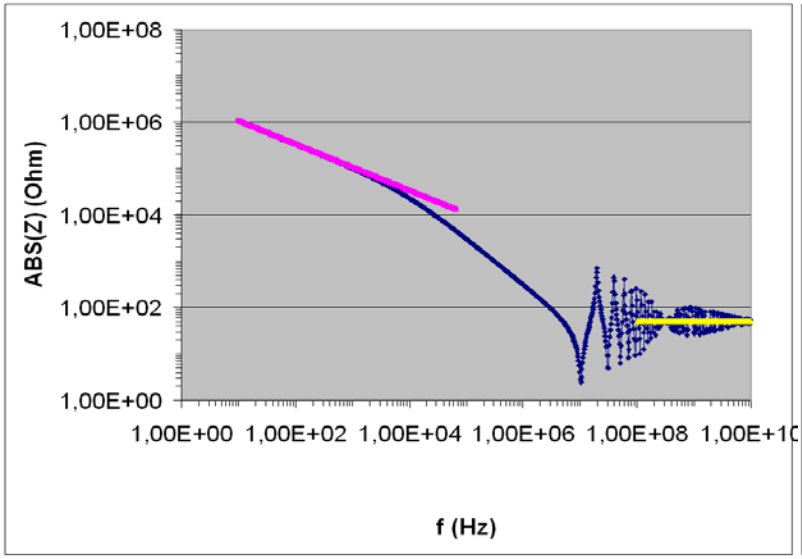
1 m



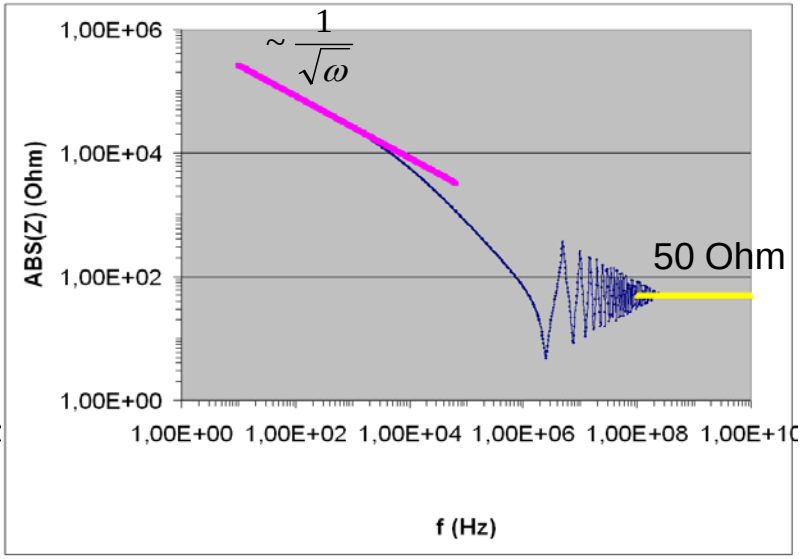
12 m



5 m



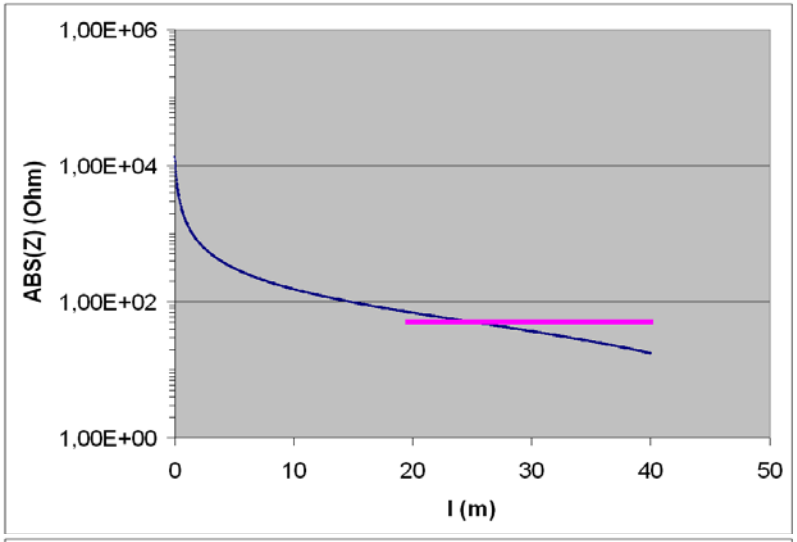
20 m

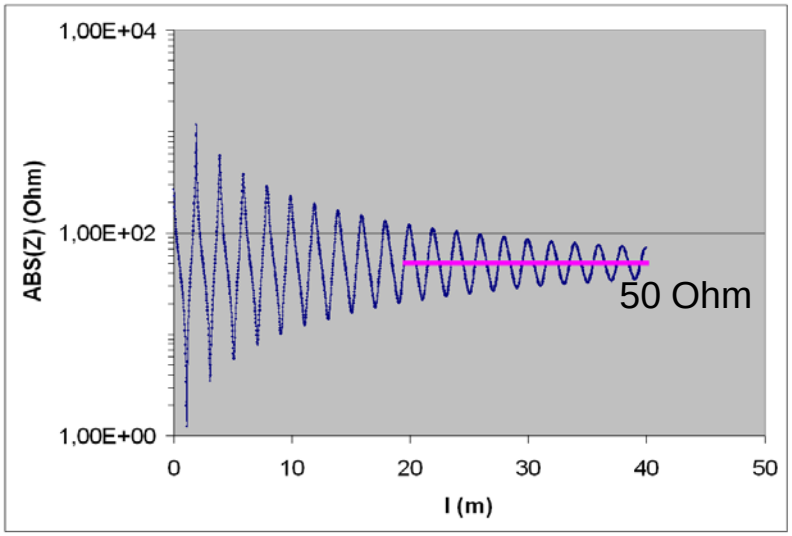


Skin effect: impedance after the cable

- Impedance seen after x m of cable towards the detector when **Z_d=1/jCw**:

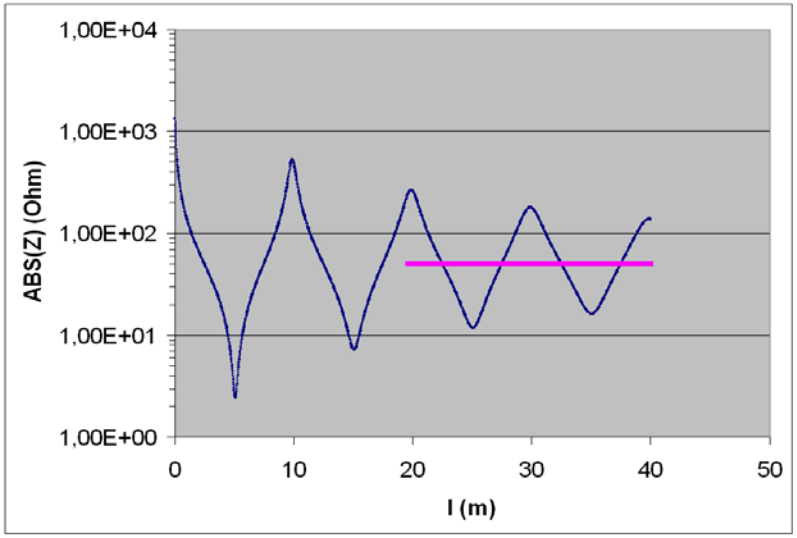
1 MHz

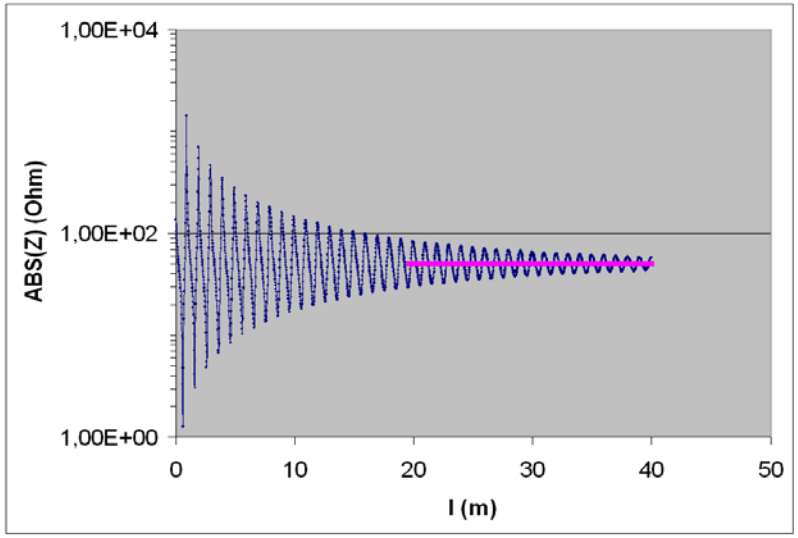




50 MHz

10 MHz

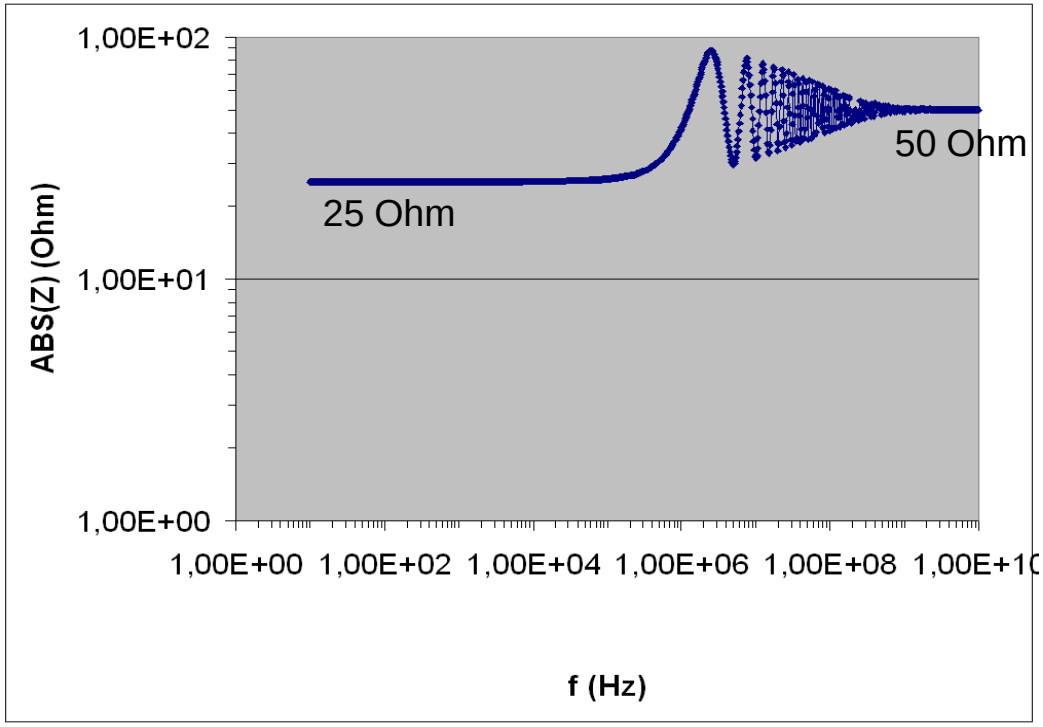




100 MHz

Skin effect: impedance after the cable

- Impedance seen after x m of cable towards the detector when $Z_d=R_d$:



$$Z(x,\omega) = R_0 \frac{R_d + R_0 tgh(\gamma x)}{R_0 + R_d tgh(\gamma x)}$$

$$Z(x,\omega) \xrightarrow{\omega \to 0} R_d$$

$$Z(x,\omega) \xrightarrow{\omega \to \infty} R_0$$

$$Z(x,\omega) \xrightarrow{x \to 0} R_d$$

$$Z(x,\omega) \xrightarrow{x \to \infty} R_0$$

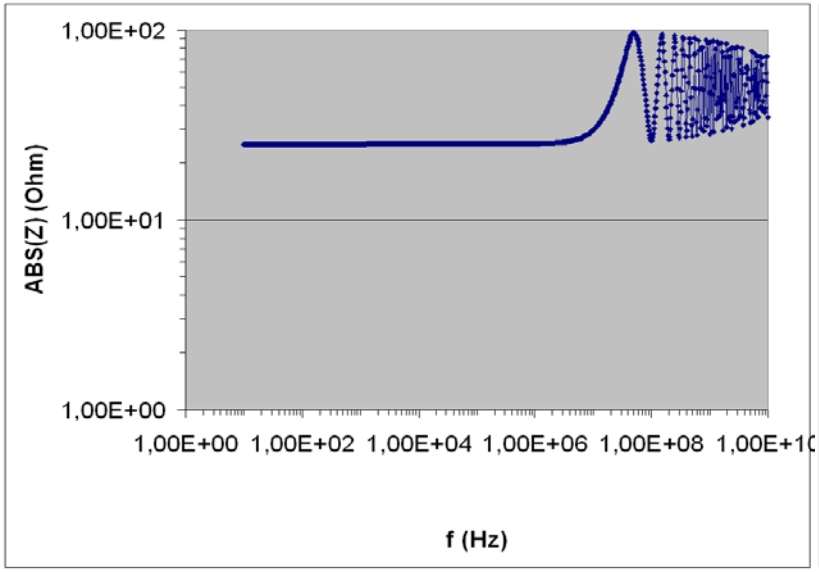
$$Z(x,\omega) \xrightarrow[\omega \to \infty]{x \to 0} R_d$$

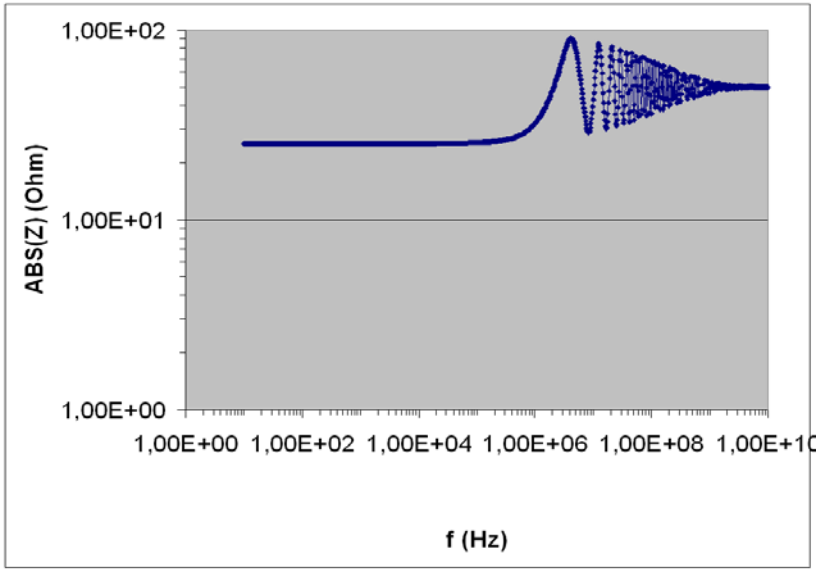
$$Z(x,\omega) \xrightarrow[\omega \to 0]{x \to \infty} R_0$$

Skin effect: impedance after the cable

- Impedance seen after x m of cable towards the detector when $Z_d=R_d$:

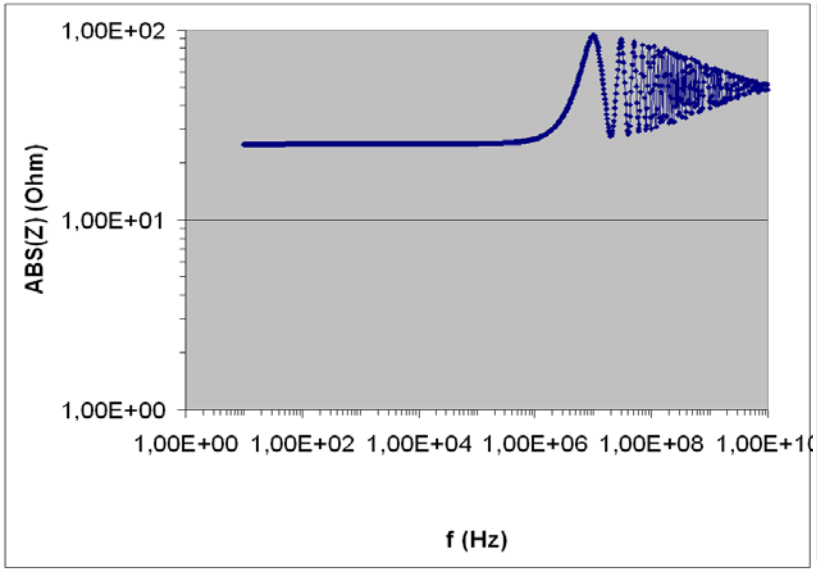
1 m

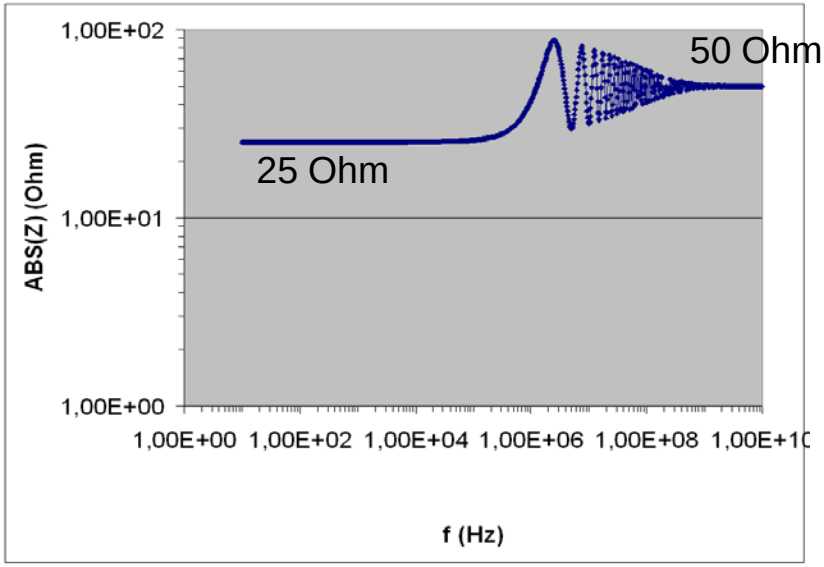




12 m

5 m



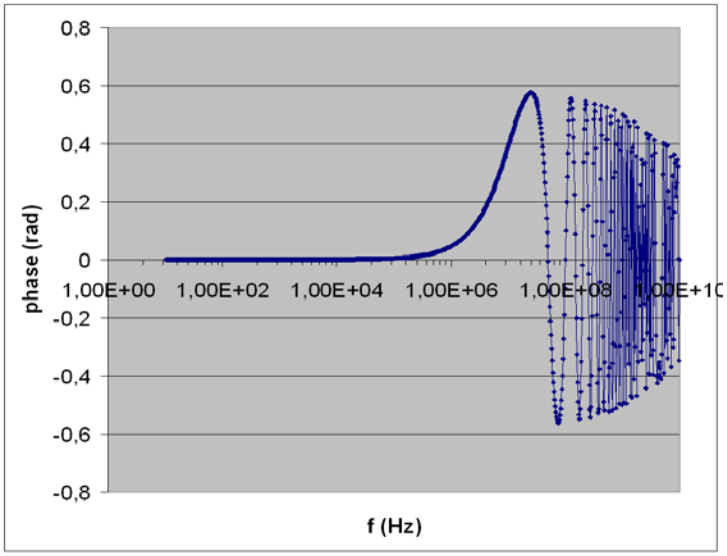


20 m

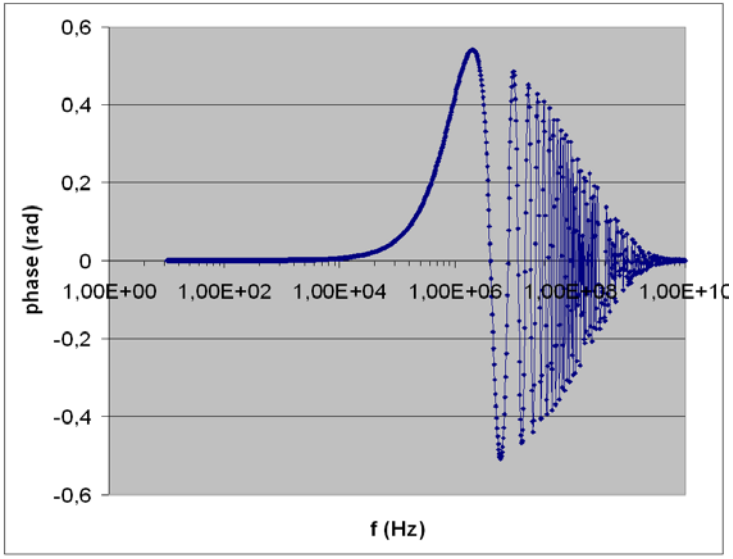
Skin effect: impedance after the cable

- Phase seen after x m of cable towards the detector when $Z_d=R_d$:

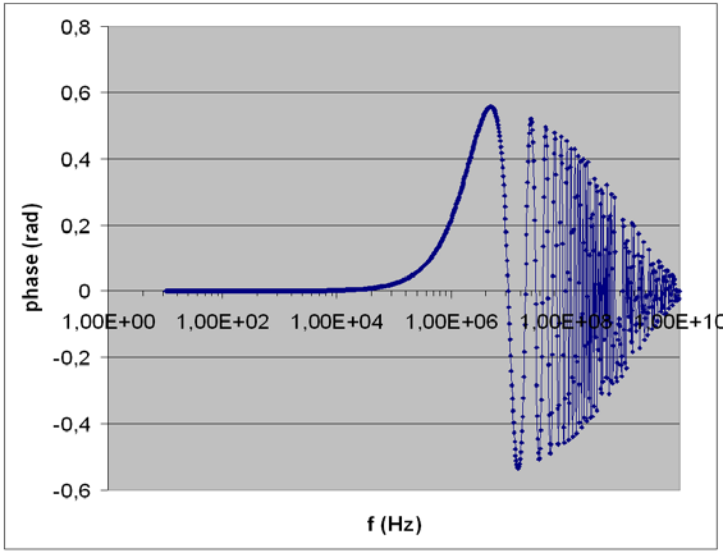
1 m



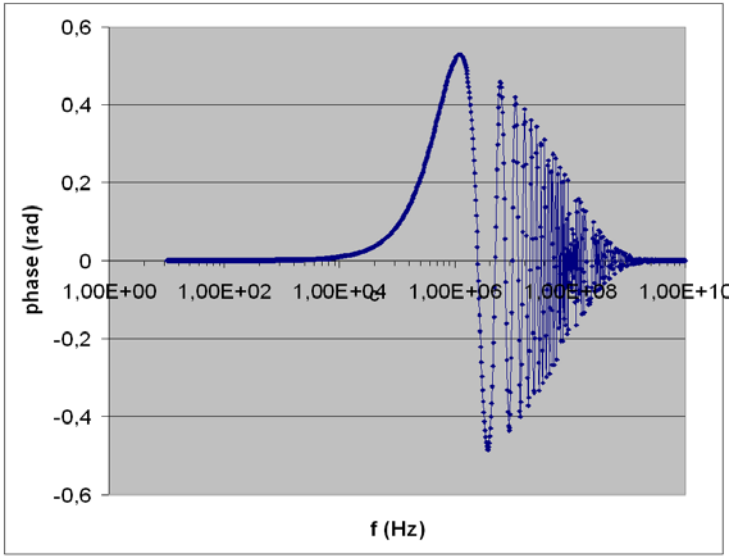
12 m



5 m



20 m



Skin effect: impedance after the cable

CONCLUSIONS:

- As expected, for
  - Very short cables, $Z \approx Z_d$
  - Long cables, $Z \approx Z_0$
- Impedance seen after 12 m of cable towards the detector when $\mathbf{Z_d = 1/jCw}$:

  $f < 1$ kHz $\rightarrow |Z| \sim 1/\sqrt{\omega}$

  1 kHz $< f <$ 2-3 MHz $\rightarrow |Z| \sim 1/j\omega C_d$ (as without the cable)

  2-3 MHz $< f <$ 1 GHz $\rightarrow |Z|$ oscillates between 2 and 200Ω

  $f >$ 1 GHz $\rightarrow |Z| \sim$ 50Ω
- Impedance seen after 12 m of cable towards the detector when $\mathbf{Z_d = R_d}$:

  $f <$ 2-3 MHz $\rightarrow |Z| \sim R_d$ (as without the cable)

  2-3 MHz $< f <$ 1 GHz $\rightarrow |Z|$ oscillates between 25 and 100Ω

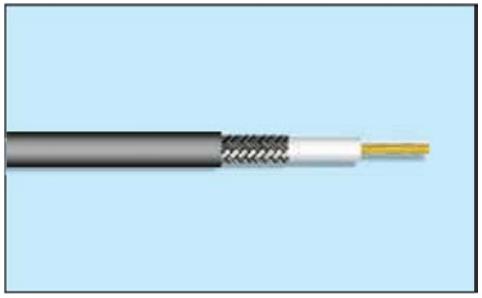
  $f >$ 1 GHz $\rightarrow |Z| \sim$ 50Ω

Skin effect: cable resistance

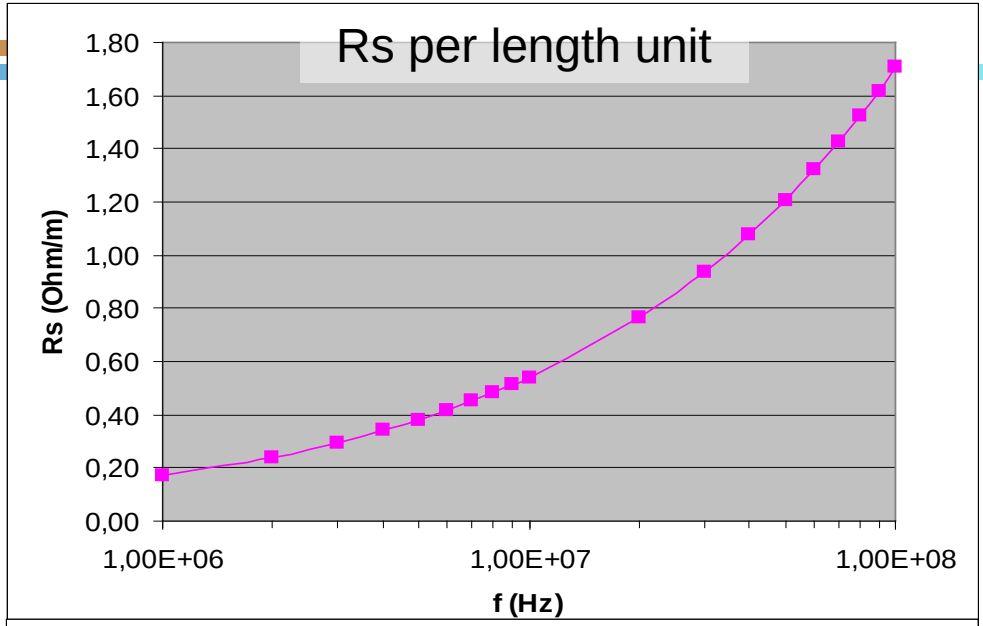
- Resistance per unit length R_S:

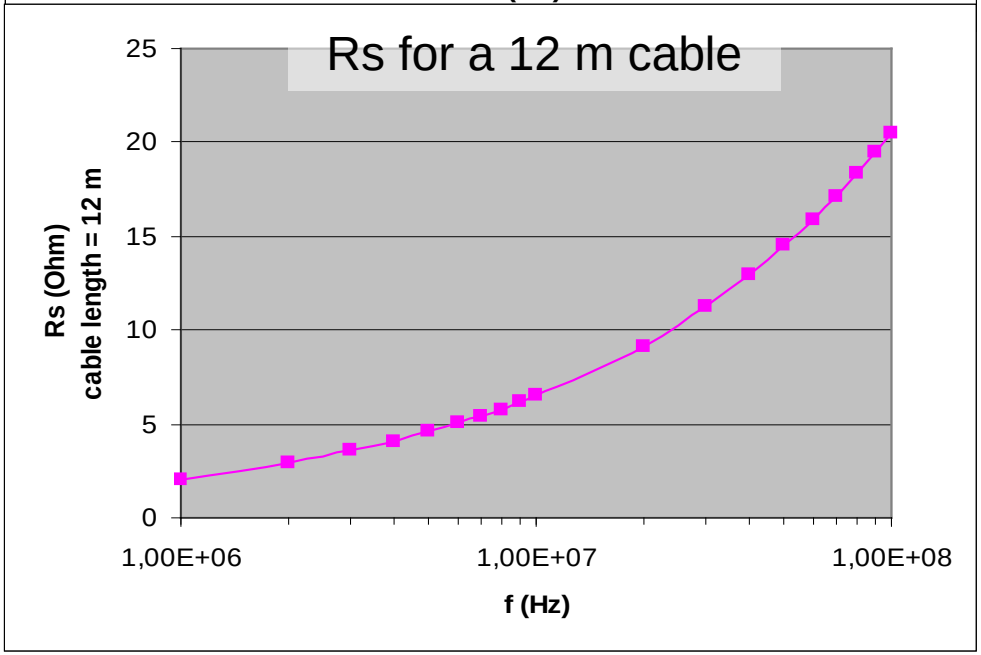
$$R_S = \frac{1}{\pi D}\sqrt{\frac{\omega\mu\rho}{2}}$$

- Skin effect resistor Rs values:
  - Freq high enough to suppose current only on the cable surface
  - D = 0.48 mm
  - $\mu_{Cu} \approx \mu_0 = 1.26*10^{-6}$ H/m
  - $\sigma_{Cu} = 5.96*10^{7}$ S/m



Cable used: coaxial KX3B





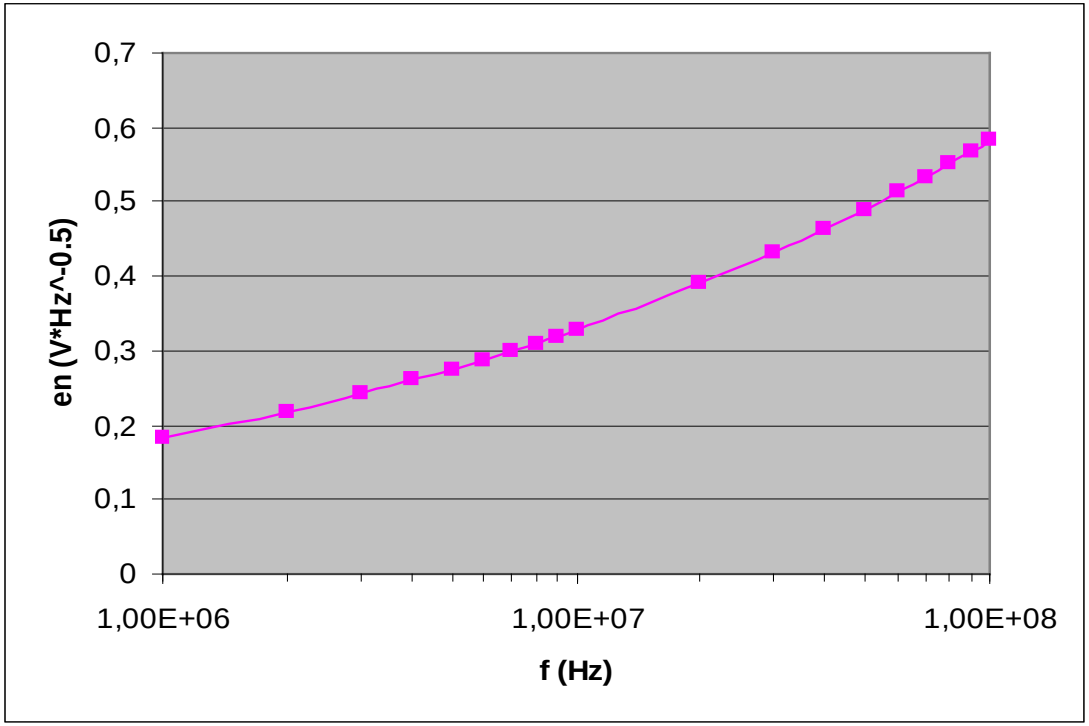
Skin effect: noise contribution

- Noise generator per unit length:

$$\hat{e}_n^{\,2}(f) = 4KTR_S(f)$$

  - Propagation constant (rearranged):

$$\gamma = \frac{R_S(\omega)}{2R_0} + j\frac{\omega}{v_p}$$



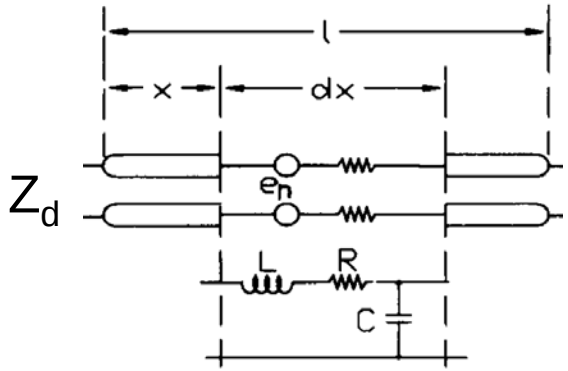
Plot e_n (nV/√Hz):

- Temperature: 300 K
- Cable length: 12 m
- Fast shaping times approximation:
  - Skin effect noise ~ single noise generator at preamp input
  - Aproximate R_S at preamp+shaper central frequency

$\Rightarrow R_S \simeq 18\ \Omega$

Noise current

- The noise current per unit length at position x (^ means per unit length):



$$\hat{i}_n^{\,2}(x) = \hat{e}_n^{\,2}\,\frac{1}{\left|Z(x,\omega)+R_0\right|^2}\left|e^{-\gamma(l-x)}\right|^2$$

$$\begin{cases} \hat{e}_n^{\,2} = 4KTR_S \\ R_S = \dfrac{1}{\pi D}\sqrt{\dfrac{\omega\mu\rho}{2}} \\ \gamma = \dfrac{R_S}{2R_0} + j\dfrac{\omega}{v_p} \\ Z = R_0\,\dfrac{Z_d + R_0 tgh\gamma x}{R_0 + Z_d tgh\gamma x} \end{cases}$$

- From which we can obtain i_n^2 integrating over the length of all the cable from the detector to the preamp:

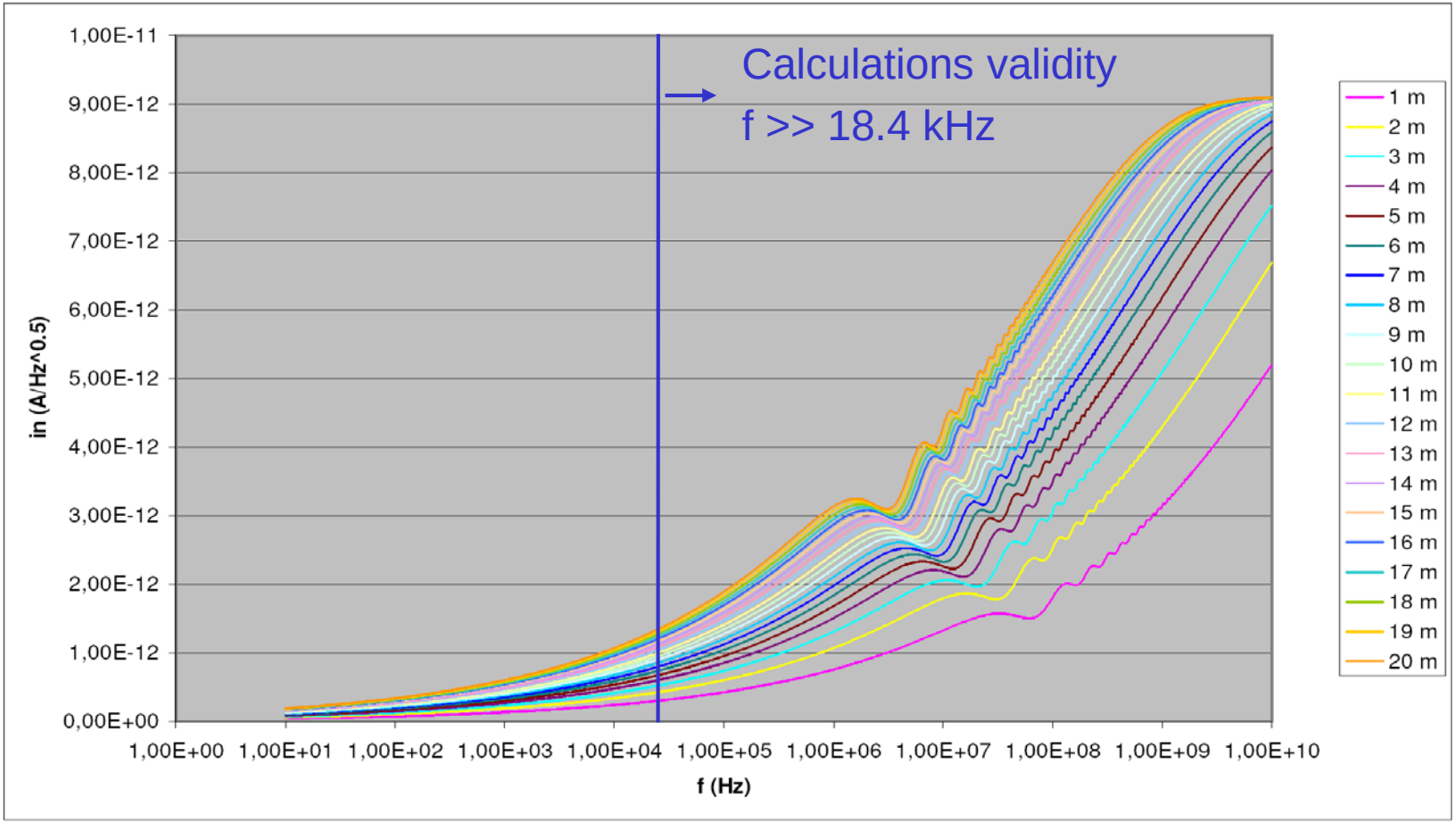
$$i_n^{\,2}(\omega) = \int_0^l \hat{i}_n^{\,2}(x)\,dx$$

- In the case of the clipping line (Z_d=R_d):

$$i_n^{\,2} = \frac{\hat{e}_n^2}{4R_0^{\,2}(R_0+R_d)^2}\left[(R_0+R_d)^2\,\frac{1-e^{-4\alpha l}}{2\alpha} + R_0R_d\,\frac{e^{-4\alpha l}-2e^{-2\alpha l}+1}{\alpha} + \left(R_0^{\,2}+R_d^{\,2}\right)e^{-2\alpha l}\,\frac{\sin 2\beta l}{\beta}\right]$$

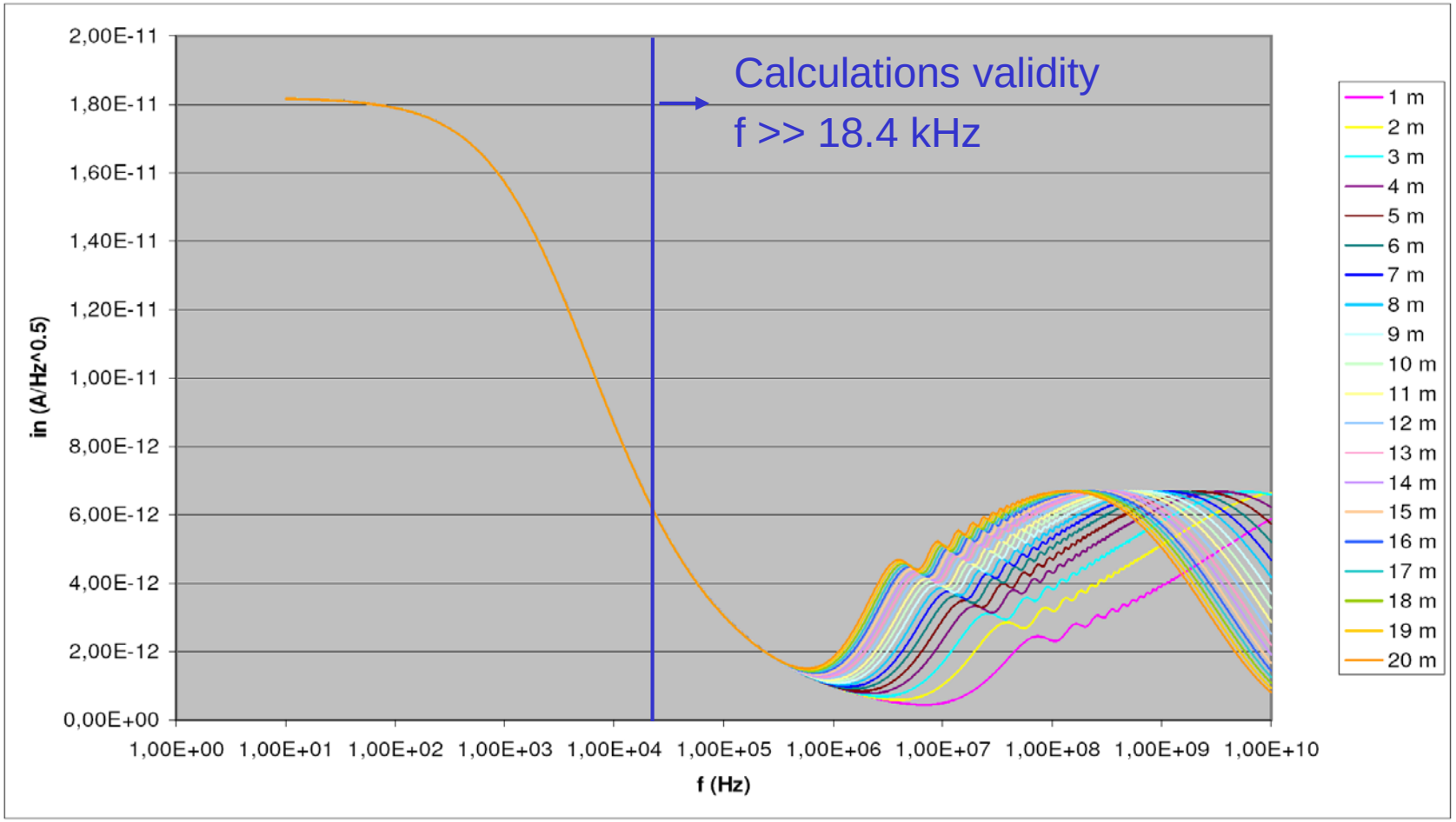
Calculated skin effect noise current

- Noise current generated by the cable In the case of the clipping line (Zd=Rd):



Calculated skin effect noise current

- Noise current generated by the cable in the case without clipping line (Zd=1/jCdw):

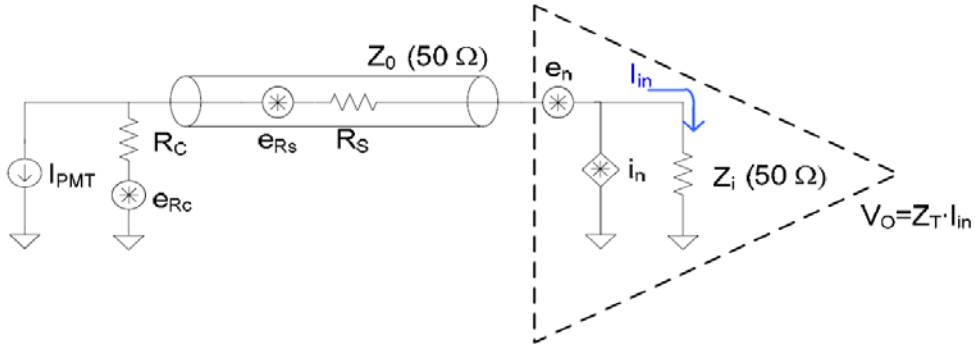


Skin effect: PSD calculation

- Case of clipping line and current amp
- On David's talk, all amp PSD is calculated:

$$i_{ni}^2 = i_{ni}^2\Big|_{e_{tRc}} + i_{ni}^2\Big|_{e_{tRs}} + i_{ni}^2\Big|_{e_n} + i_{ni}^2\Big|_{i_n} + \text{cov}\ldots$$

  - Transimpedance gain Z_T=500Ω



- PSD of the cable (skin effect) after the preamp:

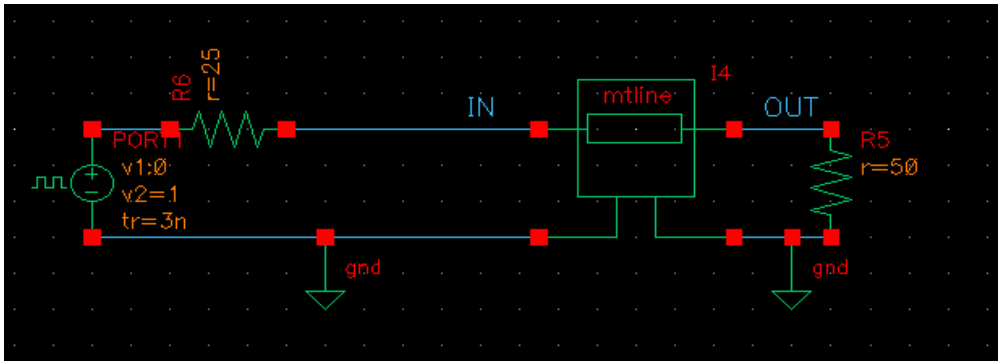
$$e_{no}(cable) = Z_T i_n$$

  - We can use the previous result (slide 16), or
  - A lumped resistor at about 18Ω:

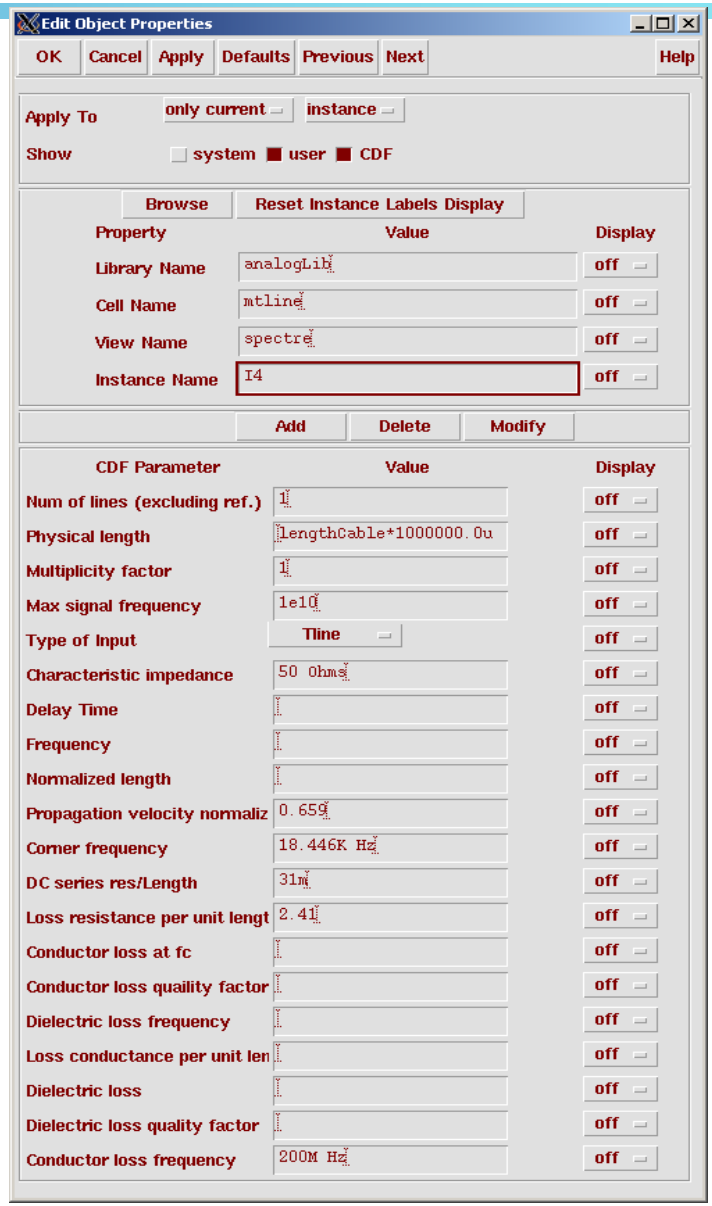
$$i_{ni}^{\ 2}\Big|_{e_{tRs}} = \frac{4KTR_S}{\left|R_S + Z_0\right|^2}$$

Skin effect simulated noise

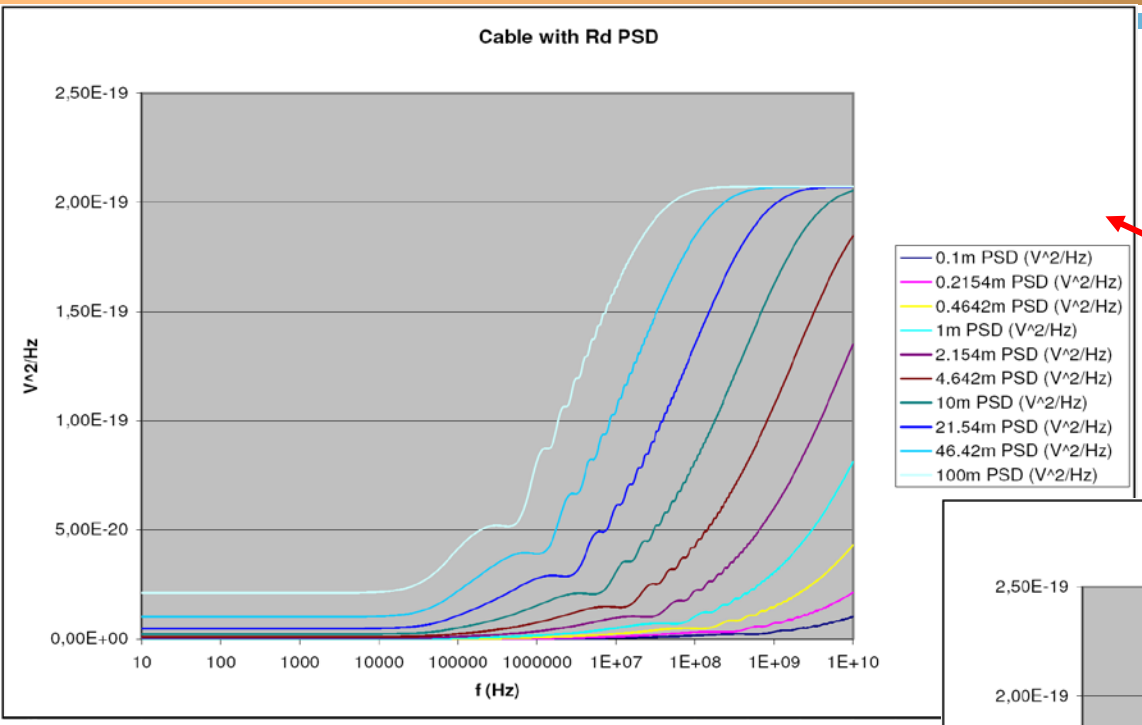
Cadence Spectre simulation circuit with mtline:



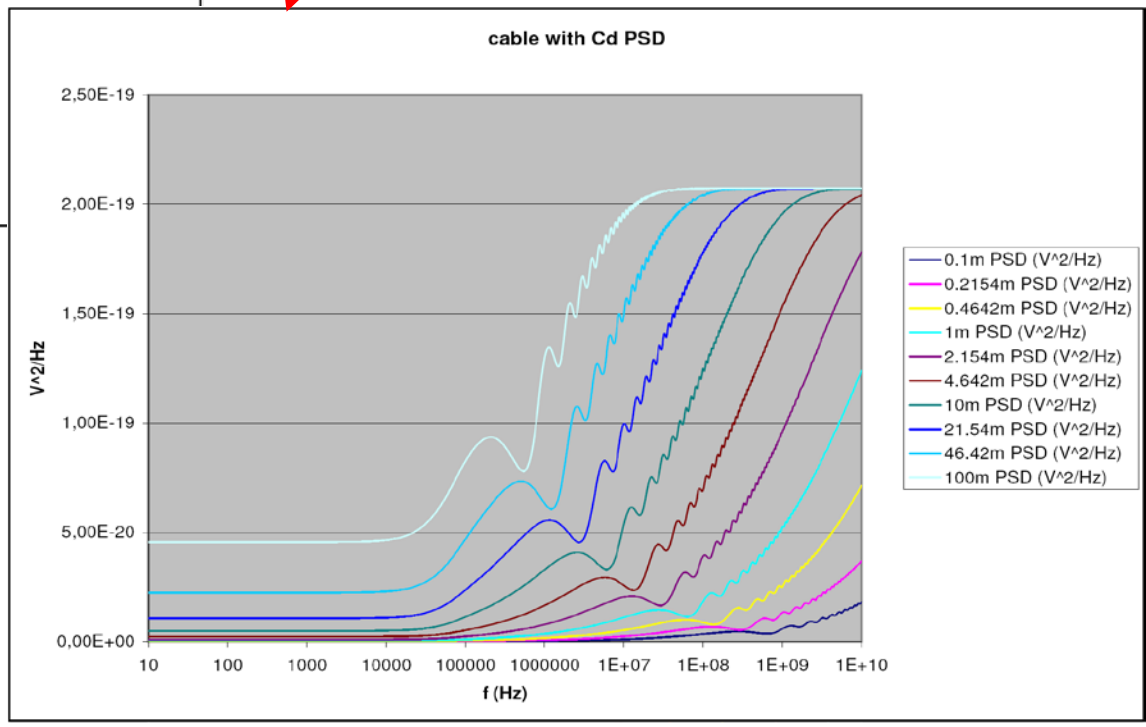
Parameter	Name	Value
Cable physical length	l	12 m
Normalized velocity	v	0.659 c
Corner frequency: f at which skin depth = conductor's width	f_{corner}	18.446 kHz
DC series resistance per unit length	R_{DC}	0.031 Ω/m
Conductor loss measurement frequency	f_c	200 MHz
Conductor series resistance per unit length at f_c	R_S	2.411 Ω/m



Skin effect simulated noise

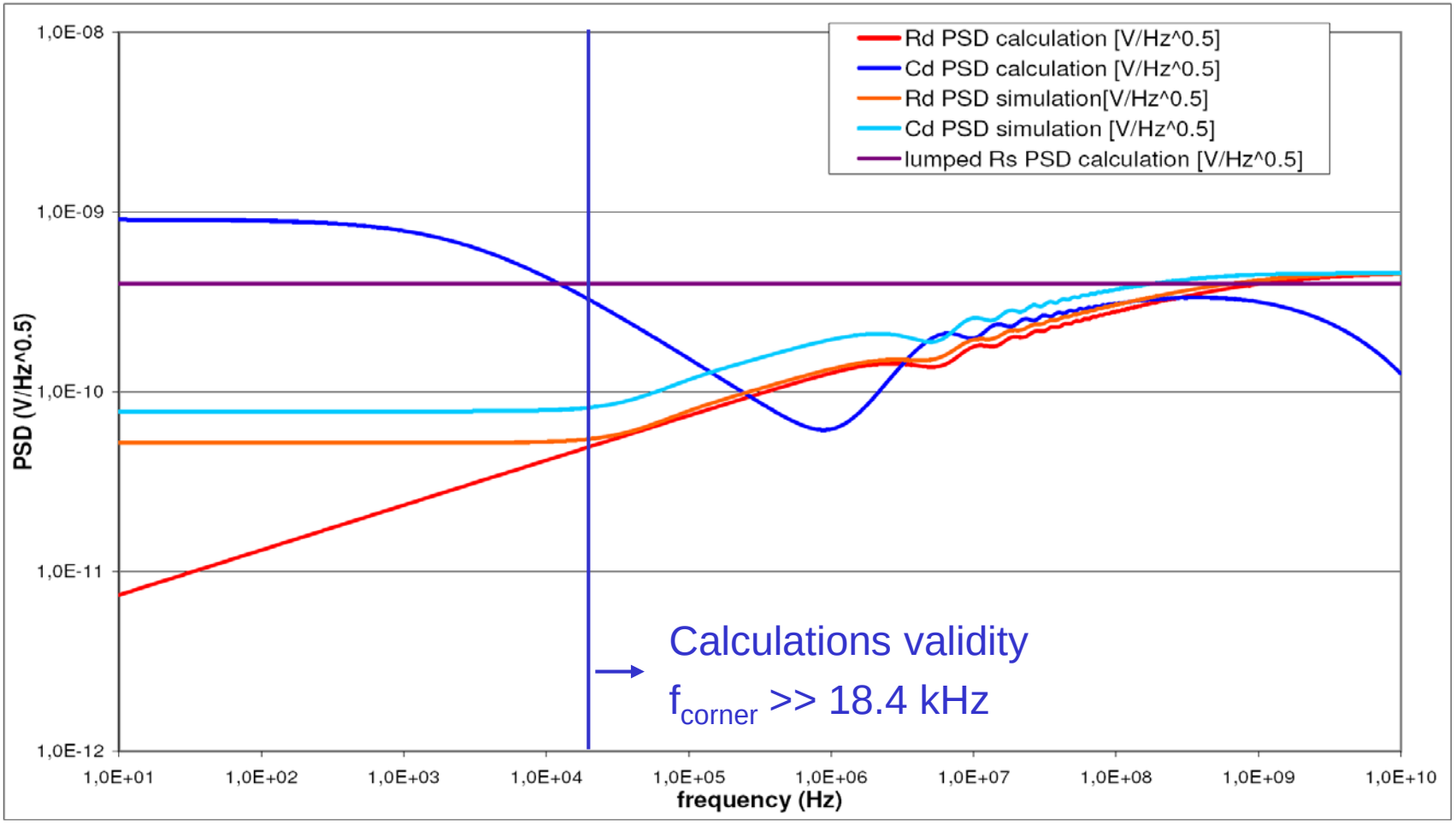


- Cadence Spectre simulation circuit with mtline and different lengthes (from 0.1 to 100 m):
  - with clipping line ($Z_d = R_d$)
  - without clipping line ($Z_d = 1/jC_d\omega$)



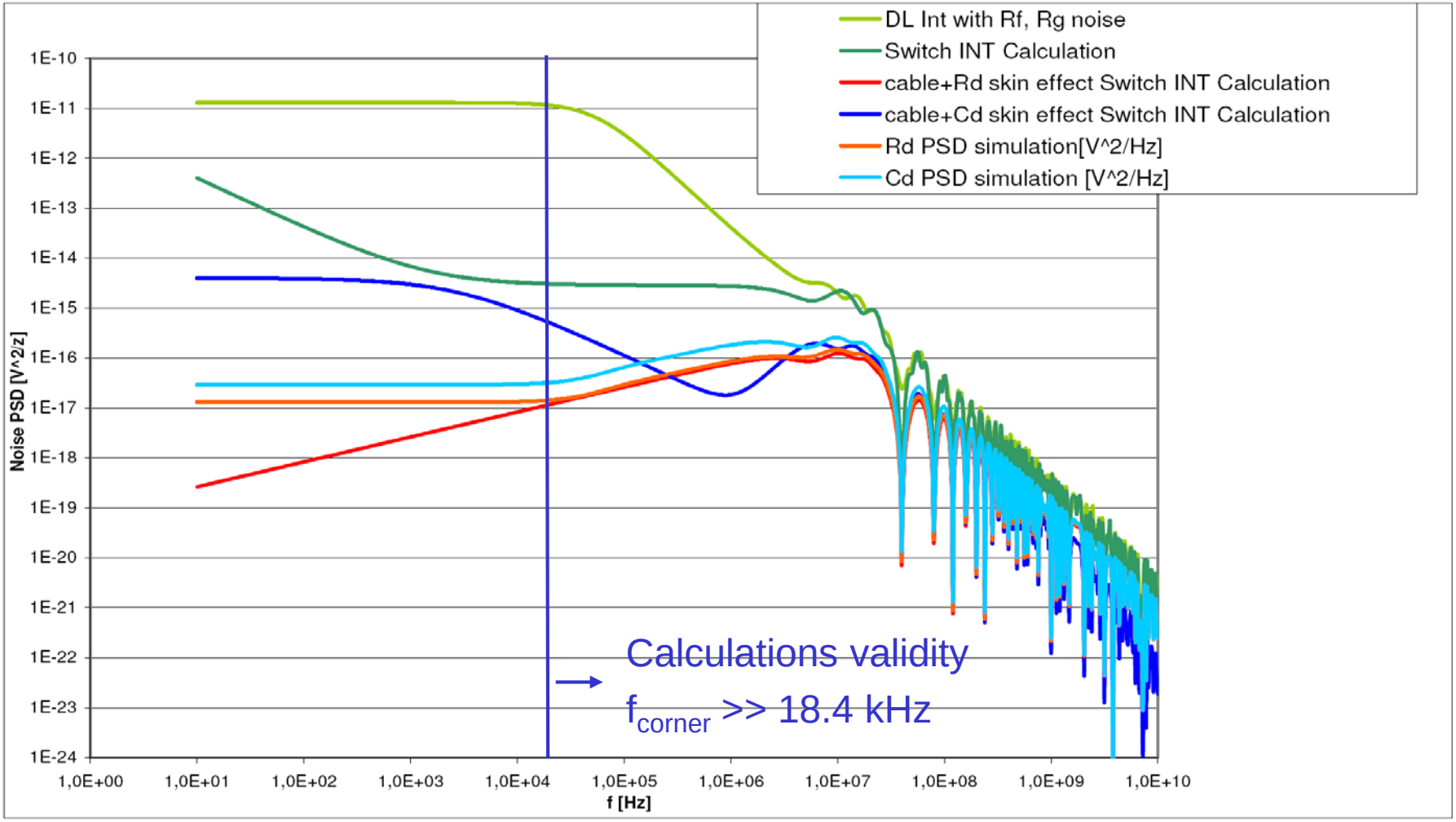
Skin effect generated noise

- Comparison between $Z_d=1/jC_d\omega$ and $Z_d=R_d$ for a cable of 12m calculation, simulation, and $R_S=18\Omega$ lumped approximation:



Skin effect generated noise

- Comparison between Zd=1/jCdw and Zd=Rd for a cable of 12m after integration:



Conclusions on cable effects

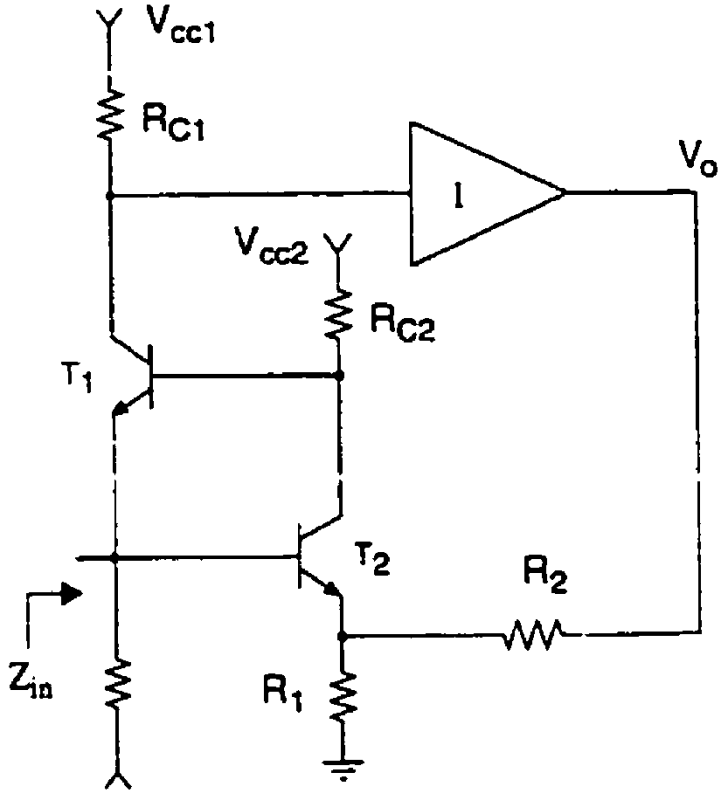
- 2 main cable effects on SNR:
  - Attenuation due to the skin effect:
    - long tail in the step response of the cable
    - part of the signal is delayed and does not contribute
  - Increase of resistance of the cables
    - noise source distributed along the cable
- Impedance for a 12m cable at 2-3 MHz < f < 1 GHz
  - Zd=1/jCw: |Z| oscillates between 2 and 200 Ω
  - Zd= Rd : |Z| oscillates between 25 and 100 Ω
- Calculated and simulated skin effect generated noise offer more precision than the approximation with a lumped resistor at preamp input
- Noise calculations are valid for f >> f_{corner} = 18.4 kHz
- **Calculated and simulated noise due to skin effect is low enough**

II. Input stage: active line termination

- Electronically cooled termination required:
  - 50 Ohm resistor noise is too high
  - e. g. ATLAS LAr (discrete component)
- Common gate with double voltage feedback
  - Inner loop to reduce input impedance preserving linearity and with low noise
  - Outer loop to control the input impedance accurately

$$Z_i \approx \frac{1/g_{m1}}{G} + R_{C1}\frac{R_1}{R_1+R_2}$$

- Transimpedance gain is given by R_{C1}
- Noise is < 0.5 nV/sqrt(Hz)
  - Small value for R1 and R2
  - Large gm1 and gm2
- Need ASIC for LHCb
  - 32 ch / board: room and complexity

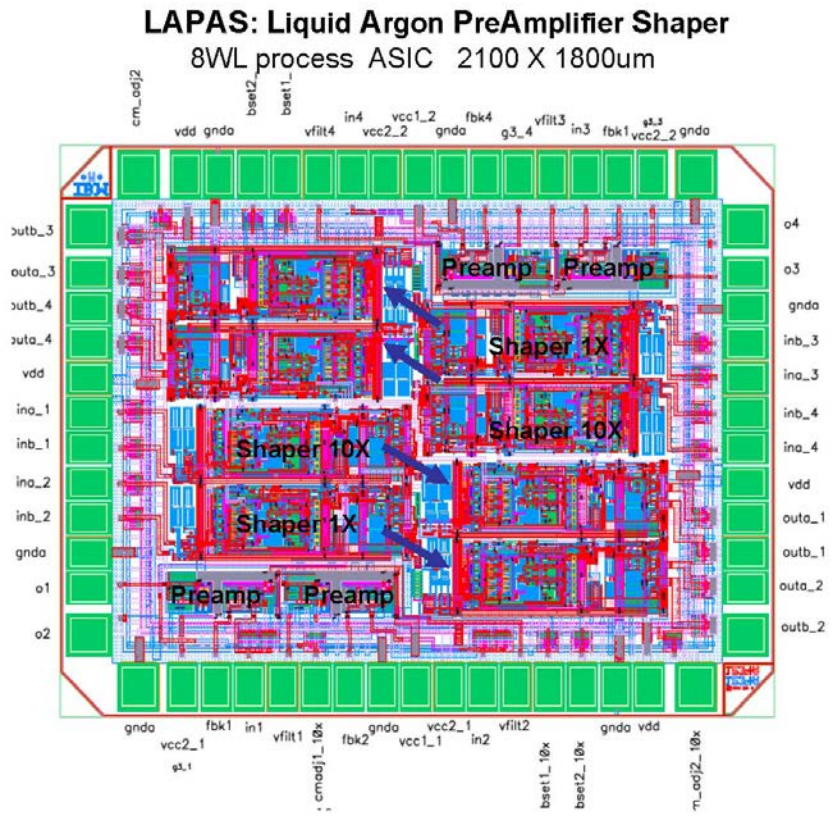


II. Input stage : LAPAS chip for ATLAS LAr upgrade

- TWEPP 09

LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter

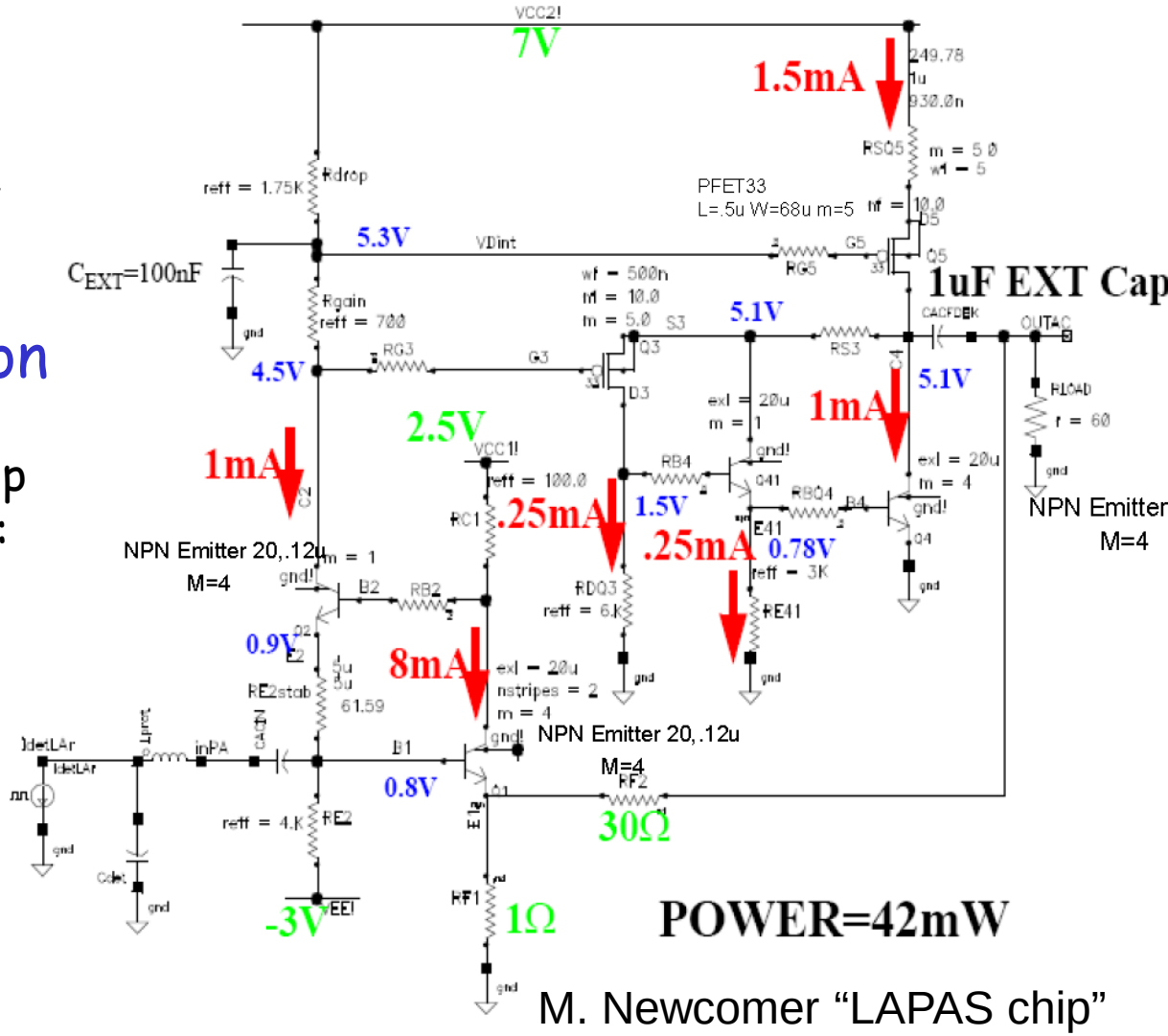
Mitch Newcomer
On Behalf of the ATLAS LAr Calorimeter Group*



Special Acknowledgment of the significant contributions of Emerson Vernon, Sergio Rescia (BNL) and Nandor Dressnandt (Penn) to this work.

II. Input stage: LAPAS chip for ATLAS LAr upgrade

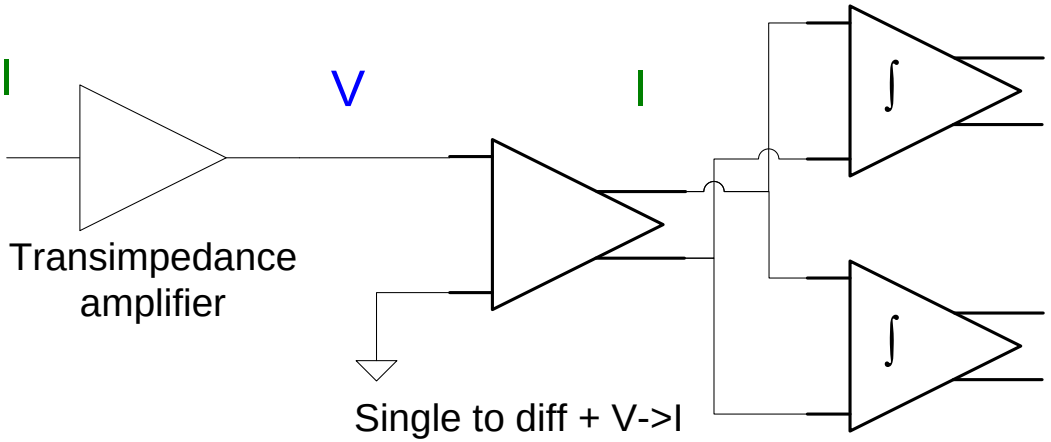
- Technology:
  - IBM 8WL SiGe BiCMOS
  - 130 nm CMOS (CERN's techno)
  - Radiation tolerance:
    - FEE Rad Tolerance TID~ 300Krad,
    - Neutron Fluence ~10^{13} n/cm^2
- Circuit is "direct" translation
  - Need external 1 uF AC coupling capacitor for outer feedback loop
  - Three pads per channel required:
    - Input
    - Two for AC coupling capacitor
  - Voltage output



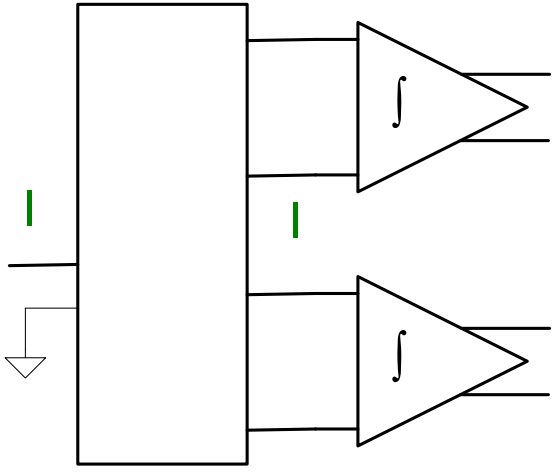
M. Newcomer "LAPAS chip"

I. Introduction: voltage output versus current output

- Voltage output:
  - Pros:
    - Tested
  - Cons:
    - I (PMT) -> V and V -> I (integrate)
    - Larger supply voltage required
    - External components
    - 2 additional pads per channel

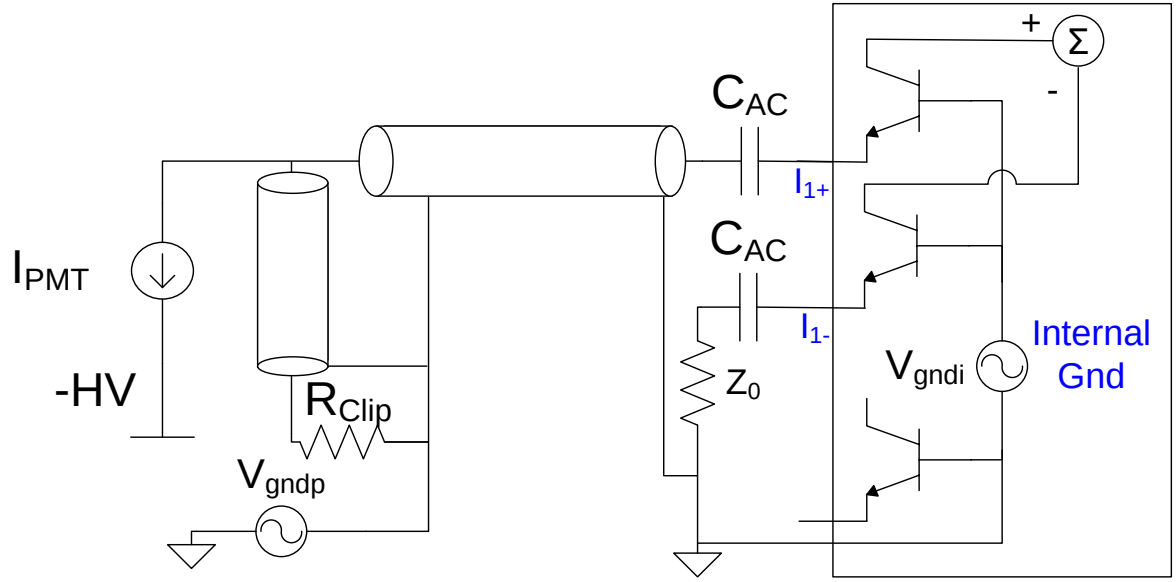


- Current output ("à la PS")
  - Pros:
    - "Natural" current processing
    - Lower supply voltage
    - All low impedance nodes:
      - Pickup rejection
    - No external components
    - No extra pad
  - Cons:
    - Trade-off in current mirrors: linearity vs bandwidth



III. Channel architecture: pseudo-differential input

- Pseudo-differential input attenuates ground (and CM) noise in FE:
  - Mitigates **Vgndi** (connducted) noise (attenuation depends on matching)
  - Symmetrical chip/PCB layout also mitigates capacitive coupling (xtalk, pick-up)



- Drawback: uncorrelated HF noise x √2
  - Predictable and stable effect
- Current mode preamplifier makes easier pseudo differential input:
  - Current: 2 pads per channel
  - Voltage (external component): 6 pads per channel

IV. Technology: choice of technology

- SiGe BiCMOS is preferred:
  - SiGe HBTs have higher gm/Ibias than MOS: less noise, less Zi variation
  - SiGe HBTs have higher ft (>50 GHz): easier to design high GBW amplifiers
- Several technologies available:
  - IBM
  - IHP
  - AMS BiCMOS 0.35 um

	IBM	IHP	AMS
HBT ft	> 100 GHz	190 GHz	60 GHz
CMOS	0.13 um	0.13 um	0.35 um
Proto Cost [€ /mm^2]	> 3 K	> 3 K	1 K

- AMS is preferred
  - Factor 2 or 3 cheaper
  - Too deep submicron CMOS not required / not wanted:
    - Few channels per chip (4 ?)
    - Smaller supply voltage
    - Worst matching
  - Radiation hardness seems to be high enough (to be checked)

IV. Technology: radiation tolerance

- Requirements:
  - Dose in 5 years (TID): 10-20 krad
  - Neutron fluence?
- AMS SiGe BiCMOS 0.35 um should be ok:
  - Omega studies about ILC calorimeters…
  - ATLAS: CNM studies: http://cdsweb.cern.ch/record/1214435/files/ATL-LARG-SLIDE-2009-337.pdf
  - ***CMS: Technology adopted for HCAL upgrade (QIE10 chip)***
    - Total radiation dose = 10 krad = 100 Gy
    - Neutron fluence = $10^{13}/cm^2$
    - Charged hadron fluence = $2 \times 10^{10}/cm^2$

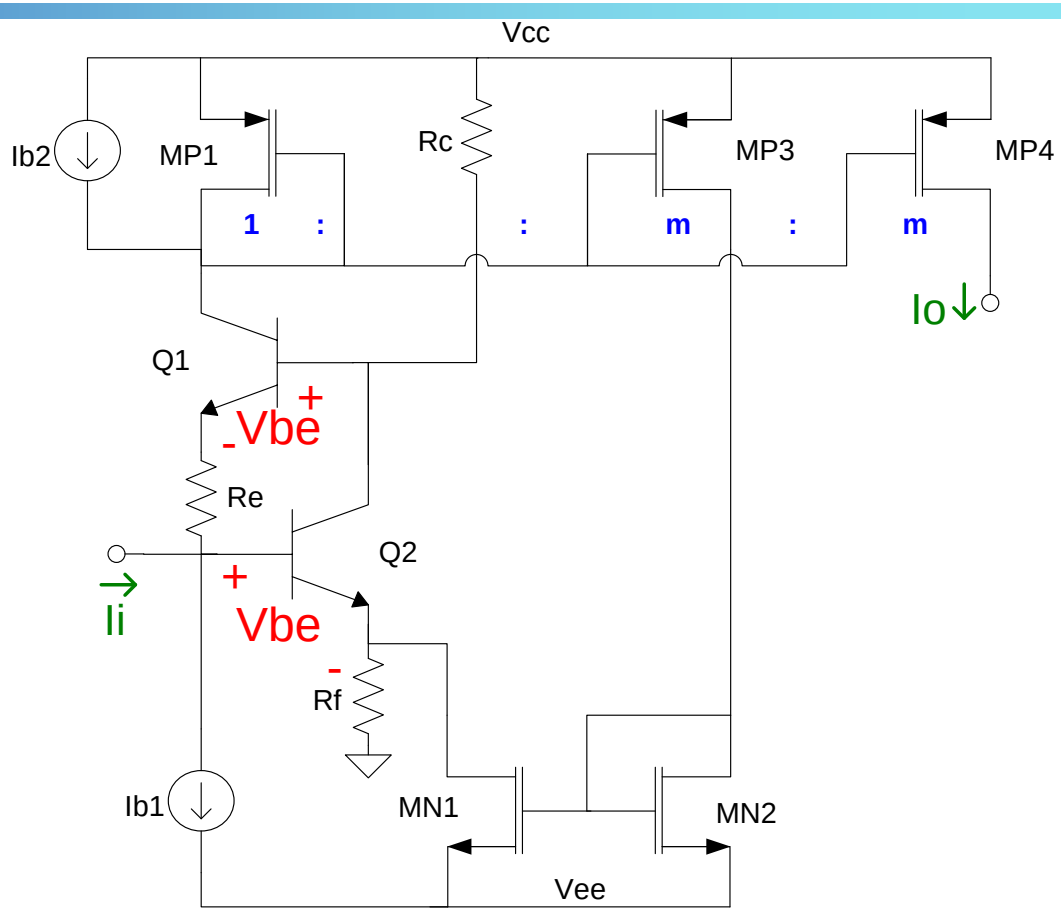
Possible to share efforts on rad qualification? Enginnering run? Cost…

- Radiation tolerance should be taken into account at design:
  - Cumulative effects:
    - Use feedback (global or local): minimal impact of beta degradation
    - Not rely on absolute value of components, use ratios but
  - Transient events:
    - Guard rings for CMOS and substrate contacts: avoid SEL
    - Majority triple voting: SEU hardened logic (if any)

II. Preamplifier: current output / mixed feedback

- Mixed mode feedback:
  - Inner loop: lower input impedance
    - Voltage feedback (gain): Q2 and Rc
  - Outer loop: control input impedance
    - Current feedback: mirrors and Rf
- Variation of LAr preamplifier
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_{m1} + \mathrm{Re}}{g_{m2} Rc} + mR_f$$



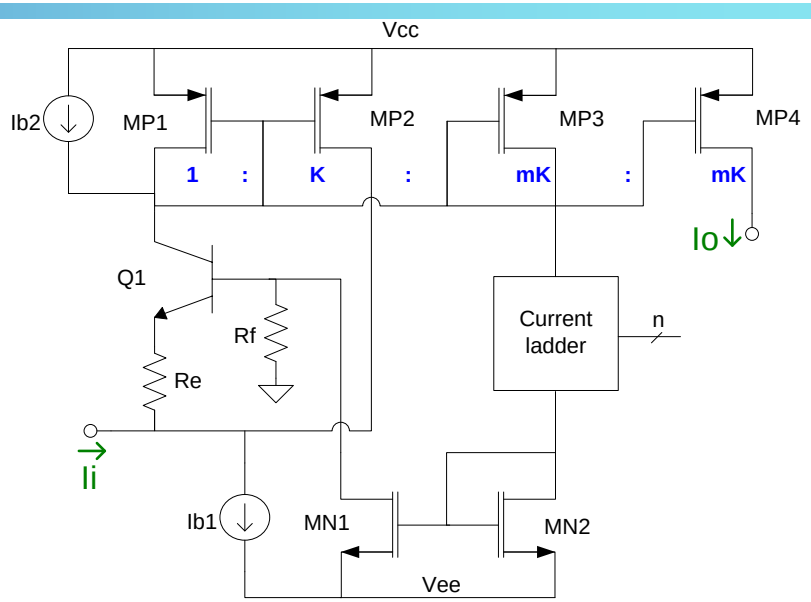
- Problem:
  - Voltage feedback for the super common base needs 2 Vbe (about 1 .5 V !)
  - Small room for current mirrors with 3.3 V
    - Need cascode current mirrors
    - 5 V MOS available: but poor HF performance

IV. Technology issues: effect of process variations

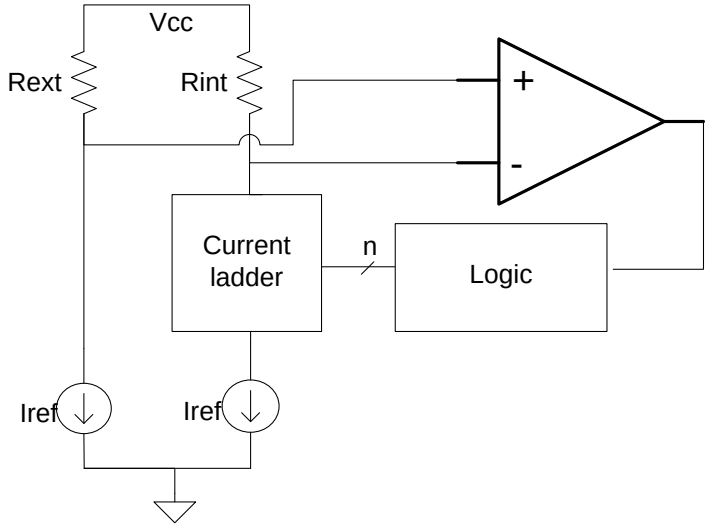
- Input impedance is the key point
- Two types of parameter variation simulated
  - Mismatch between closely placed devices (local variation component to component)
    - No problem: 1 % level
  - Process variation (lot to lot):
    - Problem: 10-30 % level !! (uniform distribution)
      - Pessimistic: experience tell that usually production parameters are close to the typical mean values
- In principle process variation affects whole production (1 run)
  - Could be compensated with an external resistor in series / parallel with the input
- Variation wafer-to-wafer or among distant chips in the same wafer:
  - Can not be simulated
  - Higher than mismatch and lower than process variation
  - According to previous experience: 2-3 % sigma: BUT NO WARRANTY
- Should we foresee a way to compensate it?
  - Group (2-3) chips and:
    - Different pcb (2 – 3 different external resistor values
    - Tune a circuit parameter
  - Automatic tunning

IV. Technology issues: effect of process variations

- Input impedance controllable by:
  - Tune feedback resistor Rf
    - Difficult: small value (Ron of the switch)
  - Tune second feedback current
    - Binary weighted ladder (3 bits?): simple



- How control current ladder control?
  - Group ASICs a fix the value, set by:
    - External jumper
    - Slow control: dig interface required
  - Automatic tunning
    - Reference voltage
      - Reference currents: external or band gap
      - External resistor
    - Wilkinson or SAR ADC style logic



Test set-up