PACIFIC: SiPM Readout ASIC for LHCb Upgrade

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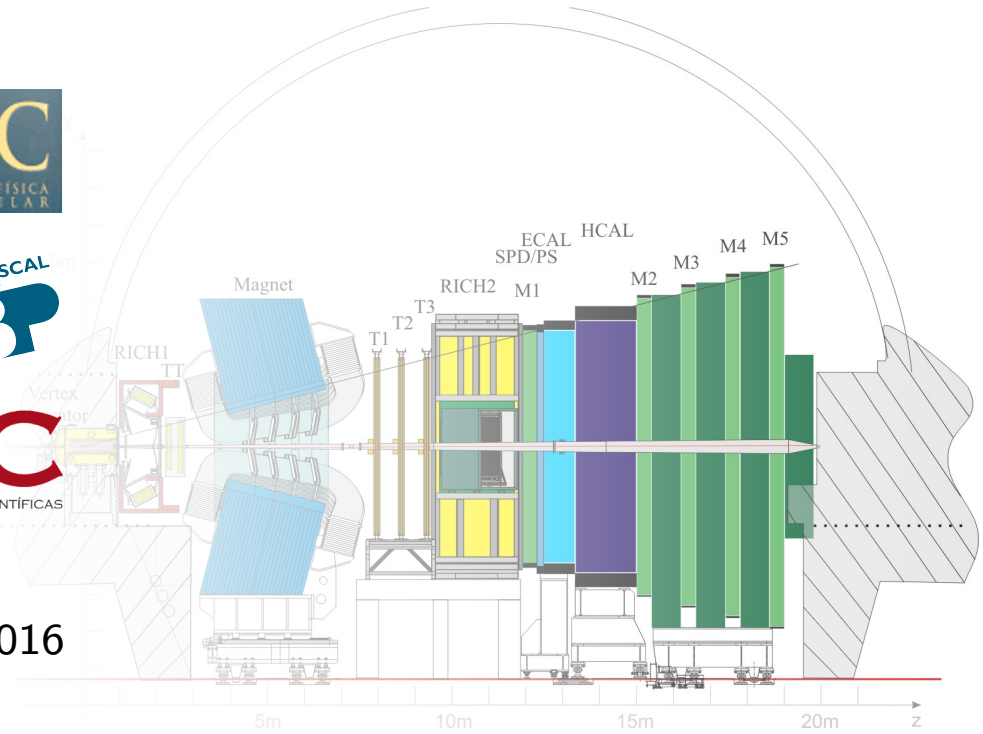

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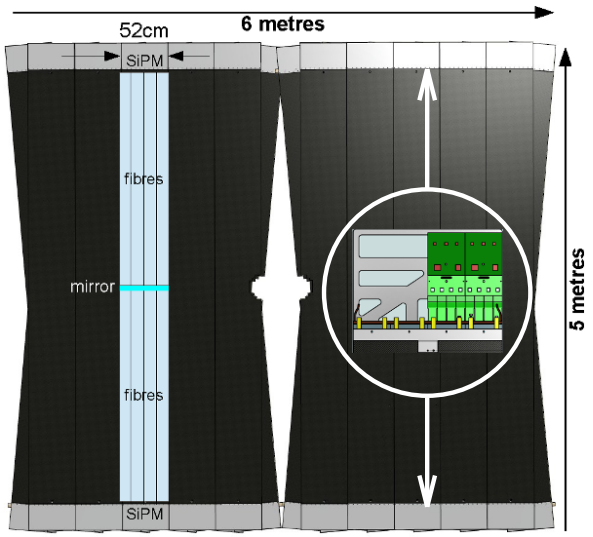
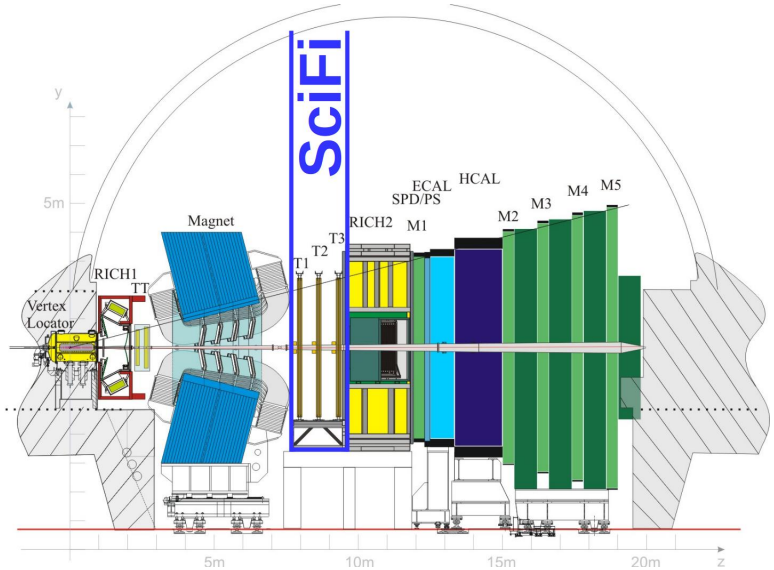
Outline

Introduction: LHCb

- Physics measurements limited by 1 MHz hardware trigger.
- Upgrade: increased luminosity, 40 MHz trigger at front-end.
- New detector for T1-T3 the Scintillating Fibre Tracker.

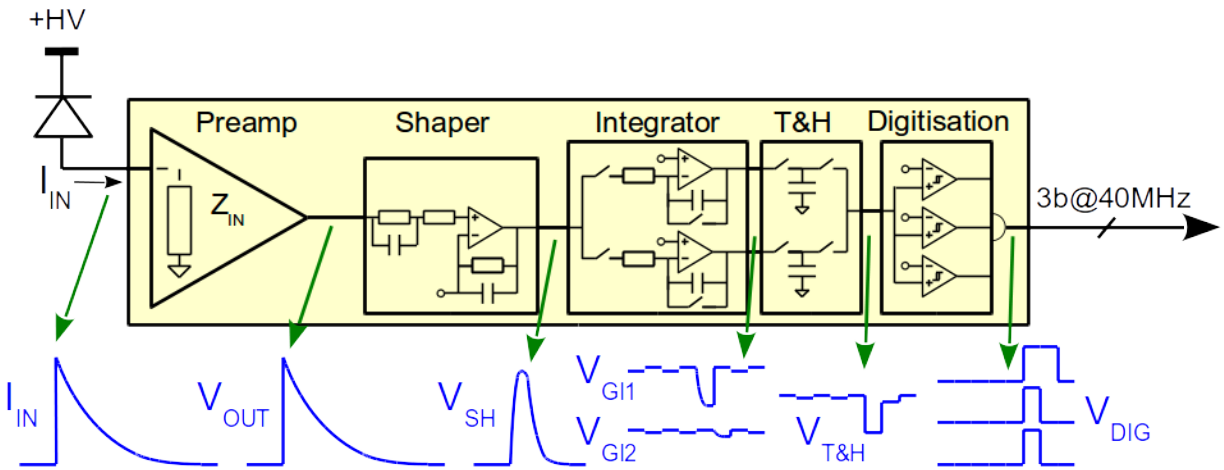




- 3 stations x 4 planes (x-u-v-x).
- 12 modules per plane.
- 6 layer fibre mats (mirrored).
- 8x2.5 m mats per module.
- 2 ROB (top/bottom) with 16 SiPMs and FE electronics.

PACIFIC

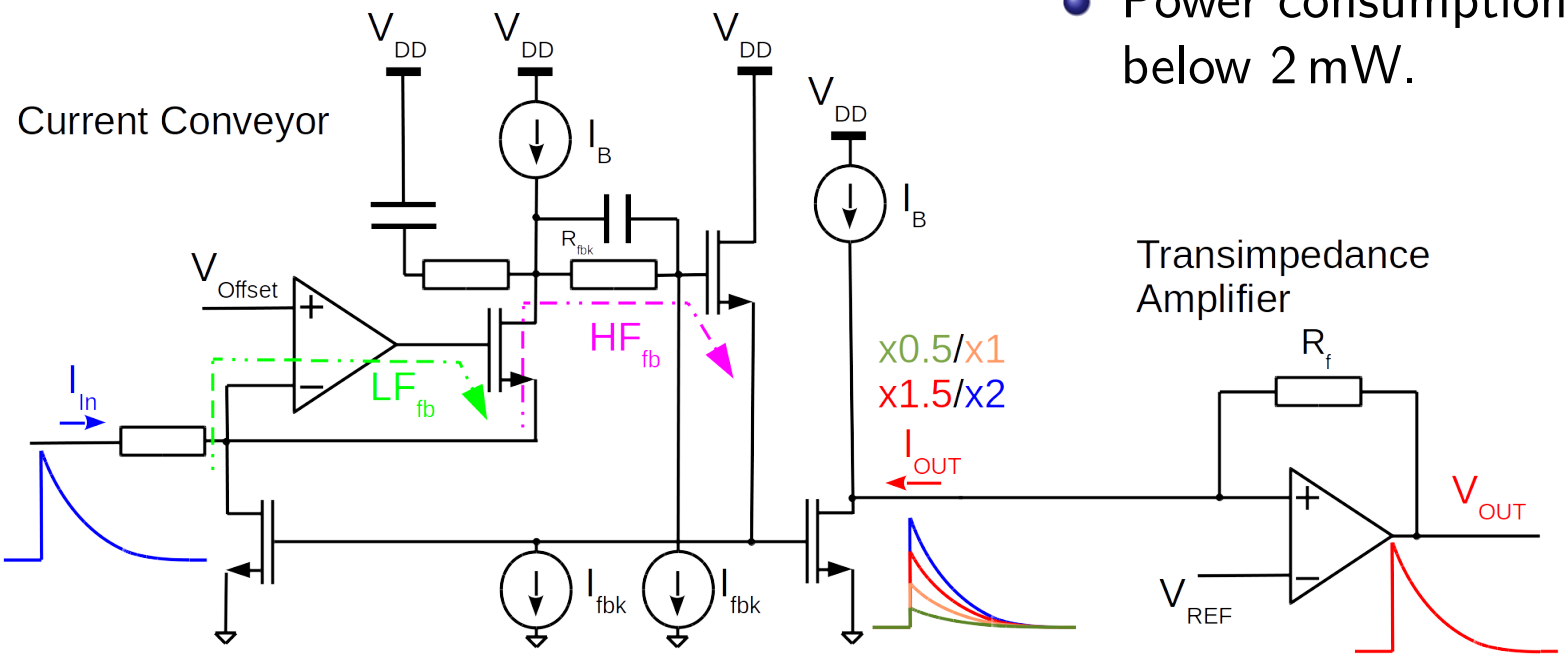
- Readout with 64 channel in CMOS 130 nm (IBM→TSMC).
- Current mode input for direct anode connection.
- Configurable non-linear digital output serialized.
- Fast shaping to minimize spillover.
- Signal integration to overcome low photostatistics using dual interleaved system to avoid dead time.
- Single photoelectron detection capability.



PACIFIC: Preamplifier

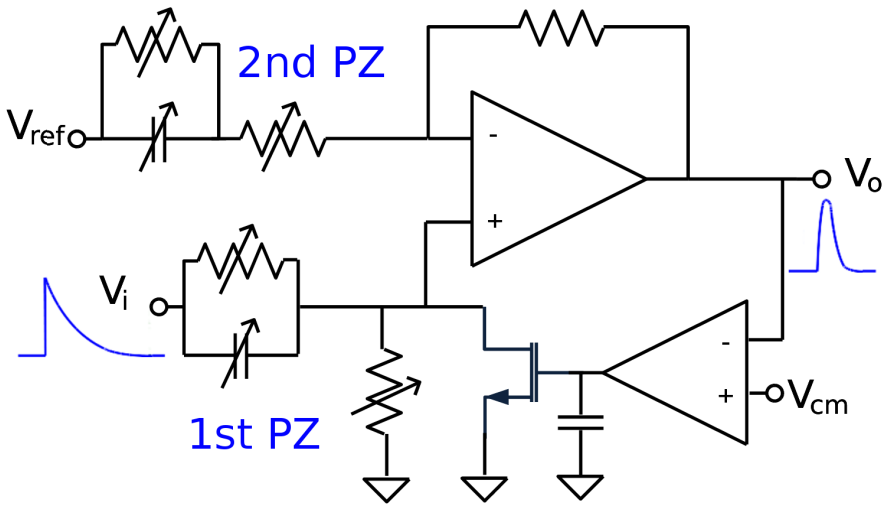
- Double feedback current conveyor:
  - Fix input voltage and impedance.
  - Selectable gains at output mirror.
- Transimpedance amplifier:
  - Current to voltage conversion.
  - Control conveyor output voltage.

- Bandwidth 250 MHz.
- Input impedance 50 Ω.
- Input voltage control range 700 mV.
- Input dynamic range 4 µA-4 mA.
- Power consumption below 2 mW.



PACIFIC: Shaper

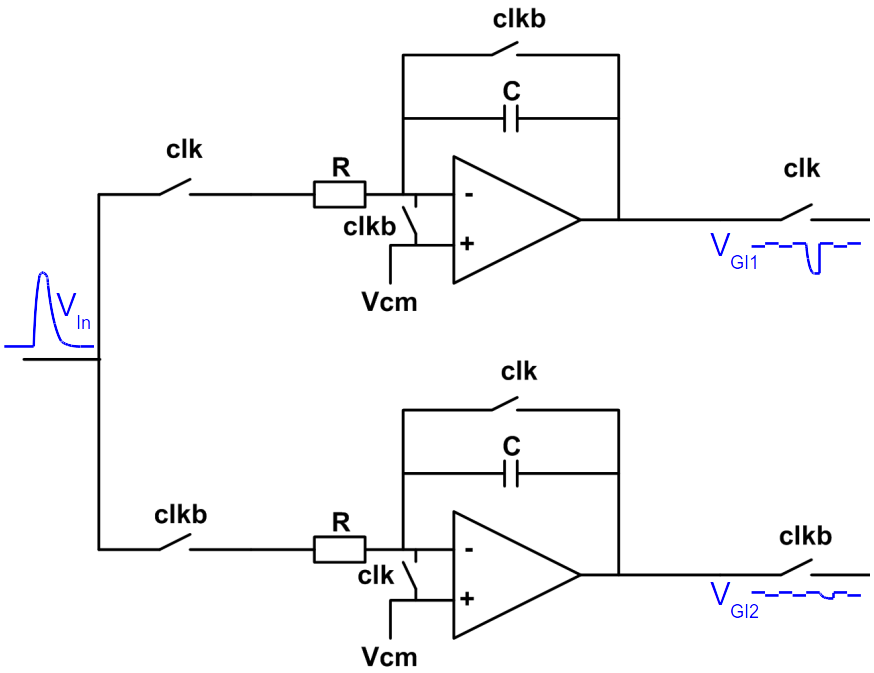
- Double pole-zero cancellation scheme for fast shaping (10 ns).
- Closed-loop OTA circuit with two configurable passive nets:
  - First pole-zero net cancels slow component (SiPM capacitance and quenching resistor).
  - Second pole-zero net cancels fast component (trace parasitics and input impedance).
- A DC feedback loop controls the quiescent output voltage (critical for the subsequent integration).



Double PZ Shaper

PACIFIC: Integrator

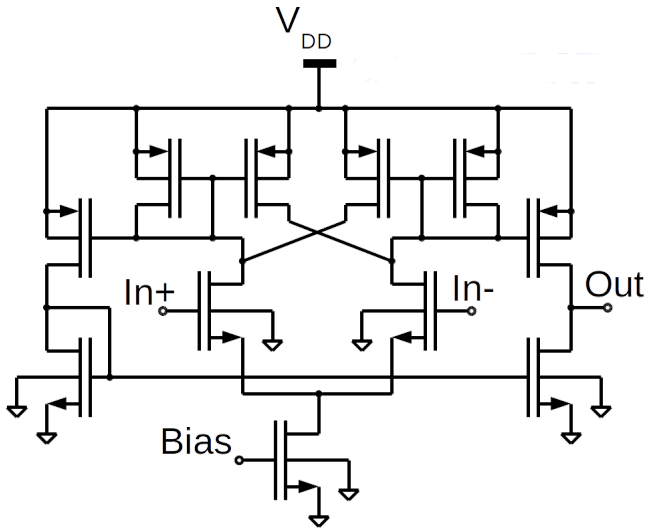
- Classic closed-loop gated integrator architecture based on a Miller OTA with increased slew rate.
- Dead times avoided by using two interleaved units with independent offset trimming circuits.
- Synchronization with the digitizer is mandatory.



Dual Gated Integrator

PACIFIC: Digitizer

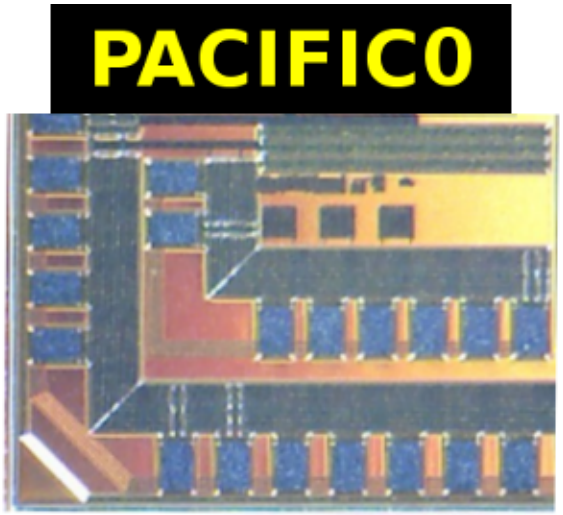
- Dual passive track and hold merges the two subchannels.
- Flash ADC using three comparator with:
  - Dynamic range: 20-850 mV.
  - Hysteresis: 10 mV.
- Three independent references, configurable per channel, with:
  - Dynamic range: 0-750 mV.
  - Resolution: 8 bits.



Hysteresis Comparator

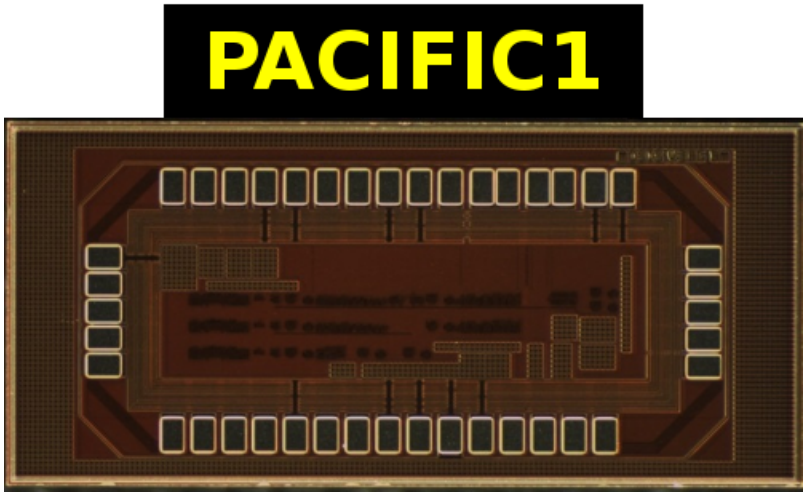
- The output of two channels is fed to a serializer that:
  - encodes the three comparator outputs into 2 bits.
  - streams out both values at 160 MHz.

PACIFICr0 and PACIFICr1



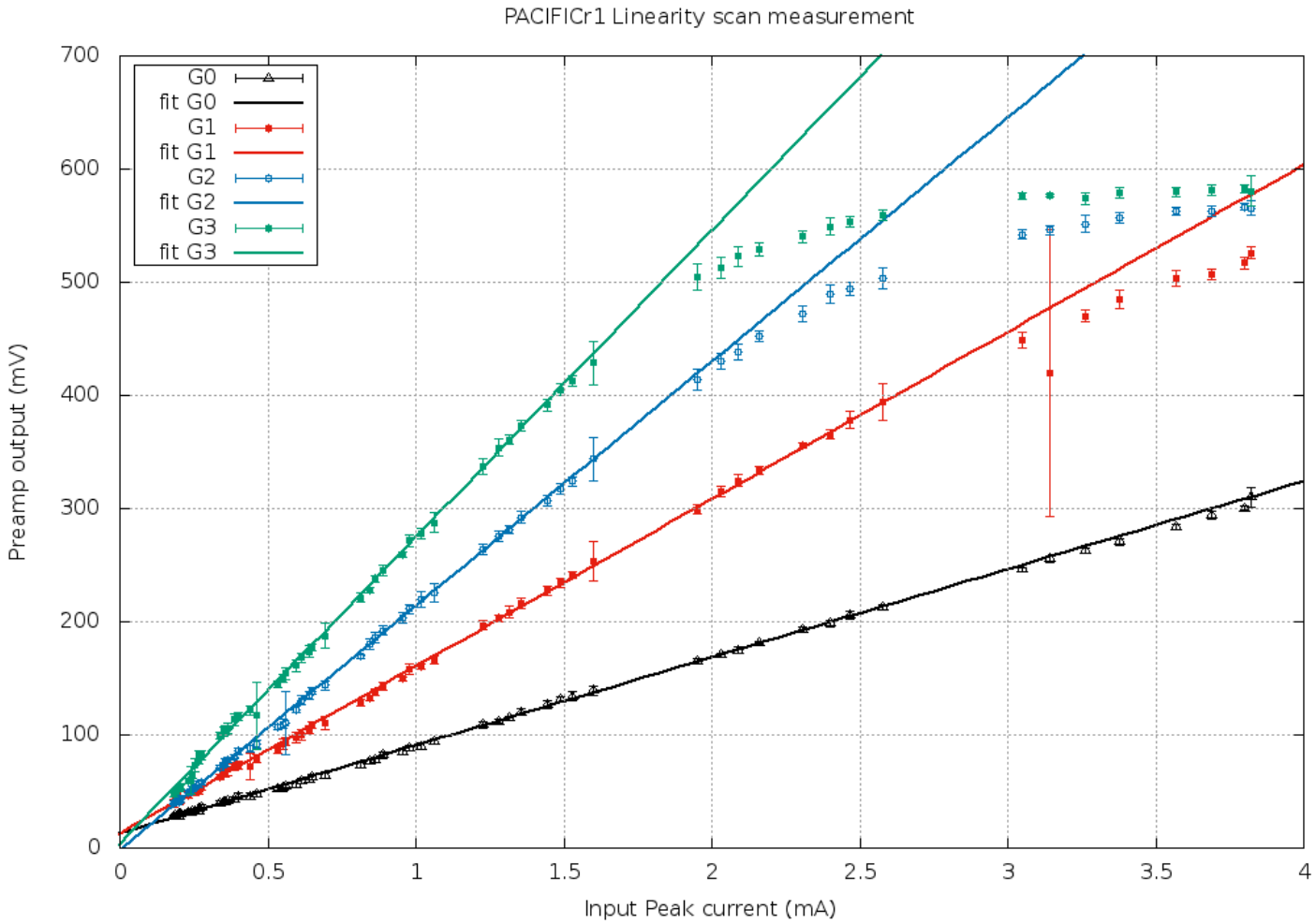
- PACIFICr0:
  - May 2013.
  - IBM 130 nm.
  - Fix gain current conveyor.
  - Design migration from AMS 350 nm BiCMOS.

- PACIFICr1:
  - November 2013.
  - IBM 130 nm.
  - One analog FE plus test blocks.
  - Analog external bias.
  - Independent GI output.



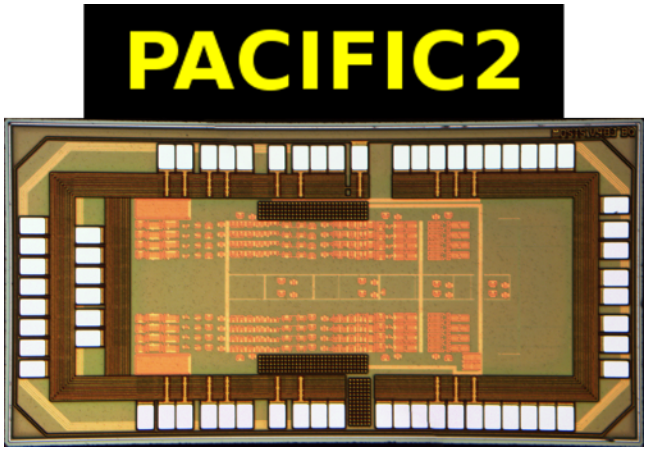
PACIFICr1: Linearity

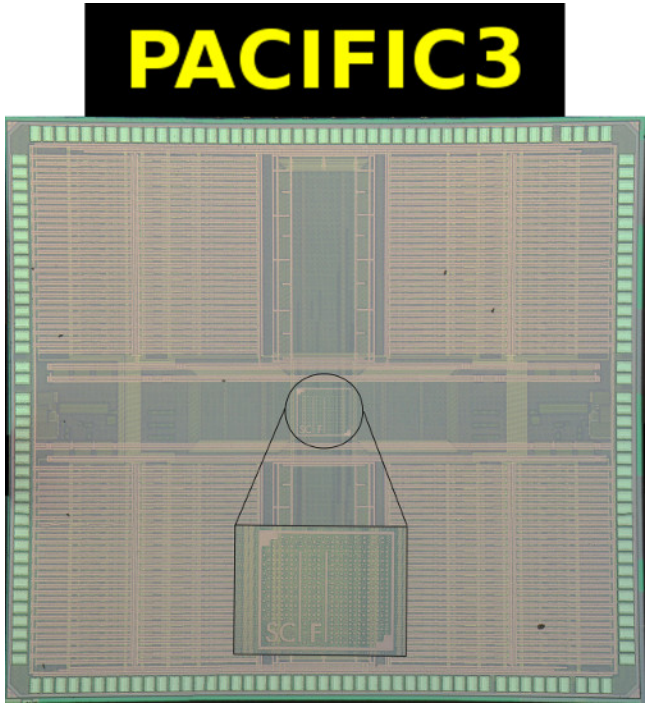
- Good Preamplifier linearity over full designed dynamic range.



PACIFICr2 and PACIFICr3

- PACIFICr2:
  - August 2014.
  - IBM 130 nm.
  - Eight full FE channels.
  - Internal biasing and I2C digital configuration.

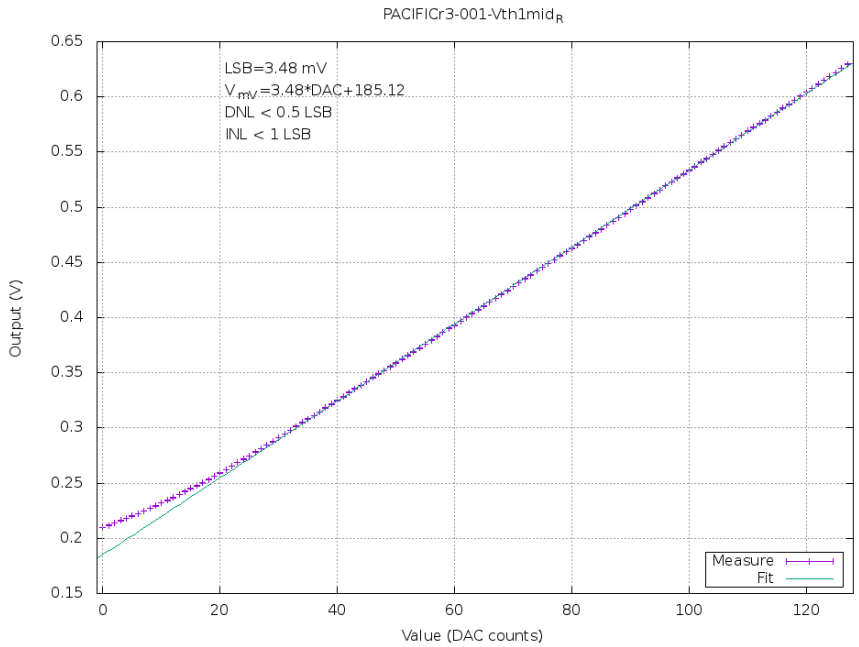


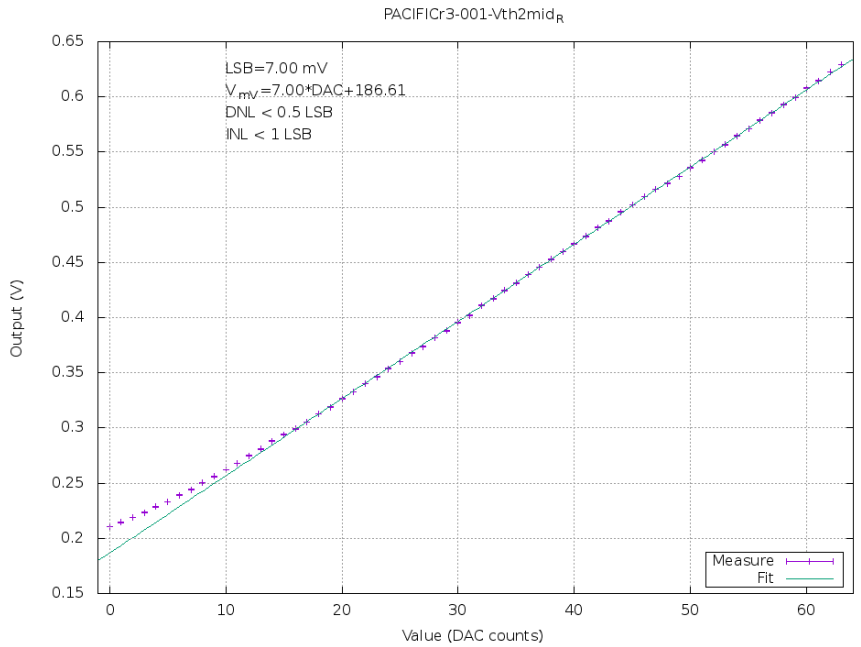


- PACIFICr3:
  - July 2015.
  - TSMC 130 nm.
  - First full size prototype.
  - Separate bias left/right.

PACIFICr3: Power and Bias

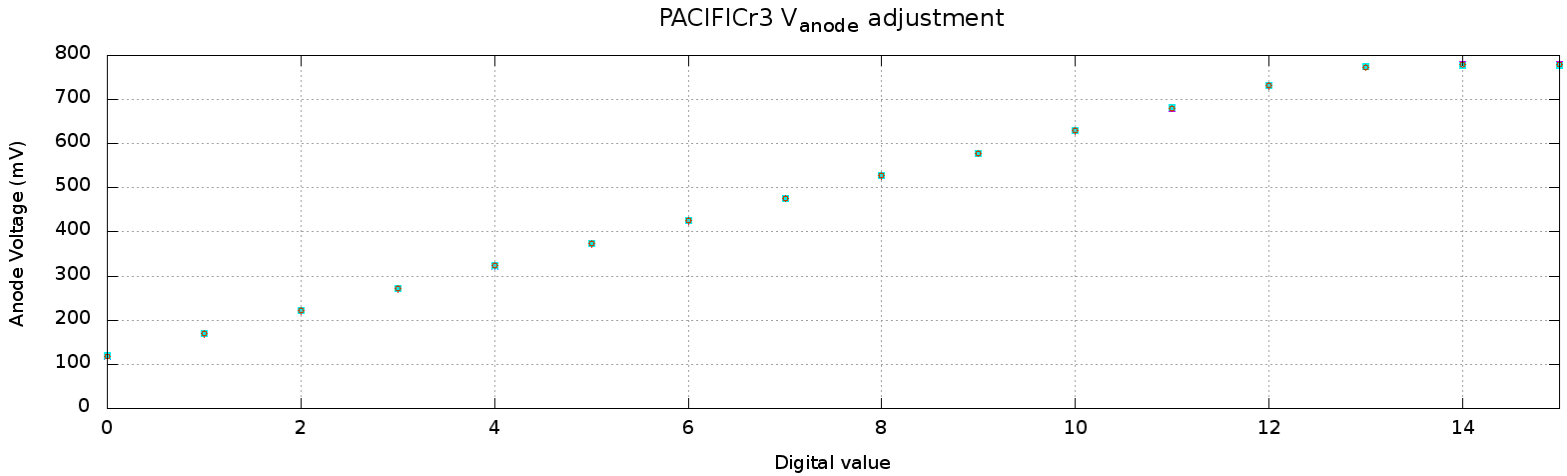
- Power consumption **10.4 mW/ch**, within specifications.
- Bandgap and derived reference voltages slightly low.
- All reference voltage use the same DAC design (6 bit) except the threshold of the first comparator (7 bit).
- Reasonably linear response in all measured instances.

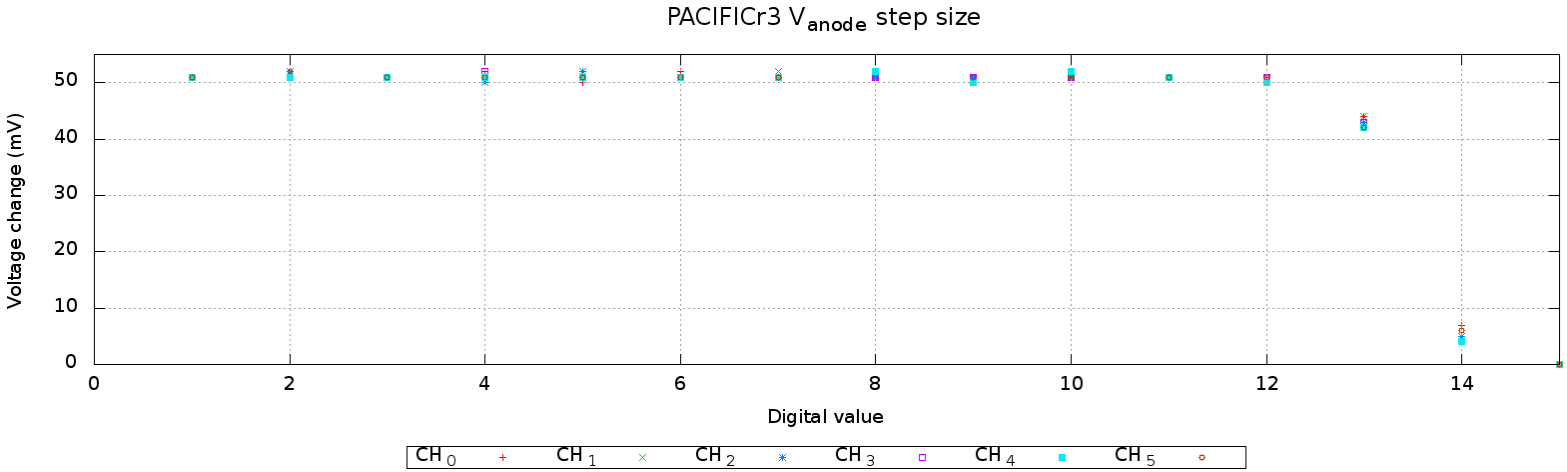




PACIFICr3: Input Voltage

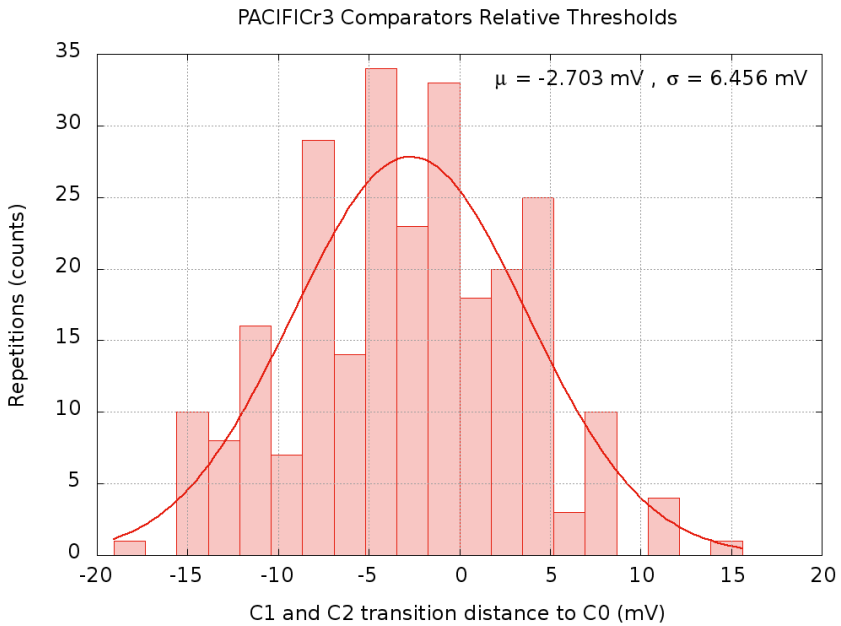
- Derived from a resistor ladder with 16 possible values.
- Range (700 mV) and step (50 mV) as simulated.

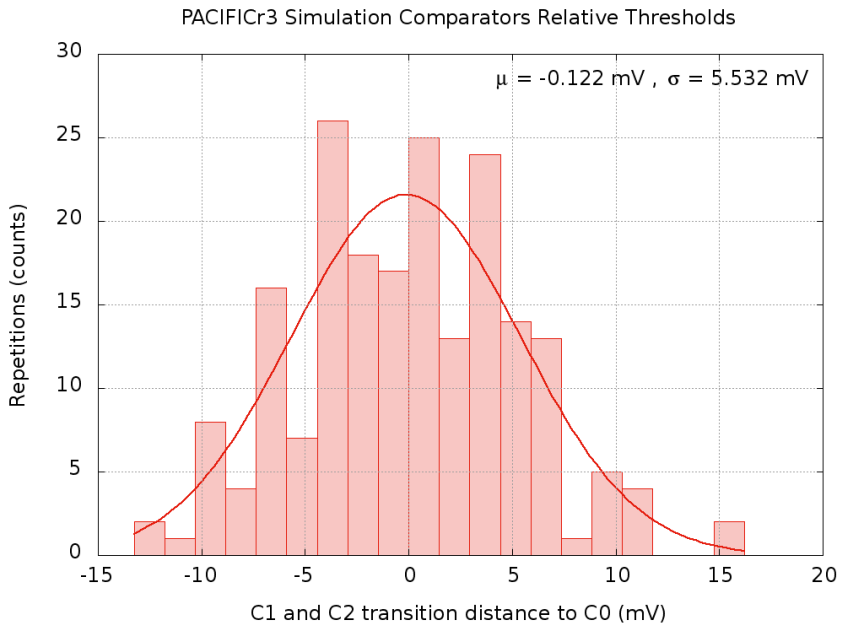




PACIFICr3: Comparator Mismatch

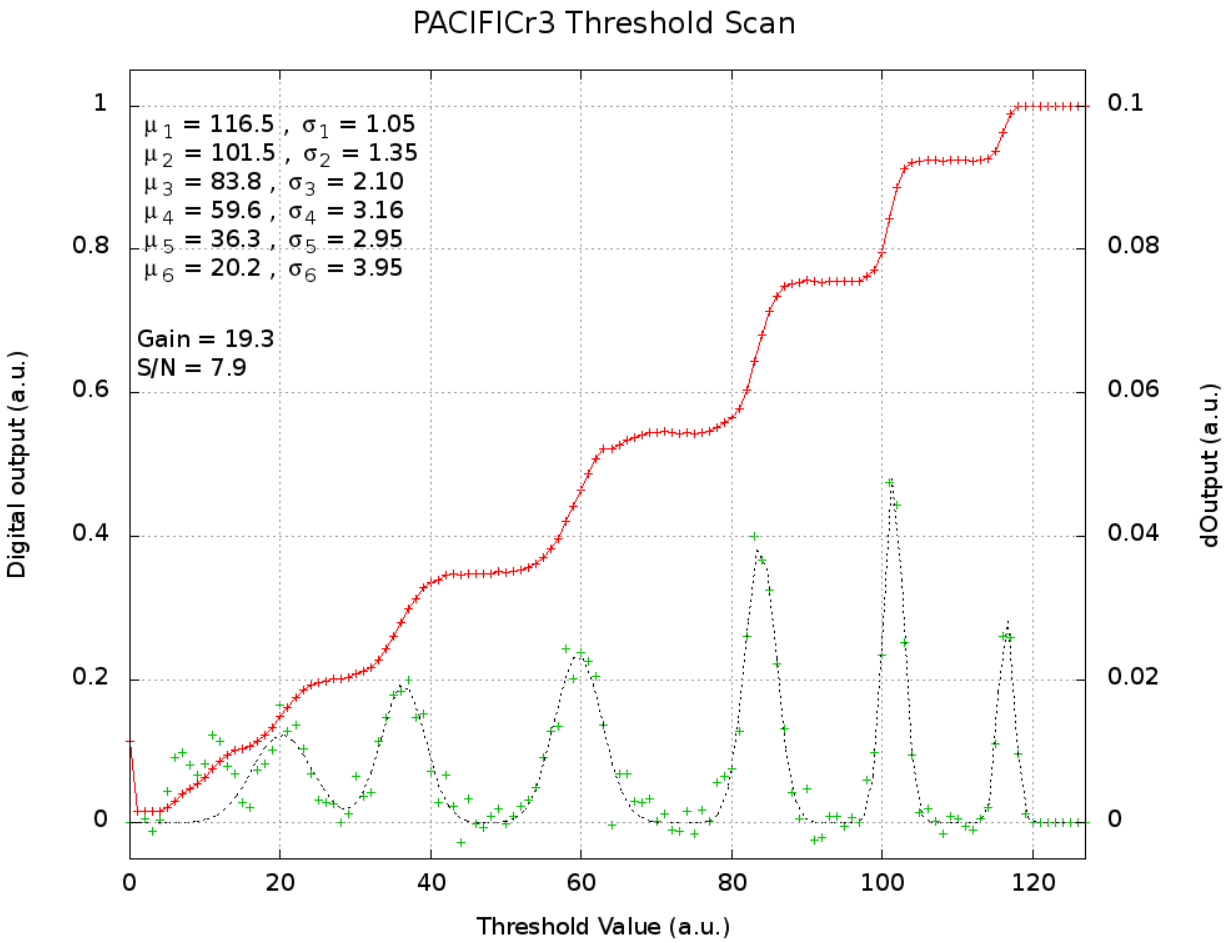
- Comparator offset voltage obtained using threshold scan.
- Calculated difference to the first comparator offset voltage.
- All channels in two chips evaluated, 256 instances in total.
- Measured 20 % increase w.r.t. Monte Carlo simulations.





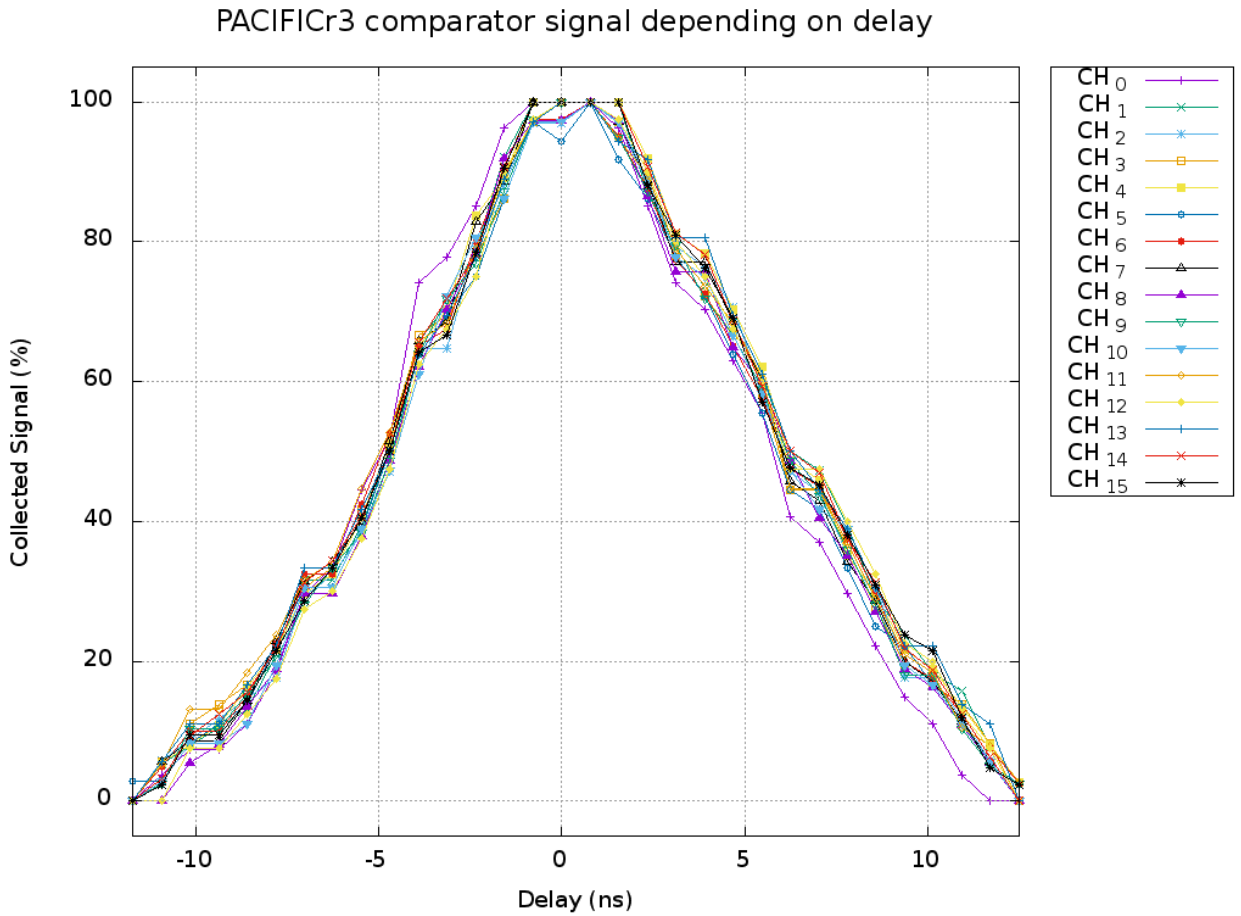
PACIFICr3: Synchronous Light Input

- Picosecond diode laser synchronously pulsed on SiPM.
- Distinct photoelectron structures are noticeable.



PACIFICr3: Delayed Charge Input

- Internal charge injection triggered externally.
- Output sorted by trigger to clock phase difference.
- Response limited by integrator slew rate.



Outlook

- PACIFIC is a SiPM readout ASIC with:
  - Current input for direct anode connection.
  - Fast PZ cancellation shaping for tail suppression.
  - Gated integrator damps statistical fluctuations.
  - Non-linear configurable 2 bit digital output.
- Channel architecture has been fully validated.
- New prototype PACIFICr4 is in production with:
  - Increased slew rate in integrator amplifier.
  - Expanded comparator transistor size a factor three, in addition threshold DACs per channel included.
  - Custom digital output pads with higher driving power.
- Production readiness review planned for Q2 2017.

Thanks a lot for your attention!