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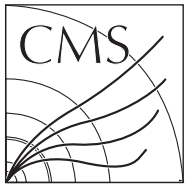

The Compact Muon Solenoid Experiment

Conference Report

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Phase 1 upgrade of the CMS forward hadronic calorimeter

Daniel Noonan for the CMS Collaboration

Abstract

The CMS experiment at the Large Hadron Collider at CERN is upgrading the photo- detection and readout system of the forward hadronic calorimeter. The phase 1 upgrade of the CMS forward calorimeter requires the replacement of the current photomultiplier tubes, as well as the installation of a new front-end readout system. The new photomultiplier tubes contain a thinner window as well as multi-anode readout. The front-end electronics will use the QIE10 ASIC which combines signal digitization with timing information. The major components of the upgrade as well as the current status are described in this paper.

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Phase 1 Upgrade of the CMS Forward Hadronic Calorimeter

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Abstract: The CMS experiment at the Large Hadron Collider at CERN is upgrading the photo-detection and readout system of the forward hadronic calorimeter. The phase 1 upgrade of the CMS forward calorimeter requires the replacement of the current photomultiplier tubes, as well as the installation of a new front-end readout system. The new photomultiplier tubes contain a thinner window as well as multi-anode readout. The front-end electronics will use the QIE10 ASIC which combines signal digitization with timing information. The major components of the upgrade as well as the current status are described in this paper.

Keywords: CMS, Calorimeter, Front-end electronics, QIE

Contents

1 Introduction

The Compact Muon Solenoid (CMS) [1] is a general purpose detector operating at the CERN Large Hadron Collider (LHC). The forward hadronic calorimeter (HF) is designed to measure hadronic energy from jets in a pseudorapidity range of $3 < |\eta| < 5$. The HF calorimeter is a Cherenkov calorimeter comprised of a steel absorber through which quartz fibers are run to collect the Cherenkov light. The light from the quartz fibers is then sent to photomultiplier tubes (PMTs), from which an electric signal is produces that is read out and digitized by the front-end electronics.

During operation of CMS during Run 1, anomalous signals were observed in HF caused by muons or particle showers interacting in the PMTs. These produce large signals, which are increasingly difficult to reject in higher luminosity running conditions. In order to reduce these signals and provide a more robust method of rejection of these anomalous signals, the phase 1 upgrade of the HF calorimeter has been undertaken [2]. The upgrade involves two main aspects. The first is the replacement of the current phototubes with a multi-anode version which has a thinner window. The second portion of the upgrade is the replacement of the front-end electronics responsible for the readout. The replacement of the PMTs occurred in 2013 and 2014 during the long shutdown of the LHC. The upgrade of the front-end electronics is planned for installation during the extended year end technical stop at the end of 2016 and beginning of 2017.

This paper discusses the upgrade of the CMS HF calorimeter. Section 2 describes the upgrade of the PMTs used on the detector. Sections 3 and 4 describe the new front-end electronics and the testing and qualification process, respectively. The results of the readout of a pilot system, installed on the detector during the 2016 data taking are described in section 5.

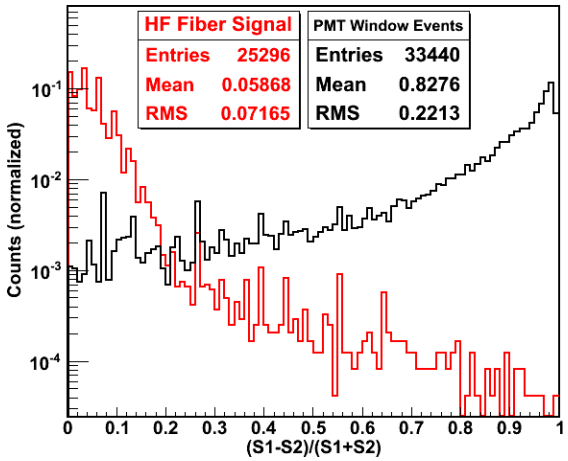

Figure 1. Distribution of asymmetry parameter for signals from HF fibers and PMT window events [2].

2 Upgrade of the photomultiplier tubes

The upgrade of the photomultiplier tubes involves the replacement of the current Hamamatsu R7525 phototubes with Hamamatsu R7600U-200-M4 quad-anode PMTs. In order to reduce the number of readout channels required while still gaining the benefits of having multiple anodes per PMT, the PMTs will be readout through two channels instead of four. This is accomplished by reading out pairs of adjacent anodes on a PMT through a single channel, so that the four anodes of each PMT are split between two readout channels.

The upgraded PMTs provide two main advantages in the reduction of the anomalous signals. First, the new phototubes have thinner optical windows, which reduces the interaction rate of incident particles. Second, the multiple readout channels of the phototubes can be used to reject the anomalous hits. Anomalous signals caused by interactions of particles within the PMT are more likely to cause a signal on one anode than are signals from light in from the quartz fibers of HF. This will lead to an asymmetric signal between the outputs of the PMT anodes. Figure 1 shows the distribution of the asymmetry parameter for the signals from HF fibers and PMT window events, observed in testbeam data. The asymmetry parameter is calculated as (S1-S2)/(S1+S2), where S1 and S2 are the outputs from the two signals of a PMT, ordered with S1>S2.

3 Upgrade to the front-end electronics

The multiple readout channels of the PMTs will double the number of output channels on the detectors. This requires an upgrade of the front-end electronics in order to be able to read out the additional channels.

The central component of the front-end electronics is the Charge Integrator and Encoder (QIE10) ASIC [3, 4]. The QIE10 is designed to integrate and digitize the signal pulses coming from the PMTs. It contains an analog-to-digital converter (ADC) for digitizing the pulse heights and

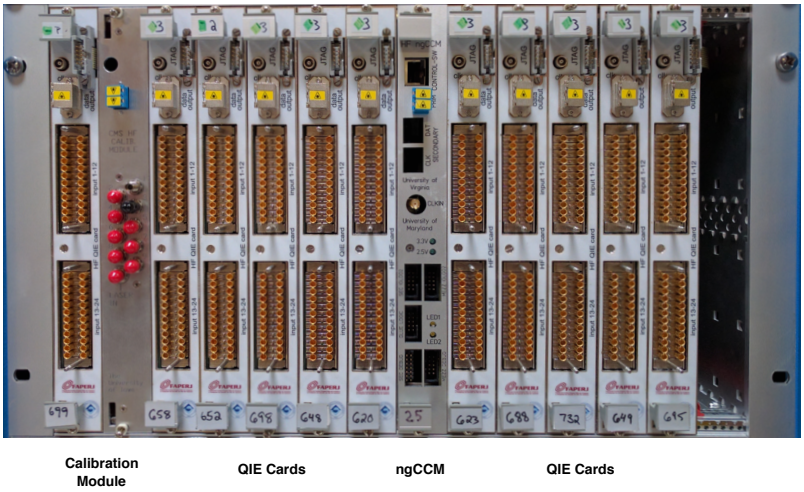

Figure 2. Photo of a front-end crate, containing a calibration module, ngCCM, and QIE cards.

a time-to-digital converter (TDC) for measuring the arrival time of the pulse. The 8-bit ADC of the QIE10 operates in a pseudo-logarithmic fashion, allowing it to cover a 17-bit dynamic range. The ADC is split between four integration ranges. Within each range, the pseudo-logarithmic response is implemented by a periodic doubling of the width of the ADC bins. The ADC can integrate charges up to approximately 350 pC, with a precision of 3 fC at the low end of the dynamic range. In order to provide dead-timeless operation, the QIE10 contains four sets of integrating capacitors and comparator circuits, referred to as the capID, which are rotated through so that as one capacitor is integrating another is being digitized and another is being reset. The 6-bit TDC of the QIE10 provides the ability to measure the arrival time of pulses with a sensitivity of 0.5 ns.

The upgrade to the front-end electronics contains three main components: the QIE card (which contains the QIE10 ASICs), the next-generation clock and control module (ngCCM), and the calibration module. The QIE card contains 24 QIE10 chips, with each chip providing the readout for an individual PMT output channel (two anodes from one PMT). A total of 144 QIE cards are required for the readout of the upgraded HF detector. The ngCCM is responsible for distributing the clock and all control commands to QIE cards in a front-end crate. The calibration module allows for injecting a narrow LED pulse into the PMTs, for testing the response of the PMT and readout a with controlled signal. Figure 2 shows the configuration of a typical front-end crate, containing a calibration module, an ngCCM, and numerous QIE cards.

4 Testing and qualification of the new front-end electronics

Nearly 200 QIE cards have been produced for the HF upgrade, in order to provide the 144 card needed for installation as well as sufficient spares. All cards undergo a thorough testing and qualification process, checking the performance of each channel before installation. Testing of the QIE cards is underway in preparation for the installation to occur at the beginning of 2017.

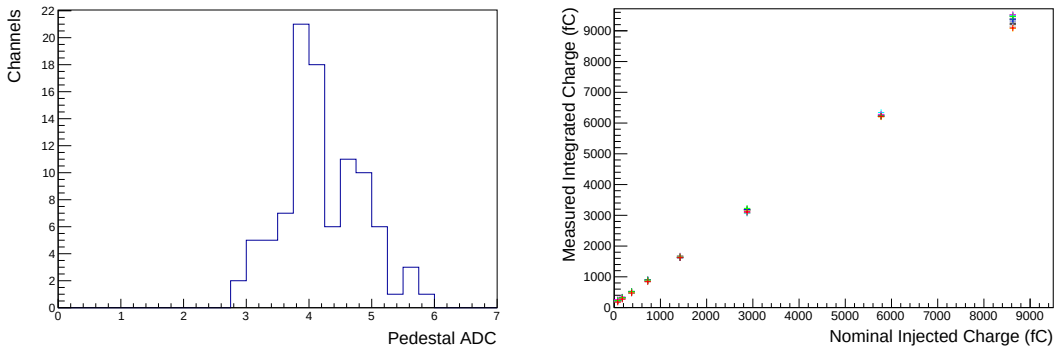

Figure 3. Results for pedestal and internal charge injection tests for an individual QIE card. The left plot shows the distribution of pedestals for all 24 QIE10 channels on a QIE card. The right plot shows the result of the internal charge injection, comparing the nominally expected charge with the measured charge for each of the eight internal charge injection levels. The different colors in the right plot represent the data points from each of the 24 different QIE channels on the QIE card.

The first level of tests measures the performance of the QIE10 chips without an external signal. The first test each card is put through is a measurement of the pedestal level, defined as the measured ADC value of the QIE10 when no input signal is present. The pedestal level is measured separately for each capID. The measured pedestal value is compared to the expected value of 4 ± 2 ADC, and a good pedestal value is good first indication that a channel is 'alive' and there are no significant problems with the QIE10 or the surrounding circuit. Additionally, the QIE10 has the ability to internally inject a pulse of charge into the integration circuits by means of charging and discharging a capacitor located on the chip itself. The internal charge injection is controlled by a 3-bit register, allowing charge to be injected at 8 different levels. This feature is used to perform a first test of the functionality of the both integrator and the TDC timing. Figure 3 shows on the left the distribution of the pedestals for all QIE chips on one card and on the right the comparison between the nominally expected and measured charges at the different internal charge injection levels.

For cards that pass the pedestal and internal charge injection tests, further tests involving injecting pulses from the PMTs are conducted. The calibration module is used for injecting a light pulse from an LED into the PMTs, and the output pulse is measured by the QIE card. The injection of the pulse from the PMT allows for testing the QIE card with the full chain of the readout, measuring signals of the same type as will be seen in the final installation. It is also the first time that the QIE's are tested with externally injected signals, potentially revealing any problems in the inputs of individual QIE channels.

The final step in the qualification process is a calibration of the QIE10 ADC response to different amounts of charge. The calibration of the QIE10 is essential for an accurate reconstruction of the measured data after installation. By injecting a precisely known amount DC current into the QIE10, we can measure the ADC output which corresponds with a specific amount of charge. The DC current is integrated by the QIE10 in 25 ns windows, providing an injection of a specific amount of charge. By varying DC current, the ADC response of the QIE10 to different amounts of charge can be measured over the full dynamic range.

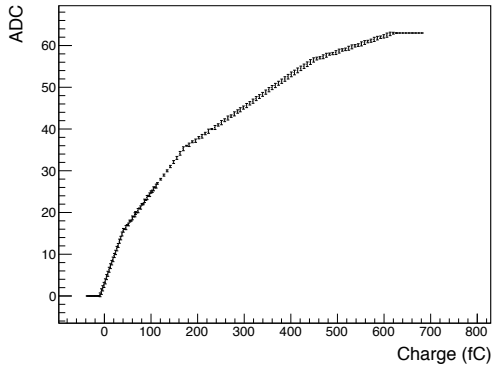

Figure 4. Distribution of the QIE10 ADC output value as a function of the injected charge. The bin width doubling of the ADC is visible in the change of the slope at distinct points in the distribution.

To carry out the calibration, a DC external charge injection board was built. The external charge injector is controlled by a 16-bit DAC, and allows for injecting a precisely known amount of DC current at a large range of values. In each of the four ranges and for each of the four capIDs, the external charge injector was used to measure the ADC value at dozens of points. Figure 4 shows the distributions of the measured ADC value as a function of the injected charge for the lowest range of the QIE10. The doubling of the ADC bin width, responsible for the pseudo-logarithmic behavior of the QIE10, is evident in this distribution by the kinks in the slope of the distribution. In order to provide the calibration conditions necessary for reconstructing future data, the ADC response of the QIE can be linearized to remove these kinks in the slope. The distribution of the injected charge versus the linearized ADC value can then be fit to provide a slope and offset parameter which define the conversion from charge to ADC for the specific QIE channel. The calibration is performed separately for each of the four capIDs and for each of the four ranges. Figure 5 shows the distribution of the linearized ADC as a function of injected charge for a single capID of a QIE chip for all four ranges.

5 Pilot system during 2016 data taking

In order to extensively test and gain experience with the operation of the new front-end electronics, a pilot system was installed on the detector during the 2016 data taking period. The pilot system consisted of two QIE cards, reading out 26 channels from the HF detector. In 22 of these channels, the signal came from one half of the output of a PMT, while the other output channel was sent to the legacy readout system. The remaining four channels represent the outputs of both halves of two PMTs. The channels from PMTs split between the upgrade and legacy readouts allow for comparisons between the new readout and the previous and well understood legacy system. The two PMTs in which both channels are readout by the upgraded front-end electronics allow for testing of the means of rejecting anomalous signals from particles interacting directly with the PMT. An example of this is measuring the difference between the arrival time of signals from interaction in the HF detector and the signals from PMT hits.

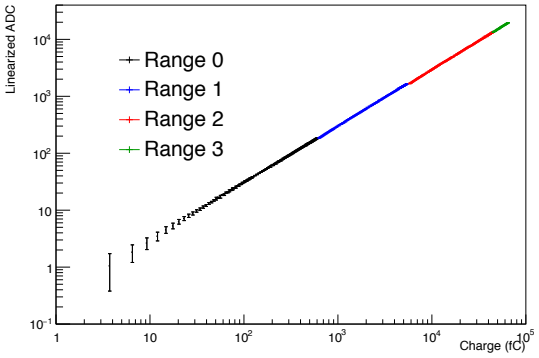

Figure 5. Distribution of the linearized ADC value as a function of the injected charge for all 4 ranges for a single capID of a QIE chip. Fitting the distributions of each of the ranges provides the calibration conditions necessary for the reconstruction of data in the future.

Muons or other particles that cause anomalous signals by interacting in the PMTs travel at near the speed of light between the interaction point and the PMTs. Signals from particles producing Cherenkov light in the HF detector have a longer time of flight, due to the index of refraction of the quartz fibers which channel the light from the detector to the PMTs. This difference in arrival time between real and anomalous signals can be used to discriminate between the two types of signals. Figure 6 shows the distribution of the reconstructed charge and TDC values observed in collision data. The TDC value represents the arrival time with respect to the beginning of the integration window of the leading edge of the pulse in half nanosecond increments (ex: a TDC value of 25 represents a signal arriving 12.5 ns into the integration window). The red line in the figure shows a potential discriminant requirement for removing anomalous signals. Signals to the left of this line are arriving earlier than the main pulse, from interactions in the HF detector, and are likely anomalous signals which can be rejected.

6 Summary

The phase 1 upgrade of the CMS HF calorimeter will provide an improvement in the rejection of anomalous signals. New PMTs with thinner windows reduce the probability of interaction of incident particles. The new front-end electronics featuring the QIE10 ASIC will improve the ability of to reject such signal which do occur.

In this paper, the components of the new front-end electronics for the phase 1 upgrade and the status of the testing of the electronics have been described. The central component of the new front-end electronics, the QIE cards, undergo thorough testing and commissioning before installation. The testing of the electronics will be completed in the coming months, in preparation for installation during the extended year end technical stop at the end of 2016 and beginning of 2017.

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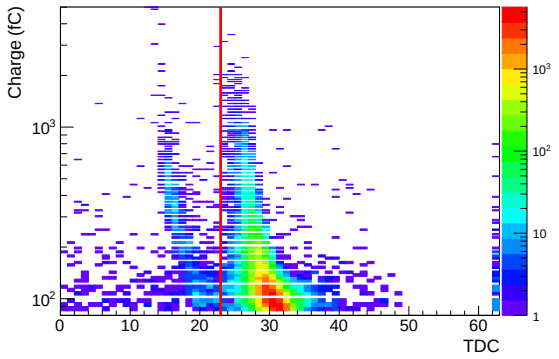

Figure 6. Distribution of the TDC value and reconstructed charge for signals reconstructed in the QIE10 pilot system. The vertical red line shows a timing threshold to discriminate between anomalous and real signals. Signals to the left of the line arrive earlier than the main pulse, and are likely coming from anomalous signals.

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