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This work investigates the current sharing effect of a high power Soft Punch Through IGBT module in the Negative Temperature Coefficient region. The unbalanced current sharing between two of the substrates is demonstrated for different current and temperature levels and its impact on the thermal stressing of the device is evaluated. The results indicate that the current asymmetry does not lead to a significant thermal stressing unbalance between the substrates.

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This work investigates the current sharing effect of a high power Soft Punch Through IGBT module in the Negative Temperature Coefficient region. The unbalanced current sharing between two of the substrates is demonstrated for different current and temperature levels and its impact on the thermal stressing of the device is evaluated. The results indicate that the current asymmetry does not lead to a significant thermal stressing unbalance between the substrates.

Introduction

The experiments at the European Organization for Nuclear Physics (CERN) create the need for the control of the electric power supplied to the particle accelerators via power electronic converters in a wide range of power levels, from the kilowatt up to the megawatt level. In the design phase of the power electronic converters, the priority is given to the reliability with an expected lifetime of at least twenty years. With the thermal stressing being a crucial factor for aging, performance degradation and, eventually, failure of the converters, it is clear that the correct thermal modelling, lifetime estimation and overall thermal design is of utmost importance.

The power cycling application leads to a thermal cycling with a significant temperature swing that accelerates the power modules aging [1]. Therefore, the power ratings of the power modules must be enhanced by increasing the silicon area per chip and limit the temperature rise. As a result, the IGBT module may operate at a current level not above 25% of its nominal ratings [2].

Previous works have demonstrated the current sharing at currents close to the nominal ratings of the power module both at steady state [3], [4] as well as at the switching dynamics [5], [6], [7]. In these cases, the uneven current sharing was a result of the temperature unbalance among the substrates due the cooling system, of the deviation at the characteristics of the chips or of an asymmetry at power module or power circuit level. The effect is already evident at high current levels, although the IGBT operates at the Positive Temperature Coefficient (PTC) region, where the device becomes less conductive with the temperature increase. The purpose of this article is to investigate the current sharing at the IGBT substrate level and for different temperature distributions in the substrates, when

the module operates at a constant DC current mode and at the low current region, namely at the Negative Temperature Coefficient (NTC) operation region. At the NTC region the device conductivity is proportional to the temperature. Therefore, a temperature unbalance among the IGBT substrates at steady state, which, in fact, can be caused by the cooling system, the thermal interface material uneven application or different characteristics among the chips, may lead to unsymmetrical current distribution among the semiconductor chips of a module.

Characteristics of the magnet supply application

One of the main applications of electric power converters in the field of nuclear physics research is the accelerators magnet supplies. Figure 1 depicts a typical medium power magnet supply. It, mainly, comprises of an 18kV-to-400V transformer, a diode rectifier, a DC-link capacitor bank, an IGBT-based H-bridge converter for the regulation of the magnet current and a filter stage.

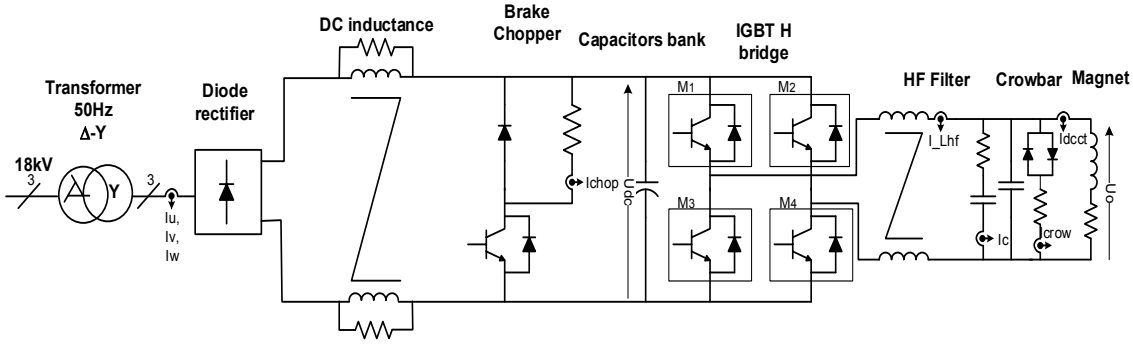


Fig. 1: Typical power circuit of magnet supply

The load current profile of the H-bridge varies depending on the current requirements of the magnet. Different magnet current profiles are shown in Fig. 2. It can be noted that the magnet supply is operating in a power cycling application.

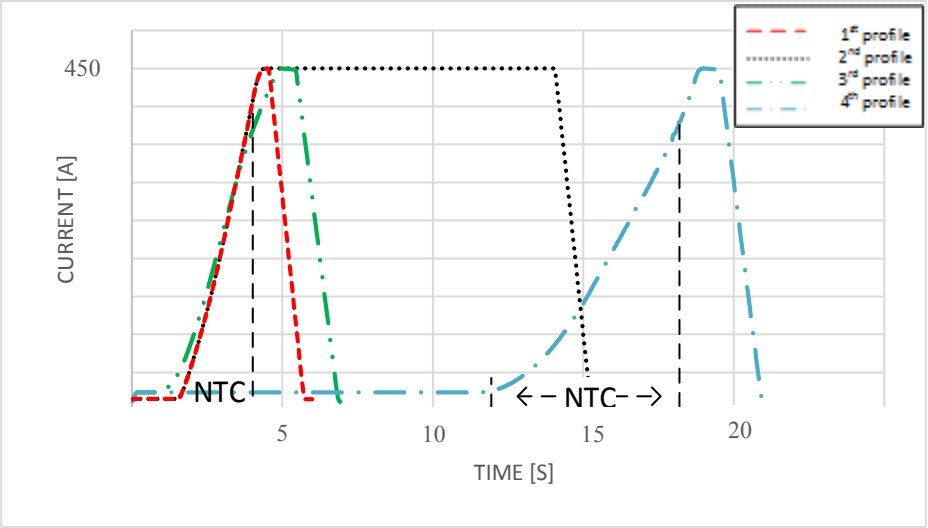


Fig. 2: Different periodical current profiles for the magnet

The flat top current level is defined at 450A but what is really of interest is the pulse duration that can vary resulting in totally different thermal stressing of the power modules. For instance, both the first (green) current profile and the fourth (blue) profile have a very short flat top but the blue has a long period with low current providing sufficient time to allow the power modules to cool down. In all

current profiles and, especially, in the blue profile, the current ramp-up and ramp-down lasts from hundreds of miliseconds up to some seconds during which the current remains in the NTC region of the IGBT for several seconds. During operation, some chips in the module are thermally stressed more than others due to their inherent properties and their location inside the module. Another particularity of the way that the H-bridge is used, is the high loading of the antiparallel diodes of the power modules M_2 and M_3, see Fig 1, due to the inductive load and the current profile.

Relation between conductivity and temperature for the IGBT

The voltage drop of the IGBT at on-state is defined by voltages over the internal PN-junction, over the voltage inversion channel and the internal MOS structure and at the drift region [4], [8], [9]. At low current the voltage drop is, mainly, caused by the PN-junction. The voltage drop goes down linearly with increasing temperature and is almost independent of the current value. This is the NTC operation region of the device, see Fig. 3.

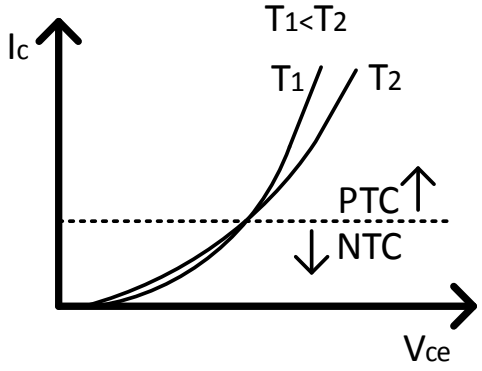


Fig. 3: NTC and PTC region in relation between the collector current versus saturation voltage

At higher currents, the drift region and the inversion channel are together considered to have a resistive behavior and the voltage drop across them dominates the IGBT collector-emitter voltage. The IGBT V_{ce}voltage is expressed as

$$V_{ce} = V_{ce,o}(T) + r_o(T, i_c)i_c \quad (1)$$

where V_{ce} is the saturation voltage drop, $V_{ce,o}$ the voltage drop across the PN junction being linearly dependent on temperature T, r_o the equivalent resistance of the drift region and the inversion channel depending on the temperature and the collector current i_c.

For relatively low current levels (up to approximately 400A) the conductivity of the Soft Punch Through (SPT) IGBT single switch that is used in this work [10], increases with the increase of temperature, leading to operation in the NTC region. This is, also, true for the antiparallel diodes for most of the current range of the device.

Method

The general overview of the test bench is illustrated in Fig. 4. The main components used for these series of measurements are listed in Table I.

The IGBT power module that is the Device Under Test (DUT) is depicted in Fig. 5a, b, c. It is painted with a black coating that has a known high emissivity [11] in the temperature range of the application, facilitating the thermal imaging. The difficulty by soldering the IGBT driver output to the Gate-Emitter to connect pads of the module and the need for a mechanically firm solution lead to the construction of a component based on spring probes, see Fig. 5a to ensure the electrical contact with the pads. In this way, the four substrates of the IGBT module, see Fig. 5b, can be controlled independently.

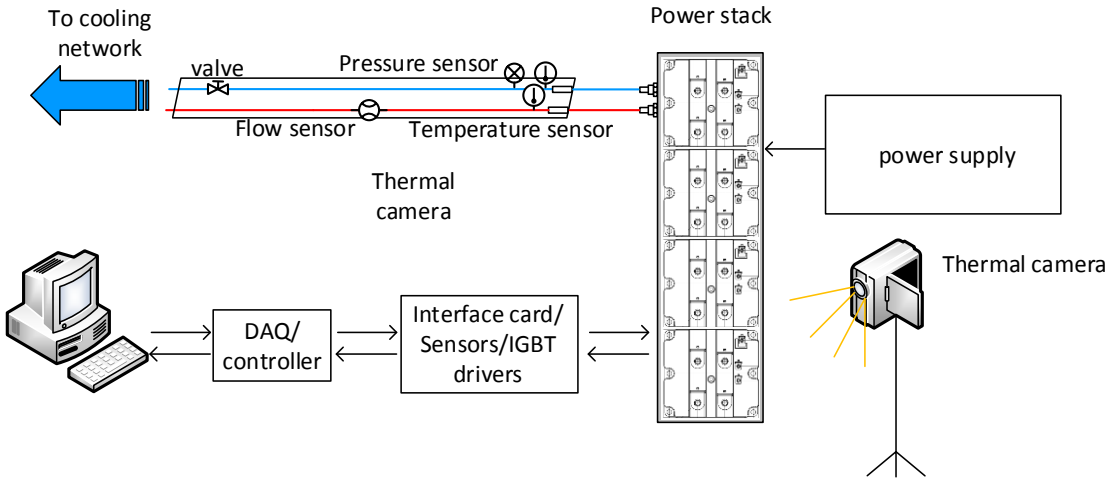
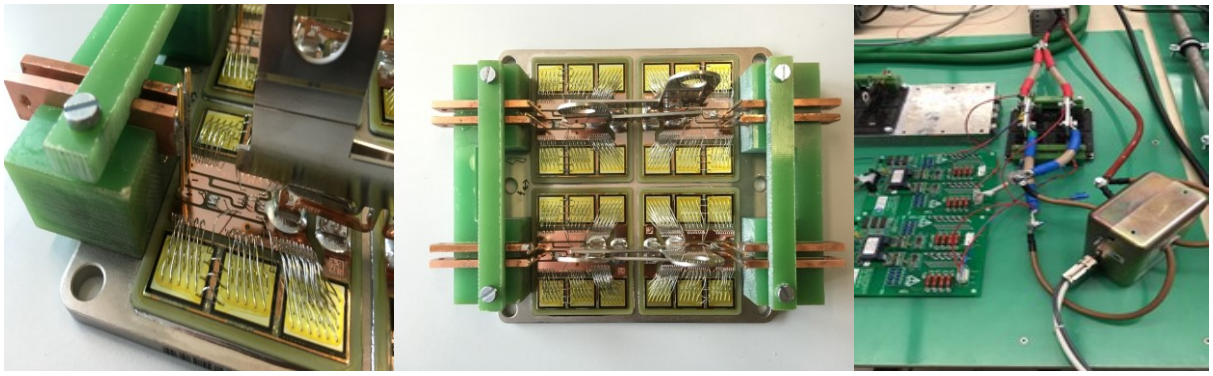


Fig. 4: Test bench for thermal measurements

Table I: Experimental setup main components

Description	Specifications
Power electronic module	open 1600A/1700V SPT ABB 5SNA 1600N170100
Data Acquisition system and controller	32AI (16 bits) / 4 AO / 48 Digital I/O
Power supply	Delta Elektronika-30V / 100A
Thermal camera	Flir T440
Current measuring device	Ritz 120A DC-DCCT /100ppm precision/ 1.2A per 0.1V output



(a) (b) (c)

Fig. 5: a) Spring probes for the electrical contact of the gate driver with the IGBT pads, b) overview of the power module, c) View of the painted power module, the gate driver and the DCCT used for the current measurements

A drawing of the power circuit of the test bench is illustrated in Fig. 6. The experiments are carried out only with the substrates 1 and 3 to measure the current sharing between them for currents up to 50A per substrate and for different temperature distributions.

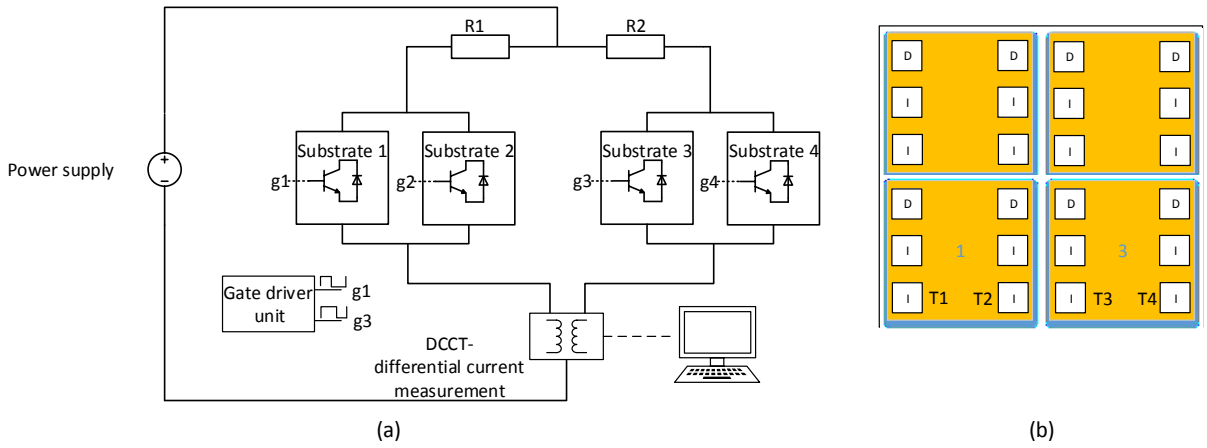


Fig. 6: (a) Power circuit of the set-up, (b) Overview of the four substrates of the IGBT power module

The first step of the experimental procedure was to thermally characterize the power module in a thermal chamber, in order to obtain the relation between the saturation voltage V_{ce} and the temperature at chip junction level T_j for various temperature levels. In this way, it is ensured that there is no significant inherent difference between the substrates.

In order to confirm that the current sharing results from the temperature difference of the substrates, and not from the power circuit unbalance, the module was placed on an insulating surface. With the power supply operated, initially, in current source mode, pulses of various current levels were applied to the DUT with a duration of up to 5 seconds to avoid any temperature unbalance among the chips. The pulse duration is long enough to avoid any current unbalance due to the leakage inductance.

For the second series of experiments, in order to achieve a temperature difference between the two substrates, the power supply is operated as a controlled voltage source and the current is shared between the substrates that are switched at the same switching frequency but at different duty cycle. The module is placed on the insulating surface, in order to be heated up quickly and achieve temperature levels comparable to the actual application. The current difference between the two substrates is measured with a Direct-Current Current Transformer (DCCT) [12] that allows high precision measurements and the temperature on four different chips, two for each substrate, was monitored with the thermal camera.

The DCCTs are, widely used at CERN. Their application started from the accelerators beam current measurement and is extended to the power converters current measurement [13], [14]. They have a current range from 50A to 20kA with a bandwidth reaching a couple of hundred kHz for low currents with a precision down to a few particles per million (ppm). No circuit interruption is needed for their connection. Their principle of operation lies on the residual flux detection between two toroidal-wound ring cores that sense the DC current part of the primary current. A third core detects the AC part of the current. The measured residual flux combined with the AC part are used in a control loop, in order to produce a secondary current that is a fractional image of the measuring-primary current.

The secondary current produces a voltage drop across a burden resistor and this voltage is the output of the DCCT.

Results

Power module thermal characterization

Figure 7 depicts the V_{ce} - T_j relation for three different measurement configurations; one series of measurements for each of the substrates and one for the two substrates operating in parallel. All the measurements are done under a controllable temperature range from 40 to 100 °C and with a sensing current of 1A to avoid the additional heating of the chip. The fact that the lines for substrate 1 and 3 coincide shows that their thermal behavior is almost identical.

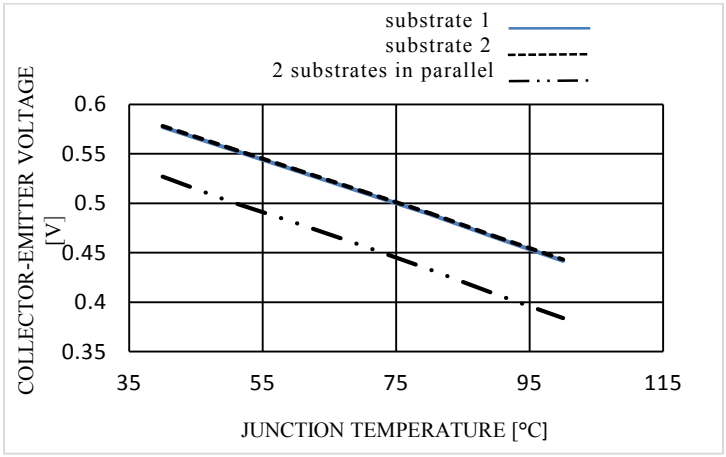


Fig.7: Relation of the saturation voltage versus temperature for two substrates connected in parallel and for each of them separately

Identification of the circuit asymmetry effect

Table II shows the current levels of the pulses and the corresponding current unbalance that was measured, keeping, always, the temperature of the substrates equal. Table II provides the current unbalance for total circuit current levels at multiples of 10. Figure illustrates that the relation of the current unbalance and total current level in the circuit is linear, see Fig. 8. This result implies that there is a constant circuit asymmetry that, as expected, is amplified as the current increases. The current unbalance due to the circuit asymmetry has to be subtracted from the current unbalance that is measured for different temperature conditions between the two substrates. The effect of the different temperatures for the cables of each branch can be neglected. Therefore, the effect alone of the NTC can be isolated and evaluated.

Table II: Current unbalance per total current level due to circuit asymmetry

Total current [A]	Current unbalance [A]
10	0.072
20	0.146
30	0.223
40	0.291
50	0.372
100	0.745

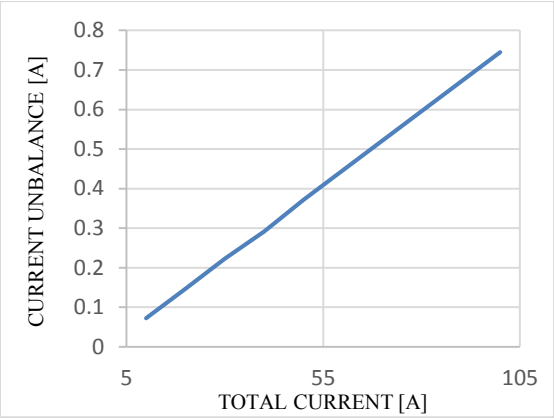


Fig. 8: Current unbalance between the two substrates due to circuit asymmetry versus total circuit current

Current unbalance due to the operation in the NTC region

As observed in Fig. 6b, each substrate consists of two diode chips that are indicated with the letter D and four IGBT chips that are indicated with the letter I. The thermal camera is monitoring the temperature at two chips on substrate 1 and on two chips on substrate 3. The current unbalance between the substrates is measured for various current levels and temperature differences. Table III lists the results.

Table III: Current unbalance for various current levels and temperature differences

Total current [A]	Temperature of 2 chips (T1 and T2) on substrate 1 [°C]	Temperature of 2 chips (T3 and T4) on substrate 3 [°C]	Maximum temperature difference between two chips [°C]	Current unbalance between the 2 substrates due to the NTC [A]
40	41, 42	46, 48	7	0.4
60	42, 44	48, 49	7	0.45
80	82, 85	90, 91	9	0.45
100	67, 71	80, 82	15	0.5

The temperature difference between the chips can be explained with respect to their positions. The chip T1 is at the outer part of the module, where there is a temperature difference towards the ambience at the side of the module. The temperature of chip T2 is influenced by the higher temperature of chip T3, which was observed with the thermal camera during the power cycling. Focusing on the current unbalance, the difference is between 0.4A and 0.5A in all cases. The highest current unbalance is measured at 100A that means at an average of 50A per substrate or 12.5A per chip. The temperature difference between the hottest and coldest chip reaches 15°C, which is not a common situation. According to [10], [15] the current level of 100A that corresponds to a current of 200A, if the whole module is engaged, is the region where the NTC effect is mostly evident. On the other hand, the current unbalance of 0.45A at 60A and 80A with a temperature difference of 7°C and 9°C, respectively, is a realistic case [3]. Furthermore, the maximum temperature difference is an indication of the different thermal conditions in the two substrates but it is not an absolute reference, since, for instance, the temperature deviation between T2 and T3 is in every case significantly lower than the maximum temperature.

Impact on thermal stressing distribution between the substrates

The next step is to evaluate the impact of the measured current unbalance on the thermal stressing distribution at the substrate level by taking the worst case of 100A and 15°C temperature difference as an example. With the assumption of no leakage inductance unbalance between the two substrates that

could influence the current sharing during the switching dynamics, the difference of the average power losses between the two substrates is calculated using a linear approximation for the low current region

$$P_{loss,av} = \left(E_{on,ref} + E_{off,ref}\right)\frac{V_{dc}}{V_{dc,ref}}\frac{I_c}{I_{c,ref}}f_{sw} + DV_{ce}I_c \quad (2)$$

$$\Delta P_{loss,av} = \left(\frac{E_{on,ref}+E_{off,ref}}{4}\right)\frac{V_{dc}}{V_{dc,ref}}\frac{(I_{c,2}-I_{c,1})}{I_{c,ref}}f_{sw} + DV_{ce}\left(I_{c,2} - I_{c,1}\right) = 1.94W \quad (3)$$

where $E_{on,ref}$, $E_{off,ref}$, are the reference turn-on, turn-off losses, respectively, both according to the device datasheet for a total module current of 200A divided by four, since the calculations are for one of the four substrates of the module, $V_{dc,ref}$ the datasheet reference voltage, V_{dc} the DC-link voltage of the application equal to 900V, $I_{c,ref}$ four times lower than the datasheet reference current, $I_{c,2}$ is the saturation current of substrate 3 equal to 50.25A, $I_{c,1}$ is the saturation current of substrate 1 equal to 49.75A and V_{ce} the saturation voltage, respectively, 1.1V at 200A. The switching and conduction losses are calculated for a given temperature of 25°C. The calculations are for operating conditions that correspond to the actual application with a duty cycle *D* of 0.43 and a switching frequency f_{sw} of 6.5kHz. In order to calculate the increase of the power losses, if the substrate operates at 50.25A compared to the balanced operation at 50A and based on (2), we get

$$\frac{P_{loss,50.25,av}}{P_{loss,50,av}} = \frac{(E_{on,ref}+E_{off,ref})V_{dc}I_{c,2}f_{sw}+4DI_{c,2}*V_{ce}I_{c,ref}V_{dc,ref}}{(E_{on,ref}+E_{off,ref})V_{dc}I_{c,3}f_{sw}+4DI_{c,3}V_{ce}I_{c,ref}V_{dc,ref}} = 0.5\% \quad (4)$$

Where $I_{c,2}$ is the saturation current of 50.25A and $I_{c,3}$ is the saturation current of 50A. The power losses increase is, only, 0.5%.

Conclusions

This work focused on the operation of SPT IGBT modules at the NTC region. The effect of the temperature unbalance between the substrates on the current sharing in the power device was investigated. A temperature difference was produced reaching values equal and above what is described in the literature and in the part of the NTC region that is mostly prone to current unbalances. The measurements and the calculations indicate that the difference in the current between the two substrates and the additional thermal stressing at the substrate that carries the highest current are not significant.

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