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Presentation

Silicon pixel-detector R&D for CLIC

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Silicon pixel-detector R&D for CLIC

Andreas Nürnberg on behalf of the CLICdp collaboration

8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging Sestri Levante, Italy 5.-9. September 2016

This project has received funding from the European Union's Horizon 2020 Research and Innovation

CLIC

- ► CLIC (Compact LInear Collider): linear e⁺e⁻ collider proposed for the post HL-LHC phase
- Energy range from a few hundred GeV up to 3 TeV, staged construction
- \blacktriangleright Physics goals:
	- \triangleright Precision measurements of SM processes (Higgs, top)
	- \triangleright Precision measurements of new physics potentially discovered at 14 TeV LHC
	- \triangleright Search for new physics: unique sensitivity to particles with electroweak charge

Possible layout near Geneva

CLIC accelerating structure

CLIC vertex and tracker detector

- \blacktriangleright Vertex detector
	- Fificient tagging of heavy quarks \rightarrow precise determination of displaced vertices
	- > 3 µm single point resolution, fine pitch, \leq 25 µm \times 25 µm pixel size,
	- Eimited material budget, $0.2\%X_0$ per detection layer, 50 µm sensor $+50 \mu m$ ASIC
	- \blacktriangleright Hybrid concept under study with either planar or active sensor
- \blacktriangleright Tracker
- \blacktriangleright Both

CLIC vertex and tracker detector

- \blacktriangleright Vertex detector
- \blacktriangleright Tracker
	- ► Good momentum resolution, $\sigma_p \tau / p_T^2 = 2 \times 10^{-5}$ GeV $^{-1}$, 7 µm single point resolution
	- \blacktriangleright 4 T field, large radius, large sensitive area
	- \blacktriangleright 1%X₀ to 2%X₀ per detection layer
	- ► Larger cell sizes, \sim 50 µm \times 1 10 mm, limited by occupancy from beam induced background particles
	- \blacktriangleright Pursue also monolithic solution

 \triangleright Both

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CLIC vertex and tracker detector

- \blacktriangleright Vertex detector
- \blacktriangleright Tracker
- \triangleright Both
	- \blacktriangleright 20 ms gaps between bunch trains
	- \blacktriangleright Trigger-less readout
	- \blacktriangleright Pulsed power operation
	- \blacktriangleright 10 ns time slicing
	- ► moderate radiation exposure: 10⁻⁴ LHC

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Technology R&D programme

Light-weight supports Detector integration

Sensors Readout ASICs Simulations

 \rightarrow Integrated R&D effort addressing CLIC vertex and tracker detector Today: focus on sensor and readout technology

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Thin sensor test beam results

- \triangleright Test beam studies on sensor assemblies with different thickness (Micron, Advacam) using Timepix(3) readout ASICs, 55 µm pitch
- \blacktriangleright Thinnest assembly: 100 µm sensor on 100 µm Timepix ASIC
- \triangleright Study performance of thin planar sensors
	- \blacktriangleright High detection efficiency even for 50 µm thin sensor under normal operating conditions
	- \triangleright Resolution limited by cluster size in thin sensors

Active edge sensors

- \triangleright Study feasibility of thin sensors with active edge using Timepix3 readout ASICs
- \triangleright Advacam MPW with 50 µm to 150 µm thick n-in-p sensors
- ▶ The DRIE (Deep Reactive-Ion Etching) process is used to cut an active edge silicon sensor
- \blacktriangleright Implantation on the sidewall of the sensor \Rightarrow extension of the backside electrode on the edge

Active edge sensors: results

- Comparing different edge layouts: without guard ring (GR), floating GR and grounded GR
- \blacktriangleright Signal loss to grounded GR
- Device without GR and with floating GR is fully efficient up to the physical edge of the sensor
- \blacktriangleright Efficiency loss in thin sensors with grounded GR, in agreement with TCAD simulations

50 um thick, floating guard ring

50 µm thick, grounded guard ring

50 µm thick, grounded guard ring

Single layer track reconstruction using drift-time

- \blacktriangleright Idea: use good time binning of Timepix3 (1.5 ns) to extract depth of charge deposit from measured drift-time
- \triangleright Track reconstruction like in a time projection chamber using a single detection layer
- ▶ Proof-of-principle using angle scan on 675 µm thick p-in-n sensor in CLIC Timepix3 telescope
- \triangleright Possible applications in CLIC tracker
	- \blacktriangleright rejection of background from back-scattered and low-momentum particles
	- \triangleright improvement of pattern recognition / track reconstruction

Single layer track reconstruction using drift-time

\blacktriangleright Two analysis methods

- ▶ Analytic: using mobility parameterization to extract drift distance
- \triangleright Machine learning: use known track angle from alignment to train neuronal network. Use as much available information as possible (time gradient, cluster size, cluster energy). Not yet fully optimized

▶ Use case for CLIC tracker currently under study: test thinner sensors

CLICpix planar sensor assemblies CLICpix planar sensor assemblies

- \blacktriangleright CLICpix
	- \blacktriangleright Timepix/Medipix chip family $m_{\rm F}$ $\mu_{\rm F}$ $\mu_{\rm F}$ $\mu_{\rm F}$ CLICpix:
	- 65 nm technology
	- Demonstrator chip with 64×64 pixels $\frac{1}{4}$ $\frac{1}{6}$ $\frac{1}{6}$
	- \blacktriangleright Pitch of 25 μm
	- \blacktriangleright Simultaneous 4-bit ToT and ToA \blacksquare
- \blacktriangleright Test assemblies produced with 200 μ m, 150 μm and 50 μm n-in-p CLICpix sensors
	- Single-chip bump-bonding process for 25 μ m pitch developed at SLAC pitch challenging, process developed at the second at
	- \blacktriangleright 200 μ m assembly tested in AIDA telescope at SPS produced UBM and Indianapolis on sensor at SPS and Indianapolis on sensor at SPS and Indianapolis
	- ► Data taking on 50 µm assembly in Edite taking on 50 pm assembly in UBM and Indium bump bonds on sensor
Timepix3 telescope took place last week

CLICpix planar sensor assemblies

- \triangleright Results for 3 test assemblies with 200 um Micron sensors:
	- \blacktriangleright 0.2% to 3% unconnected channels
	- \blacktriangleright 1% to 2% shorted channels
- \blacktriangleright Test-beam measurements:
	- \triangleright Operation threshold \sim 1000 e⁻, Vdep $~\sim$ 35 V
	- \blacktriangleright High detection efficiency (>99.5 %)
	- Figure 20 % single-pixel clusters at Vdep
	- $\blacktriangleright \sim 4$ µm single-point resolution
- ^I Characterization of assembly with 50 µm the bias voltage, explaining the increase of the cluster size and the improvement of the resolution thin Advacam active-edge sensor ongoing. $\frac{2}{9}$ 4 $\sqrt{2}$

currently under investigation.

Figure 7. Cluster fraction versus bias voltage

HV-CMOS active sensor with capacitive coupling

Capacitive coupled pixel detector (CCPDv3) used as active sensor

- \triangleright CCPDv3 chip is capacitively coupled to the CLICpix readout ASIC via a thin layer of glue \Rightarrow no bump-bonding
- ▶ 180 nm HV-CMOS process
- \triangleright Deep n-well shields electronics from substrate bias
- \blacktriangleright Two-stage amplifier in each pixel, 120 ns rise time
- ► 60 V reverse bias \Rightarrow create a depletion layer, fast signal collection by drift

SEM picture CCPDv3-CLICpix assembly

CLICpix via [Silicon pixel-detector R&D for CLIC](#page-1-0) 06. 09. 2016 14A. Nürnberg:

CCPDv3-CLICpix test-beam results

- \blacktriangleright High detection efficiency even without bias and 1000 e- threshold
- \triangleright 6.1 µm single-point resolution (\sim 1.6 µm telescope resolution unfolded)

 \triangleright Proof of principle for feasibility of capacitively coupled hybrid pixel detectors

- Improved CLICpix2 readout ASIC (128 \times 128 matrix) and matching HV-CMOS sensor (C3PD) are being produced
- \blacktriangleright First standalone characterization of new active sensor shows expected performance
	- \blacktriangleright Measured amplifier rise time: 20 ns

Thinned (50 µm) C3PD chip **CAPD**

Integrated CMOS pixel detectors: HR CMOS

- ▶ TowerJazz 180 nm High-Resistivity CMOS
	- \triangleright Quadruple well process with full CMOS: n-wells shielded by deep p-wells
	- \blacktriangleright 15 µm to 40 µm / 1 kΩ cm to 8 kΩ cm epitaxial layer, not fully depleted (Vbias $\leq 6 V$
- ▶ ALICE Investigator analog test chip
	- Pixel sizes: $20 \times 20 \mu m^2$ to $50 \times 50 \mu m^2$
	- \triangleright Optimization of collection-diode geometry to minimize capacitance (\sim 2 fF)
	- \triangleright Readout with external sampling ADCs

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Integrated CMOS pixel detectors: HR CMOS

- \triangleright TowerJazz 180 nm High-Resistivity CMOS ϵ
	- \blacktriangleright Quadruple well process with full CMOS: n-wells shielded by deep p-wells r
le
le Work in progress
	- \blacktriangleright 15 μm to 40 μm / 1 kΩ cm to 8 kΩ cm epitaxial layer, not fully depleted (Vbias $\leq 6 V$
- ▶ ALICE Investigator analog test chip
	- \blacktriangleright Pixel sizes: 20x20 μ m² to 50x50 μ m²
	- \triangleright Optimization of collection-diode geometry to minimize capacitance $(\sim 2 \text{ fF})$ and $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$
	- \triangleright Readout with external sampling ADCs $\left\{ \begin{array}{c} \epsilon_0 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \leq \epsilon_2 \leq \epsilon_1 \leq \epsilon_2 \$
	- Integration in CLIC Timepix3 test-beam setup
		- ► good spatial resolution: \sim 5 µm at 28 µm pixel pitch
		- \blacktriangleright good time resolution: few ns

Integrated CMOS pixel detectors: SOI

\blacktriangleright Lapis 200 nm SOI

- ► CMOS sensor on Silicon On Insulator (SOI) wafers
- \blacktriangleright Electronics on low resistivity wafer, separated by buried oxide from fully depleted high-resistivity sensing layer
- ▶ Test-chip from AGH Cracow
	- Different pixel sizes ($\geq 30 \times 30 \mu m^2$) and readout techniques (source follower, charge preamp., self-triggering, ...)
	- \blacktriangleright Targeted towards CLIC requirements (position, amplitude and few ns timing)
	- \blacktriangleright Integration in CLIC test-beam setup. Chip functional, first data taking finished last week, analysis ongoing

Summary

 \blacktriangleright CLIC accelerator provides

- \triangleright unique potential for discoveries and precision physics at the TeV scale
- \blacktriangleright challenging requirements for vertex and tracker detector
- Integrated R&D effort for the CLIC vertex and tracking detector on sensors and readout chips
	- \blacktriangleright Hybrid readout with planar sensors
	- \triangleright Capacitively coupled pixel detector with active sensors
	- Integrated CMOS sensors
- ▶ Not shown today: (T-CAD) simulations, mechanical integration, powering, cooling, ...

Thanks to everyone who provided material for this talk! Thank you for your attention!

Additional Material

CLIC detector and physics collaboration

CLICdp member institutes:

- Aarhus University
- · ACAS Australia
- · AGH-UST Cracow
- · Argonne National Lab
- Bergen University
- · Birmingham University
- **Bristol University**
- **Cambridge University** \bullet
- **CERN** \bullet
- DPNC Geneva
- · Glasgow University
- · IFJPAN Cracow
- **IPASCR Czech Republic**
- · Institute of Space Science Bucharest
- · JINR Dubna
- KIT IPE Karlsruhe
- LAPP Annecy
- Liverpool University
- Michigan University
- MPI Munich
- NC PHEP Belarus
- Oxford University
- · Pontificia Univ. Catolica de Chile
- · Spanish Network for Future Linear Colliders
- Tel Aviv University
- Vinca Institute Belgrade
- University of Warsaw

CLIC accelerator

CLIC accelerating structure

CERN-2012-007

- \blacktriangleright Linear e+e- collider
- ▶ 2-beam acceleration scheme, operated at room temperature
- \triangleright Gradient: 100 MV/m
- $\rightarrow \sqrt{s}$ up to 3 TeV
- ► Luminosity: 6×10^{34} cm⁻² s⁻¹ (at 3 TeV)
- \triangleright Physics + Detector studies for 350 GeV 3 TeV

CLIC detector concept

Test beam infrastructure

EUDET/AIDA telescope

- \blacktriangleright Used for initial test-beam studies at DESY II, CERN PS and CERN SPS
- Rolling-shutter readout over ∼ 230 µs → limited rate and timing capabilities

CERN LCD Timepix3 telescope

- \blacktriangleright High rate (up to 10M particles/s)
- ▶ Good tracking resolution on DUT in space $(<2 \mu m)$ and time $($ \sim 1 ns)
- \blacktriangleright Motion and rotation stages for automatic scans

Guard ring layouts

- \blacktriangleright 4 different guard ring layouts implemented
- \triangleright Edge distance is defined as the distance between the last n-implant and the cut edge
- \triangleright 20 µm edge, no guard-ring

 \triangleright 23 µm edge, floating guard-ring

 \triangleright 28 µm edge, GND guard-ring

 \blacktriangleright 55 µm edge, GND guard-ring

Efficiency and signal in the edge

Signal in the edge - T-CAD transient simulation

 \triangleright Arbitratry signal normalization, qualitative agreement

Example: TOA and TOT at 80 degree incident

MLP input

Alignment and calibration

- \blacktriangleright Laboratory and test-beam $measurable$ $\frac{1}{2}$ output signals $\frac{1}{2}$
- Simulate performance with glue correlate performance with grac-
parameters (alignment, coupling strength, uniformity) SEM picture CCPDv3-CLICpix assembly
	- Dedicated test pixels: direct access to CCPDv3 output signal
- \rightarrow Used to calibrate CLICpix ToT response

CCPDv3-CLICpix test-beam results

- ► High detection efficiency at 1000 e⁻ threshold
- \blacktriangleright Faster degradation with threshold for misaligned assemblies shows reduced gideally aligned samples, but the half pixel mission in the half p coupling capacitance and hence lower induced signal
.