On-detector electronics for the LHCb VELO Upgrade

On behalf of the LHCb VELO Upgrade Group

TWEPP 2016, 28th September 2016, Karlsruhe

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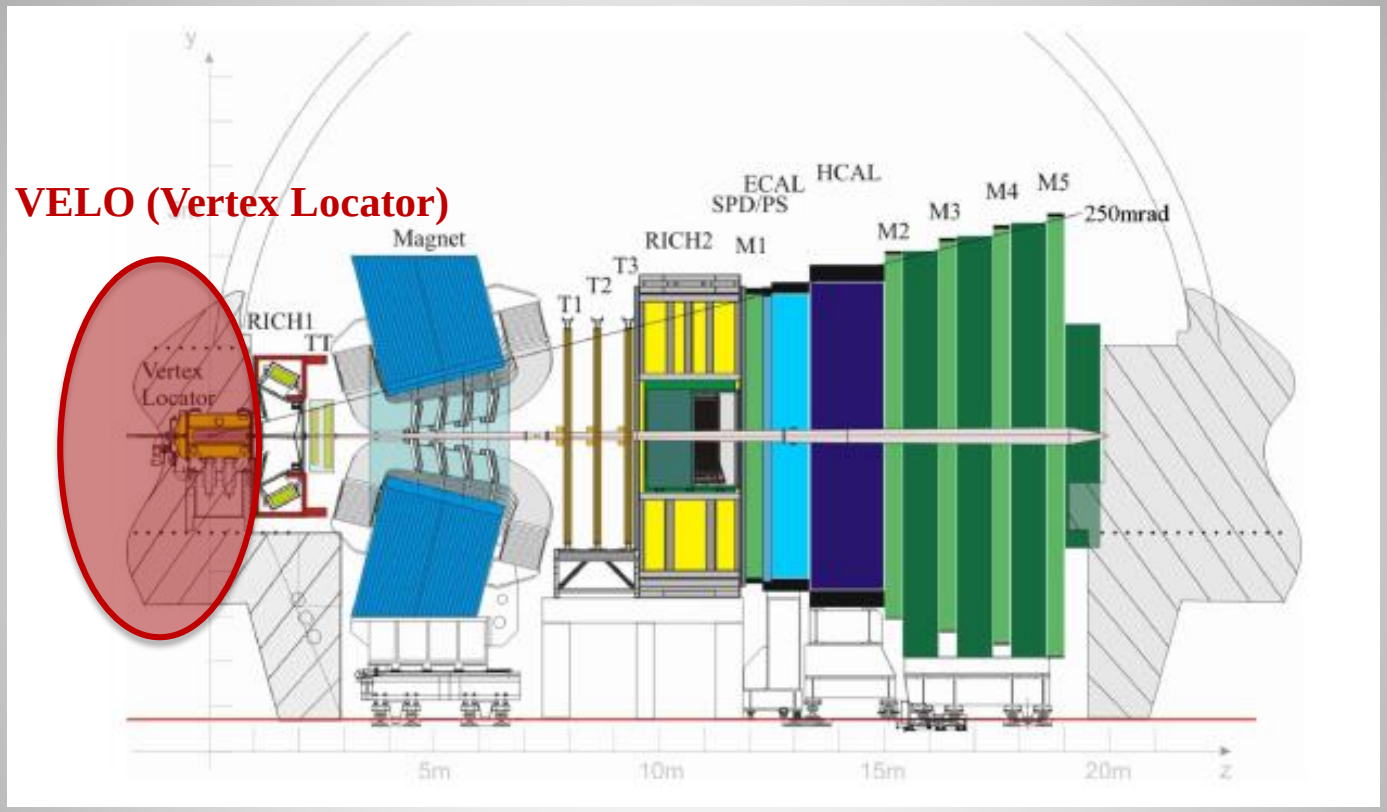
The Large Hadron Collider Beauty Experiment (LHCb)



LHCb experiment: Utilising a tracking system, 2 RICH detectors for PID, Electromagnetic and Hadronic Calorimeters and a muon system.

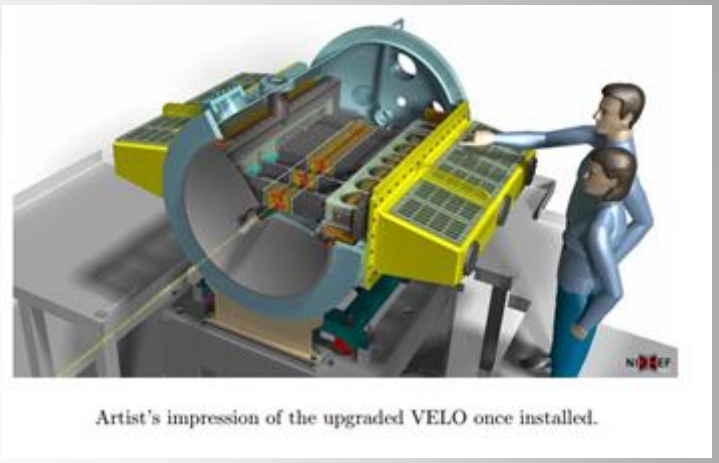
The LHCb detector is a forward spectrometer at the Large Hadron Collider (LHC) at CERN. The experiment is designed for precision measurements of CP violation and rare decays of beauty and charm hadrons.

The LHCb VELO Upgrade

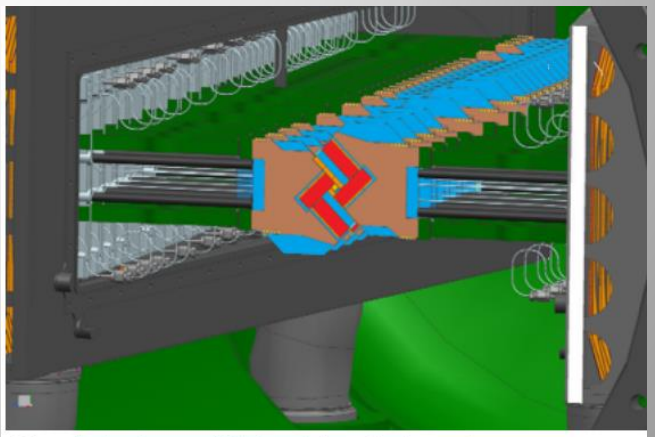
The upgraded LHCb VELO is a silicon vertex detector that will start operation together with the rest of the upgraded LHCb experiment during the LHC LS2 shutdown, currently scheduled to start in 2020.

Key features-

- A lightweight hybrid pixel detector.
- Trigger-less system reading out at 40 MHz and luminosity of 2×10^{33} cm^{-2} s^{-1}.
- Enhanced track reconstruction speed and precision.
  - New L-shaped Pixel geometry.
  - Distance of approach to the LHC beams of just 5.1 mm for the first sensitive pixel.
- Operates in vacuum and is designed to absorb the VELO motion.
- Cooling by evaporative CO_2 circulating in microchannel cooling substrates.
- 41 million 55 µm × 55 µm pixels read out by the custom developed VELOPix front end ASIC.



Artist's impression of the upgraded VELO once installed.

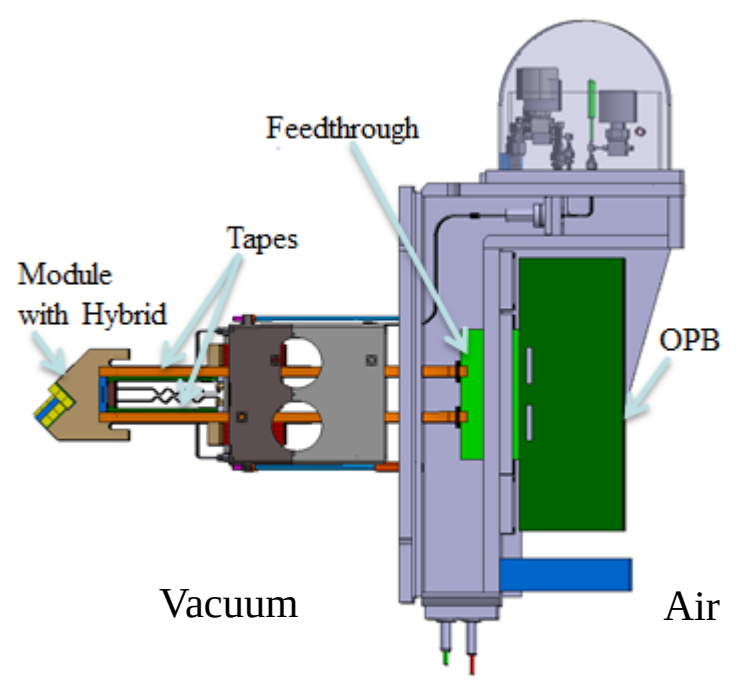


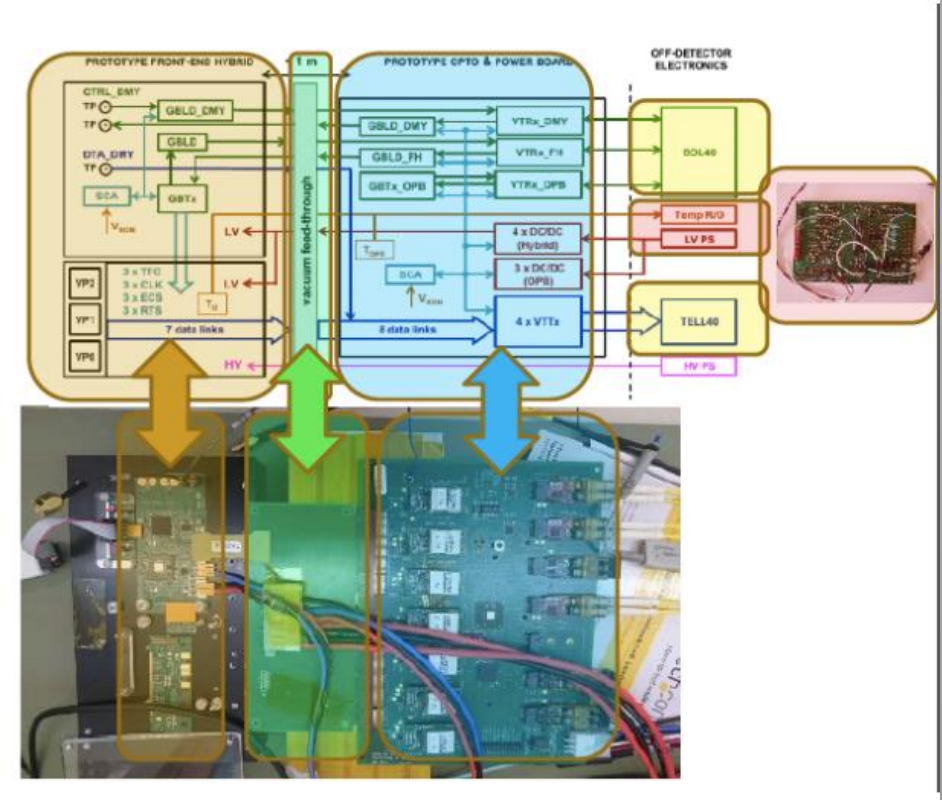
Closer look at the new VELO modules with changed geometry

VELO on-detector electronics

On detector electronics comprises of the following components-

- Front-end hybrid and VeloPix ASICs
- Data link tape
- Vacuum Feedthrough
- Opto- and power board (OPB)





Module

- Each Silicon sensor is bump-bonded to a row of three VELO Pix ASICs.

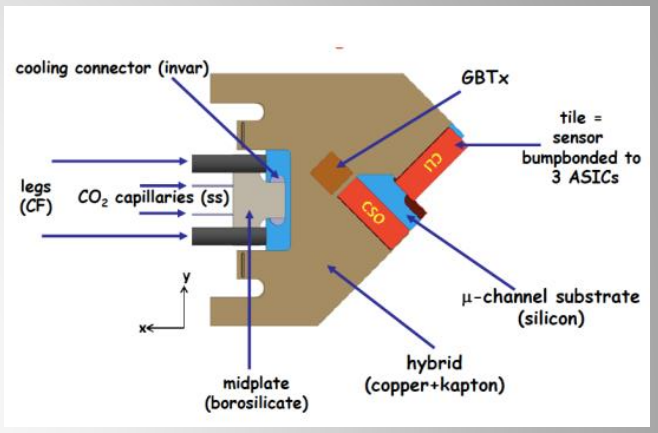
  This assembly form a **tile**.
- Each **Module** is made up of 4 such tiles,

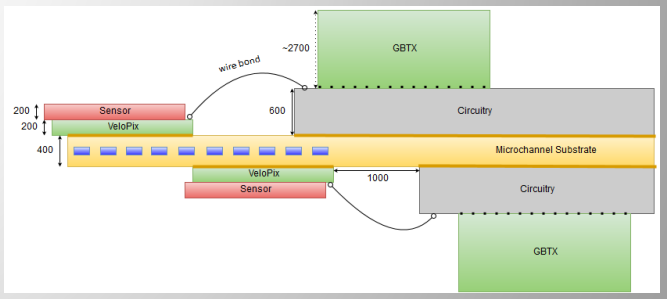
  2 on each side of the substrate.
- The VeloPix ASIC, 200 µm thick, reads out

  a sensor that has a matrix of 256 × 256 pixels of

  55 × 55 µm^2 each.
- The VeloPix ASIC is based on the Timepix3 ASIC,

  and is designed in the TSMC 130 nm CMOS process.
  - Key features-
    - Data driven and Zero suppression readout
    - 4 serial outputs of 5.12 Gbit/s each.



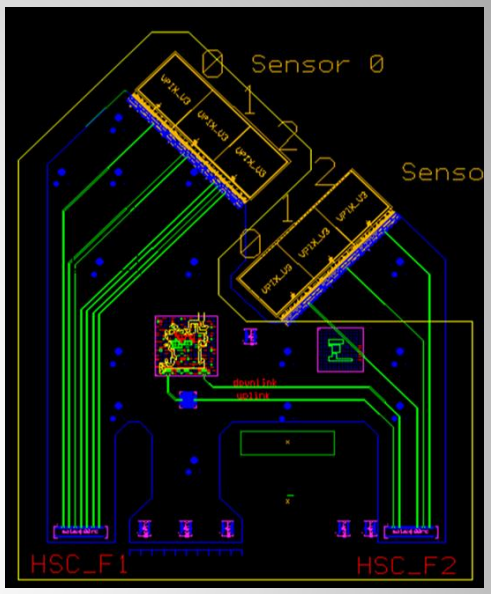


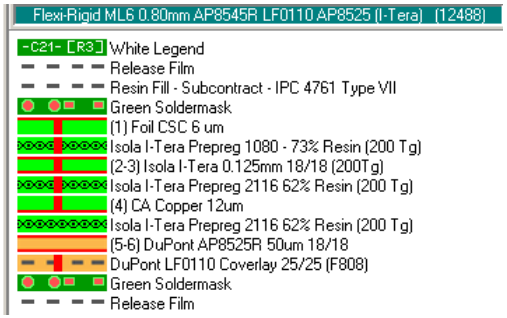
Cross section of the VeloPix Module

See talk by Tuomas Sakari Poikela (CERN) on "The VeloPix ASIC" on 30th Sept 16.

Front-end Hybrid

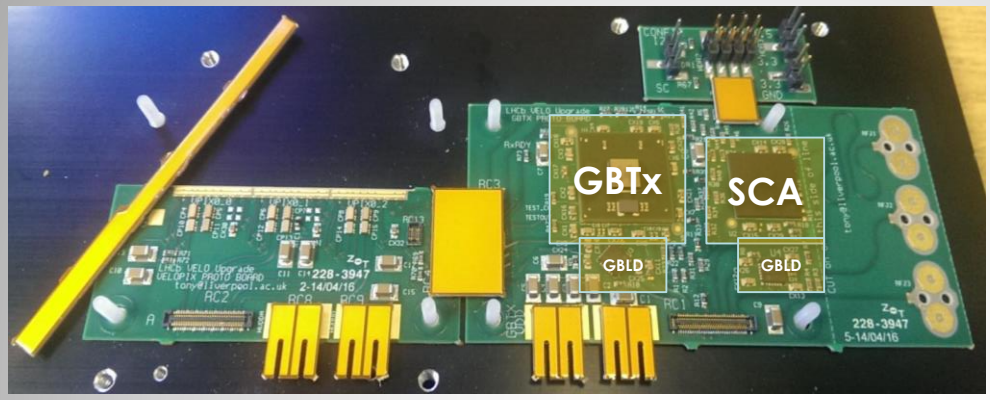
- The two hybrids in a module are electrically similar, but geometrically different, multilayer flexible printed circuit boards.
- The hybrid will provide power, high voltage, signal distribution and readout signal routing to two three-chip sensor assemblies per side of the module.
- Key Design features-
  - 6 layer flexi-rigid board with Isola Itera and Dupont pyralux material.
  - Single sided component assembly.
  - Dense(400pin and 196pin) BGA packages.
  - Controlled impedance for high speed(GHz) and mid frequency(MHz) differential traces.



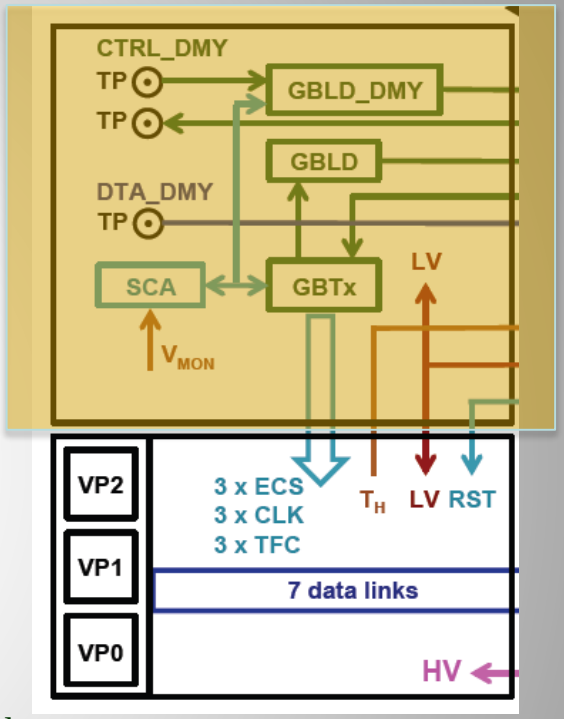


No solder mask on bottom Total thickness ~800um

Front-end Hybrid Prototype



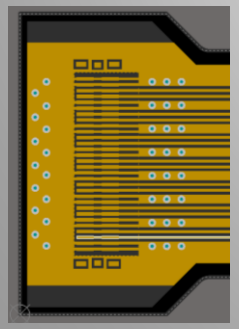
The prototype of the front end hybrid



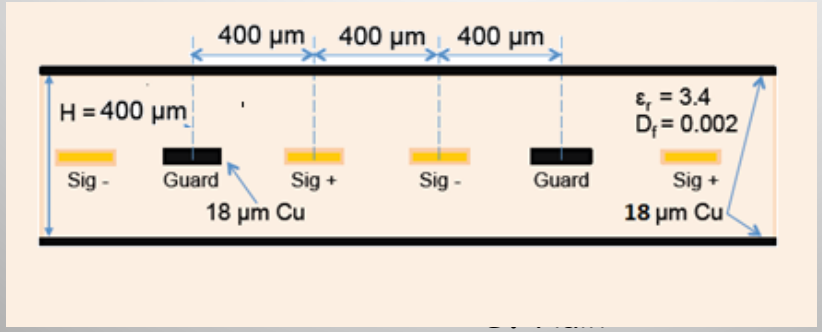
- A split hybrid is implemented with control electronics separated.
  Allows evaluation on multiple VeloPix Hybrids
- GBTX
  - Used to implement multipurpose high speed bidirectional optical links
- Slow Control Adaptor(SCA)
  - Voltage monitoring
  - Will be removed on the final hybrid
- GBLD
  - Laser driver ASIC used as a line driver (with pre-emphasis) to route the control signals from the hybrid to the VTRx on the OPB

Data Link Tapes

- Data link Tapes are low mass , 56 cms long electrical tape carrying data at 5.12 Gb/s.
  - Routes control and data signals from the modules to the vacuum feedthrough.
- The VELO has 208 tapes for 52 modules with 20 data links per module.
- Key Design Features-
  - Designed to be flexible and absorbs motion.
    - Fatigue test with 3000 bends passed
  - Prototypes are built with a special laminate (Pyralux AP-plus) from Dupont suitable for high speed signal transmission applications.
    - Dielectric with a tightly controlled thickness of 350 µm and with copper layers with special surface finish to minimize the skin effect loss.
  - Molex Slimstack connector with 400 µm pitch is used and is sunk on the inner layer(of the 3 layer stackup) to avoid vias on the high speed signal traces.



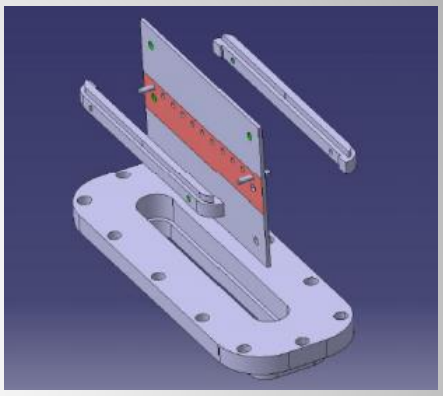
Inner layer of the tape layout

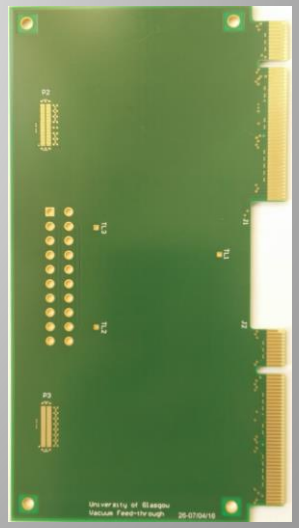


See talk by Leyre Flores (UoG) on "High speed electrical transmission line design and characterisation" on 29th Sept 16.

Vacuum Feedthrough

- The vacuum feedthrough is an interface between the high speed data link tape and the Opto Power board (OPB)
- Will be integrated with the feed through.
- Mates with 2 PCIe connector on the OPB.
- Low voltage supplied by the PCIe connector
  but a separate 20 pin Samtec connector to the hybrid.
- Key Design Features-
  - 8 layer board with FR4 and Isola Itera laminate(material characterized for high speed signal transmission)
  - High speed signal are routed as edge coupled stripline with continuous GND planes on either sides
  - Controlled impedance and matched trace lengths(difference < 1 mm)
  - Blind via technology



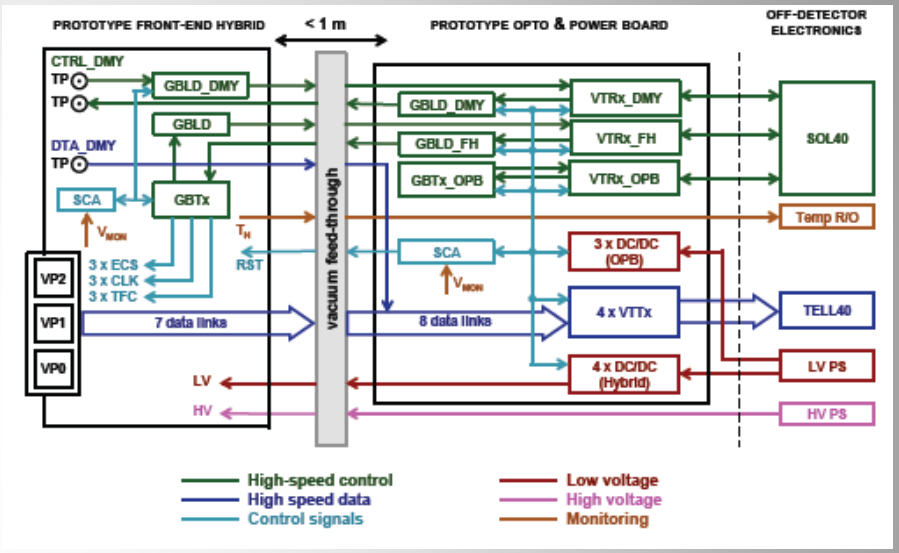


Layer	100 ohms track/gap(mm)	Cu Thickness
Top Layer (components, traces, GND plane)	ref plane	18um + plating
Signal_BH (5.12 GHz- 100ohms differential)	0.150/0.150	18um
DGND_BH (Ground plane)	ref plane	35um
PWR_BH (split plane, non-critical signals)		35um
PWR_FH (split plane, non-critical signals)		35um
DGND_FH (Ground plane)	ref plane	35um
Signal_FH (5.12 GHz- 100ohms differential)	0.150/0.150	18um
Bottom Layer (components and traces, GND plane)	ref plane	18um + plating

Opto and Power Board(OPB)

Motivation for the OPB -

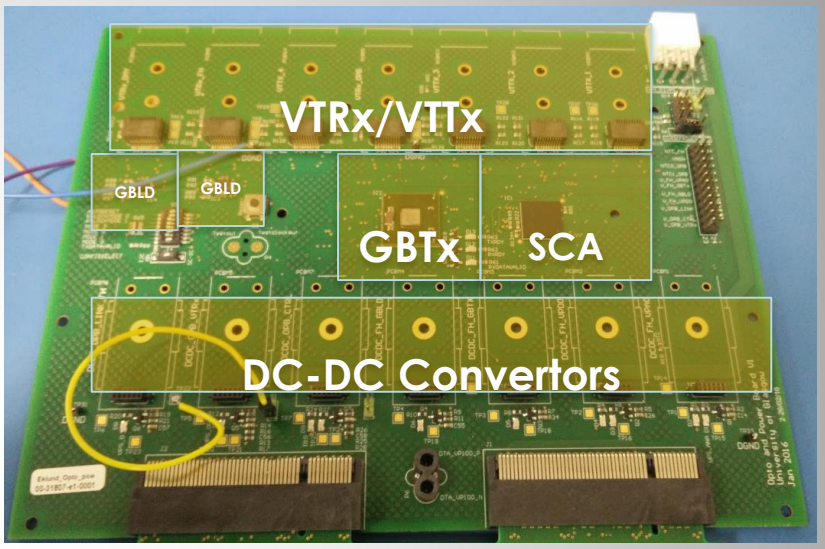
- To avoid placing optical component (lasers, diodes, fibres and optical connectors) inside the secondary vacuum.
  - Difficulty of cooling the high-power dissipating optical components in vacuum.
  - Sensitivity to radiation.
  - The delicateness of the interconnections.
  - The additional mass in the detector acceptance.
- To allow maintenance and repair during operation.



For similar reasons all DC/DC converters powering the front-end ASICs need to be moved in an accessible area outside the vacuum tank.

Prototype Opto and Power Board

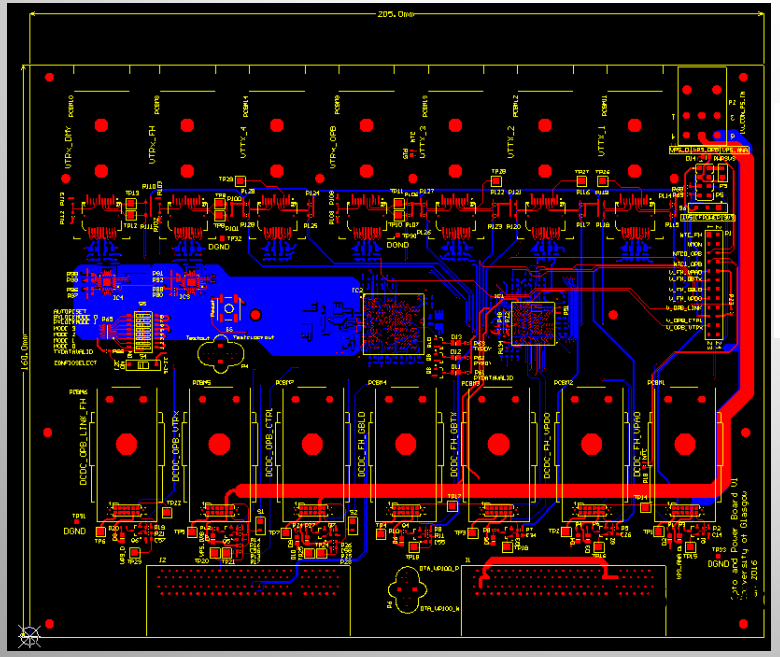
- The OPB connects the Vacuum feedthrough and the Off detector electronics. Its main functions are-
  - O/E conversion for the data and control signals
  - DC/DC conversion of the supply voltages for the hybrids and OPB itself
  - Control and monitoring of the components on the OPB.



- Is designed to test the electrical functionality of the link from the hybrid to the off detector electronics.
- Has full functionality of the production board but with a reduced number of channels.
- Is designed to supply and readout a single prototype front end hybrid with 3 ASICs.
- Each OPB will services two front end hybrids that are attached on opposite sides of detector module.
- SCA provides I2C buses to configure the opto drivers and logical I/O signals for the DC-DC convertors .
- The ADC inputs of the SCA ASIC are used voltage monitoring.
- DC-DC convertors supply voltage to the front end hybrid and the OPB itself.
- VTRx/VTTx are the versatile link transceivers/twin transmitters for Optical to electrical conversion.

Prototype OPB Design

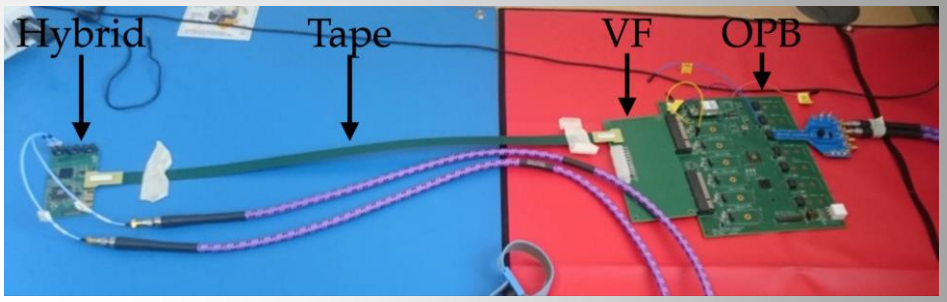
- Key Design Features
  - 8 layer board with hybrid construction of FR4 and Isola Itera laminate
  - High speed signals(5.12 Gb/s) routed as edge coupled stripline with continuous GND planes on either sides.
  - Dense (400 pin and 196 pin) and fully used BGA packages.
  - Controlled impedance and matched trace lengths(difference < 1 mm) for high speed differential signals.

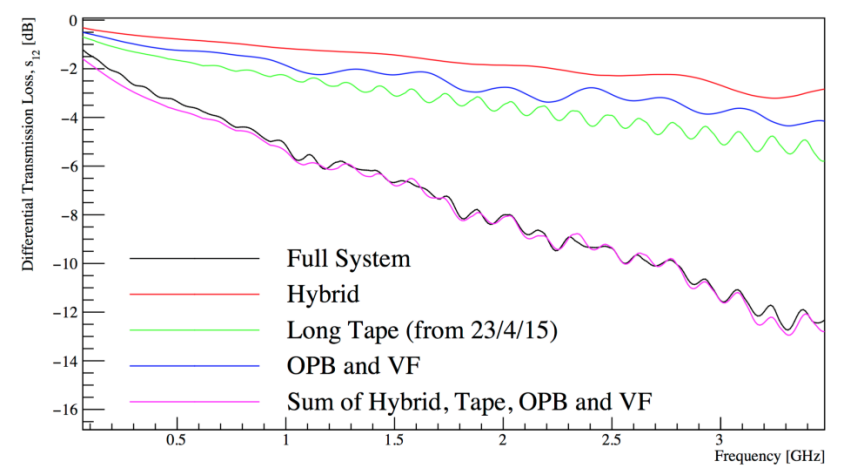


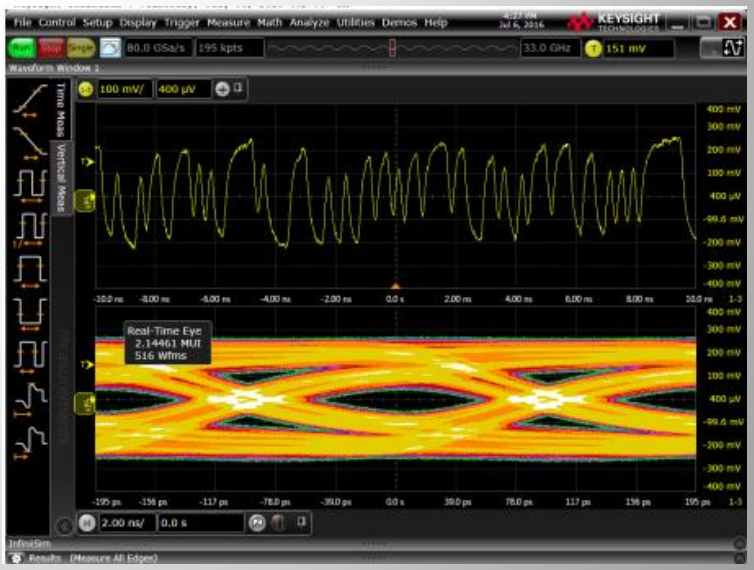
Layer	100 ohms track/gap(mm)	Cu Thickness
Top Layer (components and traces)	ref plane	18um + plating
Signal (non critical-a few differential pairs running at 80 MHz)	0.119/0.181	18um
GND_FH(Split plane)	ref plane	35um
PWR_FH(split plane)		35um
DGND_FH	ref plane	35um
Signal_FH (5.12 GHz- 100ohms diffrential)	0.150/0.150	18um
DGND_FH	ref plane	35um
Bottom Layer (components and traces)	0.160/0.140	18um + plating

Results of the full link test

- S-parameters of individual components and full link measured .
- Eye diagram with ‘ideal’ signal source
- Total loss a bit more than acceptable



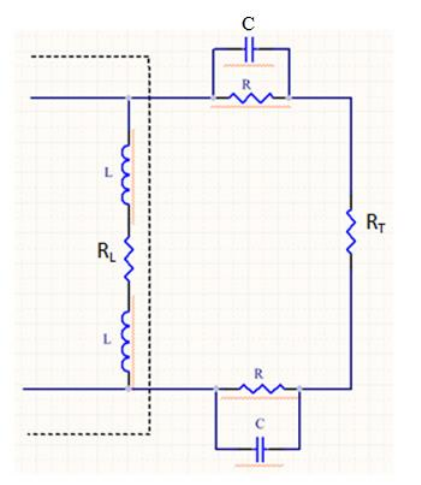




The loss is -9.5db at 2.5Ghz Nyquist frequency

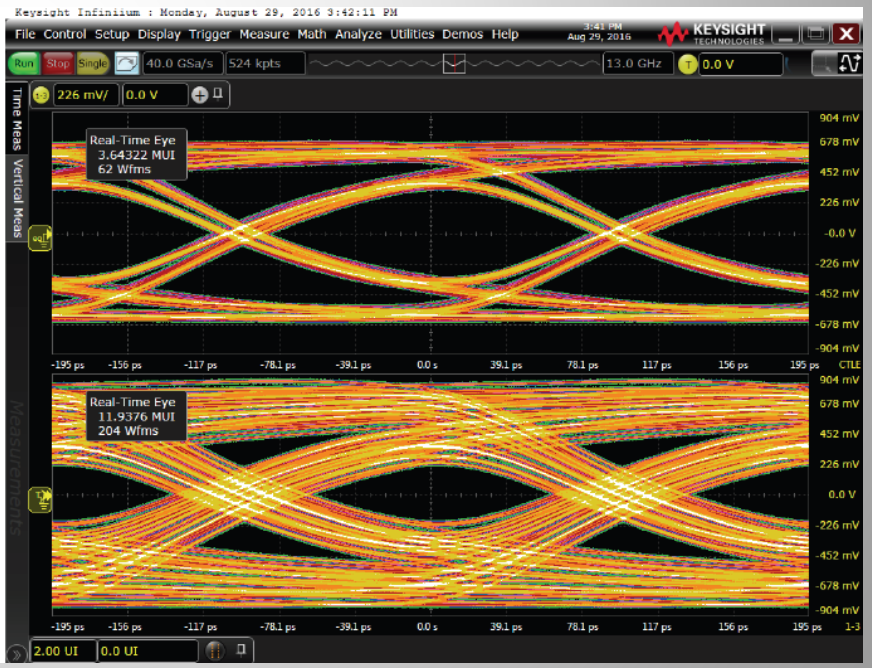
Passive CTLE (Continuous Time Linear Equalisation)

- Improved Eye diagram on applying passive CTLE circuit and using an ideal source.
- Investigating the equalization options to increase the margins of the signal transmission.
- CTLE is emulated in the scope, prototyping is in progress



Post CTLE

Raw eye diagram



Summary

- Upgraded LHCb VELO experiment will be installed during the LHC LS2 shutdown, currently scheduled to in 2020.
- Redesign of the VELO to allow for the increased data rate.Trigger-less system with readout at 40 Mhz.
- All prototypes for the electronics have been produced and tested. Very successful with the exception of minor issues.
- Further study to improve signal transmission are being investigated using passive CTLE.
- Testing of the electronics system using the new VeloPix ASIC will be done soon.

Thank you

Backup Slides

Overview of the detector module

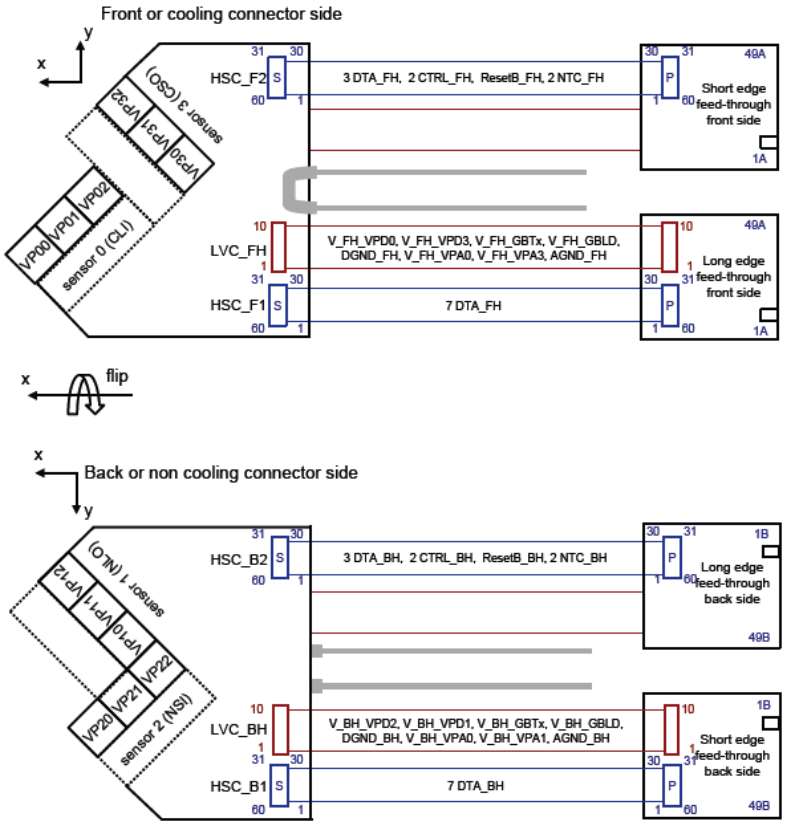


Figure 7: Overview of the detector module, cables and feed-throughs, defining sensor numbers, VeloPix numbers and connector orientations. The letters P and S stand for plug and socket, which defines the connector gender on the PCBs with pin numbers as indicated.

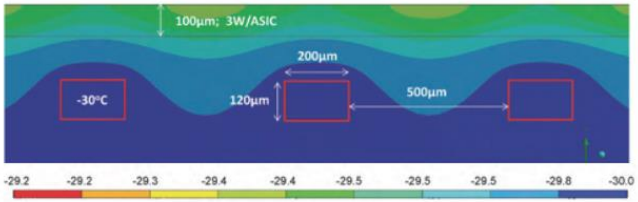
Microchannel cooling

Cooling

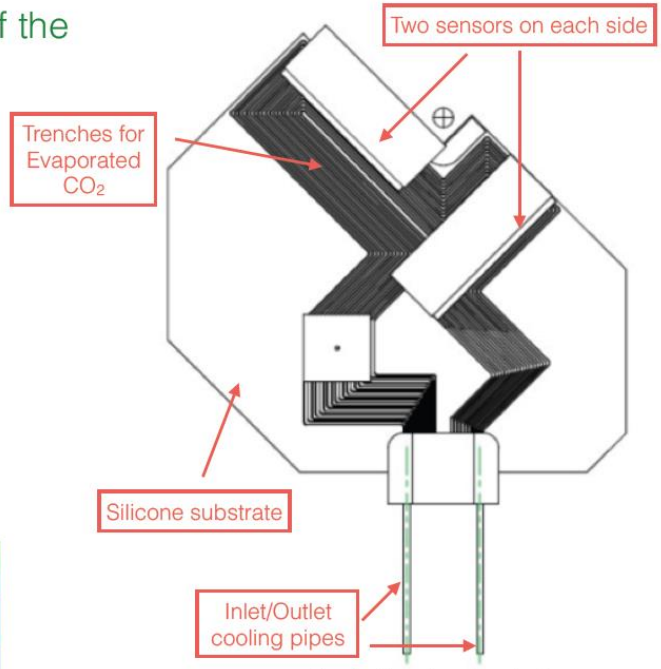
Evaporated CO2 flows via micro channel etched in the silicon substrate

Will act as the mechanical backbone of the module

- 2 sensors mounted on either side
- High thermal efficiency
  - Direct contact with ASIC surface
  - 19 channels under each ASIC
- Lower material budget
  - Combined thickness of 400μm
  - Trenches are 120μm deep
- Full sensor maintained at -30°C
- Radiation hard



Thermal map from simulation (°C), variation of less than 1°C



Sketch of the micro-channel substrate

05/09/2016 Emma Buchanan PIXEL 2016 10

Radiation Dose for the VELO

The radiation numbers for the VELO upgrade are estimated at the full integrated luminosity of 50 fb^{-1}

Sensors and VeloPix ASIC will receive 8 x 10^15 (1 MeV) neutron equivalent fluency or 400 MRad ionising dose(4 MGray)

The hottest part of the tape will receive a dose of approximately 2 x 10^13 (1 MeV) neutron equivalent or a dose of 30 kGy

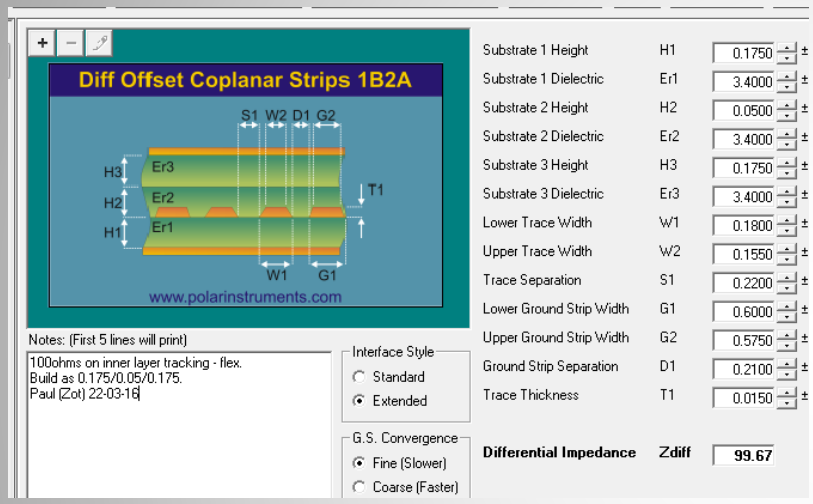
The OPBs will receive a dose of up to 2.5 kGy

NIEL is non-inonizing energy loss and is normally measured in 1 MeV neutron equivalent per cm^2

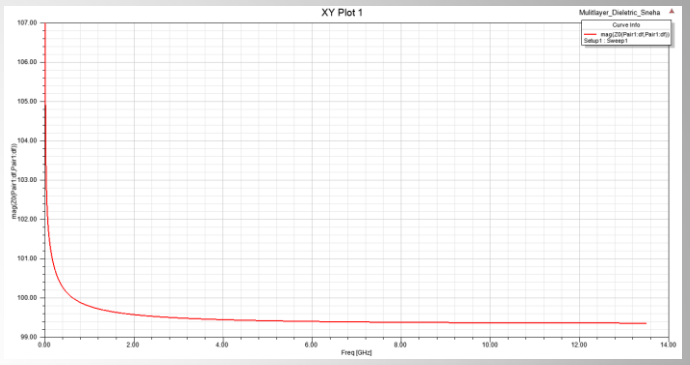
TID is total ionising dose and is measured in Rad or Gray

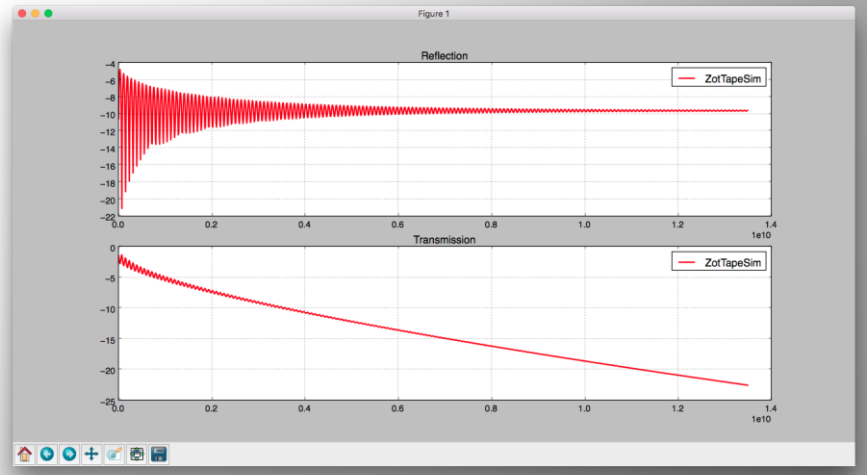
Simulation and calculation for controlled impedance

Data tape impedance calculations



Impedance calculation using Polar Calculator





Impedance calculation using Ansys software

Detail build of the OPB

8 LAYER
Construction#12289

0.236 VT47 Core 0.20mm (UL) 18/18 Tg 180c*
0.197 VT47 PrePreg 7628 Tg 180c RC 45% (U
0.270 VT47 Core 0.20mm (UL) 35/35 Tg 180c*
0.078 VT47 PrePreg 1080 Tg 180c RC66% (UL
0.197 VT47 PrePreg 7628 Tg 180c RC 45% (U
0.078 VT47 PrePreg 1080 Tg 180c RC66% (UL
0.178 Isola I-Tera 0.125mm 35/18 (200Tg)
0.093 Isola I-Tera Prepreg 1086 - 65% Resin (2
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0.178 Isola I-Tera 0.125mm 35/18 (200Tg)

Layer	100 ohms track/gap(mm)	Cu Thickness
Top Layer (components and traces)	ref plane	18um + plating
Signal (non critical-a few differential pairs running at 80 MHz)	0.119/0.181	18um
GND_FH(Split plane)	ref plane	35um
PWR_FH(split plane)		35um
DGND_FH	ref plane	35um
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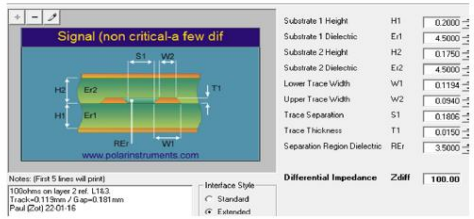
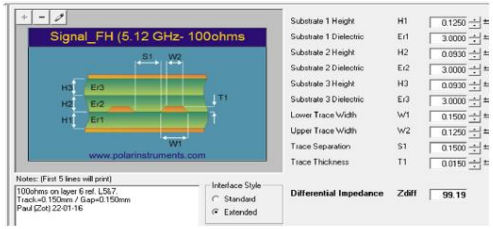
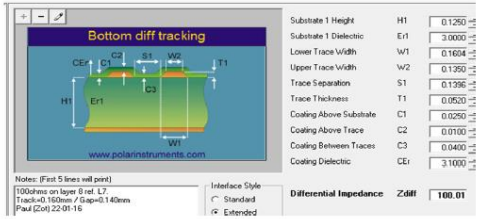
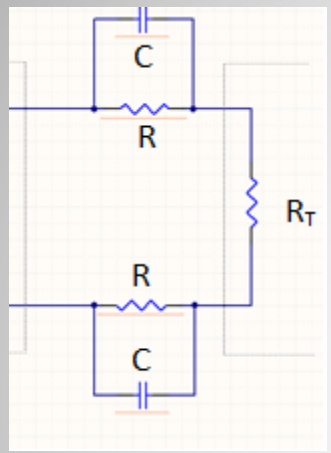


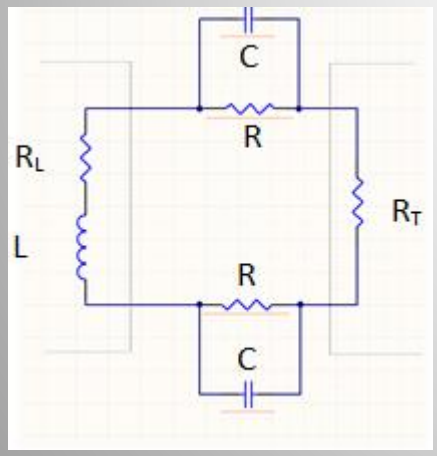




Simple CTLE circuit

Link input





Perhaps split L in two parts for symmetric design

R_T: Input impedance of GBLD
R, C: CTLE components to be optimised

Transfer function

$$H(j\omega, R, C) = \frac{1 + j\omega RC}{1 + \frac{2R}{R_T} + j\omega RC}$$

Input impedance

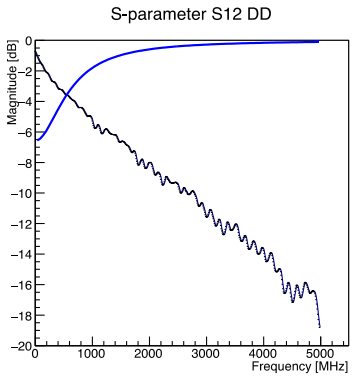
$$Z_{in} = \frac{2R + R_T + j\omega R_T RC}{1 + j\omega RC}$$

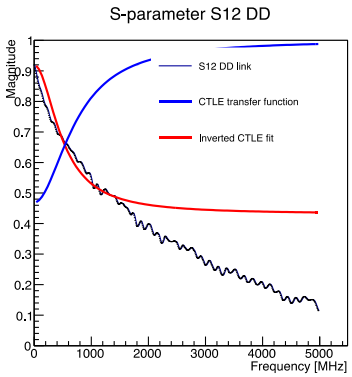
Add L-R at the input to compensate for Z_{in}

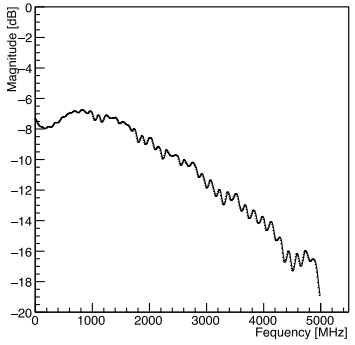
$$\begin{cases} R_L = R_T + \frac{R_T^2}{2R} \\ L = \frac{R_T^2 C}{2} \end{cases} \implies Z_{in} = R_T \ \forall \ \omega$$

Doesn't change the transfer function

Fit to f_{max} = 1750 MHz







Fit from 10 to 1750 MHz

R_T = 100 Ω

R = 56.6 Ω

C = 42.8 pF

R_L = 188.3 Ω

L = 214.2 nH

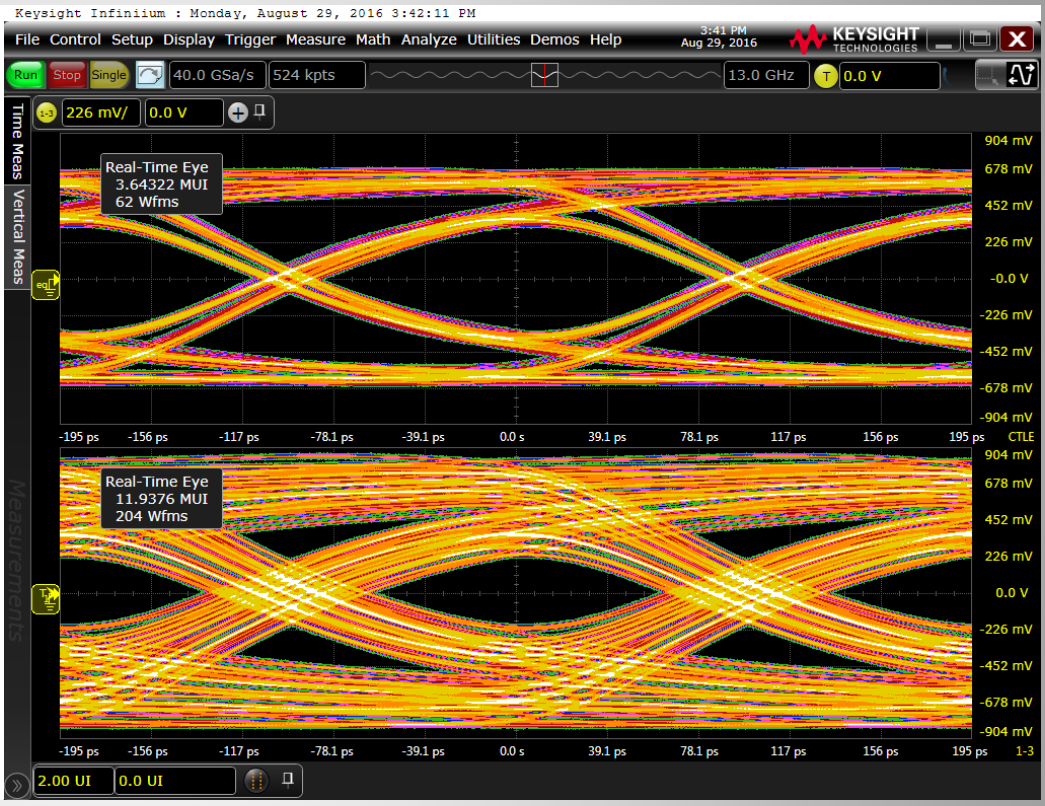
DC Gain A_{DC} = 0.469

Zero f_z = 65.6 MHz

Pole f_p = 139.9 MHz

S12DD (link x ctle) @ 10 MHz = -7.3 dB

S12DD (link x ctle) @ 2.5 GHz = -9.8 dB



Amplitude	1.34V
Jitter	32ps
Eye Width	164.5ps
Eye Height	645.7mV