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Silicon pixel-detector R&D for CLIC

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Abstract: The physics aims at the future CLIC high-energy linear e+e- collider set very high precision requirements on the performance of the vertex and tracking detectors. Moreover, these detectors have to be well adapted to the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of a few μm, ultra-low mass (~ 0.2 %X_0 per layer for the vertex region and ~ 1 %X_0 per layer for the outer tracker), very low power dissipation (compatible with air-flow cooling in the inner vertex region) and pulsed power operation, complemented with ~ 10 ns time stamping capabilities. A highly granular all-silicon vertex and tracking detector system is under development, following an integrated approach addressing simultaneously the physics requirements and engineering constraints. For the vertex-detector region, hybrid pixel detectors with small pitch (25 μm) and analog readout are explored. For the outer tracking region, both hybrid concepts and fully integrated CMOS sensors are under consideration. The feasibility of ultra-thin sensor layers is validated with Timepix3 readout ASICs bump bonded to active edge planar sensors with 50 μm to 150 μm thickness. Prototypes of CLICpix readout ASICs implemented in 65 nm CMOS technology with 25 μm pixel pitch have been produced. Hybridisation concepts have been developed for interconnecting these chips either through capacitive coupling to active HV-CMOS sensors or through bump-bonding to planar sensors. Recent R&D achievements include results from beam tests with all types of hybrid assemblies. Simulations based on Geant4 and TCAD are used to validate the experimental results and to assess and optimise the performance of various detector designs.

Keywords: Hybrid detectors; Solid state detectors; Electronic detector readout concepts (solid-state)

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1 Introduction

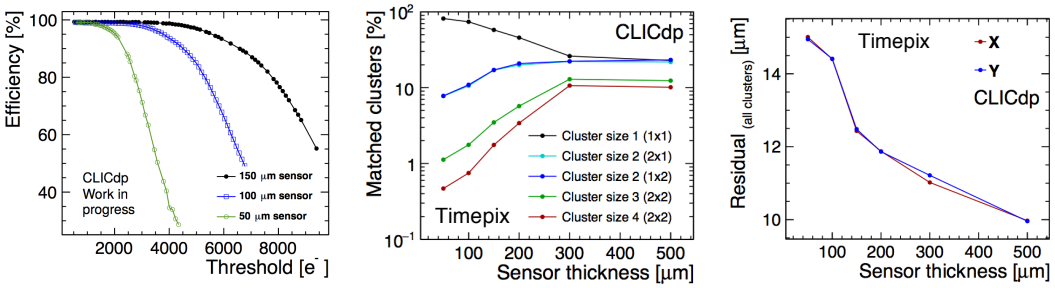
The Compact Linear Collider (CLIC) is an e+e- linear collider proposed for the post HL-LHC phase [1, 2] providing collision with a center-of-mass energy of up to 3 TeV [3]. Its physics goals are precision measurements of standard model processes, precision measurements of potentially discovered new physics at the LHC and the direct and indirect search for new physics, where its unique sensitivity to particles with electroweak charge is complementary to hadron colliders.

The prospect of precision studies imposes challenging requirements on the detector. For the vertex and tracking detector, this manifests in a very low material content of 0.2 %X_0 per layer in the vertex and 1–2 %X_0 per layer in the tracking detector, an excellent single point resolution of 3 µm in the vertex and 7 µm in the tracking detector, and a time-tagging capability of 10 ns. For the vertex detector, the tolerable material does not allow for liquid cooling of the detector. The foreseen forced air-flow cooling limits the power consumption to 50 mW cm^{-2}.

In order to demonstrate the feasibility to build the proposed detector, the CLIC detector and physics collaboration (CLICdp) is pursuing a R&D program adressing the vertex and tracking detector simultaneously.

2 Thin planar pixel sensors

Planar silicon sensors are under study as an option for the CLIC vertex detector. The stringent limit on the material budget makes it necessary to use very thin sensors and readout ASICs. Test beam studies performed in [4] on sensor assemblies with different thickness using Timepix [5] and Timepix3 [6] readout ASICs have shown that even for 50 µm thin sensors, operated at full depletion,



(a) Efficiency vs. threshold.

(b) Fractional cluster size distribution vs. sensor thickness, from [4].

(c) Residual width vs. sensor thickness, obtained using the eta-algorithm to correct for non-linear charge sharing, from [4].

Figure 1. Summary of the thin sensor test beam study using Timepix readout ASICs.

a high detection efficiency > 99 % can be achieved, if the noise conditions and the readout chip allow the detection threshold to be set at or below 1000 electrons. In Figure 1a, the achieved detection efficiency as a function of the comparator threshold in the readout chip is illustrated for sensor thicknesses ranging from 50–150 µm. The relatively small signal in the order of 4000 electrons in a 50 µm thin sensor demands the threshold to be set as low as possible for fully efficient operation, whereas the higher signal in the thicker silicon sensors allows the threshold to be set to higher values without significantly degrading the detection efficiency.

The achievable position resolution in the assemblies under study is limited by the lack of charge sharing, especially in thin sensor layers, as shown in Figures 1b and 1c. Due to the short charge collection time in thin sensors, the lateral diffusion of charge carriers is limited, leading to only a small fraction of hits for which the charge is shared between two or more neighboring pixels. Charge sharing is necessary to improve the resolution of the reconstructed position of the particle hit below the binary limit of pitch/$\sqrt{12}$, using the charge-weighted center-of-gravity of the pixels above threshold or more sophisticated algorithms, like the eta-algorithm to correct for non-linear charge sharing effects.

3 Thin planar pixel sensors with active edge

In order to further reduce the material budget in the vertex detector, planar sensors with active edge are studied. These sensors, in combination with through-silicon-via (TSV) technology on the ASIC side, would allow for a seamless four-side tiling of the sensor assemblies, and thus omit the need for overlapping sensor edges for full coverage of the detection layers.

The activation of the sensor edge is achieved by etching the sensor edge down to a handling wafer and afterwards implanting the cut edge in order to extend the backside implantation onto the edge [7]. By that, the depletion zone can reach the edge of the sensor and charge generated in the edge region by a traversing particle is collected by the first row of pixels and thus allows the sensor to be fully efficient up to its physical edge.

Due to the reduced clearance between the ground potential on the last pixel implant and the backside potential on the cut edge compared to sensors without active edge, these sensors are

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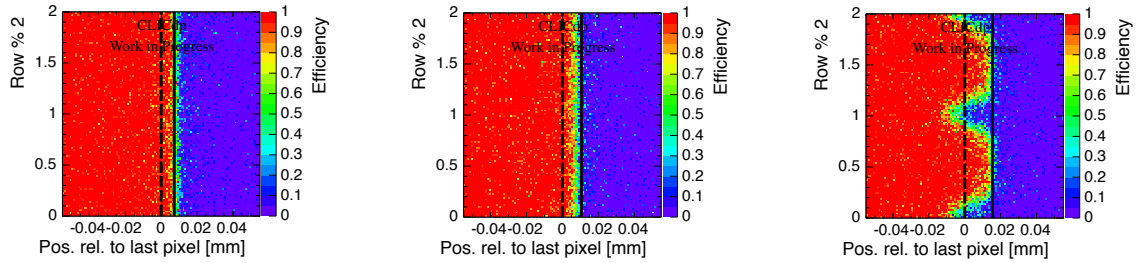

(a) No guard ring. **(b)** Floating guard ring. **(c)** Grounded guard ring.

Figure 2. Summary of the edge efficiency in 50 µm thin planar active edge sensors. Three sensors with three different guard ring configurations are shown, from [8].

potentially prone to early breakdowns in the edge region. To soften the potential drop between the pixel implant and the bias electrode, guard rings can be placed in the edge region. If the guard ring is kept floating, it can adjust to the electrostatic potential on the sensor surface and by that lead to a soft transition between the pixel and the edge, whereas if forced to ground potential, it will compete in charge collection with the last pixel.

Both guard ring configurations, as well as active edge sensors without guard ring, have been studied in test beam campaigns using Timepix3 readout ASICs [8]. Figure 2 summarizes the detection efficiency close to the edge for the three different cases. The silicon sensor is located in the left part of each figure, the end of the regular pixel matrix is indicated by the vertical dashed line and the physical edge of the sensor is indicated by the vertical solid line. The entry in the histogram is defined by the reconstructed track position, and one of the two edge columns is projected on a 110 µm × 110 µm grid. In comparison to the device without guard ring and the device with floating guard ring, which are both fully efficient up to the physical edge of the sensor, the assembly with grounded guard ring shows inefficient regions in the area between two pixel rows. For particle tracks passing in this region, the guard ring is the most dominant drain for the ionization charge, rather than the pixel implants. For this reason, the amount of charge collected by the pixel matrix is not sufficient to surpass the comparator threshold in the frontend, and the assembly is not fully efficient any more. This behaviour has been reproduced using finite-element T-CAD simulations.

4 Single layer tracking

Exploiting the 1.56 ns time binning of the Timepix3 readout ASIC, the possibility of reconstructing tracks using a single thick silicon sensor has been studied [9]. Similar to the principle of operation of a time projection chamber, the origin of the charge carriers along the sensor depth can be extracted from the arrival time on the readout electrodes.

This concept has been tested using a 675 µm thick p-on-n planar silicon sensor. The sensor has been placed at various rotation angles around the column direction in a 120 GeV pion beam in a Timepix3 reference telescope at the SPS H6 beamline at CERN. Two approaches have been pursued to extract the incidence angle from the sensor response, an analytic extraction of the depth from the drift time and a machine learning approach using additional input variables. The analytic approach is based on a parameterization of the electric field in the sensor volume. From that,

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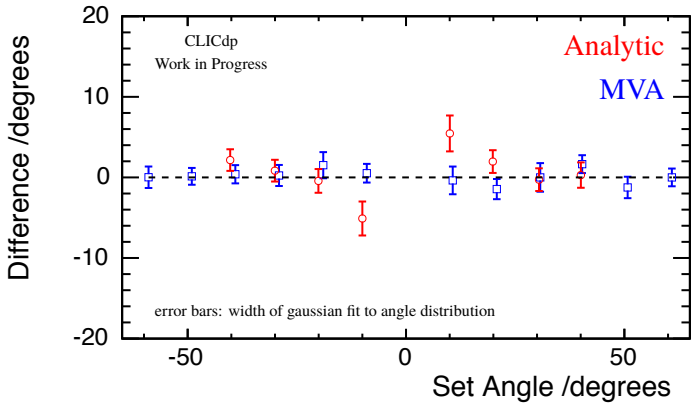

Figure 3. Difference between the reconstructed incidence angle and the true incidence angle, using single layer track reconstruction, from [9].

the drift mobility and velocity of electrons and holes is extracted along the sensor depth and by integration of the velocity, the depth can be extracted from the measured drift time. In the machine learning approach, a neural network has been given four input variables which are extracted for each particle hit: the timing gradient along the cluster, the total charge in the cluster and the size of the cluster in both directions. Using the reconstructed incidence angle in the telescope, the network is trained on a fracton of the data sample, covering the full angular range.

In Figure 3 the difference between the angle as reconstructed using the single layer reconstruction and the true angle for both methods is shown as a function of the true incidence angle obtained from the alignment in the telescope. With both methods, it is possible to extract the angle over the full range, however, the response of the neural network is more linear and on average closer to the true value. The achieved resolution is ~ 2 deg.

The single layer tracking could possibly simplify the pattern recognition for the track reconstruction in the CLIC main tracking detector, as well as be beneficial in suppressing background hits from particles not originating from the interaction point. The limit on the material budget in the main tracking detector is less stringent than for the vertex detector, the use of 675 µm thick silicon sensors is however also here not feasible. For this reason, the resolution achievable with this method using thinner sensors in the order of ≤ 300 µm thickness is currently under study.

5 Planar pixel sensors on CLICpix ASICs

As demonstrated in Figure 1c, the readout pitch of 55 µm of the Timepix ASIC is not sufficient to achieve the goal on the spatial resolution of 3 µm in the vertex detector, in particular not using 50 µm thin sensors. For that reason, a dedicated demonstrator chip, CLICpix, aiming at the requirements of the CLIC vertex detecor has been developed [10]. It is fabricated in a 65 nm CMOS process and provides a pixel matrix of 64×64 pixels at a pitch of 25 µm. The Time-over-Treshold and Time-of-Arrival are measured with 4-bit precision each.

To study the achievable resolution using such fine pitch, 200 µm thick planar sensors have been bump bonded to CLICpix ASICs using an indium process at SLAC [11]. The assemblies have been tested in a 120 GeV pion beam at the SPS H6 beam line at CERN.

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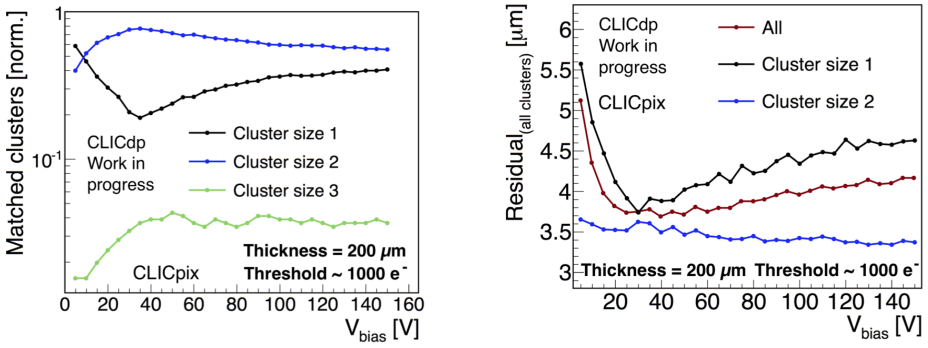

(a) Cluster size. **(b)** Resolution.

Figure 4. Summary of test beam results obtained on a 200 µm thick planar sensor connected to a CLICpix readout ASIC.

The fraction of hits with a certain number of pixels in the charge cluster is illustrated in Figure 4a as a function of the applied bias voltage. As opposed to the studies discussed in Section 2 using Timepix ASICs with larger readout pitch and the same sensor thickness of 200 µm, clusters with two pixels above threshold are most abundant. The largest fraction of hits containing two pixels is obtained at the full depletion voltage of 35 V. At that voltage, only 20 % of the hits contain a single pixel. Single pixel hits appear mostly for tracks hitting the central region of the pixel cell. Because of that, the achieved resolution for single pixel clusters it better than the geometric limit in the absence of charge sharing of pitch/$\sqrt{12}$.

The smaller pixel size of the CLICpix assemblies results in an improvement of the resolution for two reasons. One is the direct effect of the finer pixel granularity, the other is the increased charge sharing. In agreement with this expectation, the resolution has been measured to be 4 µm at the optimal operation voltage, as illustrated in Figure 4b. With 50 µm thin sensors, the resolution is expected to be worse. CLICpix assemblies with thinner planar sensors are currently under study.

6 Active HV-CMOS sensors

Active CMOS sensors with an integrated amplifier in each pixel are a possibility to overcome the need for bump bonding at the fine pixel pitch of 25 µm. Due to the amplification stage, the signal obtained by this type of sensor is large enough to couple the sensor capacitively to the readout chip, by gluing the two together, as sketched in Figure 5a. Sensors, dubbed CCPDv3, matching the CLICpix layout have been produced in a 180 nm High-Voltage CMOS process. In each pixel, a deep n-well acts as collecting electrode and is simultaneously shielding the electronics from the substrate bias. The signal collected by the n-well is amplified by a two-stage amplifier with a rise time of 120 ns. By applying a reverse bias voltage, a depletion layer around the n-well is formed, which results in a fast signal collection by drift from the depleted volume. CCPDv3 sensors have been glued to CLICpix ASICs, as depicted in Figure 5b. The assemblies have been tested in the AIDA telescope at the SPS H6 beam line at CERN in a 120 GeV pion beam.

It has been shown in [12], that even without applied bias voltage and a detection threshold of 1200 electrons the efficiency of the assembly is higher than 98 %, increasing to 99.9 % at 60 V and

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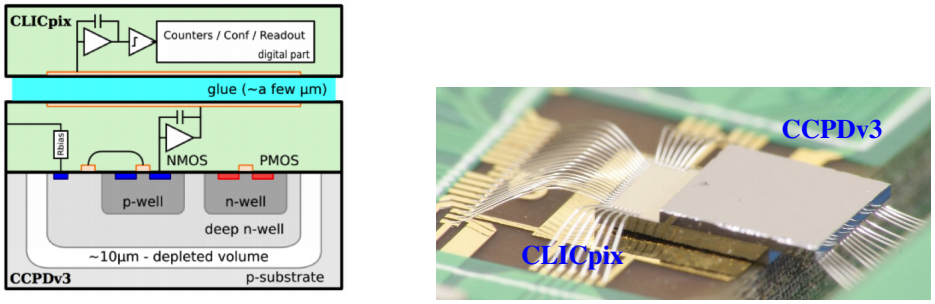

(a) Schematic. **(b)** Assembly on readout board.

Figure 5. Capacitive coupling of an active sensor to the CLICpix ASIC via a thin layer of glue.

above. Due to the small depletion layer and the resulting lack of charge sharing, the resolution obtained with the detector assembly is only about 6 µm.

An improved, larger version of the readout ASIC, dubbed CLICpix2, is currently in the final design verification stage, whereas the matching active HV-CMOS sensor, dubbed C3PD, has already been fabricated. First standalone characterizations demonstrate the expected performance of the C3PD chip, e.g. the improved rise time of the amplifier of 20 ns.

7 Integrated technologies

Fully integrated sensors would overcome the need for an electrical interconnect between the sensor and readout chip. Two different technologies are currently studied in the framework of the R&D for CLIC: a quadruple-well process allowing both n-MOS and p-MOS transistors to be used in the pixel frontend on a high-resistivity substrate, and a Silicon-On-Insulator (SOI) process where the electronics are implemented on a low-resistivity wafer, separated by a buried oxide layer from a fully depleted high resistivity sensing layer.

The Investigator chip is a test chip developed by the ALICE collaboration to study the influence of the collection diode geometry and pixel layout on the charge collection performance. It is fabricated in a 180 nm quadruple-well CMOS process on a high-resistivity epitaxial substrate. The chip consists of 134 pixel matrices with 8×8 pixels each. One matrix at a time can be connected to the readout. Each pixel contains only the analog amplification stage, the digitization of the signal is performed by 64 external ADCs located on the readout board. The pixel size varies between 20 µm × 20 µm and 50 µm × 50 µm. In order to obtain a fast signal response, the collection-diode geometry has been optimized to minimize its capacitance.

In the scope of the pixel R&D for CLIC, the Investigator chip has been tested in the Timepix3 beam telescope at the SPS H6 beamline at CERN using a 120 GeV pion beam. The spatial and timing resolution of a pixel submatrix with a pixel size of 28 µm × 28 µm has been studied at the highest possible bias voltage of 6 V. Using this pixel layout, the achieved spatial resolution is 5 µm and the timing resolution with respect to the reconstructed particle track in the reference telescope is 7 ns, indicating that the analog performance of this technology meets the CLIC tracker requirements.

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A prototype chip in the SOI technology has been fabricated and first measurements performed in a test beam are currently being analysed.

8 Summary and conclusion

The precision phyics prospects as well as the experimental conditions at CLIC set challenging requirements to the vertex and tracking detectors on spatial and timing resolution, material budget and power dissipation. A comprehensive R&D program is ongoing, adressing all technological aspects of the detector. In the scope of this program, several silicon pixel detector concepts are under consideration, ranging from thin, fine-pitch planar sensors bump-bonded to readout ASICs to more advanced concepts like capacitively coupled detectors or fully integrated approaches, combining the sensing and electronics part on the same silicon wafer. All investigated technologies have their specific advantages and disadvantages. So far, no conclusion on the best suited technology has been drawn.

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