# A FAST INTERLOCK DETECTION SYSTEM FOR HIGH-POWER SWITCH PROTECTION

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*Abstract*

Fast pulsed kicker magnet systems are powered by high-voltage and high-current pulse generators with adjustable pulse length and amplitude. To deliver this power, fast high-voltage switches such as thyratrons and GTOs are used to control the fast discharge of pre-stored energy. To protect the machine and the generator itself against internal failures of these switches several types of fast interlocks systems are used at TE-ABT (CERN Technology department, Accelerator Beam Transfer). To get rid of this heterogeneous situation, a modular digital Fast Interlock Detection System (FIDS) has been developed in order to replace the existing fast interlocks systems. In addition to the existing functionality, the FIDS system will offer new functionalities such as extended flexibility, improved modularity, increased surveillance and diagnostics, contemporary communication protocols and automated card parametrization. A Xilinx Zynq®-7000 SoC has been selected for implementation of the required functionalities so that the FPGA (Field Programmable Gate Array) can hold the fast detection and interlocking logic while the ARM® processors allow for a flexible integration in CERN's Front-End Software Architecture (FESA) [1] framework, advanced diagnostics and automated self-parametrization.

## PRINCIPLE

In Fig. 1 a simplified schematic of a kicker system is shown. In general one can assume a system with matched impedances. A typical operation consists of charging the Pulse Forming Network or Line (PFN/PFL) to a voltage V by a Direct Current or Resonant Current Power Supply (DCPS/RCPS). When the main switch closes, a pulse of magnitude V/2 (if matched) propagates through the transmission line to the magnet. The pulse's energy is dissipated in the terminating resistor and full-field is established in the kicker magnet once the pulse reaches this resistor. Note that the magnet termination can also be a short-circuit, which doubles the magnet current because of reflection but also doubles the required fill-time of the magnet [2]. The pulse length in the magnet can be controlled by adjusting the timing of the dump switch relative to the main switch. When a sharp falling edge of the magnetic field is required for systems using a PFN, a clipper switch to ground is added between the PFN and the main switch. Typical values are 50 kV and 10 kA that traverse the magnet with pulse lengths between 500 ns and 600 µs.

During operation the system might be interlocked because of malfunctioning of one of the High Voltage (HV) switches. These malfunctioning causes are called *fast interlocks*, which

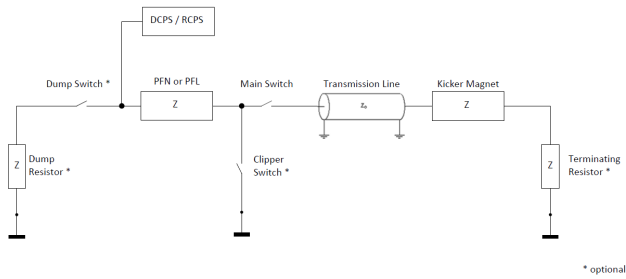


Figure 1: Simplified kicker system.

are detected over a large range of PFN voltages (i.e. the system's dynamic range). In addition to interlocking, they have often also a corrective action such as pulsing other magnets in order to fully deflect the beam and to avoid beam losses, i.e. to protect the machine. The following list gives a basic overview of the different types of fast interlock events:

- **Normal conduction** is not a fast interlock per se but for statistical reason it is useful to count the normal conduction cases.
- **Missing conduction** is registered when a trigger occurs but the switch is not pulsed. Lack of current in a HV switch or a missing load current after a certain amount of time after the trigger will result in a missing detection.
- **Erratic conduction** is the spontaneous conduction of an HV switch caused by tube or semiconductor malfunctioning as opposed to conduction following the normal triggering action. The FIDS mechanism registers an erratic when the switch conducts with no corresponding trigger pulse present.
- **Short-circuits** might happen at several locations, starting from the PFN up to a Terminating Resistor (TR). Depending on the magnet configuration several detection techniques exist, e.g. for short-circuited magnets one can compare the delay between the forward Main Switch (MS) pulse and the Dump Switch (DS) inverse current which, for normal operation, should represent the two-way transmission delay through the cable and magnet plus the single-way delay through the PFN.
- **No dump switch forward current** is the case when, for short-circuited magnets or systems with a Clipper Switch (CS) only, the short-circuit will reflect the travelling wave and the DS will have to withstand an inverse current (i.e. current from cathode to anode). In case of hollow-anode thyratron types, it is vital for the lifetime of the thyratron that it will first conduct forward current (i.e. anode to cathode) before the arrival of the inverse current.

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A generator has several pick-up probes installed for analysis of the current and/or voltage. Resistive and capacitive voltage dividers are used as well as current transformers. The idea behind the FIDS is to sample these analog signals and their related trigger signals and perform an analysis to detect as fast as possible one of the above mentioned events. In case of an erratic conduction for example, we often need to pulse other magnets within 500 ns to reduce beam losses. After a certain amount of occurrences we would want to stop, i.e. interlock, the generator for expert intervention. Important in the analog signal sampling is a high signal-to-noise ratio (SNR), especially because many kicker generators have a wide dynamic range. In a simplified view the FIDS thus generates pulse outputs based on the relative timing of its input signals and communicates events to the upper-layer control system.

## PROTOTYPE

A wide variety of electronic modules had been produced in the past and the FIDS principle of operation is based on an existing module, called Thyratron Protection Unit (TPU), by moving most of the functionality from analog discrete components to digital logic in an FPGA. This digitization will allow for more flexibility and an automated parametrization while adding improved communication possibilities. A prototype has been designed to verify the principle of operation and to perform several tests on dedicated installations available for development and testing. An FPGA was a logical choice to implement most of the digital logic because of the required reaction time (<500 ns) and the flexibility for designing hardware logic that differs per installation.

Figure 2 shows a block diagram that explains the prototype's functionality and the chosen hardware. All analog input signals need to be converted to digital values so that pulse edges and pulse lengths can easily be compared in time to detect a fast-interlock event. A possible method is to sample all signals with an Analog-to-Digital Converter (ADC) and use digital bit vectors inside the logic. Because of the high bandwidth of the pick-up signals (100 MHz) however a different approach was chosen. Analog comparators will be used to produce a 1-bit signal that indicate the presence of a current or voltage. This simplification will not limit the FIDS' performance because the signal amplitude itself is generally of no importance. It is important however that the SNR is taken into account for the full dynamic range of the input signals. This can be done by having the comparator reference follow the PFN's amplitude to control the comparators switching level at low PFN voltages. An additional advantage of the comparator-based approach is that additional latency due to ADC conversion and communication is avoided.

To implement the variable comparator reference the bipolar PFN voltage is sampled by an ADC after passing through an instrumentation amplifier and low-pass filter. Charging a PFN takes a considerable amount of time so a 10 kHz low-pass filters out transients and harmonics before digitalisation.

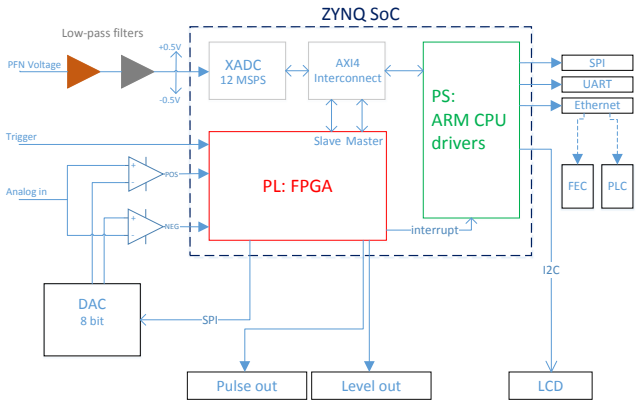


Figure 2: Prototype block diagram.

The digitalised value is used to set the comparator reference after applying a factor multiplication and offset addition. This factor and offset are user-selectable and depend on the kicker installation. A Digital-to-Analog Converter (DAC) translates the calculated value to an analog output that is used as comparator reference. Each bipolar analog input signal passes through two comparators so that a positive and negative amplitude can be detected, as often the case for the DS.

### *Hardware*

Several FPGA evaluation boards were considered to reduce prototyping time. Taking into account the lifetime of the FIDS a recent FPGA family is preferred. Historically Xilinx® has been used in TE-ABT and conveniently their relatively new 7 Series FPGA family has two ADCs (12 MSPS) included - an ideal fit for sampling the PFN voltage. Furthermore a rather recent FPGA manufacturer direction is a System on a Chip (SoC) where an FPGA, ARM® cores and Input/Output (I/O) peripherals, such as $I^2C$ and Gigabit Ethernet are included in one package. An internal interconnecting Advanced eXtensible Interface (AXI) bus can be used to link all components together - supported by the CPU cores as well. For the FIDS the Xilinx® Zynq®-7000 is an ideal fit for the prototype because the SoC can lead to significant development time gains. Finally the MicroZed™ low-cost development board was chosen. It includes the XC7Z010 SoC and several peripherals.

### *Software*

The development time gain is mainly achieved by running a bare metal application on the CPU that allows to interact with the FPGA without much effort. The bare metal application is written in Embedded C and can easily access memory-mapped registers in the designed FIDS Intellectual Property (IP) core through the AXI4-Lite protocol. Thanks to the SoC implemented UART peripheral, user I/O is as easy as using printf() and getchar() functions. In the case of a fast-interlock event the IP core will trigger a CPU in-



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terrupt which will put all data on the serial UART, such as the acquired PFN voltage and calculated comparator references. Thanks to the implemented $I^2C$ peripheral driver and C library it was no problem to quickly add a 2x16 character LCD to let the prototype run for days without needing a laptop for FIDS output visualisation using the UART.

In a second stage the SoC is used by deploying an Embedded GNU/Linux distribution, crafted together by using the Xilinx'®PetaLinux tools. The main reason for doing so was to use the kernel's TCP IP stack to easily interface the integrated MAC controller. The idea is to integrate the FIDS seamlessly in CERN's control topology by running a FESA class on the Embedded GNU/Linux distribution. Currently FESA is not available for the ARM® architecture and a port has yet to be studied and/or implemented. At the moment of writing the FIDS prototype has a user-space program that uses a free software library to communicate with Siemens PLCs over Ethernet. This is a future implementation that will often be the case for a kicker installation. Implementing GNU/Linux allows for more flexibility and better control but to properly register the FIDS IP core's interrupts and memory a kernel driver had to be written. Hence additional design time has to be taken into account for the implementation and configuration of Das U-Boot bootloader, the rootfs and the device tree.

### *Gateware*

The gateware for the FPGA is written in VHDL-2008, allowing for more generic packages and modules, and has two main functionalities:

- Interface with the XADC (Xilinx ADC), use of a linear formula to calculate the comparator reference and send it over SPI to the DAC.
- Detect the digitalised (single bit) pulse signals and generate fast-interlock events based on their relative timing and pulse length.

The implemented functionality was tested using a VHDL test bench with additional verification using the Property Specification Language (PSL) which is now part of the VHDL-2008 standard and supported by ModelSim.

Inside the design multiple clock-domains are used and to boost pulse measurement precision and pulse output latency, DSP48 slices have been used to clock the pulse length counters with a 250 MHz frequency. In a later stage the precision should be improved to 1 ns for which a more performant Zynq® SoC needs to be used so we can clock the ISERDES2 primitive at 1 GHz.

### *Preliminary Test Results*

After successful lab tests, the prototype has been tested on two different types of dedicated test installations: the 50kV SPS Beam Dump System (SBDS) and the -60kV Transfer Kicker (TK). These installations are installed in different accelerators and have different PFN lengths and charging methodologies (DCPS versus RCPS). Also the magnet configuration is different because the TK has a terminated magnet with MS and DS configuration while the SBDS has a MS that consists of a parallel combination of a thyratron with series ignitrons.

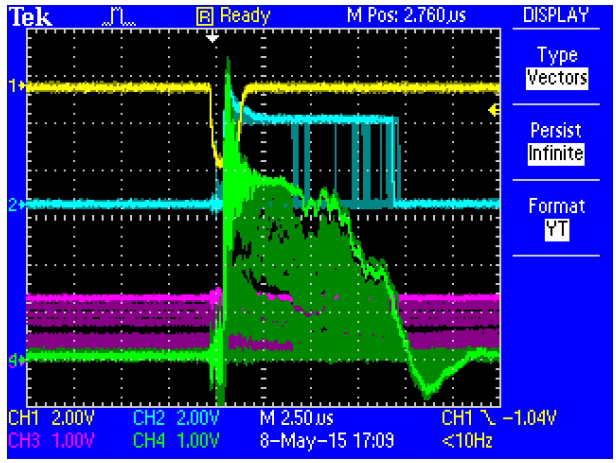


Figure 3: SBDS tests scope image; Ch1 (yellow): trigger, Ch2 (blue): comparator output, Ch3 (magenta): comparator reference, Ch4 (green): switch pick-up.

On Fig. 3 the oscilloscope waveforms of the SBDS thyratron switch are shown after a few hours of operation with infinite waveform persistence activated. The operating principle of the FIDS is clearly visible in this image because the installation was operated over its full dynamic range, i.e. from 5 kV to 45 kV. This PFN voltage, measured as a 0 to 2 V voltage from a resistive divider, is sampled by the XADC and used as comparator reference (Ch3 in magenta). When the PFN voltage increases, so does the reference according to the user parameters set by an FPGA register. In this example the linear formula used is y=1x+5 where the offset is controllable with 23 mV steps. A higher PFN voltage will result in an increased current through the thyratron (Ch4 in green). The comparator output, a digital signal, hence reflects the length of the current through the thyratron switch. This pulse is then used with reference to the trigger signal (Ch1 in yellow) to distinguish the fast-interlock event.

## FULL DESIGN

After successful concept verification, a strategy to develop a board, suitable for every existing and future installation, had to be found. Taking into account the projected lifetime it is important not to select technologies or protocols that will soon become obsolete. The form factor and scalability are equally important because of the variable size of kicker installations with single to tens of HV switches. Finally after thoroughly analysing all requirements and multiple discussions with other groups at CERN, the FPGA Mezzanine Card (FMC) approach was chosen. This ANSI/VITA 57.1 standard specifies an I/O mezzanine module that works in conjunction with an FPGA processing device. The focus is to obtain mezzanine modules that minimize the handling and formatting of the transceived data while conveniently not forcing interface protocols [3]. This allows for example to route the comparator outputs with low-latency differential

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signals directly to the FPGA while at the same time using a different subset of pins for DAC serial communication. The two main advantages of the use of the FMC standard for the FIDS are

- **Flexibility:** as mentioned before, kicker installations are complex and use several switches per generator and multiple generators per installation. Using a carrier with FMCs approach allows for adding functionality by simply plugging in an existing FMC.
- **Independency:** at the moment it is unclear what will be CERN's future CPU-bus and once chosen it is certain that this will change again, following the technology trends of the moment. Implementing the core functionality on a mezzanine allows for independency since it is easy to adapt to a new CPU bus by using the according carrier card.

In the following subsections the two basic parts of the system are detailed, being the FIDS FMC DIO 10i 80 module and the FIDS Carrier.

### *FIDS FMC DIO 10i 8o Module*

While adhering to the FMC standard has many advantages, one should not forgot the disadvantages of increased design time, small physical size and limited freedom for the Power Distribution Network (PDN). An important advantage however is that at CERN several carriers for different CPU-buses exist and a working FMC can be quickly put in use by using one of these carriers, which are open hardware [4]. FMC is a widely accepted standard and also at CERN different cards with a wide range of functionalities have been developed. In general the additional time spent for fitting a design into the FMC standard pays off if there is enough demand for the card. A high demand, thanks to a general design, could encourage the industry to include it in their catalogue which will yield smaller lead times and lower prices. Also the more users incorporate the card, the faster design mistakes can be found and resolved. Below in Table 1 the card specification is listed and it shows that the analog input stage, including the comparator reference producing DACs, are included. While still a perfect suit for the FIDS, it can easily be used by other users as a general purpose I/O card that offers more user I/O than any other card available today. The card will be made available on the open hardware repository as well [4].

### *FIDS Carrier*

As mentioned before at CERN several carriers such as the Simple VME FMC Carrier (SVEC) exist and the FIDS could make use of one of these to reduce overall design time. It was found however that none of the existing carriers included all of the required functionality so a specific carrier will be designed. The main features are two FMC slots, 6 analog inputs, fail-safe functionality and two Ethernet ports combined with the Zynq SoC. The full specification can be found in Table 2. They will be placed horizontally in a 19"rack and occupy a 1U slot.

Table 1: FIDS FMC DIO 10i 8o Specification

| Parameter | Value |
|---|---|
| Inputs | 10 analog comparator |
| Outputs | 8 TTL 1 ns rise time |
| Number of comparators | 20 (2 per input channel) |
| Comparator reference | 20 (1 per comparator) |
| Comparator input bandwidth | 1 GHz |
| Comparator input levels | ± 5V |
| Comparators to FPGA | LVDS |
| FMC to carrier interface | Low Pin Count (LPC) connector |
| Input impedance | High-Z or 50 Ohm |
| Programmable threshold | DAC with 5mV precision |
| DAC resolution | 12 bit |
| DAC Sampling rate | 166 kHz |

Table 2: FIDS Carrier Specification

| Parameter | Value |
|---|---|
| 2 FMC LPC slots | VADJ fixed to 2.5V for slot-1 and 1.8V for slot-2 |
| 6 analogue inputs | 2 MSPS ADC, 1 MHz BW, 12-bit, lemo-00, ±10 V input |
| 4 isolated outputs | 9-pin D-Sub male connector |
| 4 outputs | TTL level, rise-time < 10 ns |
| 4 high-power outputs | 15V, rise-time 20 ns, 1A peak output current |
| user-button | Momentary NO push-button |
| reset-button | Momentary NO push-button |
| 8 bi-colour user LEDs | 4 FPGA- and 4 CPU-controlled |
| Serial interface | I2C bus for connecting external LCDs and I/O expanders |
| JTAG header | Xilinx Platform Cable style |
| SPI Flash | Bootable, 2x 128 Mbit QSPI |
| SD card slot | For booting, OS mounting and persistent storage |
| Fail-safe functionality | FPGA and CPU watchdogs; voltage supervision; pulse output feedback |
| 2 Ethernet RJ45 ports | Ethernet switch; 1 SoC Ethernet MAC; 10/100 Mbps |

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