The development of the Global Feature Extractor for the LHC Run-3 upgrade of the ATLAS L1 Calorimeter trigger system

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On behalf of the ATLAS Collaboration

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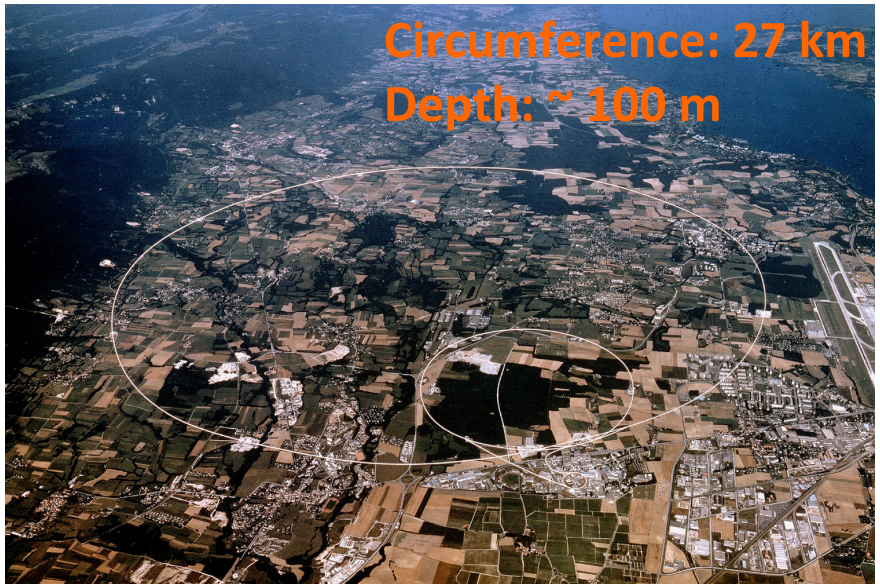
Outline

- An introduction of LHC
- An overview of Atlas with experiment and Level-1 trigger system
- gFEX in L1Calo phase-1 upgrade
- gFEX Pre-Prototype test results
- gFEX-LDPB link speed test
- gFEX Prototype design
- Summary

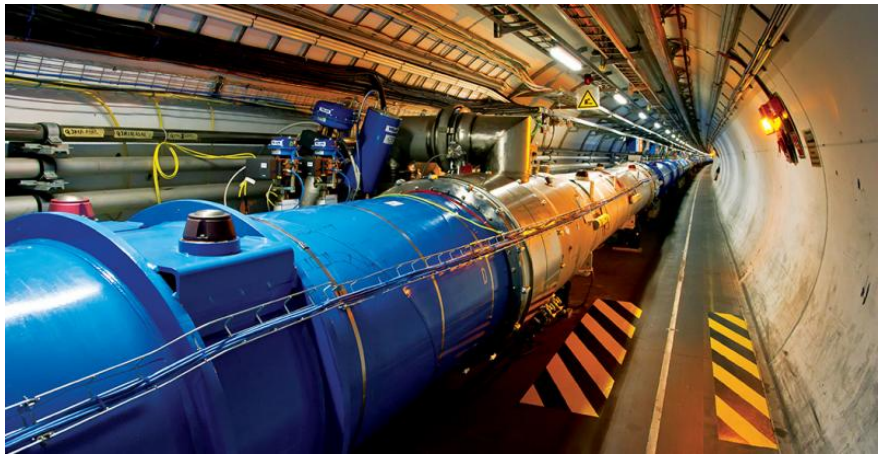
- Other ATLAS trigger system related talks:
  - The ATLAS Level-1 Topological Trigger Performance (Marek Palka, Friday)
  - Error detection, handling and recovery at the High Level Trigger of the ATLAS experiment at the LHC (Mark Stockton, Thursday)
  - FELIX: the new detector readout system for the ATLAS experiment (Julia Narevicius, Tuesday)

The Large Hadron Collider: LHC

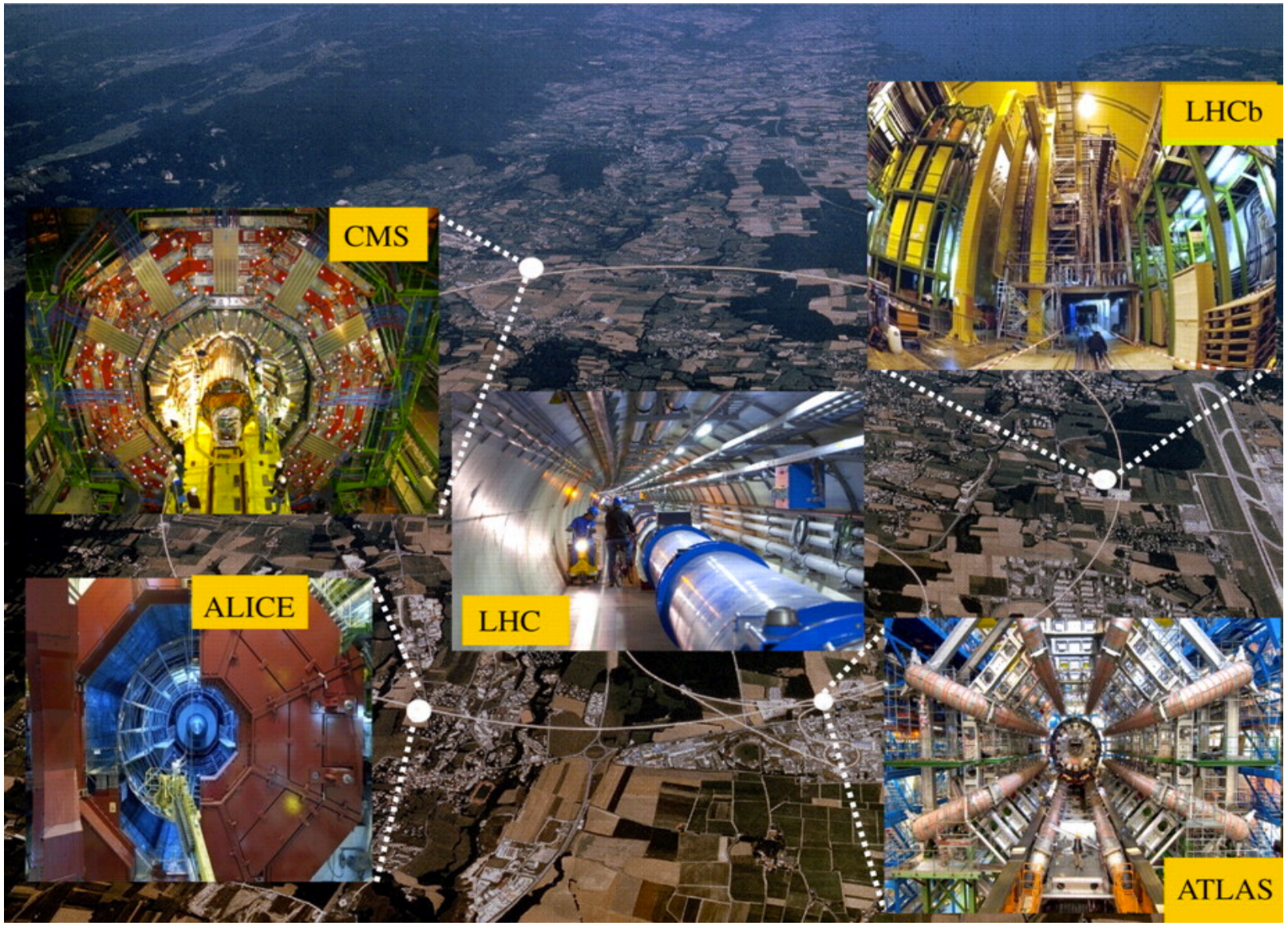
- The world's largest and most powerful particle accelerator
- Run-1: 2009 ~ 2013
  - 7-8 TeV, Luminosity ~ 0.8 x $10^{34}cm^{-2}s^{-1}$
- Run-2: started on 2015
  - 13-14 TeV, Luminosity ~ 1 x $10^{34}cm^{-2}s^{-1}$
- Run-3 starts on 2021 & Run-4 starts on 2026
  - Higher energy and luminosity



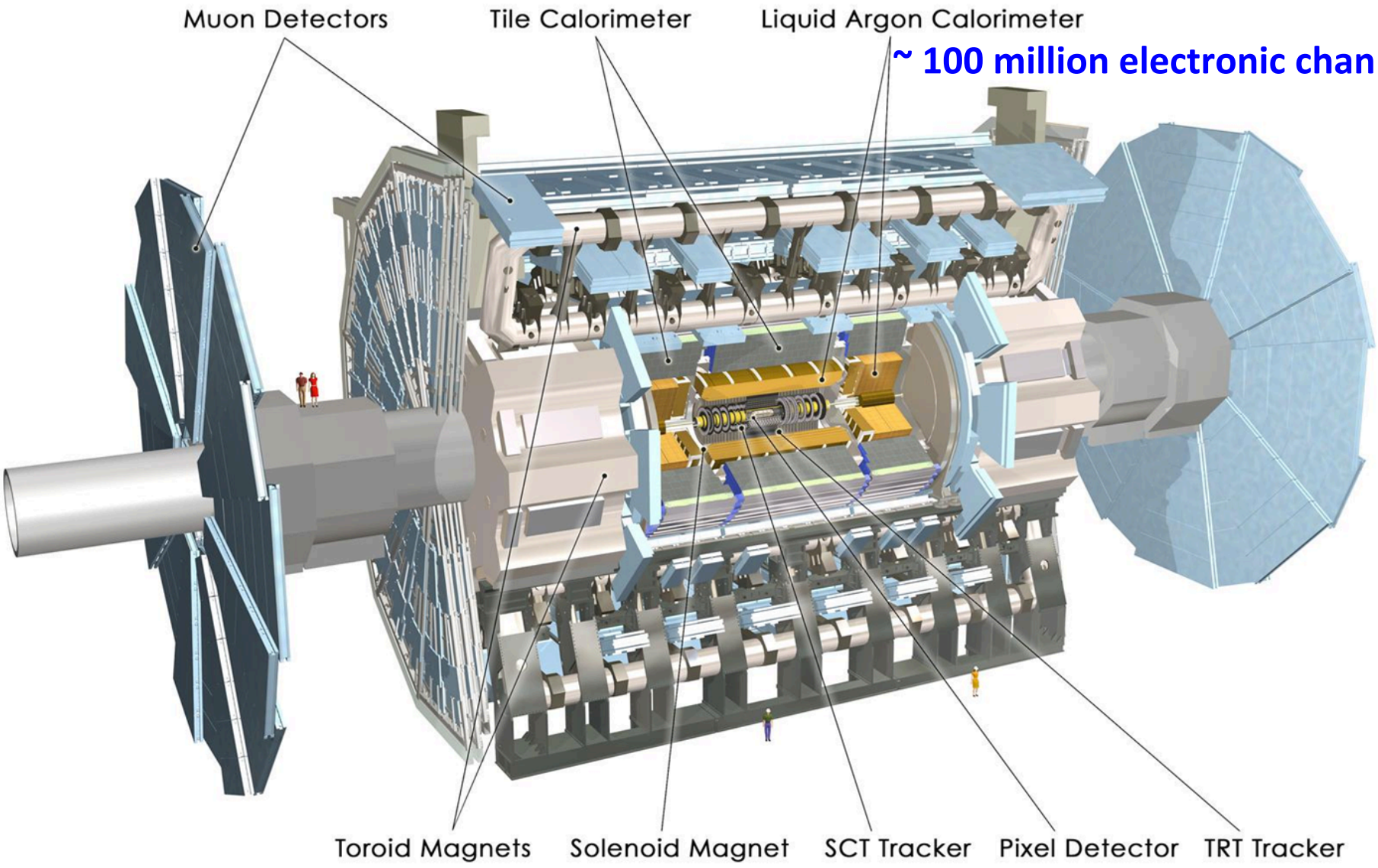
- Physics motivation
  - Standard Model is good, but still incomplete
    - Higgs particles have been found in 2012
    - 2013 Nobel Prize in Physics
  - Search dark matter and dark energy
  - Supersymmetric particles



The LHC Experiments



The ATLAS Experiment



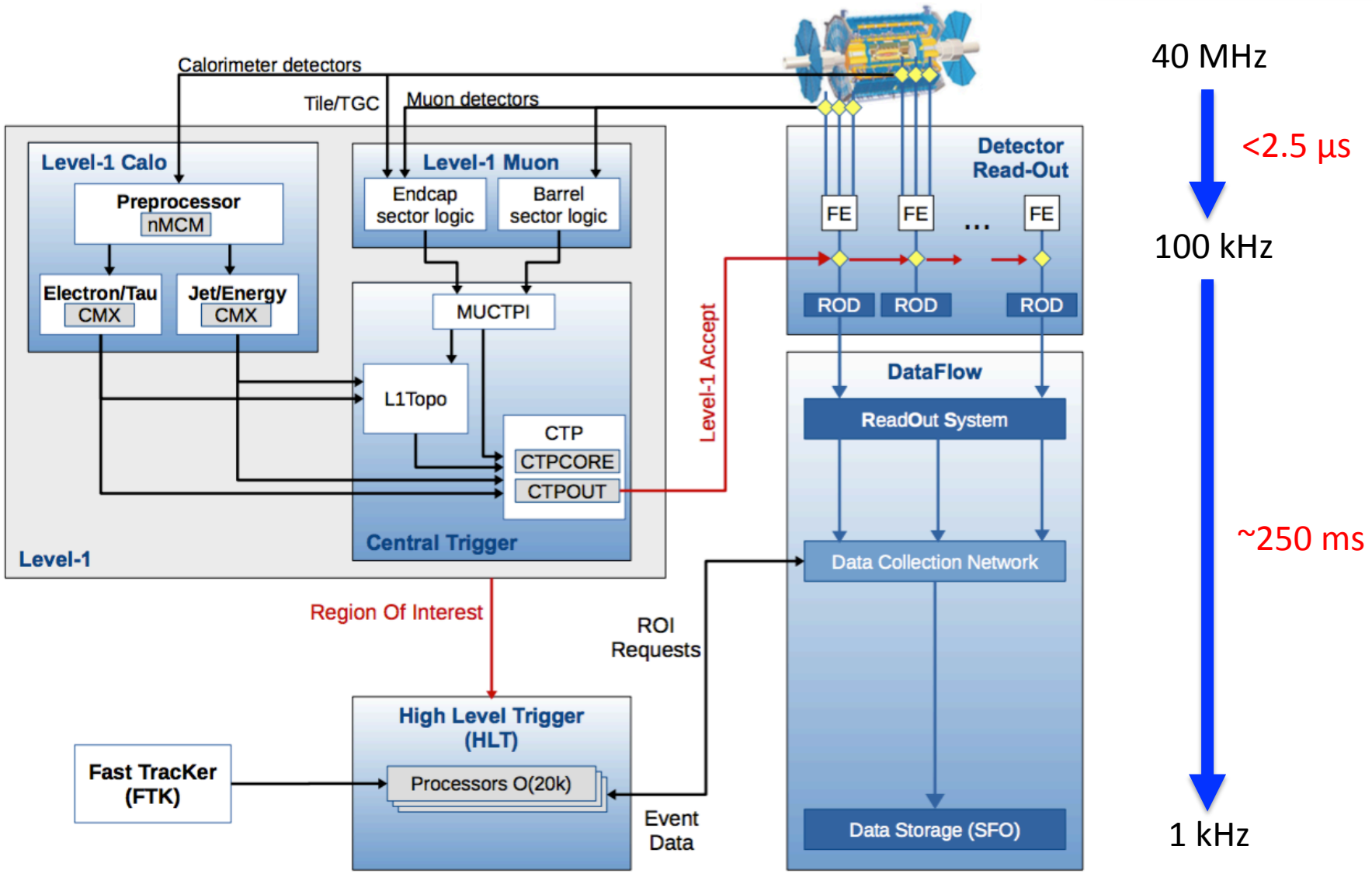
ATLAS Trigger Environment in Run-2

- Level-1 Trigger system:
  - Fast analysis of all collision events with reduced resolution
  - Select only interesting events
    - 1 MByte × 40 MHz = 40 TByte/s
    - Impossible to record all of LHC data

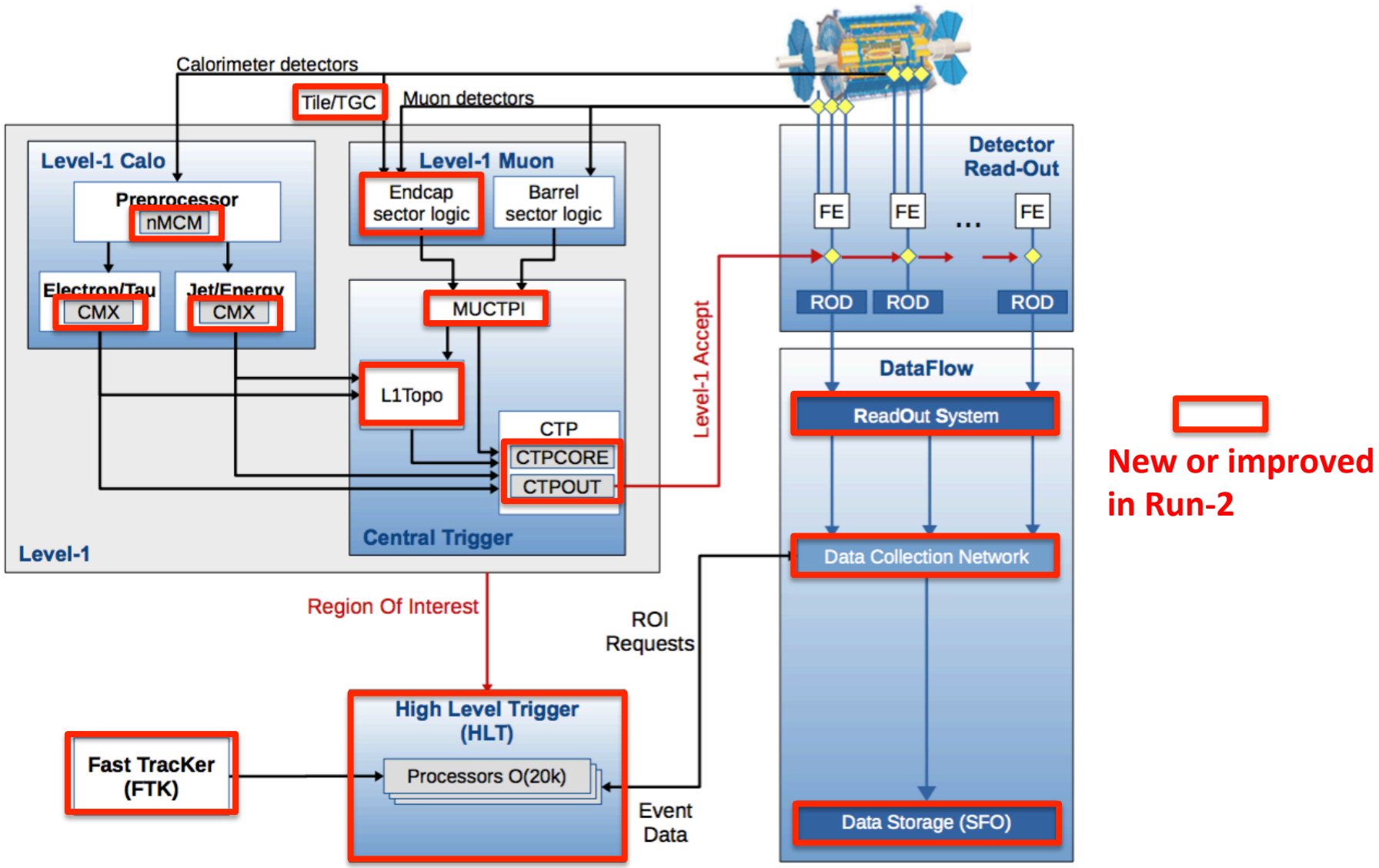
- LHC Run-2:
  - Energy increase 8→13 TeV results in 2-2.5 times higher trigger rates
  - Peak luminosity increase 0.8→1.7 × 10^{34}cm^{-2}s^{-1} results in ~ 2 times higher trigger rates

- Strategies for managing trigger rates
  - Raising thresholds (easy but risks losing Physics)
  - Improved pileup performance
  - Better feature identification algorithms
  - Topology

ATLAS Trigger/DAQ in Run-2

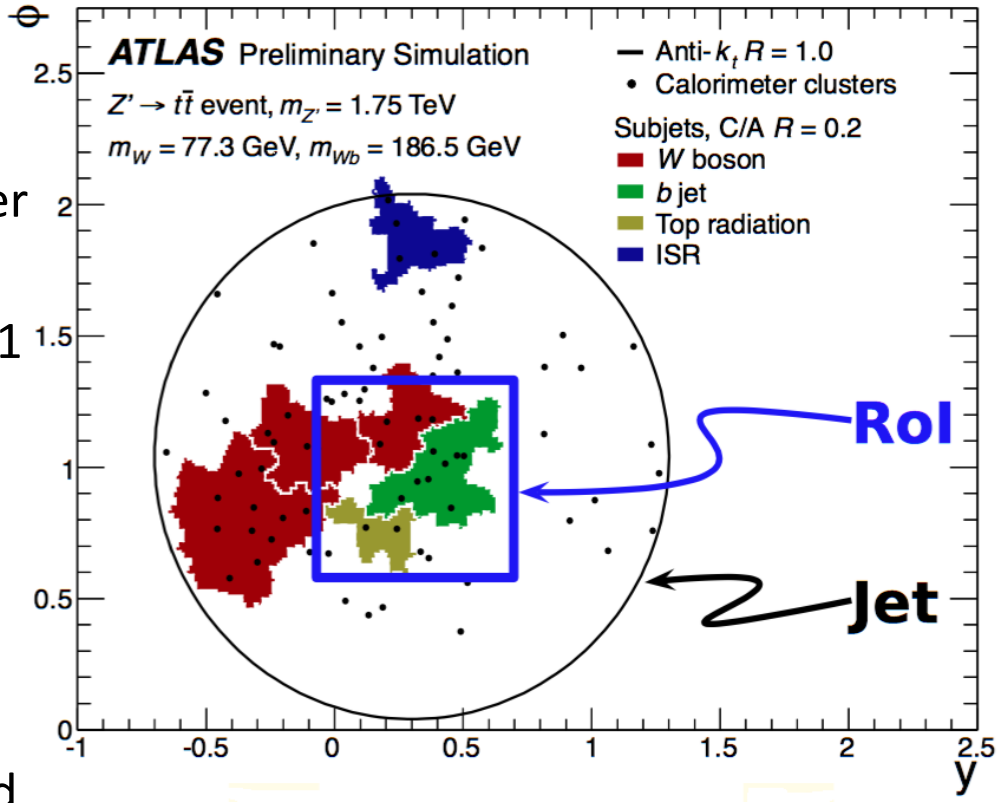


ATLAS Trigger/DAQ in Run-2



L1Calo Phase-1 Upgrade (2019-2020)

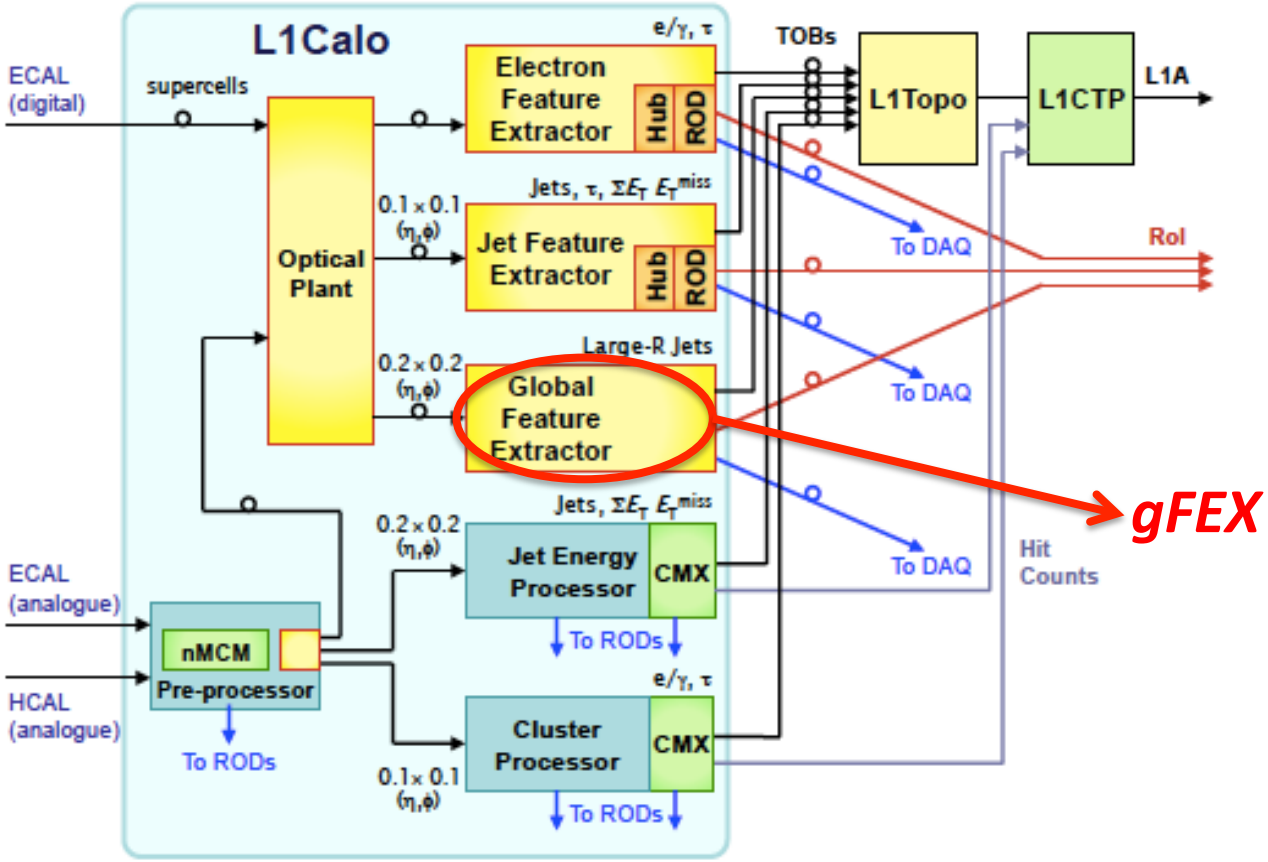
- In LHC Run-3 (2020-2022), the instantaneous luminosity: > 2×10^{34} $cm^{-2}s^{-1}$
  - High pile-up levels degrade trigger performance
  - Upgraded hardware-based level-1 algorithms are aimed at more closely resembling HLT/offline
- Lorentz boosted bosons and fermions at 14 TeV are a key component of ATLAS physics
  - W, Z and H boson, top quarks and exotic particles
  - Energy deposits are close



The decay products of Lorentz boosted particles resemble “large-radius jets”

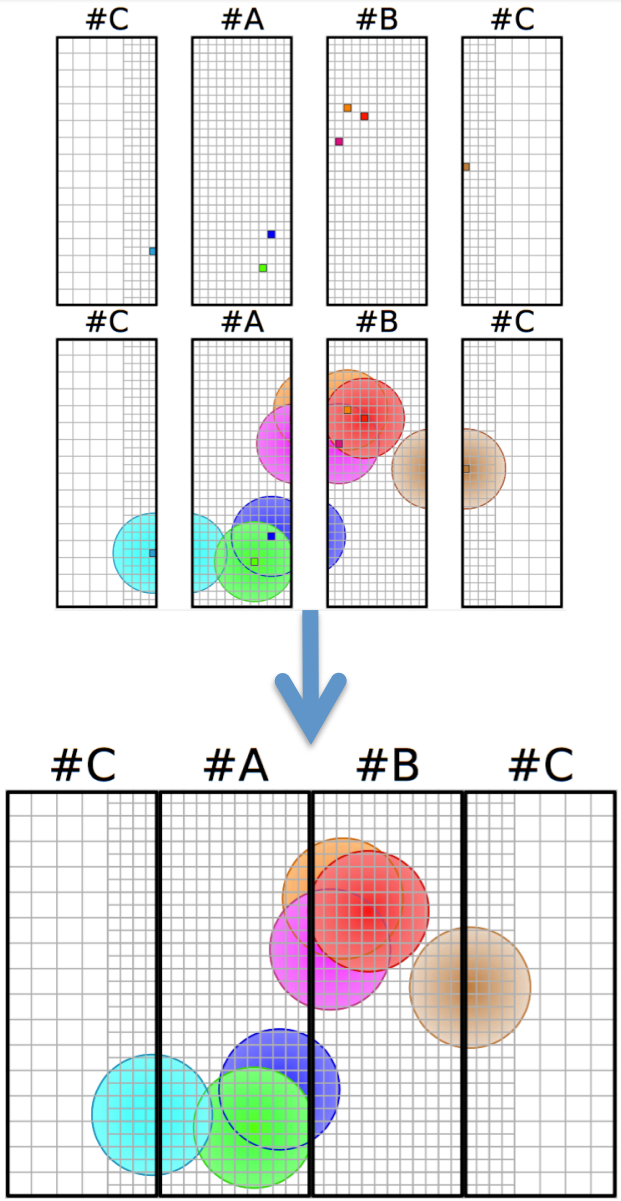
gFEX in L1Calo Phase-1 Upgrade

- gFEX (Global Feature Extractor) is one of three new ”Feature Extractors” that use higher-resolution, digital trigger data from the Calorimeters in the ATLAS L1Calo phase-1 upgrade
  - It identifies large-radius jets, typical of Lorentz-boosted objects
  - It receives information from the full Calorimeter in a single ATCA module

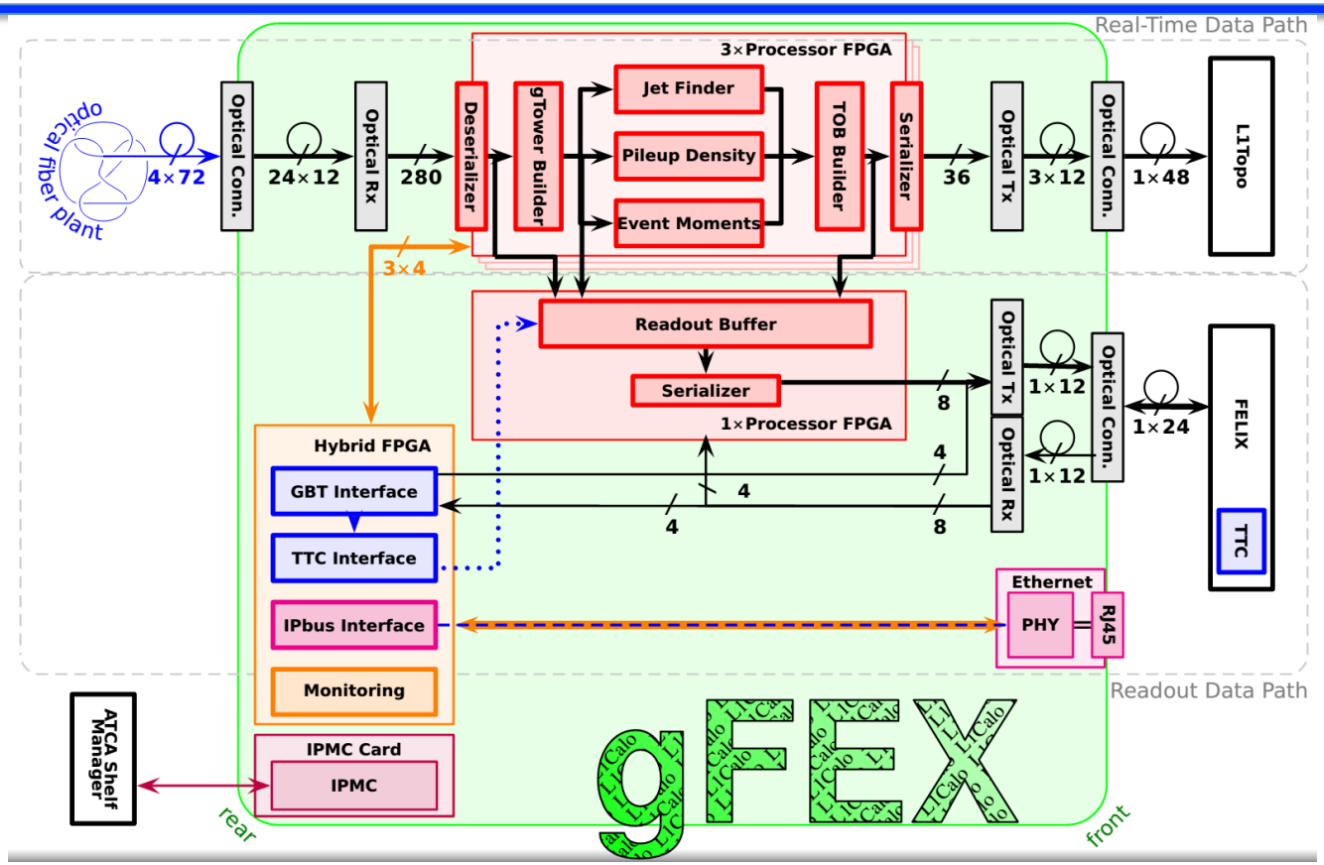


Seeded Simple Cone Jet Finding

- Choose seeds with E_T over threshold
  - 0.2 × 0.2 towers or 0.6 × 0.6 blocks
- Pass "overlapping" seeds to each neighboring FPGA
  - No local maximum requirement
  - Defines FPGA interconnections
- Sum towers around seeds
  - Radius ~ 1.0
  - Include seeds from neighbors
  - Jets allowed to overlap to maximize efficiency
- Transfer "partial" sums to neighboring FPGA
  - No overlap between FPGA
- Subtract pileup per jet



gFEX Functional Diagram



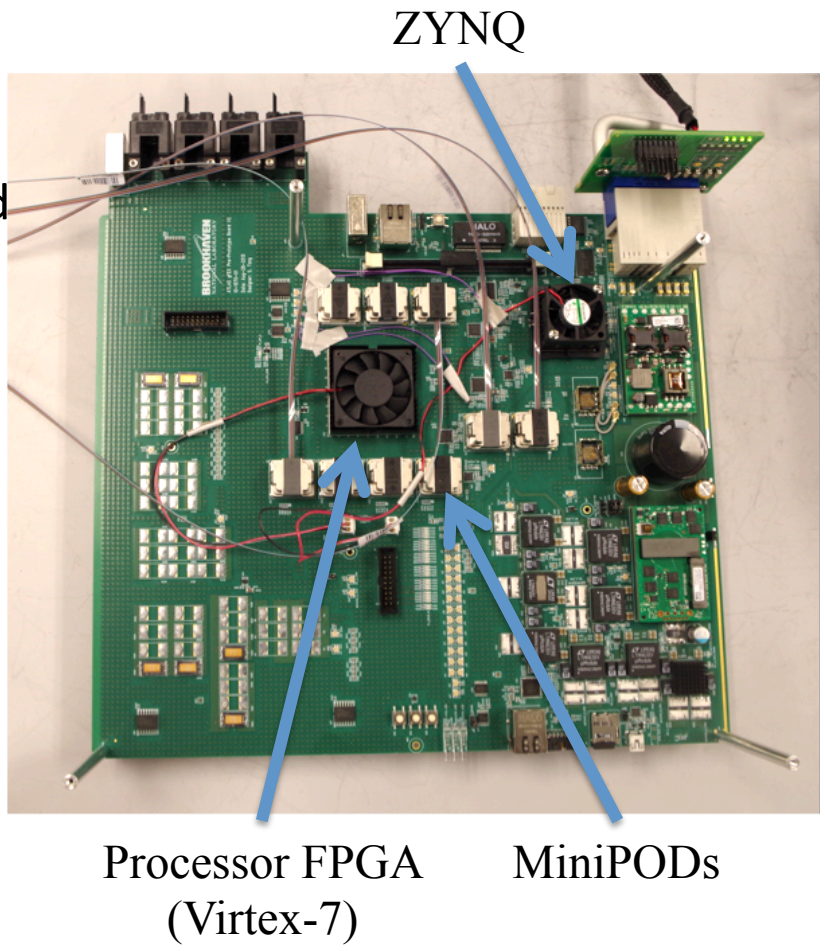
- One Hybrid FPGA (ZYNQ) for control and monitoring
- Three Virtex UltraScale FPGA function as processor FPGA (Algorithms are running here)
- 4x72 channels fibers come from optical fiber plant (280 channels are used)
- IPMC for communicating with ATCA shelf manager and monitoring
- 1x48 channel fibers to L1 Topological Trigger (L1Topo)
- 12 channel fibers to/from FELIX (Front-End LInk eXchange)
  - A new subsystem will be used in ATLAS for interfacing the custom links used in the readout system to standard commercial networks

gFEX Development Progress

- gFEX pre-prototype test results at BNL
- gFEX link speed test at CERN
- gFEX prototype design

gFEX Pre-Prototype

- A gFEX pre-prototype board has been designed to verify the key functionalities
  - Power on sequence and power load
  - Boot of FPGAs
    - ZYNQ: QSPI, JTAG and SD card
    - Processor FPGA: SPI, JTAG
  - ZYNQ's control and monitor
    - I2C, SPI, SD card, DDR3 memory and Ethernet interfaces
  - ZYNQ's GTX link speed
  - Processor FPGA's GTH link speed
  - High speed parallel bus between FPGAs
    - 50-bit LVDS data bus
    - 50-bit HSTL data bus



gFEX Pre-Prototype Functionalities Verification

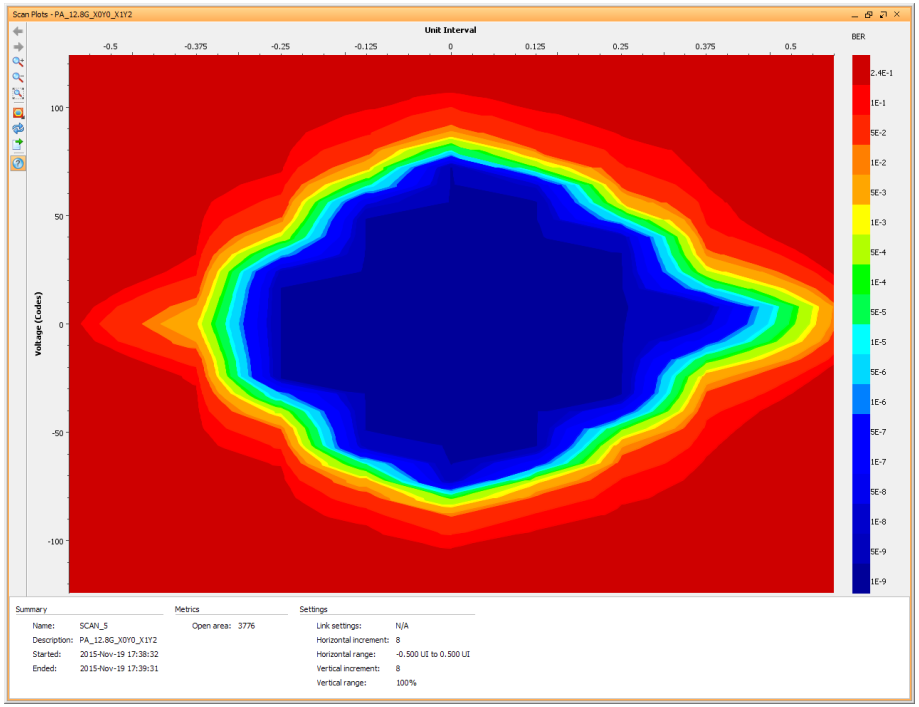
- **Basic infrastructure of gFEX pre-prototype have been tested successfully**
  - Power sequence can be controlled and programmed by two ADM1066 √
  - With power load resistors, the power module LTM4630 can drive 34 A √
  - ZYNQ can boot from JTAG, SD card and SPI flash √
  - Processor FPGA can boot from JTAG and SPI flash √
  - ZYNQ can read and write I2C, SPI, SD card and DDR3 memory √
- **All parallel data buses work well at 480 MHz in DDR mode (960 Mbps)**
  - Parallel buses loopback in Processor FPGA, ZYNQ and between Processor FPGA and ZYNQ
    - Both differential (LVDS) and single-ended (HSTL)
  - Delay of clock can be adjusted with IDELAY module
    - The step resolution of the IDELAY is about 78 ps
    - There are 32 TAPs, so the total length is about 2.5 ns
  - For half cycle, the stable range is about 10 TAPs (~0.78 ns), which is ~76.9% of half clock cycle of 1.0417 ns

High Speed Link Test at BNL

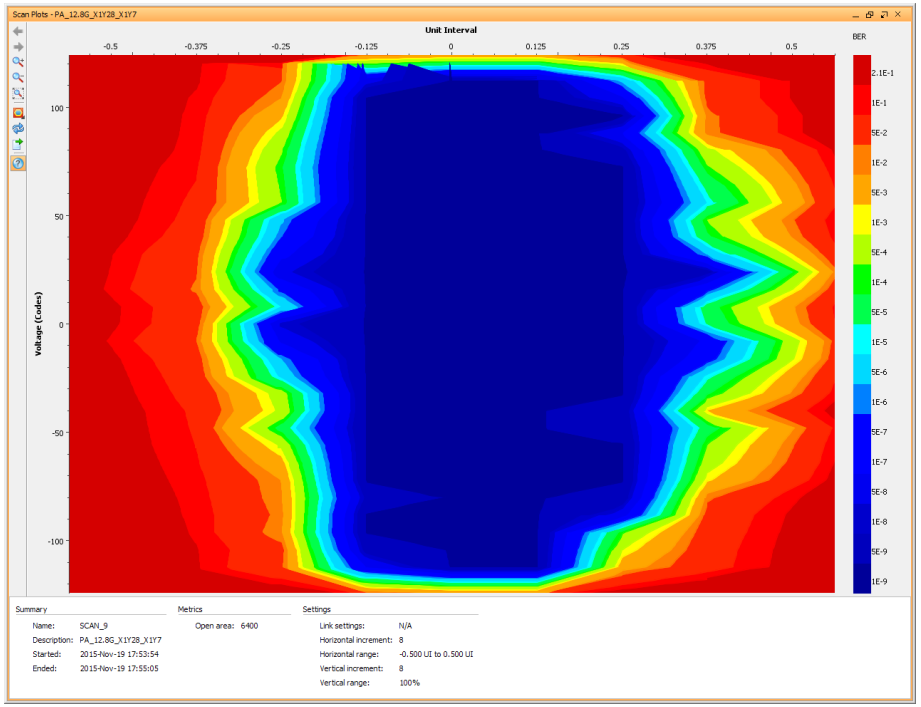
- All the links are stable, when all the 80 channels GTH of processor FPGA and 16 channels GTX of ZYNQ are turned on
  - BER $<10^{-15}$
  - 9.6 Gbps, 11.2 Gbps and 12.8 Gbps
  - Links loopback on processor FPGA
    - Processor FPGA TX → Processor FPGA RX (on board loopback)
    - Processor FPGA TX → MiniPOD TX→Fiber →MiniPOD RX→ Processor FPGA RX
  - Links loopback on ZYNQ
    - ZYNQ TX → ZYNQ RX (on board loopback)
    - ZYNQ TX → MiniPOD TX→Fiber →MiniPOD RX→ ZYNQ RX
  - Links between ZYNQ and processor FPGA
    - ZYNQ TX → MiniPOD TX→Fiber →MiniPOD RX→ processor FPGA RX
    - Processor FPGA TX→ MiniPOD TX→Fiber →MiniPOD RX→ ZYNQ RX
- The high speed links are tested with Xilinx IBERT

Eye Diagram of Links at 12.8 Gbps on Processor FPGA

- *All the links are stable at 12.8 Gbps when all 80 channels GTH of processor FPGA and 16 channels GTX of ZYNQ are turned on*



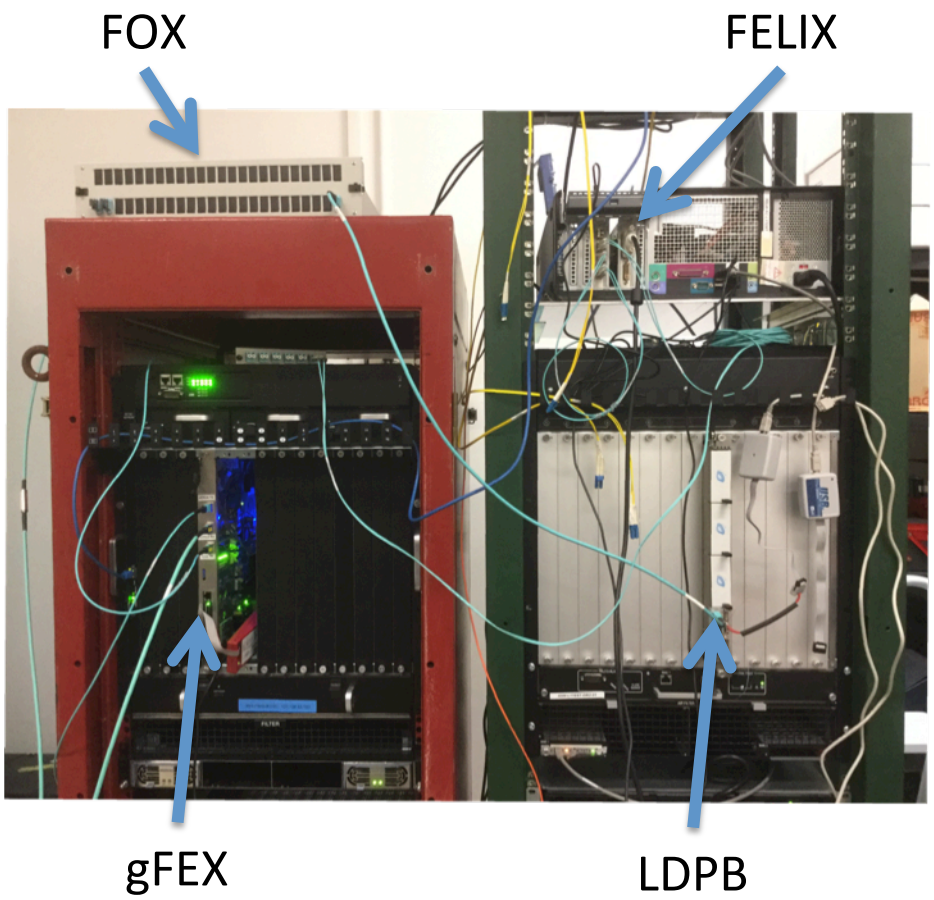
Links onboard loopback



Links through MiniPODs

Link Speed Test at CERN

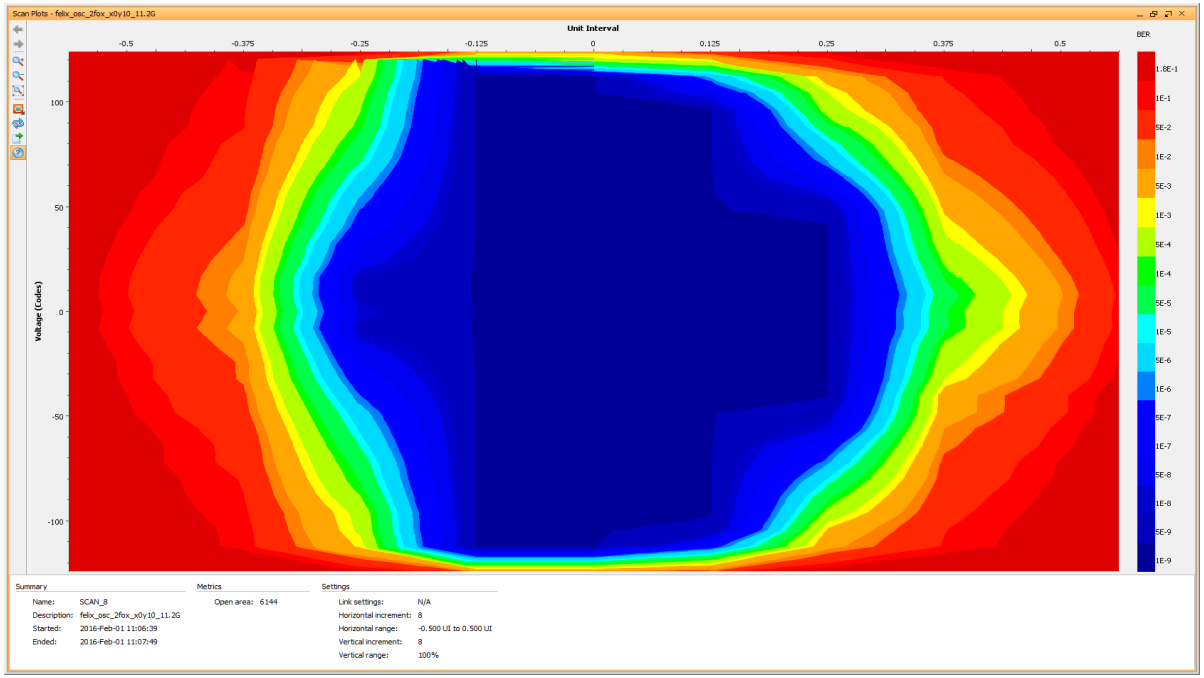
- **LAr-L1Calo link speed test at CERN on January 2016**
  - Links between LDPB and gFEX are tested
  - FELIX provides clock distribution
- Test condition:
  - 48 links run simultaneously
  - Different link speeds are tested
  - Different clock architectures are used
    - Local oscillator clock
    - Recovered clock from FELIX link
      - FELIX uses oscillator clock
      - FELIX uses TTC clock (TTCex, TTCvx)
  - Different FOX setup
    - One stage of FOX
    - Two stage of FOX
    - With or without Splitter



FOX: Fiber-Optic eXchange
FELIX: Front-End LInk eXchange
LDPB: LAr Digital Processing Blade
TTC: Timing, Trigger and Control

Link Speed Test Results I

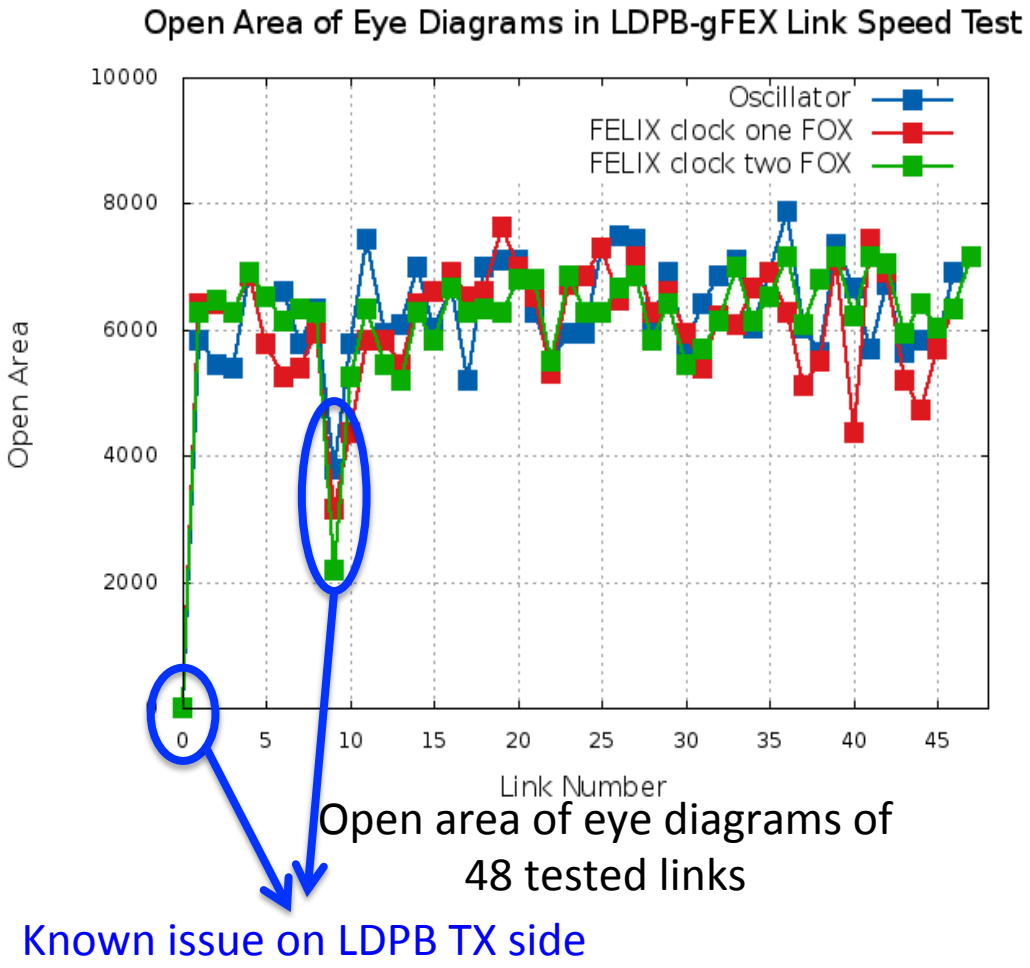
- Links from LDPB to gFEX run properly at 11.2 Gbps
  - No error observed (excluding two links have known issues at LDPB TX side)
  - BER < 10^{-14}
  - PRBS31 is used
  - With different clock architectures
  - With different FOX configurations



Eye diagram of tested link from LDPB to gFEX

Link Speed Test Results II

- Links from LDPB to gFEX have similar performance in different clock architecture
  - Good performance of jitter cleaner in FELIX
  - Good performance of jitter cleaner in both LDPB and gFEX
- Links from LDPB to gFEX have similar performance in different FOX setup
  - FOX and Splitter have little impact on links performance



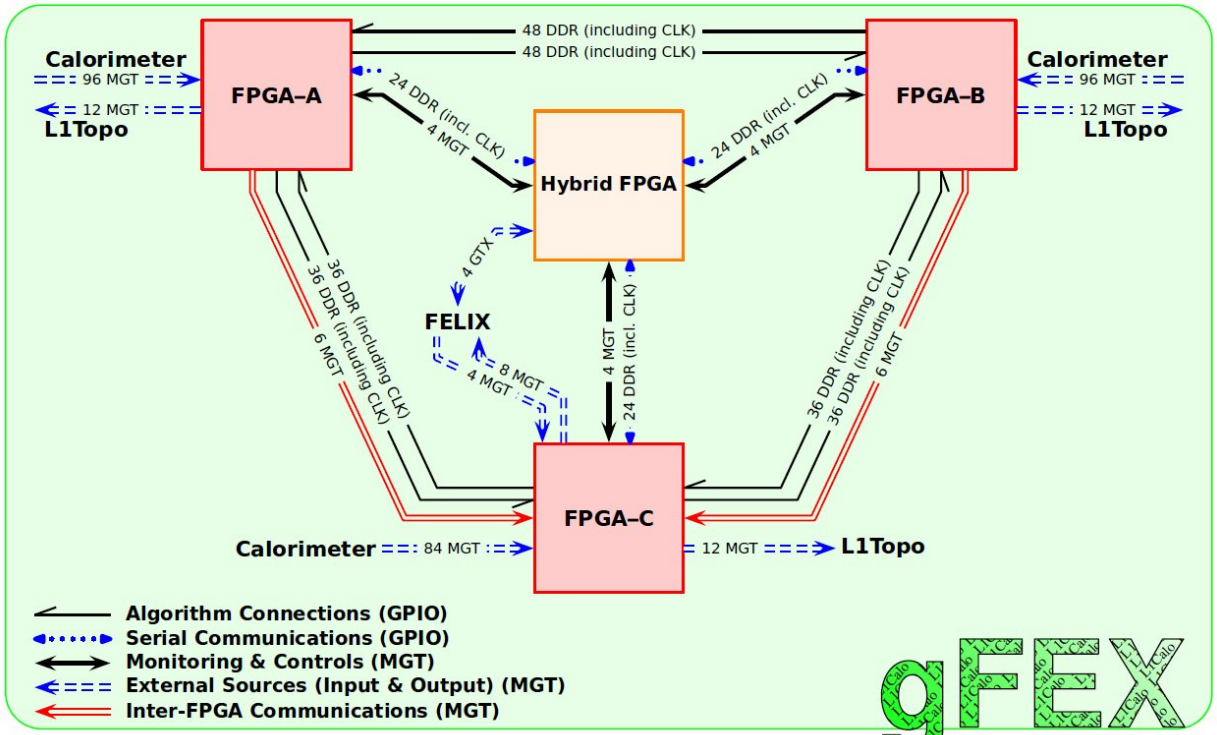
Link Speed Test Results III

- High speed links test from gFEX to L1Topo
  - All of 12 links run properly at 12.8 Gbps
  - Data pattern: PRBS7

- In the link speed test between LDPB and eFEX on April 2016, good eye opening and BER ($<10^{-14}$) at 11.2 Gbps also have been achieved
- Based on the results of link speed test between LDPB and g/eFEX, baseline link speed of 11.2 Gbps have been agreed to use between LAr-L1Calo, with options of 9.6 Gbps and 12.8 Gbps

gFEX Prototype Design

- Three Virtex UltraScale FPGA are used as processor FPGA
- One ZYNQ is used for control and monitoring



Block diagram of gFEX Prototype

- Processor FPGA A&B
  - 96 RX from Calorimeter
  - 6 TX FPGA C
  - 12 TX L1Topo
  - 4 TX/RX ZYNQ
- Processor FPGA C:
  - 84 RX from Calorimeter
  - 12 RX FPGA A+B
  - 4 RX FELIX
  - 12 TX L1Topo
  - 4 TX/RX ZYNQ
  - 8 TX FELIX
- ZYNQ
  - 12 TX/RX FPGA A+B+C
  - 4 TX/RX FELIX

gFEX Prototype Design

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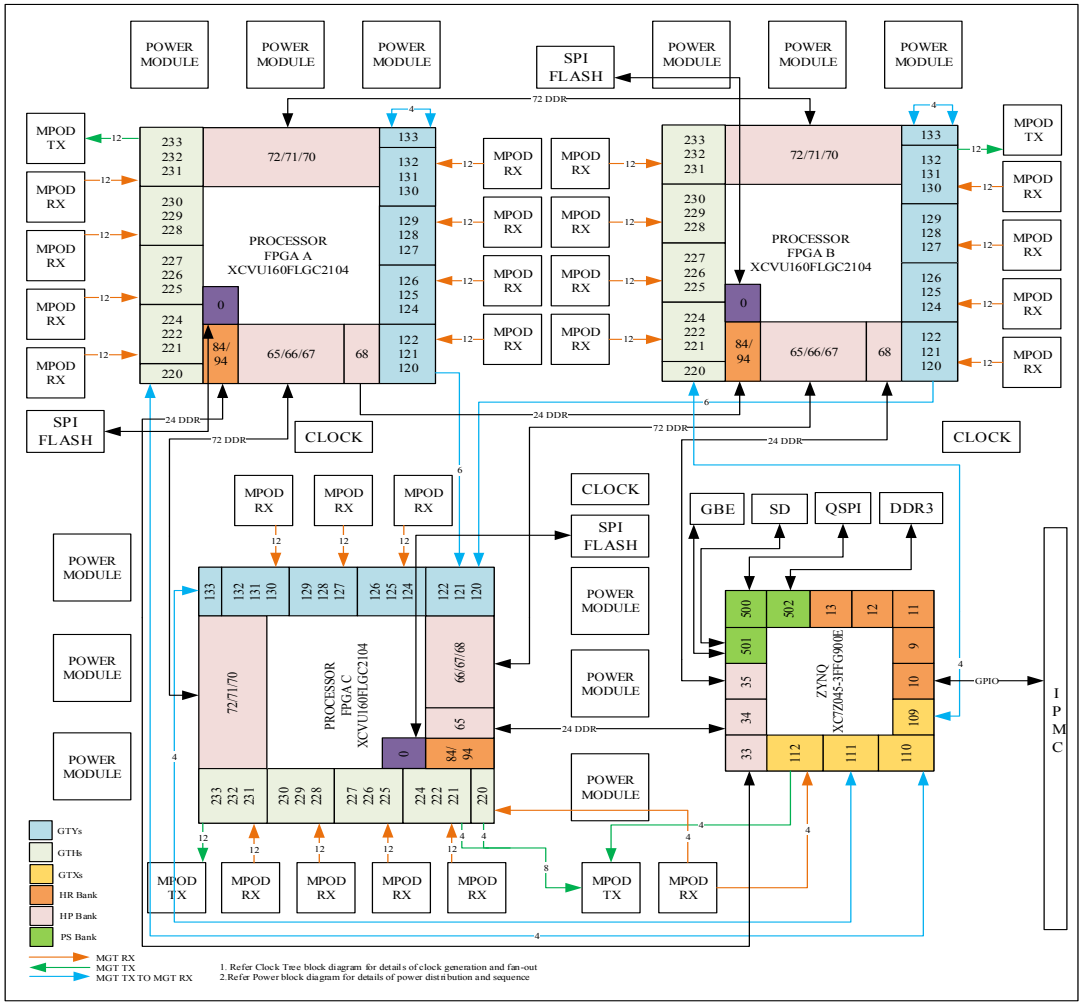
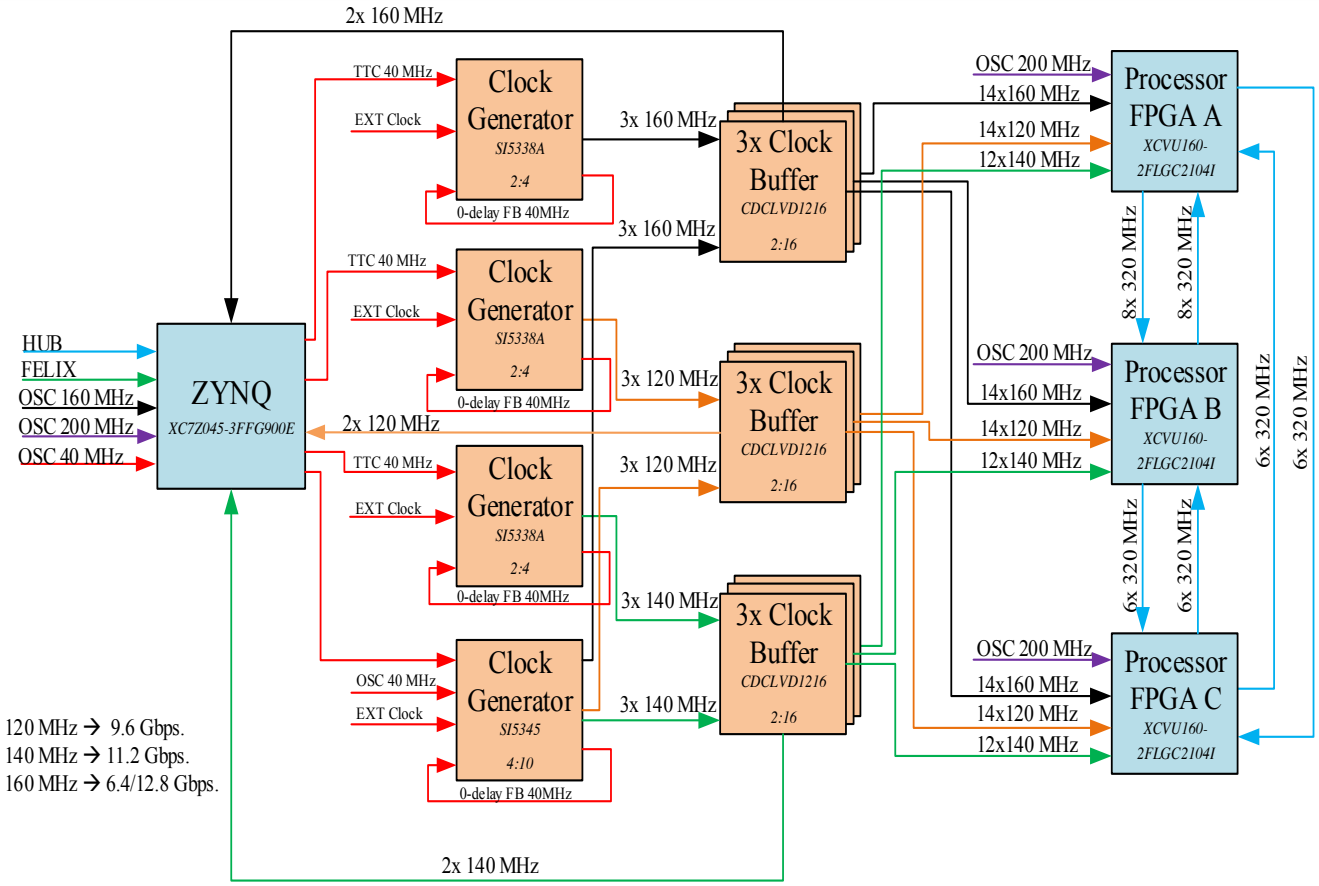


Schematic diagram of gFEX Prototype

- Processor FPGA A&B
  - 96 RX from Calorimeter
  - 6 TX FPGA C
  - 12 TX L1Topo
  - 4 TX/RX ZYNQ
- Processor FPGA C:
  - 84 RX from Calorimeter
  - 12 RX FPGA A+B
  - 4 RX FELIX
  - 12 TX L1Topo
  - 4 TX/RX ZYNQ
  - 8 TX FELIX
- ZYNQ
  - 12 TX/RX FPGA A+B+C
  - 4 TX/RX FELIX

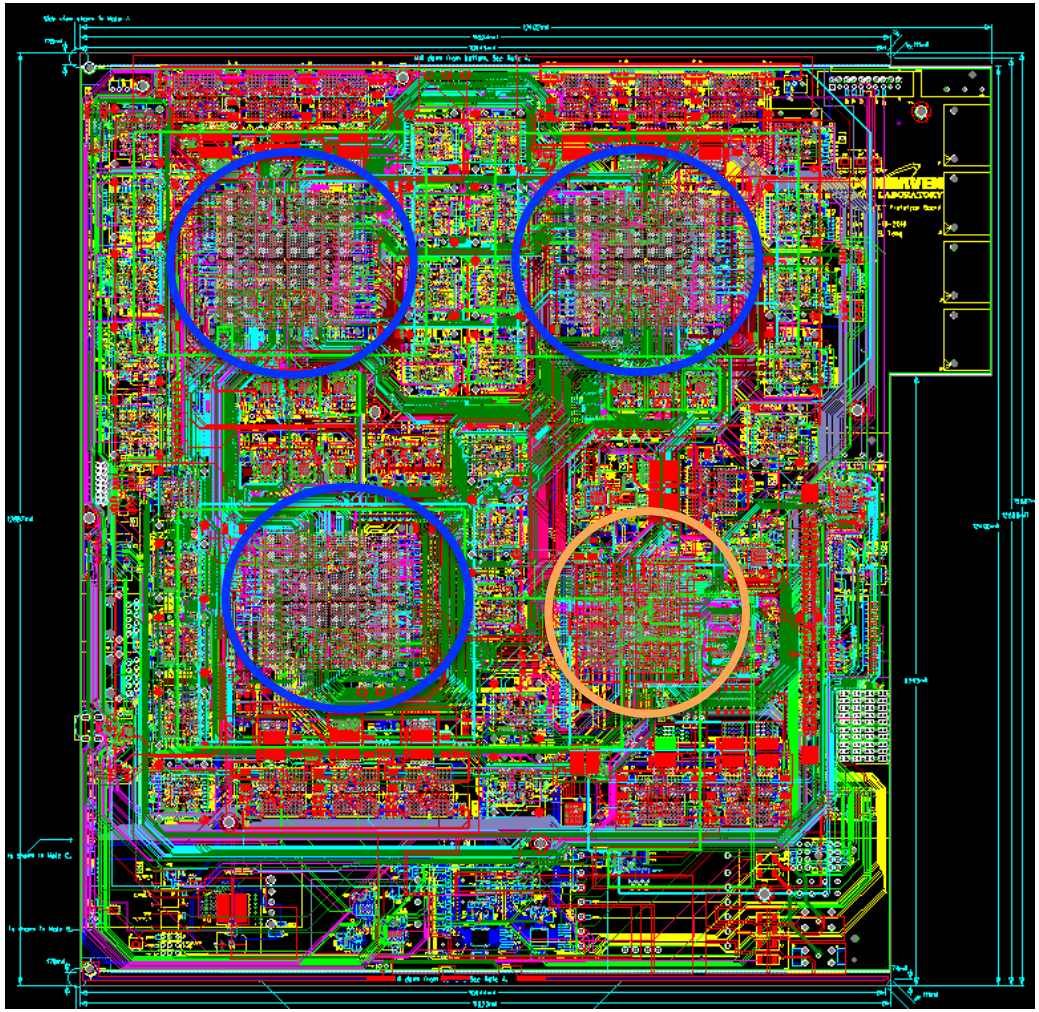
Clock Scheme of gFEX Prototype



- Si5345 is used to generate reference clock for MGT in ZYNQ and processor FPGA
  - Its input is the recovered clock from FELIX link
  - Si5338 is used as back-up plan
- CDCLVD1216 is used as clock buffer

Layout of gFEX Prototype

- Three Virtex UltraScale FPGA and one hybrid FPGA (ZYNQ)
- 26 Layers board
- 28 MiniPODs
  - Each MiniPOD has 12 TX/ RX links
- Sent out for fabrication on late April, 2016



Ultrascale FPGA ZYNQ

Summary

- gFEX Pre-Prototype:
  - Power, clocks, infrastructure, etc work well
  - ZYNQ controls and monitors as expected
  - Parallel buses operate at 960 Mbps (480 MHz) without any issue
  - High speed links are stable at 12.8 Gbps
- Link speed test at CERN succeeds
  - Links between LDPB and gFEX are stable at 11.2 Gbps
  - Links between gFEX and L1Topo are stable at 12.8 Gbps
  - Based on link speed test results, LAr-L1Calo has agreed to use 11.2 Gbps as baseline link speed
- gFEX Prototype design has been finished
  - Three UltraScale FPGA are used as processor FPGA
  - Clock generate chip of Si5345 is added