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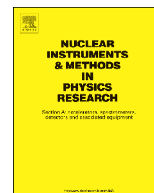

Radiation hardness of a 180 nm SOI monolithic active pixel sensor

S. Fernandez-Perez [a,b,*], M. Backhaus [a], H. Pernegger [a], T. Hemperek [c], T. Kishishita [c], H. Krüger [c], N. Wermes [c]

[a] PH-ADE-ID, CERN, Route de Meyrin 385, Geneva, Switzerland
[b] IFAE, Campus UAB 08193, Barcelona, Spain
[c] University of Bonn, Nussallee 12, Bonn, Germany

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ABSTRACT

The use of Silicon-on-Insulator (SOI) technology as a particle detector in a high radiation environment is, at present, limited mostly by radiation effects on the transistor characteristics, back gate effect, and mutual coupling between the Buried Oxide (BOX) and the sensor. We have fabricated and tested a new 0.18 μm SOI CMOS monolithic pixel sensor using the XFAB process. In contrast to the most commonly used SOI technologies, this particular technology uses partially depleted SOI transistors, offering a double well structure, which shields the thin gate oxide transistors from the BOX. In addition, an increased distance between transistors and a thicker BOX than has been previously used offers promising solutions to the performance limitations mentioned above. The process further allows the use of high voltages (up to 200 V), which are used to partially deplete the substrate. Thus, the newly fabricated device in the XFAB process is especially interesting for applications in extremely high radiation environments, such as LHC experiments. A four stage validation programme of the technology and the fabricated monolithic pixel sensor has been performed and its results are shown in this paper. The first targets radiation hardness of the transistor characteristics up to 700 Mrad, the second investigates the existence of the back gate effect, the third one targets the coupling between the BOX and the sensor, and the fourth investigates the characterization of charge collection in the sensor diode below the BOX.

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1. Introduction

Silicon-on-Insulator (SOI) technologies have been developed for military and space applications for 40 years. Nowadays, they are widely used for commercial and industrial production. SOI devices exhibit major advantages over bulk substrates including superior Single Event Upset (SEU) tolerance, better noise isolation, speed and density [1,2]. Using SOI technologies as pixelated particle detectors enable isolating standard CMOS readout electronics from a high resistivity substrate used as a sensor. This would have several advantages [3]. However, there are some performance limitations to be considered. On one hand, the total ionizing dose (TID) response of SOI devices is more complex than bulk silicon devices as the effects in the buried oxide (BOX) need to be considered as well. A significant influence of radiation damage on the transistor characteristics due to the accumulated charges in the BOX has been observed and published in SOI technologies [4,5]. On the other hand, it has been observed that the applied electric field in the sensor also affects the transistors operation, which is called Back Gate Effect [3]. Additionally, a possible coupling between charges accumulated in the BOX and sensor would also need to be taken into account.

A new 0.18 μm SOI CMOS fully monolithic pixel sensor designed by University of Bonn was fabricated using the XFAB process [6]. The first version of this chip, the so-called XTB01, is 300 μm thick, with a size of 5 mm × 2 mm. In contrast to other SOI technologies, XFAB provides a double well structure to shield the thin gate transistors from the BOX. The transistors are partially depleted (PD), but in contrast with standard PD, a larger distance between gate and BOX and a thicker BOX make the technology promising against the radiation effects on the transistors, as well as against the back gate effect described above. The process further allows the use of high bias voltages (HV) up to 200 V. The chip is composed of four matrices with different pixel sizes (25 μm × 25 μm, 50 μm × 50 μm, 50 μm × 50 μm, 100 μm × 100 μm) and test transistors of several flavours. The chip is composed of four HV rings. Three of the HV rings surround the matrices (100 μm × 100 μm matrix, 50 μm × 50 μm and 25 μm × 25 μm+50 μm × 50 μm) while the fourth HV ring surrounds the whole chip. A detailed description of the chip design is given in [7]. A pixel cross-section of this prototype is shown in Fig. 1.

* Corresponding author.
E-mail address: sonia.fernandez@cern.ch (S. Fernandez-Perez).

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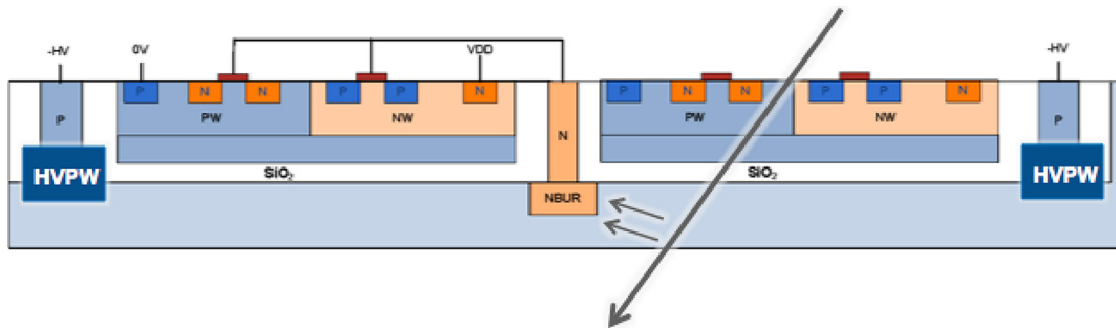

Fig. 1. A pixel cross-section of the XTB01 prototype. Not to scale.

The BOX isolates the full CMOS electronics built in 0.18 μm technology from the substrate which is used as a sensor diode. This substrate is p-type silicon with 100 Ω cm resistivity. The charge is collected in a small deep n-well, which reduces the capacitance, and is connected to the readout circuitry. The HV is applied from the top, on the p+ implants, since there is currently no backside processing. The matrix is read out by a rather simple but slow, standard 3 T pixel cell using a rolling shutter readout for the sensor diode and correlated double sampling [8].

A validation program of the technology and the fabricated monolithic pixel sensor have been carried out a in a four stage approach. The first targets the radiation hardness of the transistor characteristics with focus on possible influences of the BOX. The second stage investigates the existence of the Back Gate Effect. The third targets a possible coupling between BOX and sensor, while the fourth characterizes the leakage current and the charge collection in the sensor diode below the BOX.

2. TID effects on SOI 0.18 μm transistors

Basic TID mechanisms and damage processes in CMOS transistors are described in [9,10]. The electrical parameters of CMOS electronics degrade with accumulated TID due to radiation damage. The shift of the electrical parameters is mainly given by the sum of two contributions, a first one related to the positive charges trapped in the gate and STI oxide and a second one related to the Si–SiO_2 interface traps. The biggest difference between the radiation response of MOS transistors fabricated on bulk silicon and on SOI technology is the BOX inclusion, which make SOI devices more sensitive than bulk transistors to TID damage due to the build-up of charge in the BOX [11,12].

The threshold voltage of a bulk NMOS transistor in the presence of radiation damage is expected to shift in a rebound way. For low TID the trapped positive charges in the gate and STI oxides attract negative charges to the Si–SiO_2 interface and thus decrease the threshold voltage while for high TID the activation of traps at the Si–SiO_2 interface decreases the mobility of the charge carriers which leads to an increase of the threshold value. However, the threshold voltage of a PMOS transistor always tends to increase, because the two effects mentioned above shift the electrical parameters in the same direction. In this case, the positive trapped charges in the oxide push away holes from the p-channel, consequently, increasing the threshold voltage of a PMOS transistor. The leakage current of an NMOS transistor increases with decreasing threshold voltage. The trapped charges in the oxide will provoke an induced negative channel and hence the leakage current increases, while the interface traps will tend to reduce it. For a PMOS transistor, the leakage current is constant. The variation of an induced channel of electrons does not affect a PMOS transistor. The impact of these effects depends on the transistor geometries, for example enclosed transistors are developed to reduce it. The bias conditions of the gate during irradiation are crucial since they will influence the quantity of charges trapped in the Si–SiO_2, the location of the trapped charges, as well as the electrical field at the Si–SiO_2 interface. However for PMOS transistors it is not clear which are best or worst bias conditions, with the result that it is technology dependent.

Table 1
Bias conditions of the transistors gate during irradiation.

Bias conditions	
Campaign A	NMOS on ($G=1.8$ V, $D=S=0$ V) PMOS off ($G=D=S=1.8$ V)
Campaign B	NMOS off ($G=D=S=0$ V) PMOS on ($G=0$ V, $D=S=1.8$ V)

Two irradiation campaigns were carried out at CERN, Switzerland, with an X-ray machine. Irradiations have been performed at room temperature up to a TID of 700 Mrad in several steps with a dose rate of 8 Mrad h^{-1} (achieved by 2 cm tube distance, 40 kV and 50 mA). The dose steps are 100 krad to 600 krad in 100 krad steps, 800 krad, 1 Mrad, 3 Mrad, 5 Mrad, 15 Mrad, 50 Mrad, 100 Mrad, 150 Mrad, 300 Mrad, 500 Mrad, 700 Mrad. The transistors were various types – standard transistors with different geometries and enclosed transistors. Different bias conditions were applied during irradiation for each campaign, since the gate voltage wire bond pad is shared in PMOS and NMOS transistors. The bias conditions during irradiation are summarized in Table 1. The testing procedure followed the Standard test method ESA/SCC BS 22900 [13], in which the transistor characteristics are tested right away after the irradiation step. Therefore, the annealing is considered negligible during irradiation and testing. A full annealing program is performed at the end of the full irradiation campaign. No annealing results are included in this paper.

The setup to characterize the transistors consists of a home-made board which allows selection of every single transistor, and three power supplies (for biasing the gate, drain and AVDD respectively) which allow measuring the transistor characteristics. A dedicated routine extracts the electrical parameters (threshold voltage, leakage current, and transconductance) from the transistor characteristics. The parameter's extraction was based on the extrapolation method in the saturated region (ESR) [14]. Fig. 2 shows the characteristics of the smallest PMOS transistor 0.5/0.18 for all the irradiation steps up to 700 Mrad. This shows how the curve changes under radiation and consequently its electrical parameters.

Fig. 3a and b shows the threshold voltage shift evolution with TID for NMOS transistors of the XTB01 prototype for bias option A (NMOS on) and for bias option B (NMOS OFF) respectively. It is

observed that up to 5 Mrad the threshold voltage decreases while for TID >5 Mrad an increase of the threshold value starts. Therefore, the rebound shift explained above, and expected on bulk transistors, is similarly observed for the partial depleted SOI transistors of this prototype. By comparing Fig. 3a and b, one realizes that similar to bulk transistors the bias conditions of the gate during irradiation are crucial. While the maximum threshold variation of the transistor 0.5/0.18 is $\Delta V_{TH}=80$ mV in bias option A, the threshold variation is $\Delta V_{TH}=20$ mV in bias option B. Two additional conclusions can be extracted from Fig. 3a. The first is that the enclosed transistor – 2.7/0.27 labelled in red – is the one showing the smallest degradation, as is expected, <10 mV at 700 Mrad. The second one comes out from the strong W scaling which shows that the effect on STI oxide is dominating rather than the gate one. This is known and expected for thin gate oxide transistors.

Fig. 4a and b shows the threshold voltage shift evolution with TID for PMOS transistors of the XTB01 prototype for bias option A (PMOS off) and for bias option B (PMOS on) respectively. The same behaviour as the expected on bulk transistors is observed. The threshold voltage in PMOS transistors increases with TID. The results of both bias conditions are comparable in this technology. The maximum threshold variation is around $\Delta V_{TH}=120$ mV for the smallest transistor (0.5/0.18).

The same analysis is done for the leakage current and for the transconductance. The leakage current shift for NMOS goes from

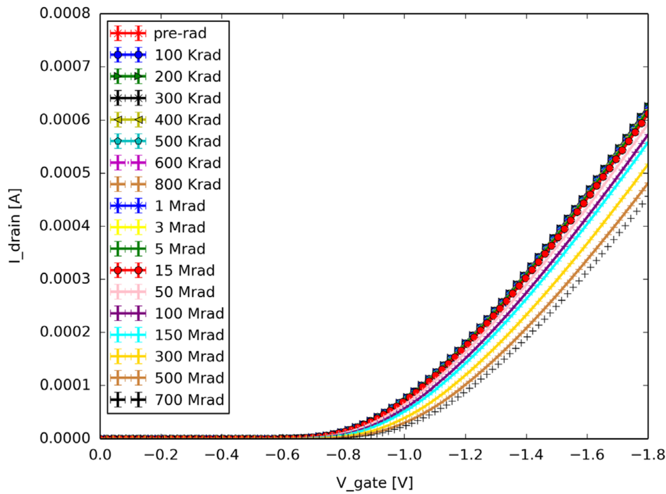

Fig. 2. Characteristics of a 0.5/0.18 PMOS for various radiation levels.

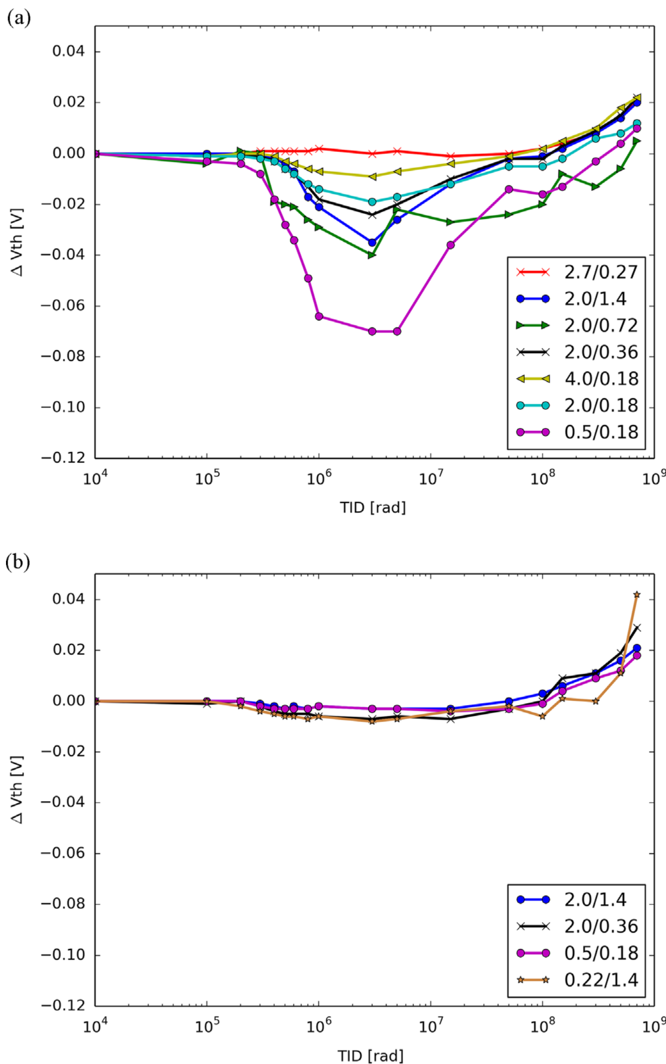

Fig. 3. Threshold shift as a function of the TID in NMOS transistors (a) for bias option A and (b) for bias option B. Note that the value 10^4 corresponds to the value before irradiation.

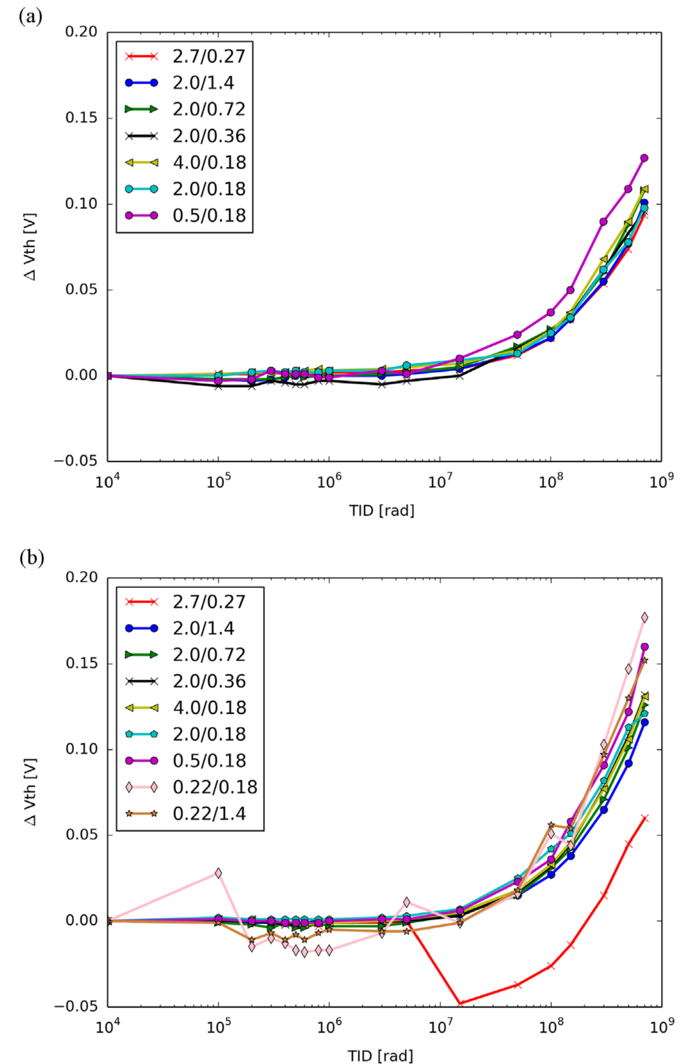

Fig. 4. Threshold shift as a function of the TID in PMOS transistors (a) for bias option A and (b) for bias option B. Note that the value 10^4 corresponds to the value before irradiation.

10^{-10} A to 10^{-6} A for the smallest linear transistor, while remains constant at 10^{-10} A for the enclosed transistor. The leakage current for PMOS transistors goes from 10^{-10} A to 10^{-9} A as well for the smallest linear transistor at 700 Mrad. The transconductance variation is around 20% for PMOS and 5% for NMOS transistors at 700 Mrad. These plots are not included in this paper.

The degradation of the electrical parameters obtained up to 700 Mrad is within the process variation and fully consistent with non-SOI thin gate technologies i.e. IBM 130 nm used for the ATLAS IBL readout chip FE-I4 [15]. In contrast to other SOI technologies in which the parameters shift after a few hundred krad [12], the accumulated charge in the BOX does not affect the electronics performance.

3. Back gate effect

As it was described in Section 1 the back gate effect consists of the coupling between the electric field in the sensor and the transistor's operation. This phenomenon limits the applicable sensor bias and therefore techniques to reduce the back gate effect are being investigated [3,16]. NMOS transistors, especially, are affected by the back gate effect. Other publications have shown an increase of up to eight orders of magnitude in the leakage current of NMOS transistors when a bias voltage of −50 V was applied to the sensor diode [3]. In order to investigate the magnitude of the back gate effect in our prototype, all transistor characteristics were measured on the 700 Mrad irradiated chip in two configurations: (a) with the sensor diode floating and (b) with a bias voltage of −40 V on the sensor diode. Fig. 5 shows the $I_{DS}-V_{GS}$ curves for three NMOS transistors. The overlapping curves show that the transistors operation and in consequence the electronic part is well shielded from the electrical field in the sensor diode. Thus no back gate effect is present in our prototype.

4. Coupling between BOX and sensor diode

The results presented in Section 2 show that the accumulated charge in the BOX does not affect the electronics performance. In order to measure if the accumulated charge in the BOX influences to the sensor behavior, current–voltage (*I–V*) measurements are carried out at room temperature in all the HV rings of the matrix. First on an unirradiated chip, and later on the irradiated chip up to 700 Mrad with X-rays. Fig. 6 shows the *I–V* curves of the different rings in logarithmic scale for the irradiated and unirradiated chip. It is observed that the current increases by a factor 80 in the irradiated chip. This is explained by the fact that the electrical field, created by the positive charges accumulated in the BOX, attracts electrons to the Si–SiO_2 interface. This way a conductive channel is created which breaks the pn diode. As a consequence the measured current increases. Therefore, accumulated charge in the BOX influences the sensor diode performance. A p-stop or p-spray will be implemented in the next prototype to avoid this channel.

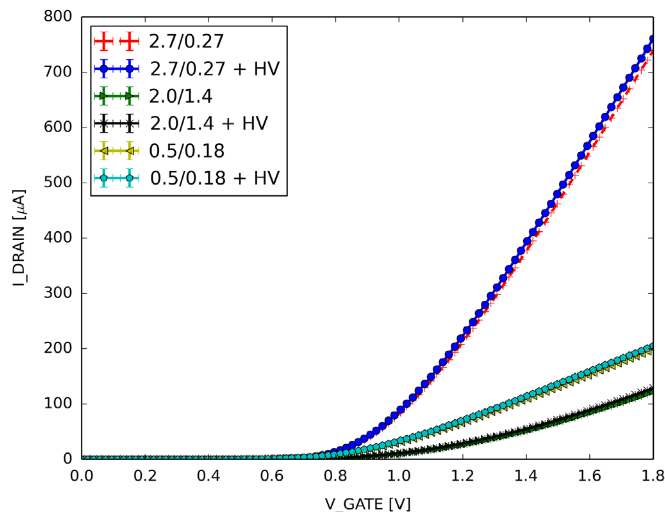

Fig. 5. Transistor characteristics of three NMOS transistors applying no voltage and −40 V to the sensor diode.

5. Leakage current and charge collection

The test system, which was developed by Bonn University, allows monitoring of the analogue signal of the prototype. It is composed of a Multi I/O board which makes the digital interface with the computer, a General Purpose Adapter Card (GPAC), which provides all the analogue functionalities to the chip, and a Device Under Test (DUT) board. The software is written in Python, and based on the Basil framework.

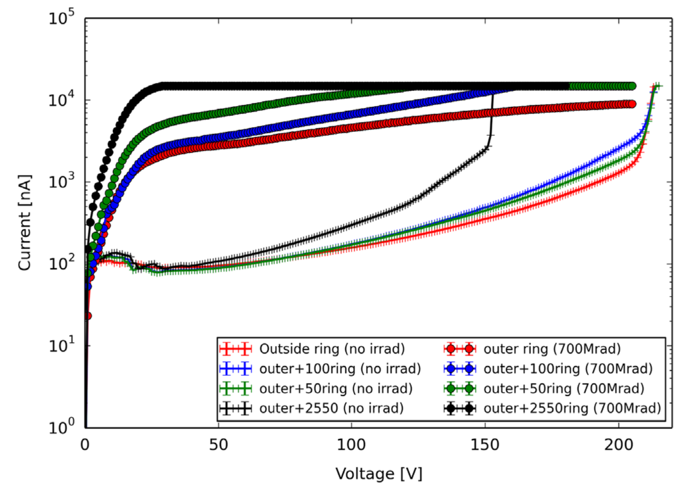

Fig. 6. *I–V* curves in logarithmic scale of each ring performed on an irradiated (700 Mrad) and unirradiated chip.

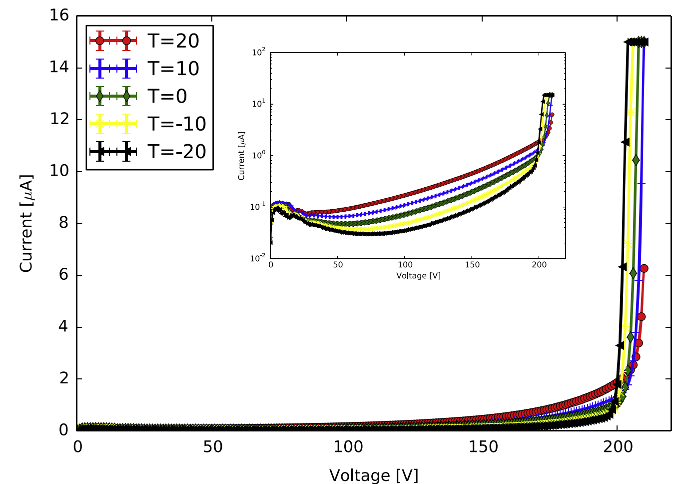

Fig. 7. *I–V* curves on ring 50 μm × 50 μm pitch for different temperatures.

Leakage current measurements were performed for all the HV rings and for different temperatures. Fig. 7 shows the *I–V* curves of an unirradiated chip at different temperatures for the ring surrounding the 50 μm × 50 μm matrix. It is seen that the prototypes breakdown is at around 200 V. The leakage current is a factor of 5–10 higher than expected for this prototype. How the current scales with temperature is observed in the inset of Fig. 7 which shows the *I–V* in the logarithmic scale. The scaling is not in agreement with the exponential law. Further analysis is being performed to extract the drift, diffusion and surface contribution.

The prototype functionality as a pixel sensor is tested using ^{55}Fe and ^{90}Sr sources. With this purpose, the analogue output of a pixel in matrix 50 μm × 50 μm pitch was selected while biasing the diode and placing the ^{55}Fe and ^{90}Sr sources on top. The sensor diode was biased to −40 V for ^{55}Fe and to −150 V for ^{90}Sr at 20 °C during 45 min and 15 h, respectively. The ^{55}Fe photoelectron deposits all its energy in few μm from the surface, while a MIP of ^{90}Sr deposits all along its path. Therefore a higher voltage to increase the depletion depth was needed to observe the ^{90}Sr spectrum. Figs. 8 and 9 show both spectra in ADC units. A threshold was set at 80 ADC and at 180 ADC to avoid the large leakage current peak. The photo peak of the ^{55}Fe photons and the landau spectrum of the ^{90}Sr proves the detection of charges generated in the sensor by ionizing particles also with the small depletion depth of 40–50 μm thanks to the amplification in the sensor layer. The depletion depth is estimated from both spectra peaks. On one hand, the ^{55}Fe peak at around 230 ADC corresponds to the 5.9 keV, which allows us to calculate a calibration constant of 1630 e^- per ADC in silicon. On the other hand, multiplying the calibration constant by the MPV of the ^{90}Sr and dividing it by 80 eh a depletion depth of 45 μm ± 5 μm is calculated.

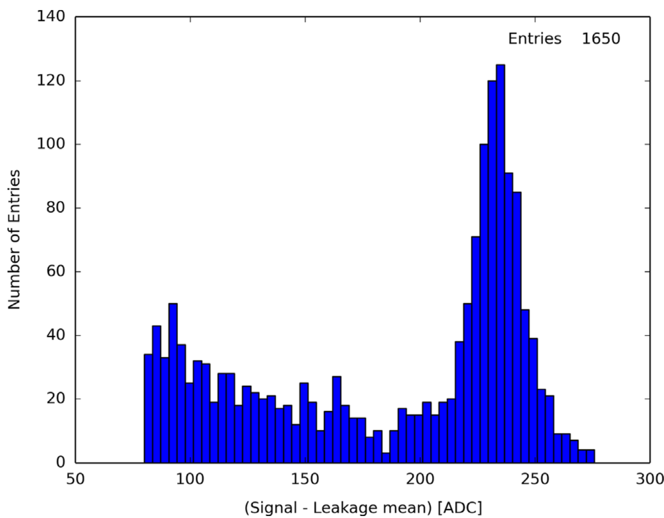

Fig. 8. ^{55}Fe spectrum on a pixel 50 μm × 50 μm pitch in ADC units.

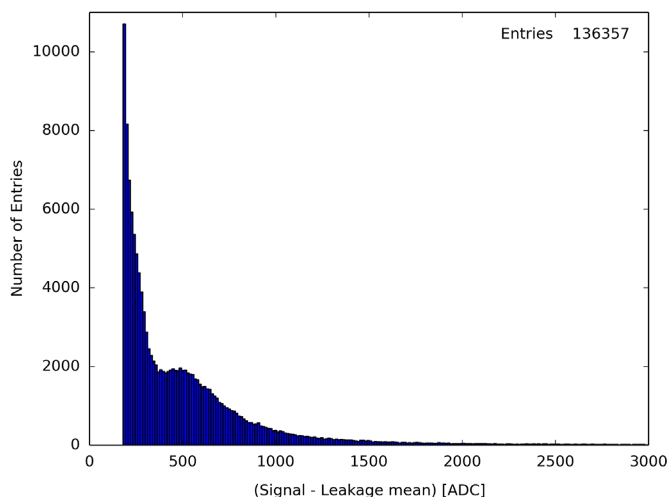

Fig. 9. ^{90}Sr spectrum on a pixel 50 μm × 50 μm pitch in ADC units. The tail of the leakage current peak and the signal from the ^{90}Sr can be seen.

6. Conclusion and outlook

The radiation hardness of the SOI transistors on the XFAB technology has been proven up to 700 Mrad. All results are consistent with non-SOI thin gate technologies (e.g. IBM 130 nm used for ATLAS IBL FE-I4), and the parameter shift is within the process variations up to 700 Mrad. Therefore, in contrast to other SOI technologies, no effect of the BOX is observed.

The overlapping characteristics of the transistors for an irradiated chip in two configurations – without HV on the diode and with −40 V on the diode – prove that there is no coupling between the electronics and the electric field in the sensor.

Unexpectedly high leakage current is observed, which increases by a factor of 80 with the accumulation of positive charges in the BOX. This shows that the charge accumulation in the BOX influences the sensor diode current. A p-stop or p-spray solution below the BOX will be implemented in the next version. The chip stands 200 V and charge collection has been proven with ^{55}Fe and ^{90}Sr sources.

Further investigations are planned: test beam studies, proton irradiations, and eTCT-TCT measurements. An improved version of the chip has been submitted. The characterization results in the next few months will help to judge the possibilities to use this technology as active sensor layer in a large scale hybrid pixel prototype using FE-I4 as readout chip.

Acknowledgements

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