HV/HR-CMOS sensors for the ATLAS upgrade—concepts and test chip results

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HV/HR-CMOS sensors for the ATLAS upgrade — concepts and test chip results

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ABSTRACT: In order to extend its discovery potential, the Large Hadron Collider (LHC) will have a major upgrade (Phase II Upgrade) scheduled for 2022. The LHC after the upgrade, called High-Luminosity LHC (HL-LHC), will operate at a nominal leveled instantaneous luminosity of 5×10^{34} cm^{-2} s^{-1}, more than twice the expected Phase I. The new Inner Tracker needs to cope with this extremely high luminosity. Therefore it requires higher granularity, reduced material budget and increased radiation hardness of all components. A new pixel detector based on High Voltage CMOS (HVCMOS) technology targeting the upgraded ATLAS pixel detector is under study. The main advantages of the HVCMOS technology are its potential for low material budget, use of possible cheaper interconnection technologies, reduced pixel size and lower cost with respect to traditional hybrid pixel detector. Several first prototypes were produced and characterized within ATLAS upgrade R&D effort, to explore the performance and radiation hardness of this technology.

In this paper, an overview of the HVCMOS sensor concepts is given. Laboratory tests and irradiation tests of two technologies, HVCMOS AMS and HVCMOS GF, are also given.

KEYWORDS: Solid state detectors; Radiation-hard detectors; Particle tracking detectors (Solid-state detectors)

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1 Introduction

At the end of 2022, the LHC will have a major upgrade, called Phase II Upgrade. From 2024, the HL-LHC will provide unprecedented pp luminosities to ATLAS [1] with a levelled instantaneous luminosity of $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, resulting in an additional integrated luminosity of around $2500\,\mathrm{fb}^{-1}$ over ten years [2]. The increased instantaneous luminosity at the HL-LHC results in the expected mean number of interactions per bunch crossing increasing from in average ~ 55 at $2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ to ~ 140 at $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ (assuming a bunch crossing time of 25 ns) [2]. By simulation, and although one should take these numbers with great care as the precise design of the ITk is not completly frozen for now, the predictions for the maximum 1 MeV-neq fluence and ionizing dose for $3000\,\mathrm{fb}^{-1}$ in the pixel system is $1.4 \times 10^{16}\,\mathrm{cm}^{-2}$ and 7.7 MGy at the centre of the innermost barrel layer [2].

The much harsher radiation and occupancy conditions of the HL-LHC requests a complete replacement of the present inner detector (ID). To withstand the HL-LHC environment, the new inner tracker (ITk) should have finer granularity, increased radiation hardness and improved material budget. Based on these requirements, an all-silicon-detector tracker is proposed, with pixel sensors at the inner radii and with microstrip sensors at larger radii [3]. The pixel sizes in the new pixel detector might be $25 \times 150\,\mu\mathrm{m}^2$ for the innermost two layers and $50 \times 150\,\mu\mathrm{m}^2$ for the two outer layers. The proposed all-silicon ITk would consist of a $192\,\mathrm{m}^2$ of strip detector and a $10\,\mathrm{m}^2$ pixel detector. These large areas have for consequences the need to reduce as much as possible the cost of construction.

Presently, both the pixel and strip detectors of ATLAS ID consist of hybrid technology and have shown sufficient radiation tolerance. But the technological solutions were in many places non-standard processes, and cause high construction cost (3D silicon, high resistivity FZ silicon, fine

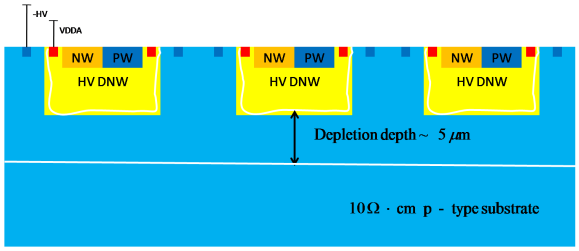

Figure 1. HV CMOS sensor conceptual overview. The DNW is typically connected to Vdda, and the bulk is biased with −HV. A relatively large depletion region can be formed due to this high voltage difference.

pitch bump-bonding...). High-voltage particle detectors in commercial CMOS technologies are a detector family that allows implementation of low-cost, thin and radiation-tolerant detectors with a high time resolution [4]. The small pixel size will improve the spatial resolution and two-track-separation. The thin thickness of the sensor will reduce the cluster size at high pseudo-rapidities, which will improve the track resolution.

2 HV/HR CMOS sensor

2.1 HV/HR sensor concept

The HVCMOS pixel sensor operating concept is shown in figure 1. The sensor is based on a triple-well structure. A lightly doped deep n-well (DNW) in p-type substrate is used as charge collecting electrode. The p-n junction formed between DNW and substrate is partially depleted by applying a reversed bias voltage. A heavy doped p-type guard-ring is drawn surrounding the DNW to bias the diode. The entire CMOS electronics is implemented in the DNW. The electron-hole pairs generated by ionization caused by charged particles passing through the depleted region, are separated and quickly collected by drift (instead of diffusion) towards the electrodes due to the electric field in the space charge regions. The fast charge collection time reduces the charge loss particularly after irradiation with respect to the traditional Monolithic Active Pixel Sensors (MAPS), which improves the radiation hardness significantly. The depletion behavior is mainly determined by substrate resistivity and polarization voltage. The HVCMOS technologies allow few tens volts of the biasing voltage, which is process depended. For example, 5 μm of depleted depth is expected for a 10 Ω·cm substrate resistivity, which corresponds to about 400 electron-hole pairs for a Minimum Ionizing Particles (MIPs).

2.2 HV2FEI4 prototype chip

Several HVCMOS prototype sensors have already been produced in 350 nm and 180 nm HV Austria Microsystems technology (AMS) and GlobalFoundries (GF) 130 nm BCDlite technologies. In this paper, the prototypes fabricated in 180 nm HV AMS technology and GF 130 nm BCDlite technology will be shown. The AMS prototype typical reverse bias voltage is −60 V and its substrate resistivity is 20 Ω·cm. The GF BCDlite prototype typical reverse bias voltage is −30 V and its substrate resistivity is 10 Ω·cm. It is to be noted that the GF process also allows keeping the direct DC-coupling of the wafer-to-wafer 3D technology. Indeed the 3D technology was experienced into a 3D consortium for High Energy Physics, which had allowed the assembly of 3D circuits using

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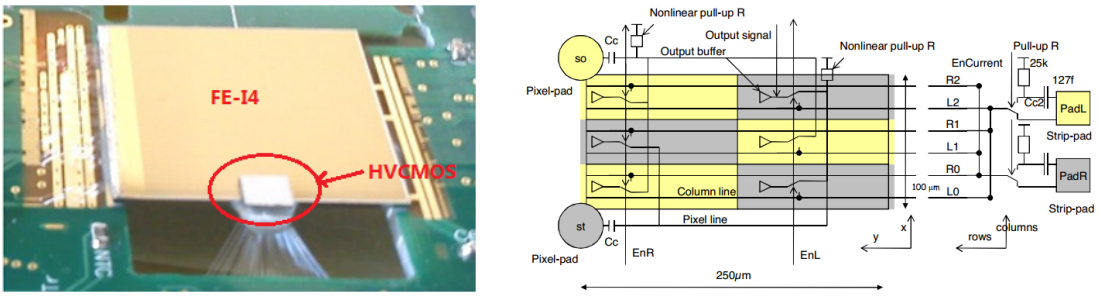

(a) HV2FEI4 test assembly.

(b) HV2FEI4 unit cell schematic.

Figure 2. (a) The HV CMOS sensor is glued onto FE-I4 face to face by epoxy glue with below 5 μm thickness ensuring good AC transmission. (b) Each six sensor pixels with chess box placement are connected to two individual FE-I4 pixels via pixel pads (st and so). The sensor output that is transmitted to FE-I4 is pulled up by a transistor (acting as a nonlinear resistor). The sensor output can also be monitored via a test pad with a 20 kΩ pull-up resistor. The pixels can be also connected together by column to be used as a strip chip with output signals PadL and PadR.

the Global Foundry 130 nm technology and the 3D Via Middle Tezzaron process [5]. All above prototypes are compatible with the FEI4 [6] chip, which is a readout ASIC developed for the ATLAS Insertable B-layer. The FEI4 pixel size is $250 \times 50\,\mu m^2$. The sensor could be coupled with FEI4 capacitively using liquid fluid epoxy glue, as shown in figure 2a, and the assembly is called HV2FEI4.

The prototypes have different pixel matrices but have the same individual pixel size, $125 \times 33\,\mu m^2$. Therefore six sensor pixels correspond to two FEI4 pixels. As shown in figure 2b, the six pixels in a unit cell are connected three by three to two FEI4 pixels in a triangular configuration. The three pixels connected together could generate different output amplitude with weighted output stage. The spatial resolution will be improved compared to using the standard FEI4 pixel size, by encoding the output pulse height of the sensor pixels. A charge sensitive preamplifier and a discriminator with local adjustable threshold are implemented in each individual pixels. The weighted discriminator output is AC coupled to the FEI4, then converted inside the FEI4 to digital Time-Over-Threshold (TOT) with a hit time stamp.

In the HVCMOS GF chip, in order to understand the pixel behavior clearly, two special pixels outside of the matrix were designed on the top region of the chip. They are called "DNW-pixel" and "Alone-pixel". The "Alone-pixel" has the same footprint as the pixels used in the matrix, but contain only the preamplifier part (no discriminator). The "DNW-pixel" also has the same footprint as the pixels used in the matrix, but it contains a sensor without electronics inside the DNW, and a additional preamplifier beside the sensor. In addition, six test transistors (three NMOS and three PMOS) with different sizes are designed to investigate the transistor radiation hardness.

3 Test results

3.1 AMS standalone chip test

Four versions of the HVCMOS AMS chips have been designed till now in AMS technology. For the HVCMOS AMS Version1 (V1), a MIP signal most probable value (MPV) of about 1500 to

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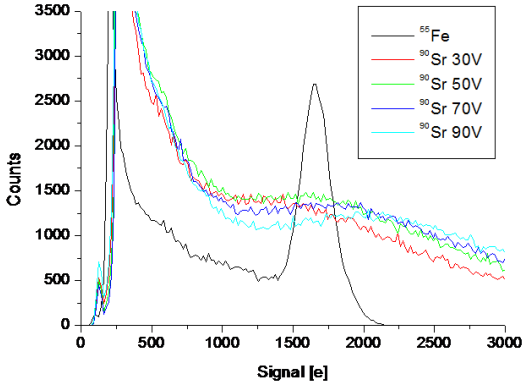
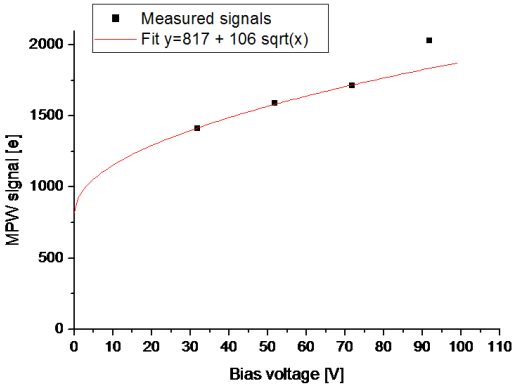


(a) Non-irradiated spectra of the AMS V1.



(b) Non-irradiated Sr90 MPV vs. bias voltage.

Figure 3. (a) The spectra are taken before irradiation. An Fe55 source is used for the SNR calculation and calibration. (b) The MPV increases with higher bias voltages, which indicates that the depletion region enlarged when the bias voltages is increased, as expected.

1800 e has been measured, depending on sensor bias (30–70 V) and using a Sr-90 source, as shown in figure 3a and figure 3b. The noise is rather high (~ 80 e) in matrix operation. Noise contribution was reduced in later prototypes by increasing the time constant of the low pass filter.

The HVCMOS AMS V1 has been irradiated with neutrons at the Jozef Stefan Institute in Ljubljana, Slovenia, up to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$. Signal to noise ratio of 20 was measured after the irradiation. The spectrum has been recorded with a single pixel's amplifier output, and has been measured with an oscilloscope. The measurement has been done at 5°C to reduce the detector leakage current; sensor bias voltage was -55 V. The Sr-90 MPV signal corresponds to about 1180 e (calibrated by Fe55 source), as shown in figure 4.

The observed MPV is larger than expected which indicates collection of non MIP-like beta particles, contribution of charge sharing and also that charges collected by diffusion contribute to the signal. An improved test setup with a scintillator trigger would remove the non MIP-like particles and edge-TCT measurements will be done in the future and will give some insight into the charge collection mechanism.

The radiation hard improved pixels of HVCMOS AMS V3 chip were also recently tested. The amplifier spectra test results (measured by spectrometer) before irradiation are shown in figure 5. The pixel can detect Fe55 source signal and the noise is ~ 70 e. The irradiation study is ongoing and results will be presented elsewhere.

3.2 GF standalone chip test

The HVCMOS GF sensor was tested before and after X-ray irradiation. The chip works well with -30 V biasing. The preamplifier noise is ~ 50 e. The preamplifier and discriminator outputs of Sr90 source observed by oscilloscope are shown in figure 6a. The spectra measurement results (measured by spectrometer) are shown in figure 6b. The sensor could detect the Fe55 source signal but show low efficiency for Sr90 detection due to some design defects. These defects have been identified and will be fixed in the next submission. The weak MPV (concealed by the noise) is ~ 850 e before irradiation at -30 V biasing. Compared with AMS HVCMOS V1, the MPV of

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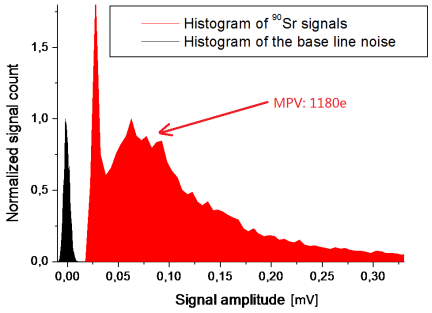


Figure 4. Sr90 spectrum after neutron irradiation.

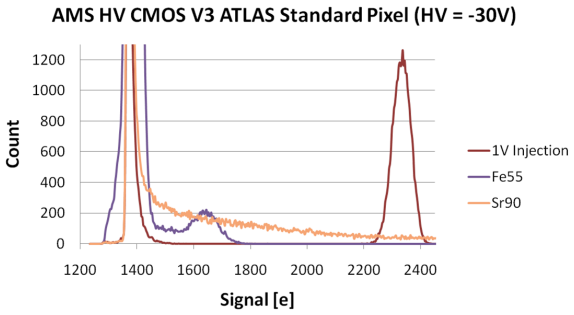
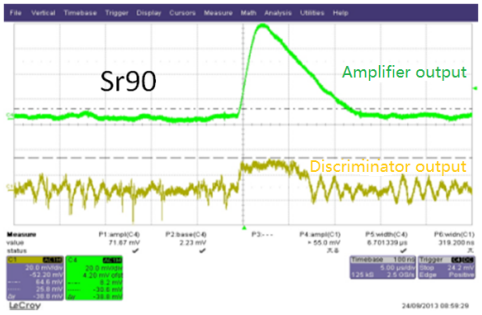
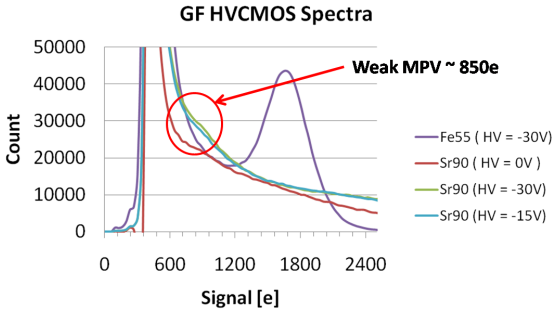


Figure 5. Non-irradiated spectra of AMS V3.



(a) Amplifier and comparator signals of Sr90.



(b) Spectra of HVCMOS GF amplifier output.

Figure 6. (a) The amplifier and comparator signals of Sr90 are taken with an oscilloscope. (b) Weak MIPs detection efficiency is due to the small depletion region and some minor design defects.

GF chip is half of AMS V1, which roughly agrees with the depletion behaviors of these two chips according to the different substrate resistivity and biasing.

In order to investigate ionizing effect on the sensor surface and verify the chips radiation hardness, we performed a X-ray irradiation test up to 1 GRad (fluence = 103.5 Krads/mn). At each irradiation step the chip was annealed for two hours at 25°C till the dose up to 600 MRad. After 600 MRad, to recover the amplifier output, two hours 70°C annealing was performed for each step. The pixel works fine at 0 MRads, but the cascode transistor inside the preamplifier of each pixels in the matrix is not able to deal with the radiations effects over 200 MRads. This issue will be fixed in the next version. More tests could be performed thanks to the two special pixels ("DNW-pixel" and "Alone-pixel") out of the matrix, which are not subject to these minor defects.

These two special pixels were irradiated to 1 GRad. As shown in figure 7a, the "Alone-pixel" could detect external test 1 V injection after a dose as high as 1 GRad. The leakage current increases to 20 μA at 1 GRad, but the chip recovers after two hours of annealing at 70°C, and the current goes back to 500 nA, as shown in figure 7b.

3.3 GF transistor test

Three kinds of transistors were designed to test the radiation hardness of the technology. The transistor sizes are listed in table 1. Some transistors were unfortunately unresponsive before irradiation, and we tested only the Mini_NMOS, Narrow_NMOS, ELT_NMOS and ELT_PMOS (ELT

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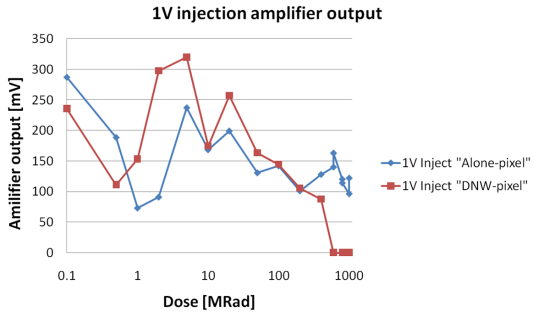
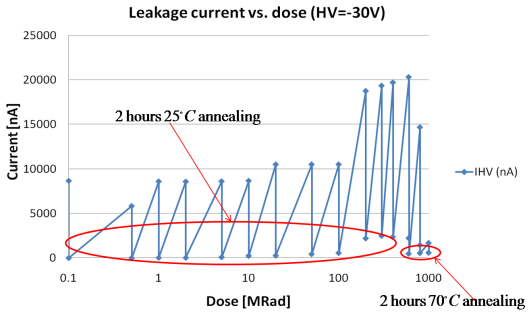


(a) Amplifier output as a function of the dose.

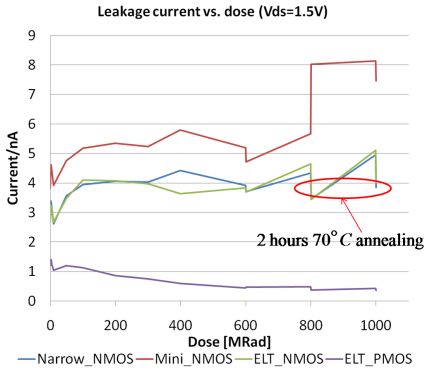


(b) Leakage current as a function of the dose.

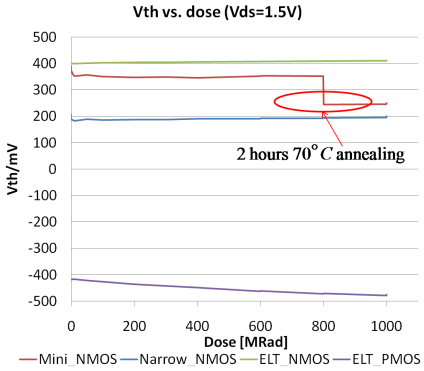
Figure 7. (a) The amplifier output is followed by a source follower and measured with an oscilloscope. (b) At 1 GRad, the leakage current reaches 20 μA and gets back to 500 nA after 70°C annealing.

Table 1. Transistor size.

Transistor	*Type*	*Width/Length*
Mini_NMOS	NMOS	50 nm/130 nm
Narrow_NMOS	NMOS	200 n/15 μm
ELT_NMOS	NMOS	2.64 μm/160 nm
Mini_PMOS	PMOS	50 nm/130 nm
Narrow_PMOS	PMOS	200 n/15 μm
ELT_PMOS	PMOS	2.64 μm/160 nm



(a) Leakage current as a function of the dose.



(b) Threshold as a function of the dose.

Figure 8. The relatively small variations of the leakage current and of the threshold voltage show that the technology is quite radiation hard, up to 1 GRad radiation dose.

stands for Enclosed LayouT transistor, transistors designed with gate all around for radiation hardness). The leakage current and threshold voltage variations with irradiation are shown in figure 8a and 8b. All transistors show good radiation hardness, in particular the ELT_NMOS transistor. We can note that a big increase in leakage current and decrease in threshold voltage occurs for the Mini_NMOS transistor after 2 hours of 70°C annealing. We think that at this stage, this transistor was lost for a reason unrelated to radiation damage and plan further exploration in the future.

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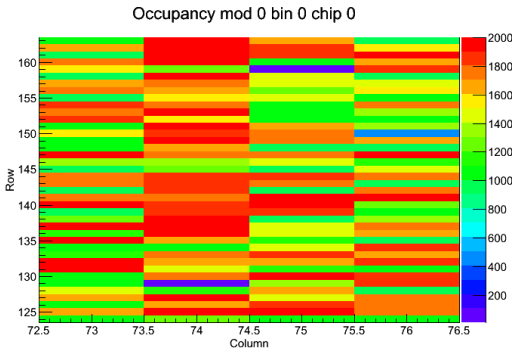
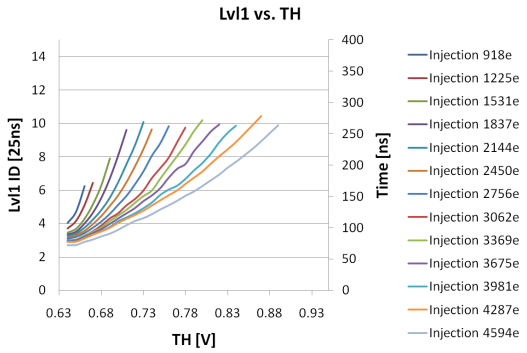


(a) Occupancy map of HV CMOS sensor.



(b) Lvl1 ID vs. threshold of HVCMOS.

Figure 9. (a) The occupancy of 1000 times injection shows the sensor is able to communicate with FE-I4. But the over counting indicates the time-walk is larger than one bunch crossing. (b) The Lvl1 ID indicates the delay of the signal. The shape of amplifier's output can be reconstructed by tuning the TH.

3.4 GF HV2FEI4 test

To demonstrate the functionality of the HV2FEI4 assembly, some tests were performed where charge is injected in the HVCMOS sensor and the hits are recorded by the FEI4. As an example, the FEI4 occupancy map when doing a 1000 external 1 V injections in each HVCMOS pixel is shown in figure 9a. This demonstrates good communication between the HVCMOS sensor glued to the FEI4 and the FEI4 chip itself, using this AC coupling method.

The 1000 external injections result in the counting range from 200 to 2000 for the matrix pixels, as shown in figure 9a. Once a hit is recorded after the correct bunch crossing (25 ns) window, it will be classified as "late hit". The "late hit" is duplicated in the FEI4, therefore leads to the over counting. The over counting indicates that the time-walk [6] is larger than one bunch crossing. We can measure the signal delay by tuning the threshold of the HVCMOS sensor with different injection charges. This measurement gives the time-walk information. The preliminary measured time walk is 29 ns with 20 mV above the base line (charge range from 918 e to 4594 e), as shown in figure 9b. 100% efficiency before threshold tuning can be reached when the input electrons are 1837 e, as shown in figure 10a. After threshold tuning, we expect that this 100% detection efficiency will be reached with lower signal.

Figure 10b shows the TOT codes of three grey sub-pixels' with weighted output amplitudes. The output of few pixels with different VNCOut codes, using a 6 bits DAC to tune the weighted output amplitudes, are shown in figure 11a. The output amplitude saturates when VNCOut are higher than 20. The saturation value corresponds to approximately 20000 e converted by the TOT/Injection plot, recorded with direct charge injection into the FEI4, which can be found in figure 11b.

4 Summary and perspectives

A new concept of particle detector based on the HVCMOS technology have been presented in this paper. Test results for two kinds of prototypes fabricated in the AMS and GF technologies before and after irradiation have been shown. A HVCMOS detector has the potential to offer

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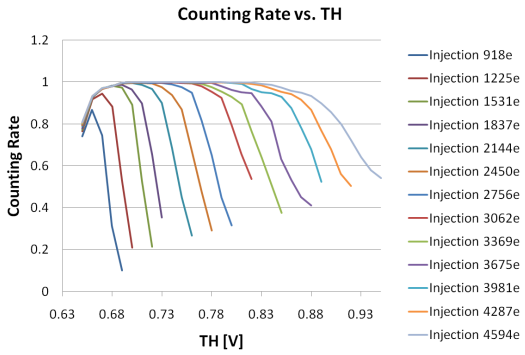
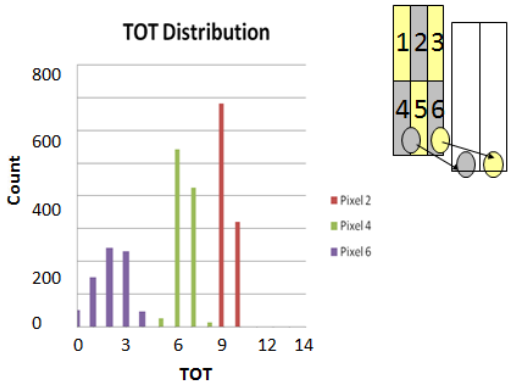
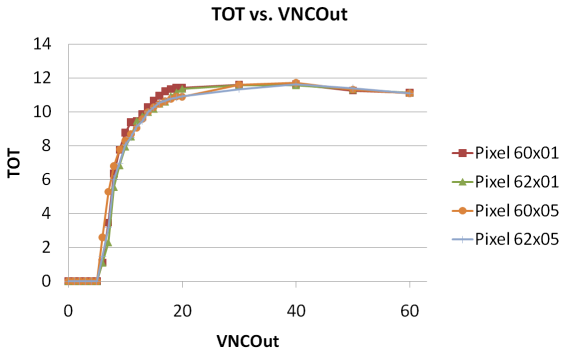


(a) Efficiency vs. threshold of HVCMOS.

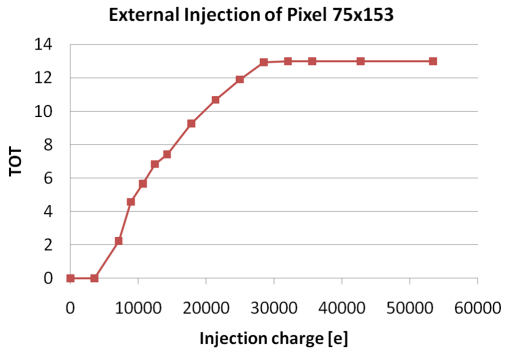


(b) TOT with weighted HV CMOS outputs.

Figure 10. (a) The counting rate is measured by tuning TH with different injections. (b) The three grey sensor pixels are connected to a single FE-I4 pixel and distinguished by weighted outputs.



(a) TOT vs. weighted HV CMOS output.



(b) ToT vs. external voltage injection.

Figure 11. (a) A sweep of the 6-bit DAC "VNCOut" (controlling the weighted comparator output) is performed to explore the output linearity of comparator. (b) Direct injection to the FE-I4 with specific charges is performed to calibrate the TOT, which can be used for the calculation of comparator amplitude.

several advantages with respect to standard silicon detectors: very low material budget, fast charge collection time, high-radiation tolerance, operation at room temperature and low cost. Both the AMS and GF HVCMOS sensors work well before irradiation. The AMS prototype can detect Sr90 signal after $1 \times 10^{15}\,\mathrm{cm}^{-2}$ neutron irradiation. The GF prototype was still responsive after 600 MRad X-ray irradiation, although with a degraded signal. The GF HV2FEI4 prototype shows good communication between HVCMOS and FEI4 and achieve the identification of individual sub-pixels within a single unit-cell based on the ToT distribution recorded in the FEI4.

To improve in particular the charge collection efficiency and radiation hardness, several prototypes with high resistivity (HR) substrate have been and will be designed and investigated. In 2015, large scale demonstrators ($1 \times 1\,\mathrm{cm}^2$ or $2 \times 2\,\mathrm{cm}^2$) will be constructed to characterize the HV2FEI4 detector for the future ATLAS upgrade.

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