CMS ECAL electronics developments for HL-LHC

2015 JINST 10 C03028

(http://iopscience.iop.org/1748-0221/10/03/C03028)

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 14, 2014*
ACCEPTED: *December 27, 2014*
PUBLISHED: *March 19, 2015*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2014,
22–26 SEPTEMBER 2014,
AIX EN PROVENCE, FRANCE

CMS ECAL electronics developments for HL-LHC

M. Hansen on behalf of CMS ECAL

CERN,
Geneva, Switzerland

E-mail: magnus.hansen@cern.ch

ABSTRACT: The High Luminosity LHC (HL-LHC) will provide unprecedented instantaneous and integrated luminosities. The CMS electromagnetic calorimeter (ECAL) will face a challenging environment at the HL-LHC: higher event pileup, higher radiation levels for the crystals and photodetectors, and a higher rate of anomalous signals from the Avalanche Photodiodes (APDs) used for the light readout in the ECAL Barrel. A redesign of the ECAL electronics (including an increase in trigger rate and latency) is planned in order to mitigate these challenges and to maintain the excellent physics performance of the detector.

KEYWORDS: Front-end electronics for detector readout; Radiation-hard electronics; Data acquisition concepts; Digital electronic circuits

doi:10.1088/1748-0221/10/03/C03028

Contents

1 Introduction

The Compact Muon Solenoid (CMS) [1] was designed to record highest quality experimental data for 10 years and for an integrated luminosity of 500 fb^{-1} at a peak rate of $1*10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. During the High Luminosity LHC (HL-LHC) [2] era CMS will receive an additional 2500 fb^{-1} of integrated luminosity at a levelled peak rate of $5*10^{34}\,\mathrm{cm}^{-2}$ delivering significantly more data for analysis provided that:

- The CMS detectors can maintain physics data quality at the higher hit density (pile-up).
- The CMS detectors can maintain physics data quality without significant degradation due to aging and radiation damage.
- The CMS trigger is capable of selecting events at high efficiency within a limited latency. The CMS requirement at HL-LHC is to cope with 12.5 microsecond level 1 trigger latency while the initial CMS requirement was 3.2 microseconds.
- The CMS data acquisition system is capable of recording events at a sufficient level 1 trigger rate. The CMS requirement is to cope with a level 1 trigger rate of 750 kHz at HL-LHC while the initial CMS requirement was 100 kHz.

The proposed CMS ECAL [3] barrel electronics upgrade, which is planned for installation during the LHC long shutdown 3 (2022–2025), is motivated to some extent by the first two points but in particular by the third and the fourth. The 61200 Lead Tungstate ($PbWO_4$) scintillating crystals and the attached photo-detectors (APDs) will perform well in the harsher environment of the HL-LHC up to 2035 [11].

2015 JINST 10 C03028

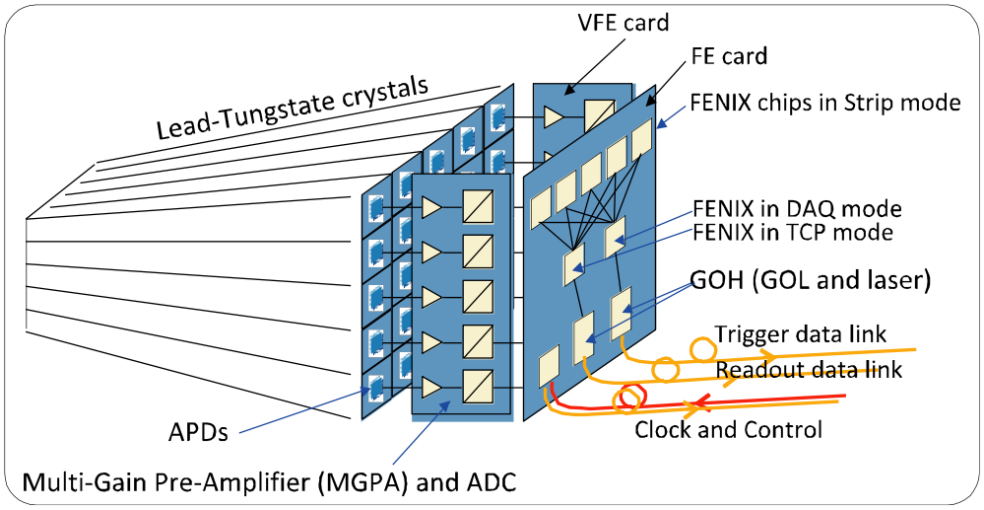

Figure 1. The legacy ECAL Barrel electronics: conceptual design of the front-end readout and trigger system for a group of 25 crystals.

2 The legacy system

2.1 Key parameters and features

The legacy front end electronics system, see figure 1, is based on the Multi Gain Pre-Amplifier (MGPA) [4], a 3 gain pre-amplifier ASIC and the AD41240 [5] a multi-channel 12 bit ADC, together yielding a 16 bit dynamic range with an LSB of 40 MeV. Data from the ADCs is input to a digital ASIC, the FENIX [6] implementing a digital pipeline, primary event buffer, and a trigger primitive generator. The pipeline depth is 256 locations corresponding to a 6.4 microsecond level 1 trigger latency. The propagation delay for the trigger primitives and the level 1 trigger distribution to the front end system is using approximately 50 LHC clocks, thus the time available for the level 1 trigger processors is limited to approximately 5 microseconds by the CMS ECAL. The primary event buffer has 256 locations and, as the number of time samples is selected to 10, 25 full events can be temporarily stored. Front end event buffer overflow is prevented by insertion of empty events. The readout is a push from the front end system to the back end, thus any buffer overflow condition is handled by the off detector system.

The trigger primitive generator calculates an energy sum based on 5×5 crystals in addition to two feature bits:

- The fine grain veto bit is calculated by comparing energy sums of five crystals (phi strips) and is set if the energy deposit is uniformly distributed over the 5×5 crystals rather than being concentrated in any 2×5 crystal region.

- The spike flag bit is calculated by comparing each ADC value in a phi strip to a threshold, thus yielding five bits of information. The five bits are fed to a look-up table (LUT) and the results of the five strip LUTs are ORed to give the Spike Flag. Thus the Spike Flag bit is set if more than one bit is set in any strip by a clever selection of LUT content.

2015 JINST 10 C03028

Fast and slow control is provided by a token ring [7]. The token ring chip set was developed for the CMS silicon strip tracker and the off detector controller module was a joint development between the CMS ECAL and the CMS silicon tracker. The token ring architecture is somewhat vulnerable as, in principle, any node failure risk to prevent a whole ring from operating. This risk is mitigated by a node bypass feature.

On average three optical fibres per unit of 25 readout channels are required in the CMS ECAL barrel.

Approximately 130 ASICs of 11 different designs are used in the legacy subsystem serving 25 readout channels. All ASICs were implemented in the well-established 250 nm radiation tolerant CMOS process with design features intended to make the ASIC more robust against single event upsets (SEU).

3 Observed features and requirements for HL-LHC

As the instantaneous luminosity is expected to increase during the HL-LHC era, some issues and features of the current system need to be addressed by the electronics system upgrade in order to maintain the required level of performance.

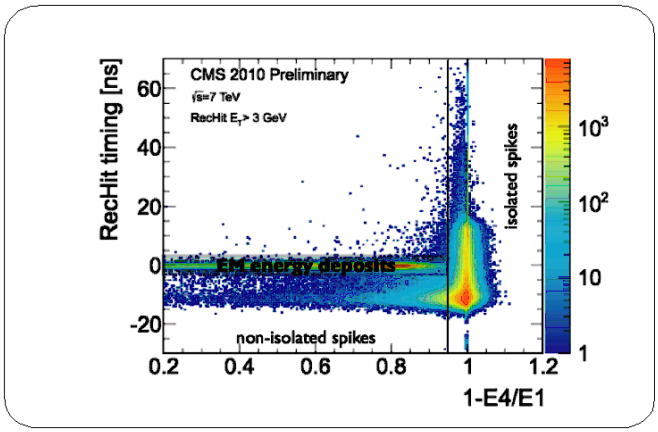

Figure 2. Hit timing versus a typical shower shape variable used for spike discrimination (ratio of the energy deposit in the 4 most energetic crystals (E4) and the central one (E1)).

3.1 Filtering of anomalous events for the CMS level 1 trigger

Anomalous events (spikes) are energy deposits directly into the bulk of the APD [11] and thus:

- Energy is deposited in a single APD as opposed to an EM shower that spreads laterally over several crystals (<95% in the centre crystal).
- Pulses arrive somewhat earlier than an EM shower that need to scintillate and propagate through the crystal
- Pulses are somewhat shorter than an EM shower pulse

The plot in figure 2 suggests that a very large fraction of anomalous events are detectable in real time using dedicated hardware in the very front end and in the back end system.

2015 JINST 10 C03028

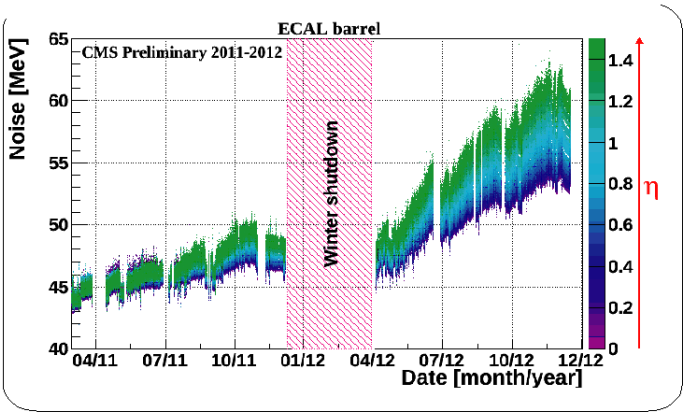

Figure 3. Noise evolution for the APDs installed in the CMS ECAL during data-taking in 2011 and 2012. The noise increase is due to the radiation-induced increase in APD dark current.

3.2 Compensation for increased APD noise

The APD dark current is expected to increase due to radiation damage, leading to increased electronic noise (see figure 3). In order to address this issue and to provide the best performance for physics, it is planned to re-optimize the parameters for the pre-amplifier. The possible gains from re-optimizing the shaping time show promising results. Shortening the shaping time of the pre-amplifier would also help in the mitigation of out-of-time pileup.

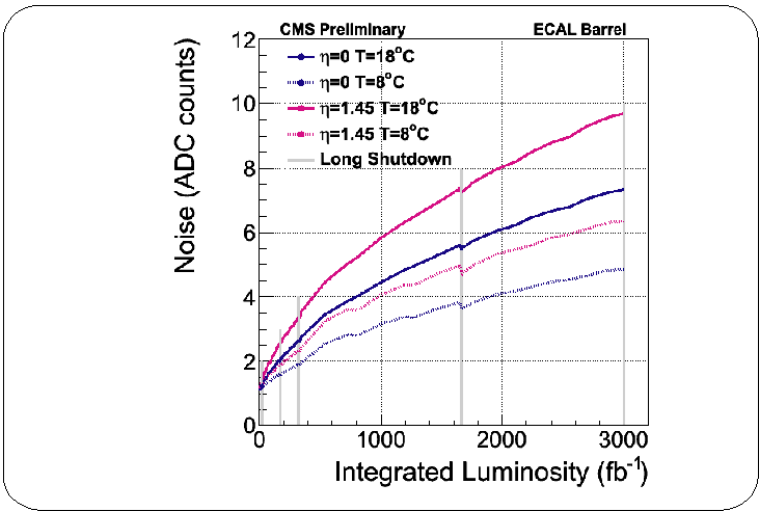

Figure 4. Prediction of the noise increase in the CMS ECAL central region (eta=0) and outer region (eta=1.45) if operated at room temperature (T=18 degrees C) or at lower temperature (T=8 degrees C).

Studies and extrapolation from Run I measurements, shown in figure 4, indicate that the APD noise can also be decreased by almost a factor of two if the ECAL barrel can be operated colder than ambient temperature.

2015 JINST 10 C03028

4 The upgraded electronics system

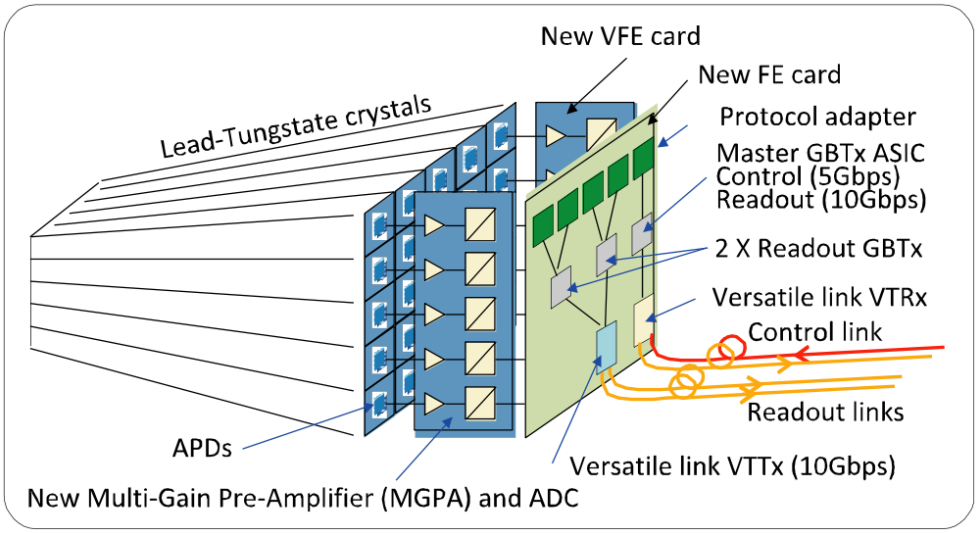

Figure 5. Artistic view of the upgraded CMS ECAL barrel electronics system.

4.1 Key parameters and features

As the luminosity increases the level of event pile-up will become more difficult to handle and in addition the APD noise increases with the dark current due to the absorbed total dose. The two facts combined ask for an improved online spike suppression algorithm. The legacy algorithm implemented using the sFGVB (strip Fine Grain Veto Bit) feature of the FENIX front end ASIC will degrade for HL-LHC conditions [12] due to the increased noise and pile-up. For the same reasons it appears advantageous to shorten the shaping time of the pre-amplifier and to optimize the resolution of the digitizer.

In order to accommodate an arbitrary trigger latency and event buffer size and to provide finer grain information the level 1 trigger the pipeline and the primary event buffer will be implemented in the back end system allowing for a significant improvement as the level 1 trigger processors can get access to single crystal granularity data. The front end is thus simplified as far as possible, requiring relatively few radiation tolerant ASIC designs. The design requires four optical fibers per unit of 25 crystals which is comparable to the legacy system. In order to decrease the currents delivered to the front end system, and thus decrease the volume of required services on the magnet surface, the power system will use radiation and magnetic field tolerant switching regulators.

The upgraded electronics system, see figure 5, will in addition to CMS ECAL-specific ASICs, use a significant fraction of generic components (e.g. 10 Gbps Giga-Bit Transceivers (GBTx) [8] and Versatile Link [9], radiation and magnetic field tolerant switching regulators [10]) derived from current and future common development projects. In addition, collaboration will be sought in order to develop and use a common hardware platform for the back end system, the ultimate goal being to limit the number of hardware designs in CMS.

2015 JINST 10 C03028

5 Summary

The CMS ECAL electronics system is performing to specification but, as the HL-LHC is planned to deliver significantly higher instantaneous luminosities, important modifications are required. The legacy front-end electronics does not meet the expected CMS trigger requirements in the increased pileup environment at the HL-LHC.

In order to provide additional flexibility for future algorithm upgrades and other enhancements, major functions currently implemented in the front end electronics, like the trigger primitive generation and the primary event buffers, will be moved off-detector. This permits the use of effective Commercial off the Shelf (COTS), like FPGAs, in the back end providing important improvements in flexibility. The current software solution to reject anomalous signals from the APDs will at least partly be implemented in a new electronics system allowing an improved rejection of anomalous events feeding into the level 1 trigger.

References

[1] CMS collaboration, *The Compact Muon Solenoid*, Technical Proposal, CERN-LHCC-94-38 (1994).

[2] M. Lamont, *LHC, HL-LHC and Beyond*, PoS(EPS-HEP 2013)149.

[3] CMS collaboration, *ECAL Technical Design Report*, CERN-LHCC-97-33, CMS-TDR-4 (1997).

[4] M. Raymond et al., *The MGPA Electromagnetic Readout Chip for CMS*, in *Proceedings of the 9th Workshop on Electronics for LHC Experiments*, Amsterdam The Netherlands (2003), pg. 83, CERN-LHCC-2003-055 (2003).

[5] G. Minderico et al., *A CMOS low power, quad channel, 12 bit, 40 MS/s pipelined ADC for applications in particle physics Calorimetry*, in *Proceedings of the 9th Workshop on Electronics for LHC Experiments*, Amsterdam The Netherlands (2003), pg. 88.

[6] M. Hansen et al., *The New Readout Architecture for the CMS ECAL*, in *Proceedings of the 9th Workshop on Electronics for the LHC Experiments*, Amsterdam The Netherlands (2003), pg. 78.

[7] A. Marchioro et al., *A system for timing distribution and control of front end electronics for the CMS tracker*, in *Proceedings of the 3rd Workshop on Electronics for the LHC Experiments*, London U.K. (1997).

[8] P. Moreira, *The GBT, a Proposed Architecture for multi-Gbps Data Transmission in High Energy Physics*, at *Electronics for Particle Physics Conference*, Prague Czech Republic (2007).

[9] F. Vasey et al., *The Versatile link, a common project for super-LHC*, 2009 *JINST* **4** P12003.

[10] S. Michelis et al., *DC-DC converters in 0.35um CMOS technology*, 2012 *JINST* **7** C01072.

[11] F. Addesa and F. Cavallari, *Performance prospects for the CMS electromagnetic calorimeter barrel APDs for LHC Runs 2 and 3: radiation hardness and longevity*, *New Developments In Photodetection (NDIP) 2014*, Tours France (2014).

[12] D.A. Petyt, *Mitigation of Anomalous APD signals in the CMS Electromagnetic Calorimeter*, *J. Phys. Conf. Ser.* **404** (2012) 012043.

2015 JINST 10 C03028