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The eCDR-PLL, a radiation-tolerant ASIC for clock and data recovery and deterministic phase clock synthesis

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ABSTRACT: A radiation-tolerant CDR/PLL ASIC has been developed for the upcoming LHC upgrades, featuring clock Frequency Multiplication (FM) and Clock and Data Recovery (CDR), showing deterministic phase and low jitter. Two FM modes have been implemented: either generating 40, 60, 120 and 240 MHz clock outputs for GBT-FPGA applications or providing 40, 80, 160 and 320 MHz clocks for TTC and e-link applications. The CDR operates with 40, 80, 160 or 320 Mbit/s data rates while always generating clocks at 40, 80, 160 and 320 MHz, regardless of the data rate. All the outputs are phase programmable with a resolution of 195 ps or 260 ps, depending on the selected mode. The ASIC has been designed using radiation-tolerant techniques in a 130 nm CMOS technology and operates at a 1.2 V supply voltage.

KEYWORDS: Analogue electronic circuits; Data acquisition circuits; Radiation-hard electronics; Digital electronic circuits

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Contents

1 Introduction

The eCDR-PLL (CDR for Clock and Data Recovery and PLL for Phase-Locked Loop) is a radiation-tolerant ASIC, capable of working either as a CDR or as a PLL. Based on the eCDR IP block [1] developed at CERN, the eCDR-PLL has been designed to feature an additional PLL mode and thus being able to operate either as a clock multiplier or as clock and data recovery circuit. This development targets front-end and back-end applications of the future Large Hadron Collider (LHC) upgrades.

The GBT project framework, part of the LHC upgrade program, has developed radiation-tolerant ASICs to implement a bidirectional 4.8 Gb/s optical link between on-detector and off-detector electronics. These links revolve around the GBTX transceiver ASIC [2], which acts as an interface between the counting room and up to 56 front-end modules that are connected to the GBTX by means of electrical links (e-links). Each electrical port (e-port) drives an e-link, which maximally consists of three differential lines: one for the uplink data input, one for the downlink data output and one for the clock signal. When the clock line is available and active, the received data can be directly retimed by means of the received clock in the front-end module. However, in situations where congestion on the front-end board or mass budget restrictions occurs, providing a clock line to the front-end device might not be feasible. In such situations, a CDR circuit is required to properly recover the data. This functionality is already provided by the eCDR IP block [1] and it is also included in the eCDR-PLL ASIC. The incoming data, which can be at 40, 80, 160 or 320 Mbit/s, is retimed by the CDR circuit while generating output clocks at 40, 80, 160 and 320 MHz with a programmable output phase resolution of 195 ps.

By adding the PLL mode to the eCDR-PLL ASIC, a second application can be addressed. The clock in the LHC experiments is the 40 MHz bunch crossing clock, which is distributed to every experiment crate by the Timing, Trigger and Control (TTC) system [3]. For all applications requiring fixed latency data transmission the distributed clock has to have a fixed and deterministic phase with respect to the LHC machine clock. Otherwise, it will not be possible to properly synchronise

the detectors and data acquisition systems. Although the 40 MHz clock is readily available, one typically needs frequencies that are multiples of this clock. This is the case when implementing the GBT-FPGA core in FPGAs, which needs the 40 MHz clock and a Multi-Gigabit Transceiver (MGT) clock to drive the 4.8 Gb/s high-speed link. Since the MGT clock frequency is vendor specific (e.g. 120 MHz for Kintex 7 and 240 MHz for Virtex 6 Xilinx FPGAs), a programmable PLL is required. To achieve fixed latency data transmission, a fixed phase in relation to the 40 MHz LHC machine clock is required [4].

Few Commercial-Off-The-Shelf (COTS) PLLs can provide fixed-phase functionality, allowing the GBT-FPGA to be implemented in the counting room. However, although radiation-tolerant FPGAs are readily available (e.g. IGLOO2 from Microsemi), allowing the GBT-FPGA core to be implemented on the detector, most COTS PLLs have not been characterized in a radiation environment and thus are not suitable to be implemented on the detector [5, 6]. The presented radiation-tolerant eCDR-PLL ASIC addresses this requirement by providing 2 PLL modes:

- 40, 60, 120 and 240 MHz output clocks with 260 ps phase resolution, targeting the 4.8 Gb/s GBT-like link applications while accepting a reference clock input at 40, 60, 120 or 240 MHz;
- 40, 80, 160 and 320 MHz output clocks with 195 ps phase resolution, targeting typical TTC and e-link applications while accepting a reference clock input at 40, 80, 160 or 320 MHz.

The eCDR-PLL ASIC, based on the eCDR IP block [1], has an I^2C interface for external programming and a Control Block for start-up, watchdog and power management. In comparison to the eCDR IP block, the loop filter parameters have been enhanced to cope with the new PLL mode.

The architecture and an overview of the ASIC are presented in section 2 and its major building blocks are discussed in section 3. A summary and outlook are presented in section 4.

2 Architecture

As discussed above, the eCDR-PLL ASIC has been designed to operate either as a CDR or as a frequency multiplying PLL. Its simplified block diagram, depicted in figure 1, reflects this dual functionality. Three error detectors can be seen: a Phase Detector (PD), a Frequency Detector (FD) and a Phase-Frequency Detector (PFD). The first two are used to lock the Voltage-Controlled-Oscillator (VCO) to the incoming data in CDR mode while the latter one is only used in PLL mode. The two Charge-Pumps (CP1 and CP2) are driven by the phase/frequency detectors and control the VCO frequency through the loop-filter. Sixteen equally spaced clock phases are generated by the VCO allowing the Phase-Shifter (PS) to properly deskew the clock and data outputs. The data rate is set by modifying the Feedback Frequency Divider (FFD) ratio. Finally, a Wien-Bridge Frequency Calibration (WB-FC) circuit allows an internal calibration of the VCO frequency, allowing the CDR to lock without the need of an external clock.

The ASIC is controlled by the Control Block, which implements a state machine with a built-in default configuration that depends on the operation mode. The I^2C interface allows the user to change the default configuration if desired. The active watchdog function implements a robust locking to the input reference, automatically restarting the eCDR-PLL whenever is necessary.

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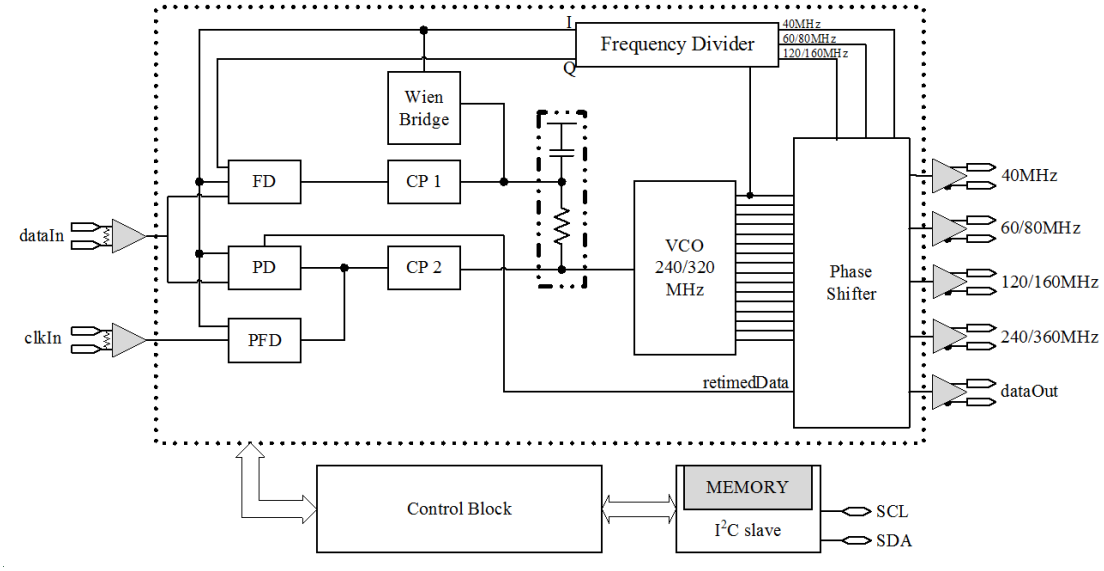

Figure 1. eCDR-PLL ASIC simplified block diagram.

The operation of the eCDR-PLL can be understood as follows [1]. When in CDR mode, the input data is applied to both the FD and the PD. The latter also retimes the data once the loop is locked. Each detector controls a Charge Pump (CP1 and CP2, respectively) that charge or discharge the loop filter capacitor, thus controlling the VCO frequency. In CDR mode, the VCO always oscillates at 320 MHz, regardless of the data rate. The VCO generates 16 VCO clock phases, which are required for the phase-shifter circuit to operate properly. The data rate programmability is implemented by the FFD, which has a programmable division ratio of 1, 2, 4 or 8 when working at 320 MHz. When in PLL mode, the VCO can also work at 240 MHz and in this case the programmable division ration can be 1, 2, 4 or 6. Both an in-phase and a quadrature version of the divided clock are generated by the FFD.

The Alexander-based PD determines if the VCO clock is early or late by means of a bang-bang type decision. The Rotational FD has been added in order to increase the acquisition range of the CDR loop. However, although the 2 detectors are present, the total acquisition range of the CDR is still relatively limited, therefore, it is necessary to bring the VCO frequency within the CDR loop acquisition range before the CDR loop is enabled. Two calibration methods are provided with the eCDR-PLL. The first is to calibrate the VCO by means of the built-in switched capacitor Wien-Bridge frequency calibration circuit [7]. This method is preferred for applications where no reference clock is available. The second method is to start the eCDR-PLL in PLL mode and, as such, allow the VCO to lock to the reference input clock before switching to the CDR mode. The advantage of the latter method is that it provides a faster lock acquisition time, although requiring an extra input.

When operating in PLL mode, the FD, PD and CP1 are disabled while CP2 is driven by the PFD. Since the PFD has a virtually unlimited acquisition range, CP2 will bring the VCO to the frequency of the applied clock signal, regardless of its initial value.

In order to reduce the power consumption, the Control Block state machine switches off any unused blocks and VCO clock phases depending on the selected mode and the desired output phase

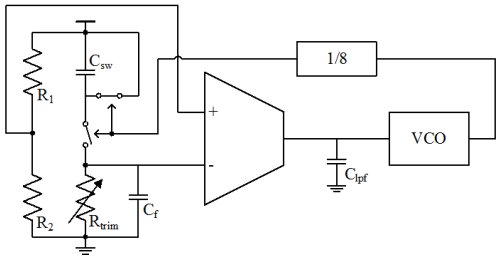

Figure 2. Simplified switched-capacitor Wien-Bridge schematic.

shifting. Regarding I/O, the eCDR-PLL is equipped with line-driver e-ports (e-portTX) and line-receiver e-ports (e-portRX), equivalent to the ones found in the GBTX ASIC [8]. The e-portRX has SLVS/LVDS compliant inputs, with programmable on/off 100 Ω on-chip termination while the e-portTX has SLVS outputs with programmable output current, being compliant with FPGAs reference clock inputs. The eCDR-PLL has a radiation-tolerant design, is integrated in a 130 nm CMOS technology, operates at a supply voltage of 1.2 V and has a specified working temperature range between $-20°$C and 100°C. The ASIC is packaged in a QFN 5×5 mm package.

3 Building blocks

The eCDR-PLL core building blocks are the same as presented in the eCDR IP block [1]. The added features such as the Control Block and I^2C interface offer full control over the eCDR-PLL functionalities. Several blocks had to be redesigned (e.g. VCO) to cope with the new PLL mode which can operate with a VCO frequency of 240 MHz or 320 MHz.

3.1 Wien-bridge frequency calibration

The Wien-bridge frequency calibration circuit, shown in figure 2, allows the VCO oscillation frequency to be brought close to the desired frequency, thus allowing the CDR to lock without the need of an external reference clock. The main idea is to equalize the voltages in the Wien-bridge, one half of which is composed of resistors R_1 and R_2 while the other half consists of R_{trim} and the switched-capacitor C_{sw}. For a switching frequency, f_{sw}, the equivalent resistance of the switched capacitor can be calculated as follows:

$$R_{\text{eq}} = \frac{1}{f_{\text{sw}} C_{\text{sw}}}$$

In steady-state, the closed loop, consisting of the Wien-bridge, integrator, VCO and frequency divider, establishes a control voltage to the VCO which is such that it oscillates at the frequency that keeps the Wien-bridge in equilibrium, i.e. the voltages of the two branches in the Wien-bridge being equal. This equilibrium frequency can be calculated as follows:

$$f_{\text{sw,eq}} = \frac{R_2}{R_1} \frac{1}{R_{\text{trim}} C_{\text{sw}}}$$

Since the Wien-Bridge frequency calibration circuit is only used in CDR mode, the VCO has to be calibrated to 320 MHz with a fixed divider ratio of 8 in the calibration loop, resulting in a

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40 MHz $f_{sw,eq}$. In the eCDR-PLL, R_1 being equal to R_2 results in an equilibrium voltage that is half the supply voltage. Since R_{trim} has a mid-scale resistance of 18 kΩ, C_{sw} needs to be 1.4 pF for $f_{sw,eq}$ to equal 40 MHz. In order to correct for process variations and integrator offset, R_{trim} can be programmed between 12.5 kΩ and 25 kΩ with a resolution of 190 Ω. As only the voltage difference between the left and right node is considered, the Wien-Bridge does not suffer from power supply variations [7].

3.2 VCO

The VCO, depicted in figure 3, is an 8-stage differential ring oscillator composed of cascaded delay cells. The minimum target VCO frequency when the eCDR-PLL is locked is 240 MHz, resulting in a cell delay of approximately 260.4 ps. Due to this relatively large delay, the input pairs of the delay cells are biased at a relatively small overdrive voltage in order to slow them down. Furthermore, in order to avoid the need for a common-mode feedback circuit, nMOS diodes have been added in parallel to the current source loads. This creates a trade-off between the small-signal gain decrease due to the nMOS diodes insertion and the stability of the common-mode output level [9].

The cell delay is controlled by means of the pMOS current source. Decreasing the pMOS gate voltage increases the current flowing though the differential pair, which, in its turn, decreases the delay and increases the oscillation frequency. The gate voltage of the nMOS current sources in the active load is generated by means of a replica biasing circuit, which is common for all 8 delay cells.

The feedback divider and the phase-shifter block require rail-to-rail signals (1.2 V CMOS). As the oscillation amplitude of the delay cells from figure 3 is significantly smaller than the supply voltage, 8 differential-to-single-ended (D2S) converters have been included in the design in order to generate a full swing digital signal from the differential VCO signals. This enables to create 16 VCO clock phases, each being phase-shifted with 22.5^o, by simply inverting the 8 generated phases. In order to save power, all D2S converters can be switched off, except for the one that processes the 0^o and 90^o VCO clock phases, which are required to close the eCDR-PLL loop. This is done by the Control Block state machine which switches off any unused phases depending on the desired output phase. The VCO has been redesigned to work at 240 MHz as well as 320 MHz, by resizing its pMOS current sources and the correspondent replica biasing. Figure 4 depicts the new extracted VCO transfer function using typical-typical (TT), fast-fast (FF) and slow-slow (SS) corners, where both target frequencies can be met in any corner.

3.3 Control block

A simplified version of the Control Block's finite state machine (FSM) is depicted in figure 5. When the reset is asserted, the FSM goes into the Reset State, resetting the VCO and configuring the eCDR-PLL with a known initial setup (i.e. charge pump currents, filter parameters, etc), which is mode dependent. When the reset is released the FSM can follow three different branches, depending on the selected mode: PLL mode, CDR mode with external reference clock or CDR mode with internal calibration. The CDR mode with external reference clock is taken as an example:

- After the Reset State, the FSM goes into the WaitForPLLLock state, setting the eCDR-PLL in PLL mode to externally calibrate the VCO;

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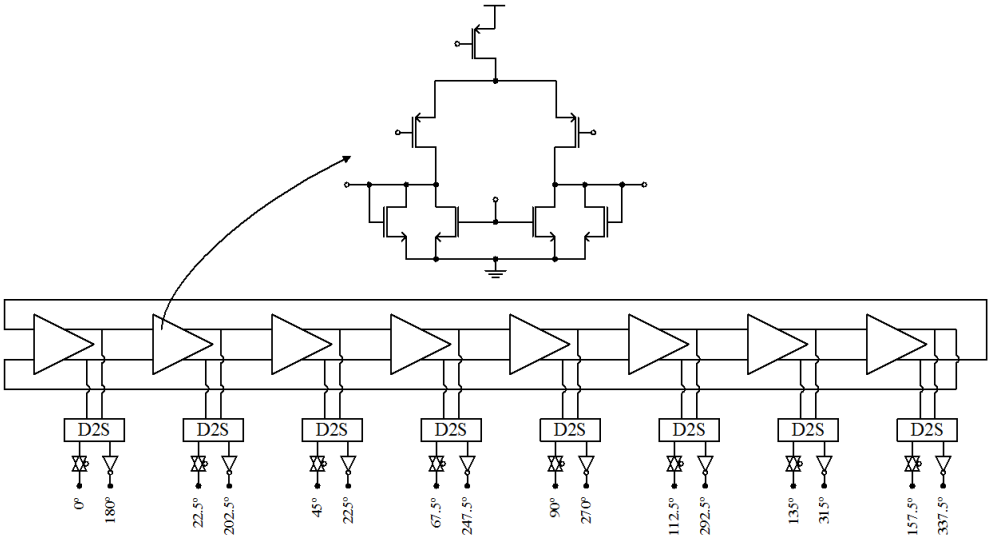

Figure 3. Topology of the VCO and circuit diagram of a delay cell.

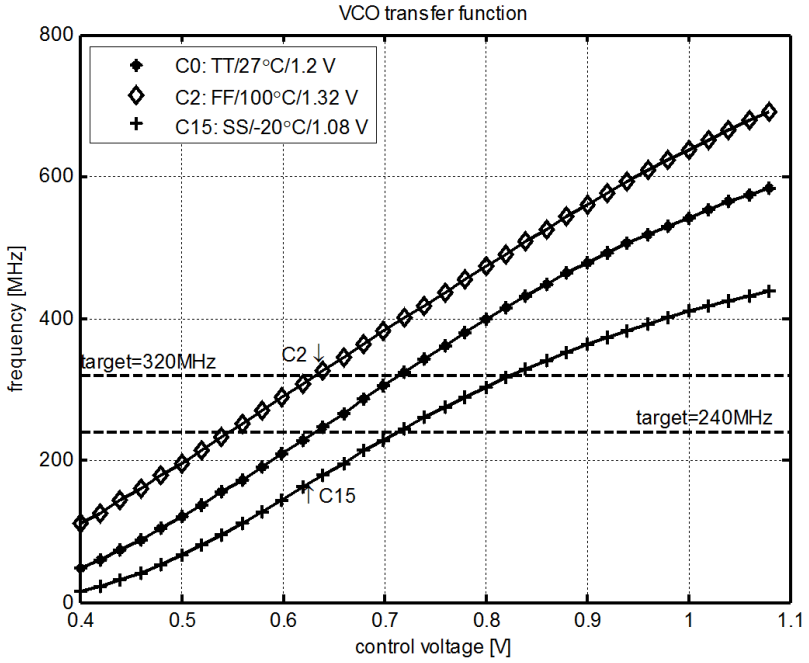

Figure 4. Simulation results of the extracted VCO transfer function using TT, FF and SS corners.

- The PLL Locked signal, which indicates if the VCO has locked to the incoming reference clock, is monitored. Once locked, the FSM passes through the state PLLLocked, goes into the waitForCDRLock state and sets the eCDR-PLL in CDR Mode;
- The FSM waits for the eCDR-PLL to lock in CDR mode, and once the Locked signal is high the FSM goes into the CDRLocked state;
- Finally a watchdog monitors the Locked state and resets the eCDR-PLL if the lock is lost.

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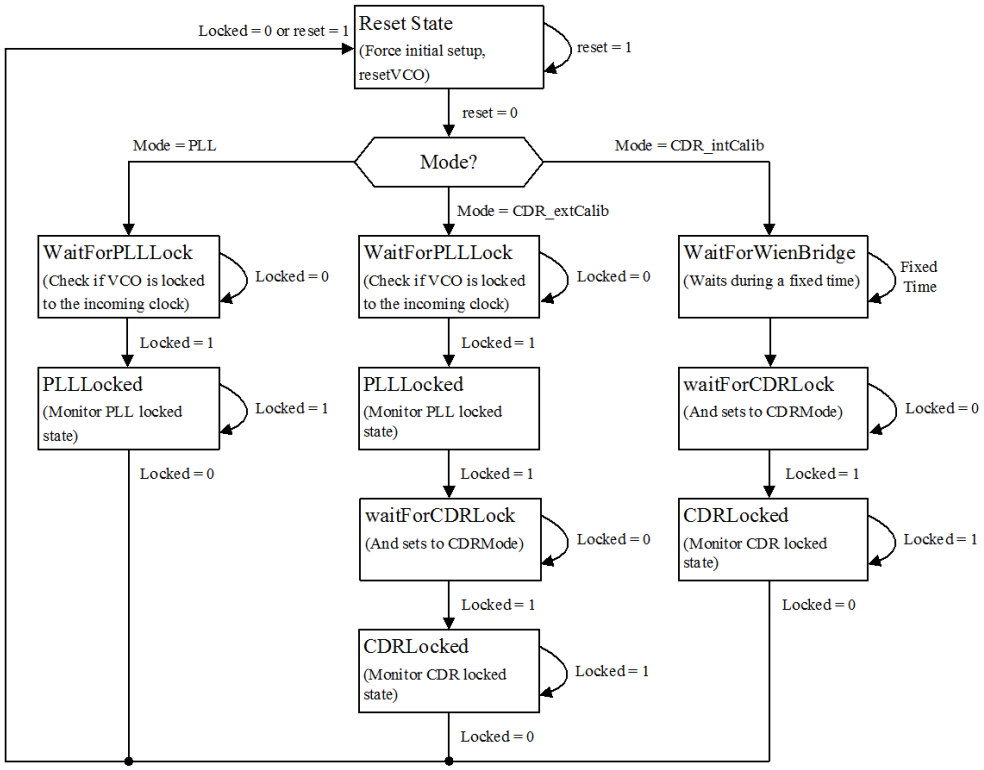

Figure 5. Simplified Control Block state machine.

4 Summary and outlook

A highly flexible and radiation tolerant PLL and CDR ASIC for the upcoming LHC upgrade has been presented. Designed to be used both in back-end and front-end applications, the programmable eCDR-PLL ASIC is a step-up of the previous eCDR IP block. It can work as a PLL, synthetizing clocks at 40, 80, 160 or 320 MHz or 40, 60, 120 or 240 MHz, depending on the feedback divider ratio. It can also operate as a CDR, generating retimed data aligned with 40, 80, 160 and 320 MHz clock outputs. The phases of all the outputs are phase programmable with a resolution of either 195 or 260 ps, depending on the selected mode.

The ASIC will be availabe in a QFN 5×5 mm package, featuring a 7-bit I^2C slave for external configuration. Designed in a 130 nm CMOS technlogy with 1.2 V supply voltage and based on the eCDR IP block, it is expected to achieve the same temperature and power supply stability and less than 10 ps RMS jitter. The prototype fabrication is expected to take place in the first quarter of 2015.

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