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A 10 Gb/s laser driver in 130 nm CMOS technology for high energy physics applications

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ABSTRACT: The GigaBit Laser Driver (GBLD) is a key on-detector component of the GigaBit Transceiver (GBT) system at the transmitter side. As part of the design efforts towards the upgrade of the electrical components of the LHC experiments, a 10 Gb/s GBLD (GBLD10) has been developed in a 130 nm CMOS technology. The GBLD10 is based on the distributed-amplifier (DA) architecture and achieves data rates up to 10 Gb/s. It is capable of driving VCSELs with modulation currents up to 12 mA. Moreover, a pre-emphasis function has been included in the proposed laser driver in order to compensate for the capacitive load and channel losses.

KEYWORDS: VLSI circuits; Analogue electronic circuits

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1 Introduction

The GigaBit Laser Driver (GBLD) is the main building block at the transmission side of the versatile link project, which is currently under development at CERN [1]. The GBLD transmits experimental data and control information from the GBT chip to the transceiver in the counting room through an optical fibre. As an on-detector component of the GBT system for data transmission in High Energy Physics (HEP) applications, the GBLD needs to be able to operate at high data rates while displaying high radiation tolerance. A 5 Gb/s laser driver (the GBLD) was designed for the phase I detector upgrades [2] and is currently being mass produced. That device will be embedded in detector systems to be installed during the LHC long shutdown (LS2) foreseen for 2018 / 2019. With a more long term perspective, the phase II upgrades of the LHC machine and detectors (with the installation foreseen to start in 2022 (LS3)) aim at high-luminosity operation with the objective of collecting ten times more data than in the initial design by 2030. Data transmission for the phase II detector systems will require very high data rates and low power dissipation systems. Data transmission systems operating at 10 Gb/s are now being considered. The laser driver GBLD10 described in this work aims at such systems.

While most 10 Gb/s laser driver designs take advantage of scaling in more advanced fabrication technologies [3, 4], the GBLD10, presented in this paper, is implemented in a 130 nm CMOS technology. In order to achieve the high data rate of 10 Gb/s, a novel circuit technique for laser drivers has been developed. In contrast to the conventional current modulators, a distributed-amplifier (DA) based modulator with pre-emphasis is proposed here.

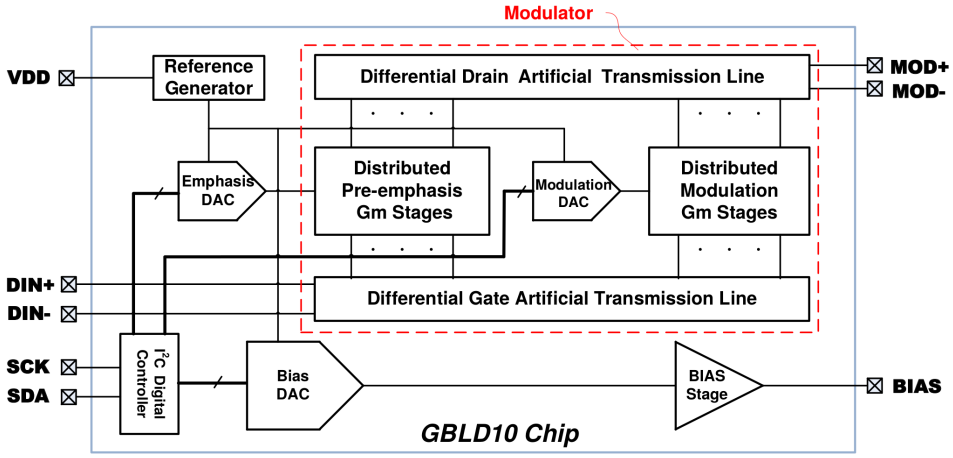

Figure 1. GBLD10 block diagram.

The GBLD10 chip has a die size of 2 mm × 2 mm and fits in a 4 mm × 4 mm QFN24 package. Both electrical tests, where the GBLD10 die is directly bonded to the PCB, and optical tests have been carried out to fully characterize the performance of the GBLD10.

2 Design of GBLD10

2.1 GBLD10 architecture

The block diagram of the GBLD10 chip is shown in figure 1. The two main functions are laser biasing and laser modulation. The biasing circuit, described in section 2.2, needs to be able accommodate the large expected voltage drop across the VCSEL diode. The modulator, described in section 2.3, needs to be designed with high bandwidth in order to enable data rates up to 10 Gb/s. Moreover, the correct operation of both biasing and modulation functions need to be guaranteed across Process, Voltage and Temperature (PVT) variations. Therefore, all currents are programmable: the modulation current can be programmed between 0 and 12 mA by means of a 6-bit DAC; the pre-emphasis current can be programmed between 0 and 6 mA by means of a 4-bit DAC; the laser biasing current can be programmed between 2 and 43 mA by means of an 8-bit DAC. The pre-emphasis function, which is intended to compensate for the performance degradation due to the unforeseen external capacitive load and/or channel losses, has been designed by means of the capacitive degeneration technique. The GBLD10 is powered by a single 2.5 V supply. An on-chip voltage regulator generates an internal 1.5 V for the digital circuits and DACs. The modulator itself is powered by the external 2.5 V supply directly.

2.2 Laser biasing

Because the DC voltage drop across a biased VCSEL diode is 1.5–2.3 V, the voltage headroom available for the laser biasing circuit can be as low as 0.2 V, with the supply voltage of only 2.5 V. Moreover, the biasing circuit is required to show a high output impedance in order to be insensitive to output voltage variations. To meet both requirements, a current mirror with a cascode and feedback has been designed, as shown in figure 2. The current mirror has a ratio of 1:10. The lower

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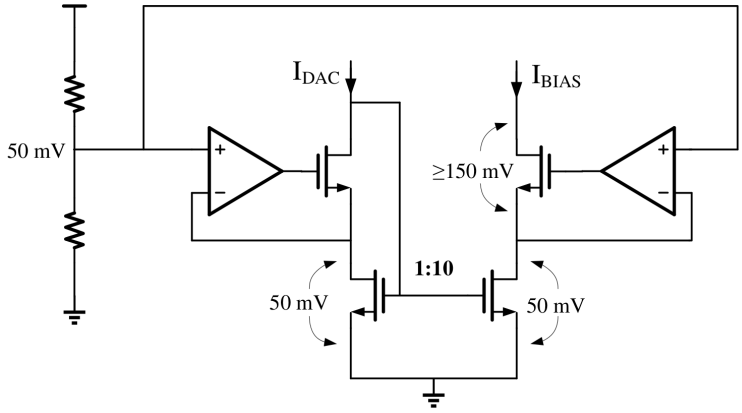

Figure 2. Laser biasing circuit.

two devices are thin-oxide NMOS transistors working in the linear region while the upper devices are thick-oxide NMOS transistors in saturation. Since the current cannot be copied accurately by transistors in the linear region because of channel length modulation, a feedback loop has been added in order to guarantee that the drain-source voltage of both thin-oxide devices is equal to 50 mV, resulting in accurate mirroring with the linear devices. The cascode transistors have been implemented by thick-oxide devices in order to tolerate voltages up to the supply voltage of 2.5 V. In order to operate properly, the current mirror of figure 2 needs at least 200 mV, namely 50 mV over the linear devices and 150 mV to keep the cascode transistors in saturation. On this condition, the output impedance of the proposed circuit is guaranteed to be sufficiently high.

2.3 Laser modulation

2.3.1 Basic modulator topology

The topology of the current modulator is shown in figure 3. It consists of two trans-conductance (Gm) stages, one to provide modulation current and one to provide pre-emphasis current. The latter has been implemented by means of the capacitive degeneration technique. The trans-conductance of both stages can be programmed by changing the respective tail currents. To provide proper matching, on-chip 50 Ω resistors have been placed, both at the input and the output terminals. The small-signal transfer function of the circuit in figure 3 can be expressed as follows:

$$\frac{I_{\mathrm{OUT}}}{V_{\mathrm{IN}}}(s) = \frac{g_{m3,4}\left[1 + s \cdot 2C_{\mathrm{pre}}\left(\frac{1}{g_{m1,2}} + \frac{1}{g_{m3,4}}\right)\right]}{1 + s \cdot \left(\frac{2C_{\mathrm{pre}}}{g_{m1,2}}\right)} \tag{2.1}$$

From (2.1), we can see that $\frac{I_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = g_{m3,4}$ at $s = 0$, which means that the pre-emphasis function does not affect the modulation amplitude. The transfer function in (2.1) also shows a system with a zero and a pole. They are located at the following frequencies:

$$z_1 = \frac{g_{m1,2}}{2\left(1 + \frac{g_{m1,2}}{g_{m3,4}}\right)C_{\mathrm{pre}}} \tag{2.2}$$

$$p_1 = \frac{g_{m1,2}}{2C_{\mathrm{pre}}} \tag{2.3}$$

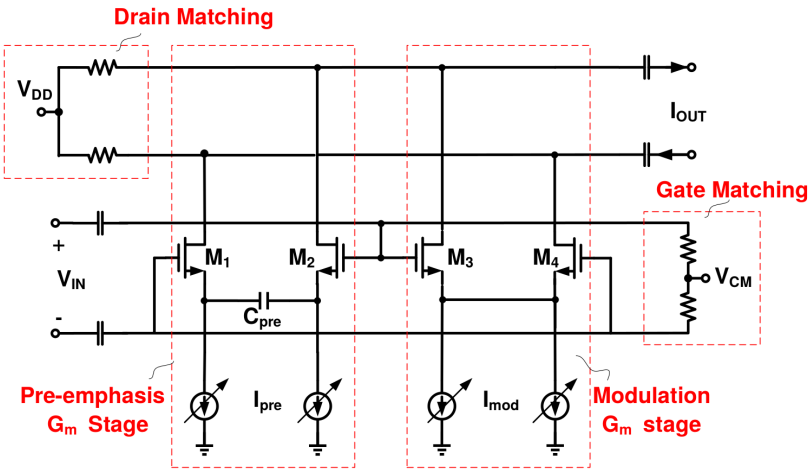

Figure 3. Modular topology.

From (2.2)–(2.3), it is clear that the zero and pole locations can be modified by changing $g_{m1,2}$. As a result, the pre-emphasis magnitude is modified as well.

2.3.2 Proposed DA-based modulator

The speed of the modulator in figure 3 is limited by the parasitic capacitances. These parasitic capacitances can be very large because of the following reasons. First, the NMOS differential pairs are large in order to deliver large modulation currents. Second, the ESD diodes at the input and output of the modulator, which are required for reliability considerations, need to be large. This is especially a problem at the input of the modulator, where gates have to be protected. The ESD diodes at the output can be designed with a smaller size because a drain is more robust than a gate. Finally, the layout can have a significant influence on the speed of the modulator as well. This is especially a problem considering that, in order to meet the electro-migration requirements, the metal width needs to be large enough to accommodate the large modulation currents. Consequently, significant parasitics originate from the metal wiring.

In order to circumvent the bandwidth penalty of these parasitic capacitances, we propose the distributed-amplifier based modulator. By designing the input and output nodes in figure 3 into differential transmission lines made of L-C sections, the gate and drain parasitic capacitances can be considered as being part of the transmission lines. As a result, they will only have little impact on the circuit bandwidth. As shown in figure 4, the single modulator and pre-emphasis stage from figure 3 has been uniformly distributed over 3 stages and 2 stages respectively. Three-terminal inductors are inserted at the gates and drains between adjacent stages to form artificial transmission lines together with the gate and drain capacitances.

In a distributed amplifier, the group delay over the gate and drain transmission lines must be the same in order for the signals to add constructively at the output. It can be easily achieved if the values of inductance and capacitance used to form the two transmission lines are the same. This is however not necessarily the case in practice since the drain and gate capacitances are intrinsically different. In the case under study, the following also needs to be taken into account: first, relatively high bias currents lead to high output conductance of the gain stage. Second, large signal

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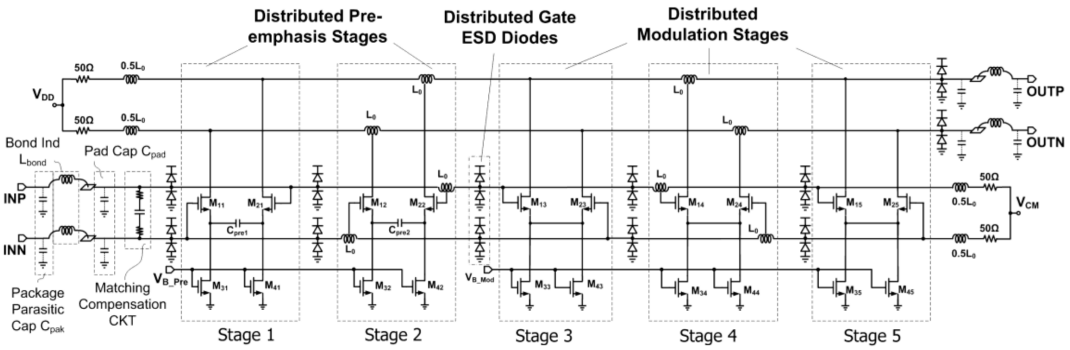


Figure 4. Proposed DA-based modulator.

amplitudes at the drain make the output conductance even higher (on average, since they take the transistor into the linear region of operation). Since the output conductance is high, the parasitic drain-to-bulk capacitance of the very large differential pair tail current source actually loads the drain circuit making the equivalent drain capacitance (200 fF/stage) actually higher than the gate capacitance (140 fF/stage). Fortunately, this difference can be compensated by distributing the ESD protection circuit along the input transmission line. The equivalent ESD capacitance becomes then distributed with the dual advantage of equalizing the gate/drain transmission line capacitances and of avoiding that a lumped ESD element at the chip input would degrade the modulator bandwidth.

Both the gate and the drain transmission lines are designed with a characteristic impedance of 50 Ω. For minimal chip area, the required number of inductors should be minimized. This has been achieved by using three-terminal inductors, as shown in figure 4. In order to save the area of extra inductors, the bonding wires, which have an inductance of approximately 750 pH, have also been used as being part of the designed transmission lines. The resulting total number of inductors for the DA-based modulator is only 12, which was possible to integrate on a 2 × 2 mm^2 die.

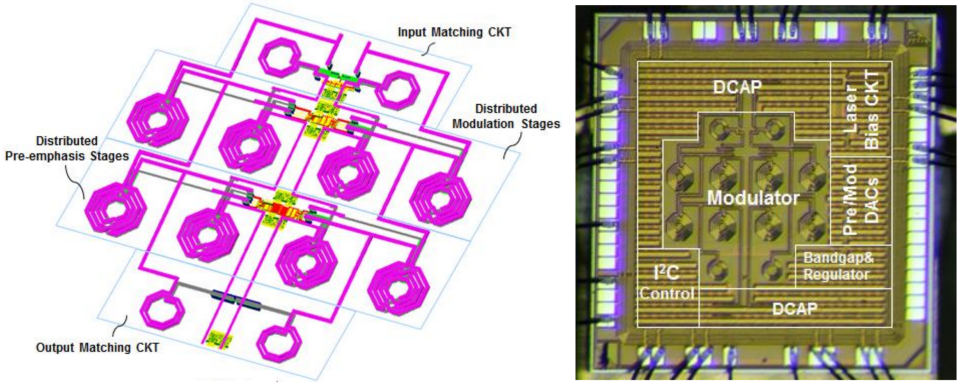
2.3.3 GBLD10 implementation

The GBLD10 is implemented in an 8-metal 130 nm CMOS technology. The high-speed signals are routed with the thick top metal layers to reduce parasitics. figure 5(a) shows the layout of the modulator. The three-terminal octagonal inductors have a diameter of 150 μm. The distance between two adjacent inductors is larger than 120 μm, which is sufficient to circumvent the inductive coupling. figure 5(b) shows the entire die photo. The die size is 2 mm × 2 mm with a modulator area of 0.69 mm^2.

3 Test results

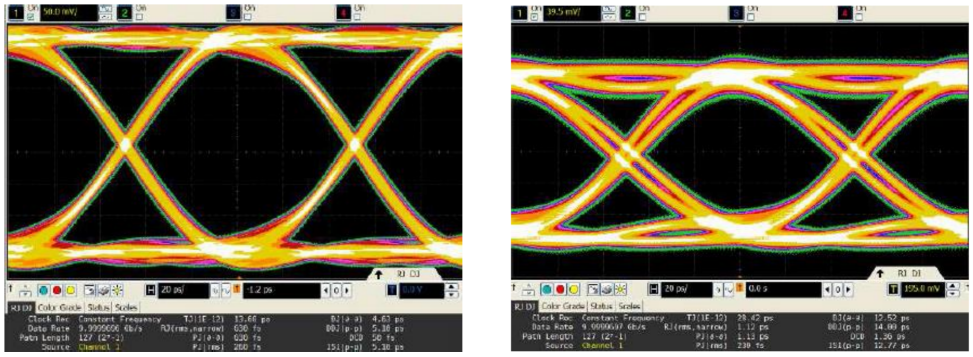
3.1 Electrical and optical test results

Both electrical tests and optical tests have been carried out to characterize the GBLD10 performance. An Agilent J-BERT N4903B was used to generate the differential PRBS input signal. An Agilent DSA91204A oscilloscope was used to observe the outputs. In the optical tests, the GBLD10 was placed in the Enhanced Small Form-factor Pluggable (SFP+) module, developed by the Versatile Link project [5], with the differential outputs AC coupled to an 850 nm VCSEL laser



(a) (b)

Figure 5. GBLD10 implementation: (a) modulator layout; (b) GBLD10 die photo.



(a) (b)

Figure 6. 10 Gb/s eye diagrams: (a) electrical eye diagram; (b) optial eye diagram.

diode. An Agilent 8163B light-wave multi-meter was used to convert the optical output from the VCSEL into an electrical signal.

The jitter performance at 10 Gb/s has been measured with PRBS 2^7-1 input data and at a BER of 10^{-12}. Figure 6(a) and (b) show the electrical and optical eye diagrams respectively with a 6 mA modulation current. The total jitter in the electrical eye is 13.68 ps with an RMS random jitter component of 0.63 ps and a data-dependent jitter component of 5.1 ps peak-to-peak. The optical eye shows 28.42 ps total jitter with an RMS random jitter component of 1.12 ps and a data-dependent jitter of 14 ps peak-to-peak. Because the bandwidth of the VCSEL used is smaller than that of the driver circuit, the optical tests show larger amounts of jitter than the electrical tests.

The supply current of the GBLD10 has been measured at different modulation settings with a fixed 6 mA bias current. As shown in figure 7, the supply current increases linearly with the increasing modulation current settings. The power consumption is 85 mW in the typical case with a 6 mA current for both modulation and biasing, which is only 1/4 of the power consumption of the laser driver reported in [2].

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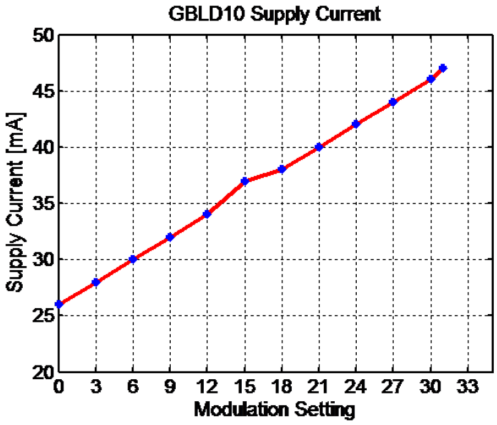

Figure 7. GBLD10 supply current at different modulation settings.

Table 1. GBLD10 performance at different dose rates.

Dose Rate	RMS Jitter (ps)	Data-dependent Jitter (ps)	Total Jitter (ps)	Rise Time (ps)	Fall Time (ps)	Supply Current (mA)*
0	0.73	12.28	21.85	44.1	42.2	42.36
700k	0.78	13.05	23.05	46.3	43.98	42.40
5M	0.78	10.70	20.70	45.5	43.4	42.25
10M	0.72	10.82	20.29	46.2	44.1	42.37
20M	0.82	12.64	23.06	43.4	44.2	42.38
100M	0.74	11.20	20.84	45.8	43.5	42.38
200M	0.81	11.69	22.00	46.5	44.2	43.76
500M	0.76	12.02	21.97	46.4	44.1	45.91

(*) Supply current is tested at default register settings after power-on reset operation.

3.2 Radiation test results

Radiation tests have been carried out up to a total ionizing dose of 500 Mrad. At every intermediate dose step, the functionality of the I^2C read/write and power-on reset circuitry has been checked. Also, the electrical eye diagram and the supply current have been measured at every step. The performance of the GBLD10 as a function of irradiation is shown in TABLE I. It shows that the GBLD10 can be considered to be radiation-hard with only negligible performance degradation up to 500 Mrad.

3.3 Other test results

The functionality of the pre-emphasis circuitry has been tested by cascading a pair of co-axial cables with a length of 2 m to mimic channel loss. The eye diagrams with and without pre-emphasis are shown as figure 8. From the test results, the pre-emphasis can improve the rise and the fall times as well as increase the vertical eye opening when driving loads with large losses.

Due to its simple architecture with only a few stacked devices, the modulator can work at lower voltages than what is required to drive a VCSEL, namely 2.5 V. To verify this, the GBLD10 has been tested at lower supply voltages as well. From the test results shown in figure 9, the GBLD10 can still operate down to 1.5 V supply while maintaining the same performance.

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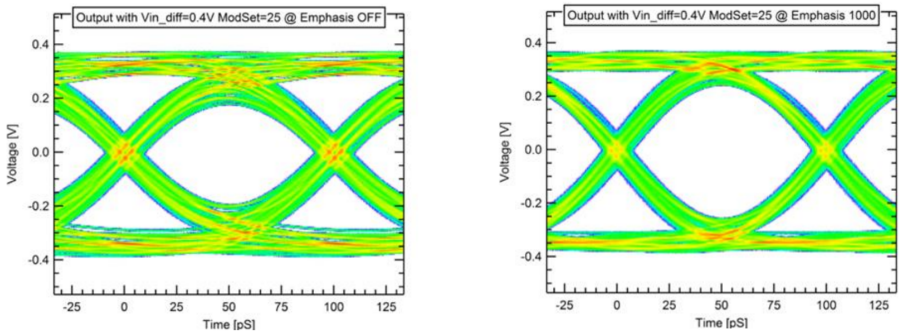
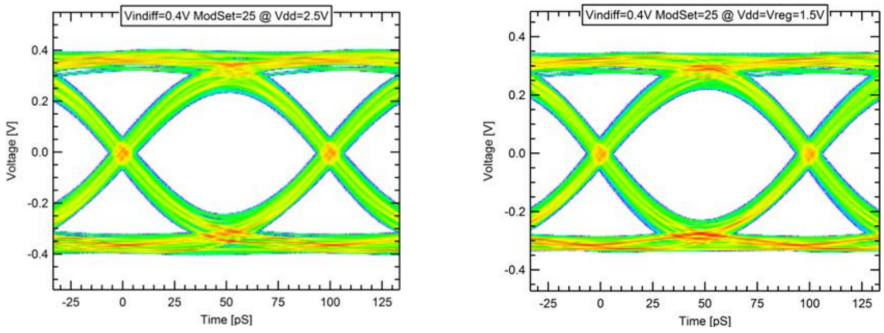


(a) (b)

Figure 8. GBLD10 pre-emphasis test: (a) 10 Gb/s eye diagram without pre-emphasis; (b) 10 Gb/s eye diagram with pre-emphasis.



(a) (b)

Figure 9. GBLD10 slow voltage test: (a) 10 Gb/s eye diagram at 2.5 V; (b) 10 Gb/s eye diagram at 1.5 V.

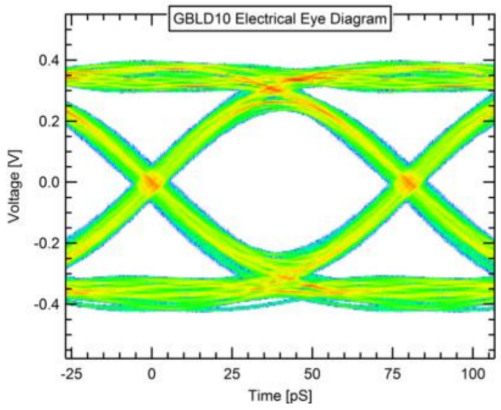


Figure 10. 12.5 Gb/s eye diagram for GBLD10.

The GBLD10 has also been tested at 12.5 Gb/s, which is the maximum speed of the test instruments. As shown in figure 10, a clean and well opened eye can be observed.

4 Conclusion

A 10 Gb/s VCSEL laser driver (GBLD10) has been designed for high-energy physics applications in a 130 nm CMOS technology. To minimize the bandwidth limitations from the parasitics, a

DA-based modulator is proposed. By carefully designing the gate and drain transmission lines, the parasitic capacitances of the modulator can be absorbed. As a result, the GBLD10 is able to operate at a data rate of 10 Gb/s. The pre-emphasis function, implemented by the capacitive degeneration technique, has been verified by means of electrical tests. The potential of the GBLD10 to operate at low supply voltages and at even higher data rates has been demonstrated as well.

Acknowledgments

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